Fast Transient Fully Standard-Cell-Based All Digital Low-Dropout Regulator With 99.97% Current Efficiency

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***Abstract*—A fully standard-cell-based digital low-dropout (D-LDO) regulator with low-level quiescent current and fast load transient response is proposed for efficient power management in a system-on-a-chip. For the design of a fast and accurate voltage comparator, we propose a logic-threshold triggered comparator (LTTC) based on a standard CMOS digital inverter. The LTTC is employed to implement the binary voltage comparator for a bang-bang loop control and a multimode detector, which senses the output voltage with three segmented ranges during its transition, is also employed. Further, we implement a multiloop controller composed of components, such as a fixed-gain accumulator, successive approximation register, and variable-gain accumulator (VG-ACC), which accelerate the transient response while being switched over adaptively to the finely segmented voltage range. In particular, the proposed VG-ACC enables a constant unity-gain frequency overload current variation such that it enhances the load transient response in terms of over/undershoot and settling time. The proposed D-LDO is fabricated using a 65-nm CMOS process technology with an active area of 0.014 mm^2. The measurement results show a peak current efficiency of 99.97% with the enhanced load-transient response and load regulation of 2.08 μs and 0.040 mV/mA, respectively, with a 20-MHz clock.**

***Index Terms*—Current efficient, digital low-dropout regulator (D-LDO), fast transient, logic threshold voltage (V_{LTH}), successive-approximation-register (SAR), variable-gain accumulator (VG-ACC).**

I. Introduction

AN INTEGRATED power management unit for power-efficient system-on-a-chip (SoC) design should be more versatile in terms of voltage scaling, quiescent current, and transient response, as the functional blocks are further divided into smaller segments [1]. According to this trend, the power supply networks commonly have a hierarchical structure composed of a power-efficient switching-mode regulator and a post regulator for more precise voltage and current scaling adaptively to various load circuits [1]–[3] as shown in Fig. 1(a). Conventionally, analog low-dropout regulators (A-LDOs) have prevailed as post regulators owing to their fast transient response, low quiescent current, large unity-gain bandwidth (UGF), and high power supply rejection, and also because they do not require load capacitors in many cases [4]–[8]. Digital LDOs (D-LDO) have hitherto been considered as an inferior alternative, because most of the performance metrics can be enhanced at the expense of power-hungry clock boosting.

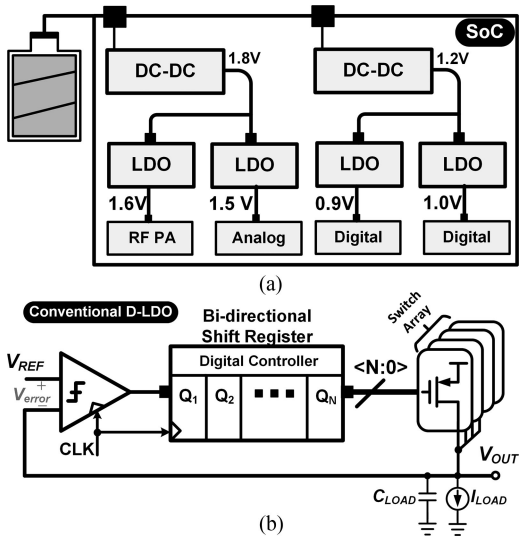

Fig. 1. (a) Low-voltage power management solution of a mobile SoC. (b) Block diagram of conventional D-LDO.

However, the D-LDOs have started to provide better performance in a design environment where the supply voltage range is in the near-/subthreshold voltage as the CMOS process is further developed into the ultradeep submicron technologies, because the error amplifiers in the A-LDOs are degraded by the reduced dynamic range and lowered gain at such a low supply voltage [9]–[11]. The block diagram of the conventional D-LDO is shown in Fig. 1(b). It consists of a comparator, digital controller, and binary-weighted array of PMOS switches. The comparator quantizes the voltage error (V_{error}) between

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the reference voltage ($V_{\rm REF}$) and the output voltage ($V_{\rm OUT}$), and the digital controller tunes up the PMOS switch array to generate a target voltage by reducing $V_{\rm error}$ while securing stability.

In D-LDOs, bi-directional shift registers are extensively used as digital controllers either in single-loop [12], fine/coarse dual loop [13] or tri-loop [14] operation owing to their simple architecture and ease of control. However, in this synchronous system, the main characteristics of transient response, load regulation, quiescent current, and even voltage ripples are dependent on clock frequency and can only be enhanced by boosting the clock frequency, which requires more current consumption. Therefore, the enhancement of these performance characteristics in D-LDOs should be evaluated in terms of current efficiency.

For a power-efficient design, the scheme of gain boosting was developed in [15], where the loop gain is boosted only when the D-LDO is in transient response, and it is returned to the decreased gain for minimizing quiescent current. However, its transient response is still not competitive even in the boosted gain mode. Another scheme based on the Johnson counter for the switched gain mechanism demonstrated the improved transient response time, but its quiescent current is too high at the cost of fast transient response [16]. A good design tradeoff between fast transient response and high current efficiency was demonstrated in [17]–[19]. The work in [17] enhanced the over/undershoots of $V_{\rm OUT}$ during load transient response by using the proposed hill-climbing and binary search controller. Another work in [18] implemented a binary search algorithm with sub-LSB duty control and achieved very fast response time and eliminated the external de-coupling capacitor with on-chip integration. Furthermore, the work in [19] showed enhanced performance by using a bidirectional barrel shifter instead of the conventional single-bit shift registers for faster controller operation. However, all the works in [17]–[19] have limited applications owing to low driving capability and the work in [18] suffers from large steady-state ripples owing to sub-LSB duty control and exhibits poor load regulation. In addition to using the multiloop controller to provide switched loop gain, the tradeoff problem between clock frequency and power consumption, innate in the synchronous D-LDO, can be resolved by the techniques of an asynchronous multi-step switching controller [20], [21]. However, these structures are inherently too sensitive to process-voltage-temperature (PVT) variations because their delay increases significantly and can be made unpredictable around near-/subthreshold supply voltage.

Accordingly, we present a new fast transient D-LDO using a new scheme of logic-threshold triggered comparator (LTTC) based on a combination of voltage reference and CMOS inverter circuits, and a multimode switchable controller to achieve high current efficiency. This paper is divided into the following sections. The architecture of our D-LDO and the proposed transient enhancement scheme are described in Section II. The implementation of the building blocks is discussed in Section III. The measurement results are shown in Section IV. We finally conclude our paper in Section V.

II. Proposed D-LDO Regulator: Architecture

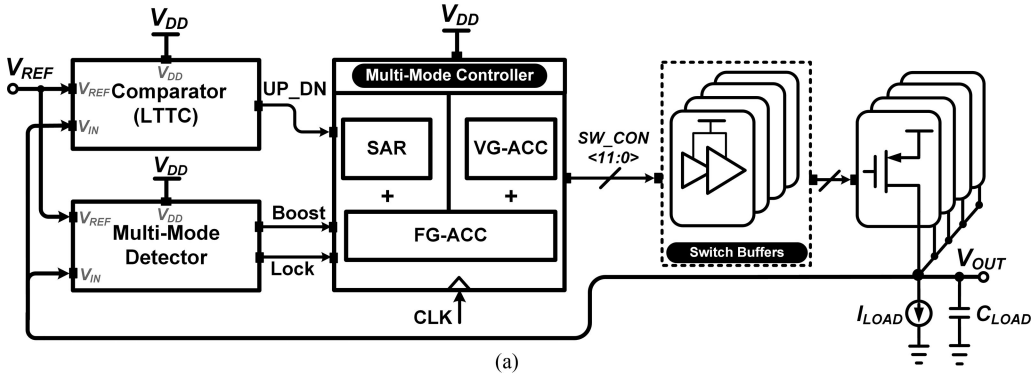
Fig. 2(a) shows the block diagram of the proposed D-LDO which consists of an LTTC, a multimode controller, and a 12-bit binary-segmented MOS array for power transistor. The proposed multimode controller includes three subcontrollers: a successive approximation register (SAR) controller, a variable-gain accumulator (VG-ACC), and fixed-gain accumulator (FG-ACC). The LTTC circuit produces a single-bit digital output of UP_DN such that it goes "HI" if $V_{\rm OUT} < V_{\rm REF}$ and "LOW" if $V_{\rm OUT} > V_{\rm REF}$, where the former and the latter cause the output of controller, *SW_CON<11:0>,* to be incremented and decremented, respectively. By the feedback loop operation, *SW_CON<11:0>* is settled to a target value such that the switch array can supply the required load current while maintaining the target voltage $V_{\rm REF}$. The multimode detector selectively activates a subcontroller in the multimode controller with two bits "Boost" and "Lock" according to the *in situ* detection of $V_{\rm OUT}$. Depending on the bit combination shown in Fig. 2(b), the multimode controller is switched as follows: VG-ACC for [0, 0], FG-ACC for [0, 1], and SAR for [1, 0] in the order of [Boost, Lock], which are enabled during load transient state(STA2), steady state(STA1), and start-up state(STA0), respectively, as shown in the state diagram in Fig. 2(b). The [Boost, Lock] signals cannot be [1, 1] at the same time, because those signals are mutually exclusive each other.

Fig. 3 shows an example transient response of the proposed D-LDO. At the initial start-up mode, the large difference between $V_{\rm OUT}$ and $V_{\rm REF}$ triggers the SAR controller for fast acquisition, which performs a binary search algorithm starting from the MSB of the control word, *SW_CON <11:0>*. After the iteration corresponding to the number of bits, the FG-ACC with a 1-LSB incremental gain is activated to reduce the voltage ripples and quiescent current simultaneously. If the load current is abruptly changed during the steady state at t_2, $V_{\rm OUT}$ deviates from $V_{\rm REF}$ owing to the over/undershoot peaking, whose magnitude is dominantly proportional to the load capacitor and the rate of change of the load current. If the multimode detector senses the voltage error outside the lock range, the VG-ACC is switched ON such that $V_{\rm OUT}$ is quickly settled again to $V_{\rm REF}$ according to the change of the load current. When the voltage error is reduced within the lock range again, our multimode controller is returned to FG-ACC. In this mode of operation, the proposed VG-ACC enhances the performance of load transient response by effectively reducing the over- or under-shoot peaks.

III. Circuit Design of Building Blocks

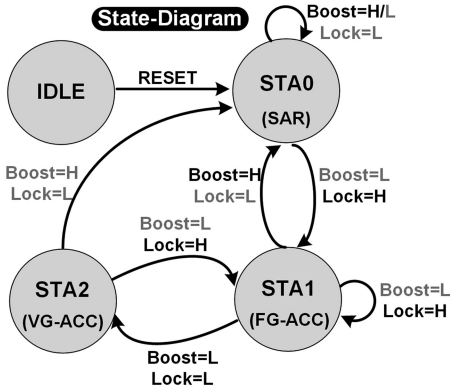
A. Logic-Threshold Triggered Comparator

Conventionally, the voltage comparator has been designed using an open-loop high-gain amplifier or dynamic latch-based circuits. The voltage comparators that use amplifiers offer high precision and high speed at the cost of power consumption, and the voltage comparators that use dynamic latches reduce the power consumption drastically, but require clocking for a regular balancing of the latch. Moreover, such the dynamic comparators



(a)

Multi-Mode Detector Bit Combination		
Mode	Boost	Lock
Not Possible	1	1
SAR	1	0
FG-ACC	0	1
VG-ACC	0	0



(b)

Fig. 2. (a) Block diagram of a proposed D-LDO. (b) Output bit combination of a multimode detector and state-diagram illustrating the switching of a proposed multimode controller.

suffer from input-referred latch offset, mismatches owing to unbalanced parasitic capacitance, and kickback noise [22]–[24]. As an alternative design, a transition-inverter-quantizer comparator (TIQC) can be used as a nonclocked voltage comparator [25]. We propose a new scheme based on such an inverter-based comparator, which provides the advantages of simple structure, enhanced power efficiency, faster speed and significant area reduction, compared with the conventional comparators. The logic threshold voltage ($V_{\rm LTH}$) of a CMOS inverter is determined by the aspect ratio between PMOS and NMOS and the supply voltage, $V_{\rm DD}$, as follows:

$$V_{\rm LTH} = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}} V_{\rm DD} + \left(V_{Tn} - \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\,|V_{Tp}|\right)}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}} \quad (1)$$

where NMOS and PMOS are defined using the mobility (μ_n, μ_p), channel width (W_n, W_p), and threshold voltage (V_{Tn}, V_{Tp}). In this equation, we can observe that $V_{\rm LTH}$ is linearly scaled with $V_{\rm DD}$ because such $V_{\rm LTH}$ can be defined as the input voltage required to achieve the same output as the input in voltage domain, and it can be easily derived from dc analysis of a CMOS inverter using a quadratic current equation in a long-channel device [26]. Using this property, we propose an LTTC as shown in Fig. 4(a), where M1 and M2 have the same size as M3 and M4, respectively.

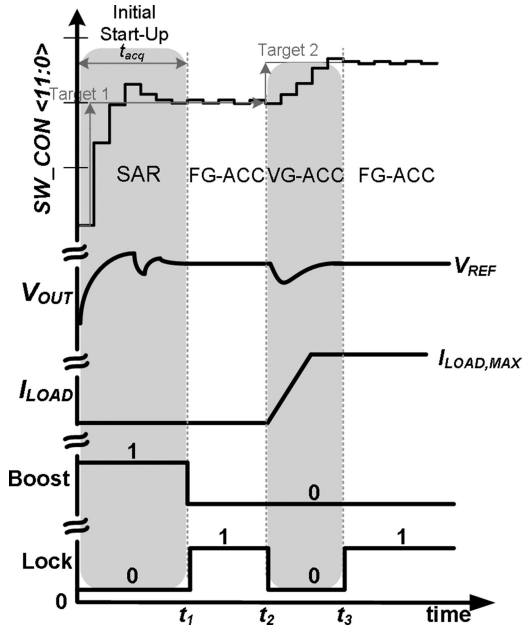


Fig. 3. Example transient response of a proposed D-LDO.

The first diode-connected inverter (M1, M2) generates the logic threshold voltage ($V_{\rm REF'}$) from the input of $V_{\rm REF}$, and it is fed to the next inverter (M3, M4). Fig. 4(b) illustrates the

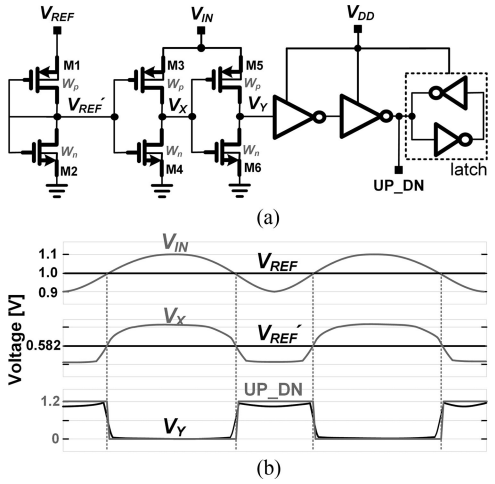


Fig. 4. Proposed LTTC: (a) circuit diagram and (b) example waveforms illustrating the operation of LTTC.

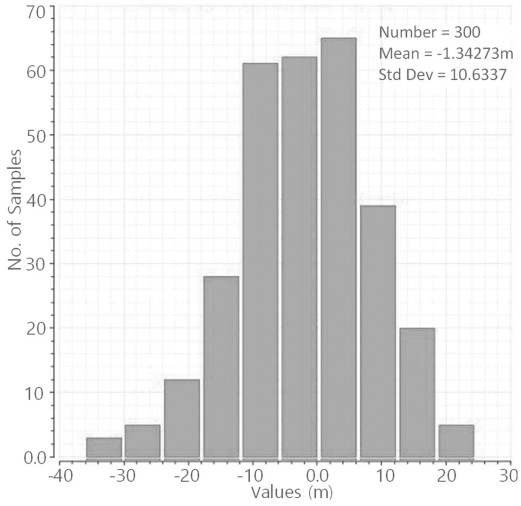


Fig. 5. Monte-Carlo simulation result of the proposed LTTC.

example waveforms of LTTC when $V_{\rm REF}$ is at 1.0 V and $V_{\rm IN}$ is varied in a sinusoidal waveform with an amplitude of 100 mV from 0.9 V–1.1 V. Fig. 4(b) shows that $V_{\rm REF'}$ is generated according to $V_{\rm REF}$ level and it is approximately 0.582 V for this case. While, V_X is toggled to "HIGH" or "LOW" when $V_{\rm LTH}$ varied by $V_{\rm IN}$ crosses $V_{\rm REF'}$. As shown in Fig. 4(b), if $V_{\rm IN} < V_{\rm REF}$, $V_{\rm LTH}$ of the second inverter (M3, M4) becomes lower than $V_{\rm REF'}$ and causes V_X to be $V_{\rm IN}$. Contrarily, if $V_{\rm IN}$ is greater than $V_{\rm REF}$, V_X falls to GND. The chain of inverters and latch supplied with $V_{\rm DD}$ recovers the voltage level to $V_{\rm DD}$, so that it resolves the problem of metastability that happens when $V_{\rm IN}$ comes too close to $V_{\rm REF}$. Theoretically, if $V_{\rm IN}$ becomes exactly equal to $V_{\rm REF}$, V_X will be kept at the same level as $V_{\rm REF'}$. But, the noise or fluctuation on $V_{\rm IN}$ (i.e., $V_{\rm OUT}$) trips the point toward "HIGH" or "LOW". When we design this circuit, we should consider two design issues: the employed CMOS inverter is highly sensitive to PVT variation and the static current should be drawn from the ports of $V_{\rm IN}$ and $V_{\rm REF}$. To solve these issues, we designed the transistors to have a long channel

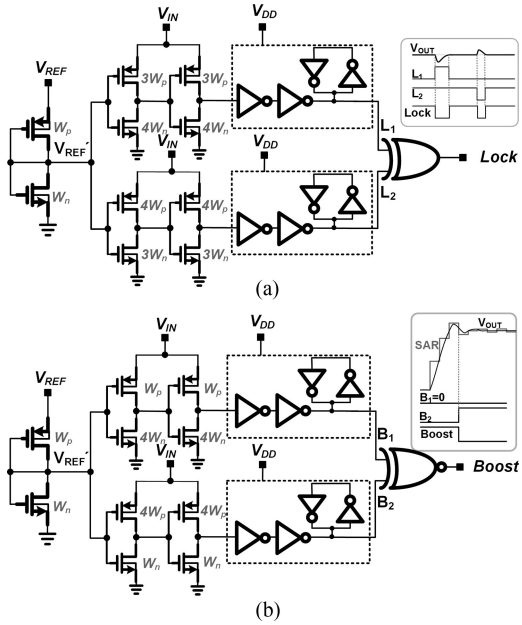


Fig. 6. Schematic and operational waveforms of the proposed multimode detector. (a) Lock detector. (b) Boost detector.

length and small aspect ratio. Moreover, the width of PMOS is designed to be much larger than that of NMOS such that the designed inverter has $V_{\rm LTH} \asymp V_{\rm DD} - |V_{Tp}|$.

When we consider the issue of the static current, we need to observe the short-circuit (SC) current from the inverter made of M3 and M4, where the condition of the maximum SC current happens when $V_{\rm IN}$ is exactly equal to $V_{\rm REF}$. With this condition, the maximum static current is 1.9 μA totally in our LTTC when $V_{\rm IN}$ and $V_{\rm REF}$ are commonly set to 1.1 V. As we concerned above, the static current can be a problem to connect the LTTC to the bandgap and the D-LDO output, we found that it is low enough to avoid the issue. The Monte Carlo simulation was performed 300 times to see the voltage offset caused by process variations in a statistical way. We recorded the offset between $V_{\rm IN}$ and $V_{\rm REF}$ at the instant when V_X is toggled, while $V_{\rm IN}$ is swept from 0 to $V_{\rm DD}$. Also, $V_{\rm REF}$ and $V_{\rm DD}$ are set to 1 and 1.2 V, respectively. In this simulation, LTTC has the voltage offset with the mean value of –1.34 mV and the standard deviation of 10.6 mV as shown in Fig. 5. Moreover, in our case, $V_{\rm IN}$ and $V_{\rm REF}$ are connected to the regulated output of $V_{\rm OUT}$ and the band-gap voltage having high PSRR, respectively. Therefore, our LTTC can avoid the problem that the logic threshold is varied by the supply variation, which happen in the conventional TIQC.

B. Multimode Detector

We propose a multimode control scheme that selects a subcontroller in the multimode controller depending on the segmented voltage range defined by the proposed on-the-fly multimode detector in order to achieve fast transient response and low-level quiescent current simultaneously. For the design of the multimode detector, we modified the scheme of the LTTC to have a skewed logic threshold voltage ($V_{\rm LTH}$), obtained by tweaking the size ratio between PMOS and NMOS using the

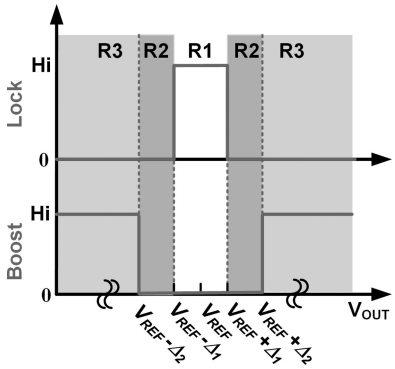


Fig. 7. Segmented voltage regions for the lock and boost detection technique to activate the controllers.

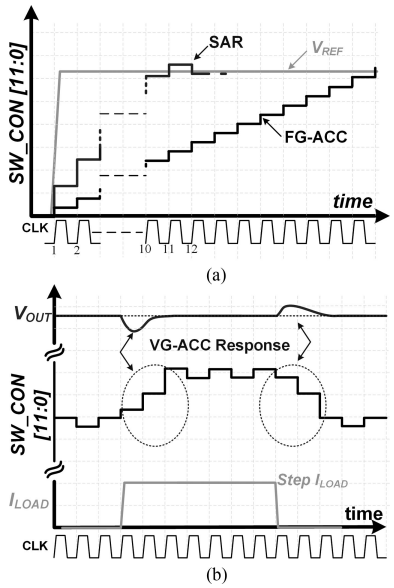


Fig. 8. Illustration of the response of the proposed multimode controller. (a) Acquisition time comparison of SAR controller with FG-ACC. (b) Proposed VG-ACC.

reference ratio of W_p/W_n. We have designed two detectors lock and boost detectors. Each detector has two LTTC cores with a logic threshold separated symmetrically from the common reference $V_{\mathrm{REF}'}$.

In the lock detector shown in Fig. 6(a), the quantization levels of the upper LTTC and lower LTTC determine the lower and upper limits of the lock range, respectively. Similarly, the boost detector sets the upper and the lower limits of the wider boost range and subsequently it negates the output to cover the region outside the limits as shown in Fig. 6(b). Unlike other mode detectors in [13] and [27], where external or on-chip resistor divider networks were required, respectively, to provide the segmented V_{REF} for two comparators, the proposed multimode detector is designed using the logic gates like CMOS inverter and latch with small area. Moreover, it reduces the current consumption by eliminating the redundant transition caused by recharging in the dynamic comparator.

With this design, we can define the three-segmented regions region_1 (R1), region_2 (R2), and region_3 (R3) around the center of V_{REF} as presented in Fig. 7. The lock detector and boost detector generate "HI" for region 1 and region 3, respectively. Therefore, region 2 can be sensed by all zero values from both the detectors. The signal of lock is triggered as "HI" when the target voltage is approached, and it activates the FG-ACC. When the voltage difference between V_{REF} and V_{OUT} is sufficiently large to be placed in R3, the signal of boost is triggered and it activates the SAR controller to achieve fast acquisition response. Moreover, the VG-ACC is activated between the regions of lock and boost, such that the D-LDO re-acquires the target V_{OUT} quickly by providing the load-adaptive current.

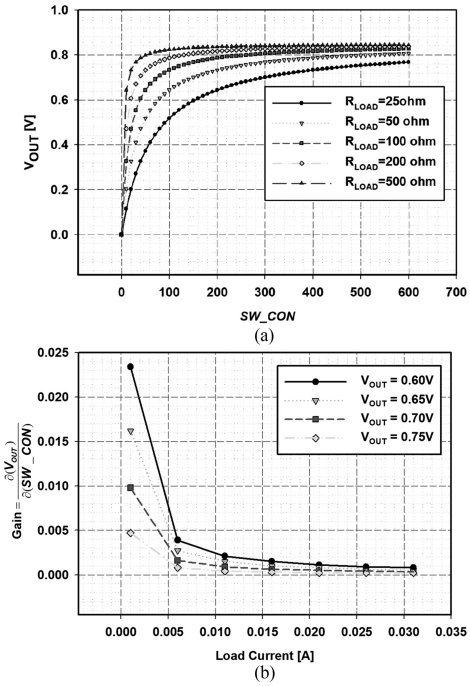


Fig. 9. (a) Output response of the proposed D-LDO, V_{OUT} versus SW_CON by varying the load resistor. (b) Small-signal gain of switch array versus load current.

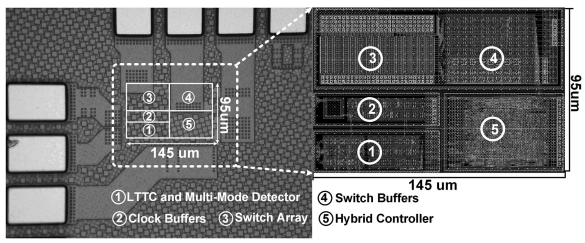


Fig. 10. Layout and chip micrograph of the proposed D-LDO.

C. Digital Programmable Multimode Controllers: SAR and VG-ACC With FG-ACC

The proposed multimode controller incorporates three different kinds of controllers: FG-ACC, SAR, and VG-ACC as previously discussed. The default controller is FG-ACC designed using only an accumulator that increments or decrements by one LSB every clock cycle. The other two controllers enhance the transient response of the D-LDO. The proposed SAR controller

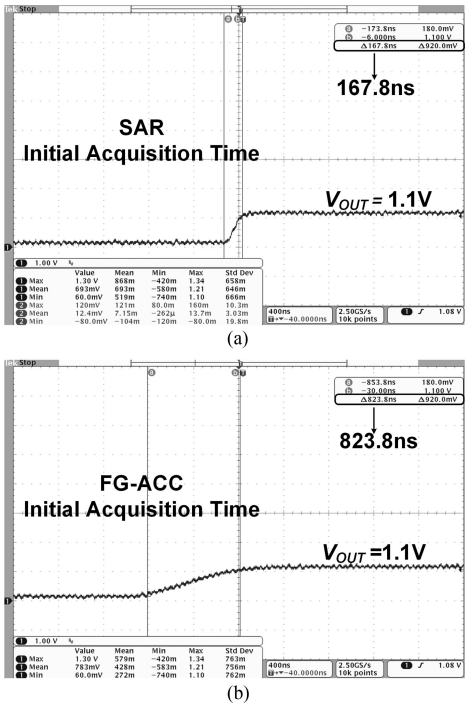


Fig. 11. Oscilloscope captures illustrating the initial acquisition response time using (a) SAR and (b) FG-ACC.

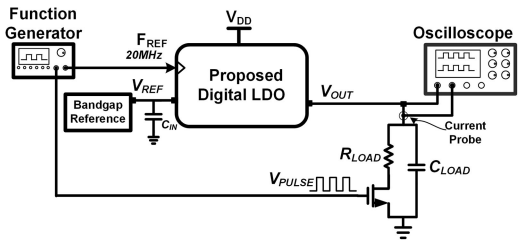


Fig. 12. Complete set-up to measure the load transient response of the proposed D-LDO.

performs a binary search algorithm, which is activated when there is a significant change in V_{REF}, V_{OUT}, or load current, including the initial start-up process after every RESET in an SoC environment. It is not an accumulator-based controller unlike two other controllers, but a state machine that performs a binary-search algorithm.

Fig. 8(a) shows the example waveforms of SAR controller and its comparison with the default FG-ACC. In the SAR mode, the proposed D-LDO operates based on the binary-search algorithm, and each bit of *SW_CON <11: 0>* is determined bit by bit per a clock period in order of MSB to LSB according to the resolving output of LTTC. For the loop stability, the loop delay until when the variation of V_{OUT} caused by the triggering output of the LTTC becomes stable was made shorter than the clock period in this design. Once the discrimination of each bit is finished at LSB, all the bits in *SW_CON* are maintained unchanged independent of further variation of V_{OUT}. This algorithmic approach offers the fast acquisition independent of the initial voltage difference. A more aggressive fact is that V_{OUT} can be reached to the target voltage more quickly than the number of cycles, because some of lower bits have a trivial effect on

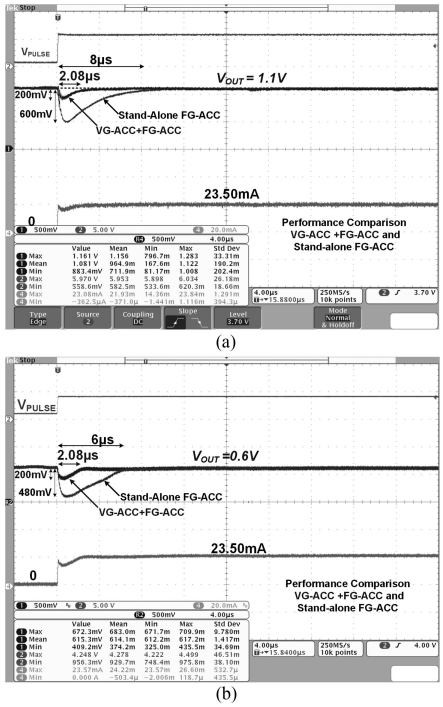


Fig. 13. Representative oscilloscope captures illustrating the measured transient response using the proposed multimode controller VG-ACC+FG-ACC and its comparison with the stand-alone FG-ACC at (a) $V_{\mathrm{OUT}} = 1.1$ V with $V_{\mathrm{DD}} = 1.2$ V and (b) $V_{\mathrm{OUT}} = 0.6$ V $V_{\mathrm{DD}} = 0.7$ V.

the voltage. But, such an SAR controller does not provide the desirable operation for a load transient case because it can cause large under/overshoots during the load change. These large and infrequent under/overshoots are highly undesirable particularly in the case of infrequent and large current transients. Therefore, we propose an accumulator-based VG-ACC with a variable gain functionality specifically to achieve the fast-transient response time effectively for load current change as compared to FG-ACC and less voltage ripples and spikes as compared to SAR. Fig. 8(b) illustrates the response of the proposed VG-ACC. Fig. 9(a) is a characteristic curve of the switch array given by V_{OUT} versus *SW_CON,* from the 2, while V_{DD} is set to 0.85 V and the load resistor (R_{LOAD}) is swept from 25 to 500 Ω:

$$V_{\mathrm{OUT}} = \frac{R_{\mathrm{LOAD}}}{R_{\mathrm{LOAD}} + \frac{r_O}{\mathrm{SW\_CON}}} V_{\mathrm{DD}} \tag{2}$$

As we can see here, V_{OUT} is more rapidly saturated to V_{DD} as R_{LOAD} becomes higher, thus the load current is decreased.

At extremely no-load condition, V_{OUT} is saturated to V_{DD} even when only a single LSB transistor is turned ON. Assuming that the dropout voltage is 100 mV and V_{OUT} is 0.75 V as a result of the D-LDO operation, the value of *SW_CON* increases as the number of turned-on transistors must increase as the load current increases. Also, with V_{OUT} fixed at 0.75 V, the gradient of each curve decreases as the load current increases. The decrease in the effective gain of the switch array with the load current is redrawn in Fig. 9(b), where it shows the small-signal gain of the switch array against the load current, obtained while V_{DD} is set to 0.85 V and V_{OUT} is swept from 0.6 to

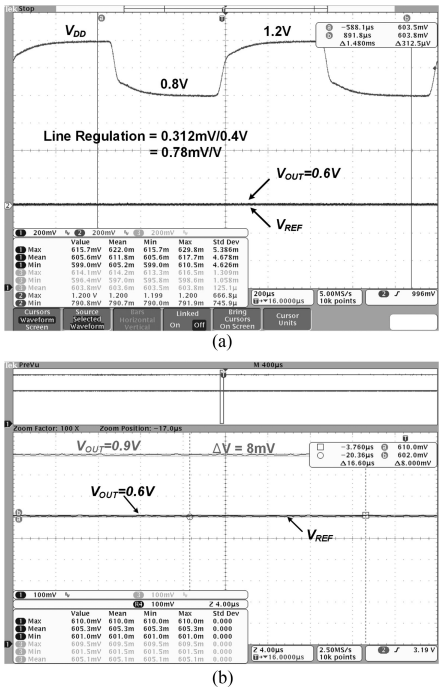


Fig. 14. Oscilloscope captures illustrating the (a) dc line regulation performance of the proposed D-LDO at $V_{\rm OUT} = 0.6$ V and (b) steady-state ripples of the proposed D-LDO at $V_{\rm OUT} = 0.6$ V and at $V_{\rm OUT} = 0.9$ V.

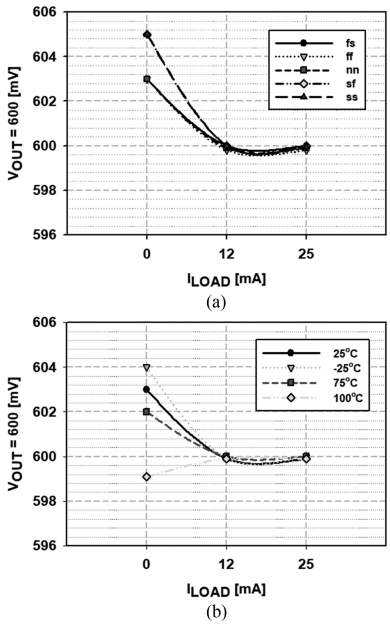


Fig. 15. Simulation results for dc load regulation of the proposed D-LDO for (a) process variations and (b) temperature variations.

0.75 V. This effect causes to reduce the whole loop gain (i.e., UGF) of the D-LDO at higher load current, which is a common problem of D-LDO. Our proposed VG-ACC responds to the *in situ* value of *SW_CON*, so it increases its incremental gain of accumulation at larger *SW_CON*. The variable gain, starts from one and then increases up to 32 by a power of two depending on the *SW_CON* value and it is programmed in a lookup table. This results in compensation of the loop gain degraded at a higher load current, which means that the VG-ACC provides a small gain at a lower load current and a large gain at a higher load current into the whole loop gain.

Moreover, as shown in the state diagram of Fig. 2(b), the controller does not switch from VG-ACC to SAR, because the undershoot on the $V_{\rm OUT}$ for load current change within the maximum driving capability is not big enough to trigger the boost signal, i.e., to activate SAR. If the load current changes beyond the limit, the transition of STA2 (VG-ACC) to STA0 (SAR) can be triggered by the multimode detector when a big voltage deviation is induced on the $V_{\rm OUT}$ at a steady state.

In this case, our D-LDO forces to set the *SW_CON<11:0>* to "1000_0000_0000" as an initial value, not to all zero unlike in the case of the system reset.

IV. Measurements

The proposed D-LDO has been fabricated using a 65-nm CMOS process. Fig. 10 shows the chip layout and die photograph, with an active area of 0.014 mm^2. The proposed D-LDO is designed to produce $V_{\rm OUT}$ in the range of 0.6 to 1.1 V by having the minimum dropout voltage of 100 mV with the supply voltage at 0.7 to 1.2 V. Fig. 11 shows the initial acquisition process of D-LDO with the SAR mode and the FG-ACC mode for comparative study. As expected, the SAR controller for the initial start-up decreases the initial acquisition time significantly. As shown in Fig. 11, with a 20-MHz clock, the D-LDO in the SAR mode spends 167 ns or more to reach the target voltage, whereas it requires more than 823 ns in the FG-ACC mode. Hence, it is observed that the initial acquisition time is reduced by 80% using only the SAR controller. The load transient response of the D-LDO is evaluated by switching the $R_{\rm LOAD}$ with the N-type MOSFET (2N7000) as shown in Fig. 12. Fig. 13(a) and (b) shows the load transient response at $V_{\rm OUT} = 1.1$ V and at $V_{\rm OUT} = 0.6$ V from $V_{\rm DD} = 1.2$ V and $V_{\rm DD} = 0.7$ V, respectively, enabled by the multimode controller (VG-ACC+FG-ACC), when $I_{\rm LOAD}$ is switched from 0 to 23.50 mA. The proposed multimode controller (VG-ACC+FG-ACC) shows a transient response time of 2.08 μs and undershoot of 200 mV at both output voltage levels for $I_{\rm LOAD}$ step of 23.50 mA. However, the performance comparison of VG-ACC+FG-ACC and the stand-alone FG-ACC shows that the stand-alone FG-ACC exhibits poor transient response, i.e., the load transient response time of 8 and 6 μs, and the undershoot of 600 and 480 mV, at $V_{\rm OUT} = 1.1$ and 0.6 V, respectively, because it increments (or decrements) the *SW_CON* by only one LSB per single clock cycle. Therefore, we can observe that, with the assistance of VG-ACC, the load transient response is reduced by 65.3% and the peak of undershoot is reduced by 58.3% at $V_{\rm OUT} = 0.6$ V from $V_{\rm DD} = 0.7$ V, compared with the stand-alone FG-ACC. In addition to the enhancement in transient response time and undershoot, the proposed D-LDO achieves the precise load regulation with 0.04 mV/mA while driving a load current of 23.50 mA. Moreover, the proposed D-LDO consumes a low-level quiescent current of 6 μA when it drives the load current of 23.50 mA at $V_{\rm DD}$ of 0.7 V, and thus the current efficiency amounts to 99.97%. Therefore, the VG-ACC contributes to the improvement of the load transient response, and subsequently the FG-ACC enabled

TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART D-LDOS

Parameters	Proposed	[12] 2010	[16] 2014	[17] 2016	[18] 2017	[19] 2016
Process [nm]	65	65	32	130	65	130
Input Voltage [V]	0.7–1.2	0.5–1.2	0.7–1.0	0.45–1.2	0.5–1.0	0.5–1.2
Output Voltage [V]	0.6–1.1	0.45	0.5–0.9	0.35–1.15	0.3–0.45	0.45–1.14
Max. I_{LOAD} [mA]	25	0.2	5	1.5	2	4.6
Load Capacitor [nF]	1	100	0.1	1	0.4	1
ΔV_{OUT} [mV] @ ΔI_{LOAD} [mA]	200 @ 23.5	40 @ 0.18	150 @ 3	100 @ 1.48	40 @ 1.06	90 @ 1.4
Transient Response [μs] @ ΔI_{LOAD} [mA]	2.08 @ 23.50	590 @ 0.18	0.01 @ 3	1.6 @ 1.48	0.1 @ 1.06	1.1 @ 1.4
Load Regulation [mV/mA]	0.04	0.65	2	0.6	$<$5.6	$<$10
Line Regulation [mV/V]	0.78	3.1	N. R	1.6	2.3	$<$2*
Quiescent Current [μA]	6	2.7	92	8.9	14	751
Current Efficiency [%]	99.97	98.7	97.8	99.40	99.8	98.30
FOM1 [pA.s]**	0.06	66	0.64	0.77	0.23	53
FOM2 [ps]***	2.17	333330	153	406	199	34500
Area [mm^2]	0.014	0.042	0.0077	0.030	0.0023	0.114

For the proposed D-LDO, both FOMs are calculated based on $V_{\mathrm{DD}} = 0.7$ V and $V_{\mathrm{OUT}} = 0.6$ V. Smaller FOMs are better.
N. R: Not Reported. * Estimated form the line regulation graph.
** $\mathrm{FOM1} = \frac{C_{\mathrm{LOAD}} \times \Delta V_{\mathrm{OUT}}}{\Delta I_{\mathrm{LOAD}}} \times \frac{V_{\mathrm{IN}}}{V_{\mathrm{OUT}}} \times I_Q$ *** $\mathrm{FOM2} = \frac{C_{\mathrm{LOAD}} \times \Delta V_{\mathrm{OUT}}}{\Delta I_{\mathrm{LOAD}}} \times \frac{I_Q}{\Delta I_{\mathrm{LOAD}}}$

automatically by the mode detector minimizes the use of the quiescent current and improves the current efficiency.

Fig. 14(a) shows the measurement results for the line regulation of the proposed D-LDO at $V_{\mathrm{OUT}} = 0.6$ V. When V_{DD} is changed from 0.8 to 1.2 V, dc line regulation is equal to 0.78 mV/V as shown in Fig. 14(a). The line regulation accuracy of proposed D-LDO is decided by the factors of the input offset in LTTC and the loop gain at dc in steady state. Fig. 14(b) shows the measured steady-state output ripples at $V_{\mathrm{OUT}} = 0.6$ V and $V_{\mathrm{OUT}} = 0.9$ V, respectively, while driving the I_{LOAD} of 3.11 mA. It is seen that the steady-state ripples become slightly larger at lower load current and higher output voltage, because of the resolution of the switch array. In Fig. 15, the dc load regulation of the proposed D-LDO is evaluated with the corner simulation for process and temperature. It is observed that the dc level of the output voltage increases slightly under the light-load conditions, because the driving current is larger than the required load current.

A comparative study with the existing state-of-the-art D-LDO regulators is presented in Table I. The proposed D-LDO reveals better performance in terms of transient response at a large I_{LOAD} step, load regulation, line regulation, and current efficiency as compared to the other D-LDOs. The proposed D-LDO achieves the smallest figure-of-merits (FOM) among all the compared state-of-the-art D-LDOs.

V. CONCLUSION

In this paper, we presented a D-LDO based on the LTTC with a multimode detection circuit and a multimode programmable controller to achieve fast-transient response with an enhanced level of quiescent current and load regulation. The measurement results, obtained using a 65-nm CMOS prototype chip, demonstrate the maximum current efficiency of 99.97%. While the load current is switched by 23.50 mA, the proposed D-LDO using VG-ACC shows that the transient response time and peaks of V_{OUT} are reduced by 65.3% and 58.3%, respectively, when compared with the conventional FG-ACC. In addition to the enhanced transient response, it also achieves efficient load regulation of 0.04 mV/mA.

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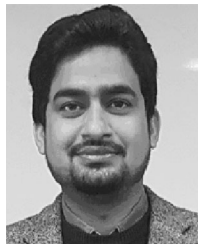

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