Analysis and Design of a Wide-Range Soft-Switching High-Efficiency High-Frequency-Link Inverter With Dual-Phase-Shift Modulation

Shilin Guo, *Student Member, IEEE*, Jianhui Su, Jidong Lai, and Xiang Yu

***Abstract*—A wide-range soft-switching high-efficiency cycloconverter-type high-frequency-link inverter with dual-phase-shift modulation strategy is proposed in this paper. By adding an auxiliary inductor in primary-side full bridge circuit and adopting center-tapped four-winding transformer structure, the soft-switching range for primary-side switches has been extended. The secondary-side active clamper network is designed to recycle leakage inductor energy, and suppress voltage spikes caused by the resonance of the leakage inductor and the parasitic capacitance of switches. One feature of the proposed inverter is that both the primary-side full-bridge and active clamper network employ phase-shift modulation technique where all switches are driven with nearly 50% duty cycle square signals, hence a simple and reliable transformer-isolated gate drive circuit with small transmission delay is presented. Moreover, all switches in the proposed inverter achieve zero voltage switching, which contributes to higher conversion efficiency as well as higher switching frequency. Analysis, design, and implementation of the proposed inverter are discussed in detail. A 200-kHz laboratory prototype for the high-voltage audio amplifier application is developed and the experimental results are presented to validate the analysis and performance of the proposed inverter.**

***Index Terms*—Active clamper network, dual-phase-shift (DPS) modulation strategy, high-frequency–link (HFL) inverter, transformer-isolated gate drive (TIGD) circuit, zero voltage switching (ZVS).**

I. Introduction

COMPARED with the conventional sinusoidal pulse width modulation (SPWM) dc–ac converters with bulky and heavy line-frequency transformers, the high-frequency-link (HFL) inverters employ a high-frequency (HF) transformer to realize galvanic isolation and to match the input and output voltages, which have attributes of more compact size, lighter weight, and higher power density [1]–[23]. HFL inverters have widespread applications in recent decades [1]–[8], including uninterruptible power supply systems [1], renewable energy processing units [2]–[4], electric vehicles battery chargers [5]–[6], direct-conversion audio power amplifier [7]–[8], and especially in submarine or aerospace applications, where the efficiency and power density are very critical features.

HFL inverters could be broadly classified into three typical topologies [9]–[13]: the conventional HFL inverters, the rectifier-type HFL (RHFL) inverters, and the cycloconverter-type HFL (CHFL) inverters. The conventional HFL inverters have three power conversion stages and require intermediate bulky dc-link *LC* filter, leading to lower efficiency and larger size. RHFL inverters have a structure similar to that of the conventional HFL inverters except for removing the bulky dc-link *LC* filter, which reducing the cost and the size of the circuit. However, the dc-link voltage is pulsating dc resulting in more complicated modulation for the secondary-side dc/ac stage [10]–[11]. The CHFL inverters reduce the power conversion stages by directly placing a cycloconverter to the secondary side of the HF transformer, which is of benefit to system efficiency. Additionally, the architecture of CHFL inverters offers bidirectional power flow and reduces system complexity [9], [12]–[13]. Two typical phase-shift modulation strategies, bipolarity and unipolarity, have been proposed and investigated in the literatures [2]–[3], [7] and [8]–[9], [12]–[20], respectively. For the unipolarity phase-shift modulation strategy, the output SPWM voltage waveform is three level, including positive level, negative level, and zero level, thus, secondary-side cycloconverter can realize natural commutation during the zero-level state guaranteeing zero voltage switching (ZVS) of the cycloconverter switches [8].

However, CHFL inverters based on unipolarity modulation strategy suffer from load current commutation problem during the dead time of bidirectional switches of cycloconverter because there is no current flowing path for the filter inductor current, which definitely causes high voltage spikes on SPWM waveform [17]–[20]. A derecouple modulation strategy was proposed to solve the problem [17]. Nevertheless, there is still the issue of synchronized trigger between the primary-side and the secondary-side switches during the zero-crossing point of output voltage [18]. In [19] and [20], overlap commutation switching method was employed to enable natural load current commutation between the bidirectional switches. However, the secondary-side voltage oscillation of HF transformer due to the resonance between transformer leakage inductance and

Manuscript received April 18, 2017; revised September 15, 2017; accepted November 1, 2017. Date of publication November 9, 2017; date of current version June 22, 2018. This work was supported by the National Key R&D Program of China under Grant 2017YFB0903503. Recommended for publication by Associate Editor M. Tavakoli Bina. *(Corresponding author: Jidong Lai.)*

The authors are with the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei 23009, China (e-mail: shilinguo@mail.hfut.edu.cn; su_chen@126.com; laijidong@126.com; yuxiang_hfut@163.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2771765

parasitic capacitances of switches is still serious, which leads to electromagnetic-interference problems, and usually drives MOSFETs into avalanche mode [19]–[23]. An active voltage clamper circuit (ACC) was developed to suppress voltage oscillation in [1] and [20]. However, the duty cycle of driving signals for switches of ACC is a variable value from 0 to 1 and contains low-frequency sinusoidal components, thus, it is difficult for these switches to operate normally in the case of the narrow duty cycle. Meanwhile, adopting optocoupler (OC) is the common way to provide isolation driver for switches of ACC in [1] and [20]. However, the optocoupler has the disadvantages of transmission delay, distortion, low reliability, and limited range of operating temperature [24]–[26].

In addition, the primary side of CHFL inverters in [1] and [20] is constituted of the conventional full-bridge mode circuit, where the soft-switching conditions are highly dependent on primary current of transformer, resulting in primary-side switches partially operating in ZVS across different output power or output voltage range. Especially, when the primary current of transformer is small, the primary switches in [20] are impossible to achieve soft-switching. Passive auxiliary circuits in conventional pulse width modulation (PWM) dc/dc converter have been presented in detail to extend ZVS range for full bridge [27]–[29]. Due to the facts that the phase-shift angle of primary-side H-bridge varies with the output sinusoidal voltage, and the leading bridge and the lagging bridge are automatically alternately switched in the case of zero output voltage, the passive auxiliary circuit for wide ZVS range in the CHFL inverter is required to be reconsidered.

In this paper, an isolated wide-range soft-switching high-efficiency CHFL inverter is proposed. Compared with the inverters in [1] and [20], the proposed CHFL inverter has following features:

1) By adding an auxiliary inductor in conventional full bridge mode circuit and adopting center-tapped four-winding transformer structure, the soft-switching range of primary-side switches has been extended and the proposed CHFL inverter achieves ZVS for all switches under different operating conditions.
2) A dual-phase-shift (DPS) modulation strategy for CHFL inverter is presented, where both the primary-side H-bridge and secondary-side active clamper network employ phase-shift modulation strategy. The active clamper network is utilized to recycle leakage inductor energy and suppress voltage spikes.
3) The duty cycle of driving signals for all switches in the proposed inverter is nearly 50% due to the DPS modulation strategy, thus, a simpler transformer-isolated gate drive (TIGD) circuit for all switches is presented.
4) Two high-voltage clamping diodes that are required to assist commutation in [20] can be omitted and the proposed DPS-CHFL inverter achieves higher efficiency.

This paper is organized as follows. In Section II, the proposed inverter topology, modulation strategy, and the gating signal generation logic are introduced. The operation principles and soft-switching conditions are described in Section III. Design guidelines and processes for key parameters of the proposed inverter are detailed in Section IV. Experimental results of a high efficiency and high switching frequency prototype for the single-stage high-voltage audio power amplifier application [7]–[8], [30]–[31] are demonstrated in Section V. The conclusion is presented in Section VI.

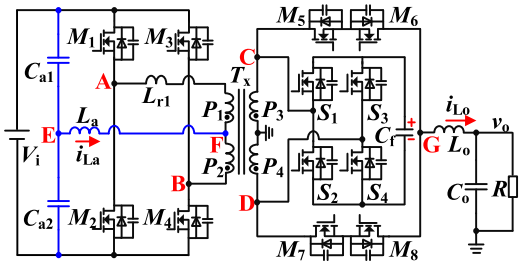


Fig. 1. Proposed DPS-CHFL inverter.

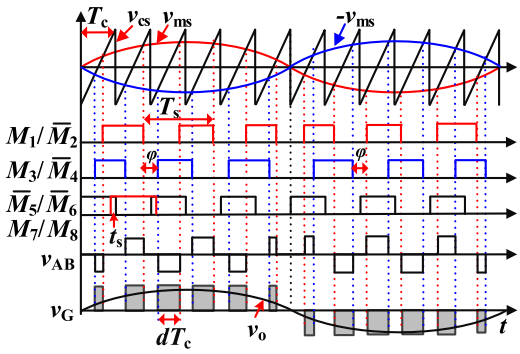


Fig. 2. Phase-shift modulation strategy of DPS-CHFL inverter.

II. DPS-CHFL Inverter and Modulation Strategy

A. DPS-CHFL Inverter

The circuit configuration of the proposed DPS-CHFL inverter is shown in Fig. 1, where V_i represents the input dc voltage and C_{a1} and C_{a2} are two equal capacitors for halving the input voltage. The H-bridge converter at primary side contains switches $M_1 - M_4$ and $T_{\rm X}$ is a four-windings $(P_1 - P_4)$ HF galvanic isolation transformer with turns ratio $n:n:1:1$ $(N_{P1} = N_{P2}, N_{P3} = N_{P4}, n = N_{p1}/N_{p3})$ and the equivalent leakage inductor L_{r1}. The auxiliary inductor L_a is connected to the center tap of primary windings P_1 and P_2, which extends ZVS range for switches $M_1 - M_4$. The secondary-side cycloconverter comprises bidirectional switches M_5/M_6 and M_7/M_8. The active clamper network composed of full-bridge converter $(S_1 - S_4)$ and clamping capacitor C_f is employed to recycle leakage inductor energy and eliminate voltage spikes. L_o, C_o, and R are the filter inductor, filter capacitor, and equivalent load resistance, respectively.

B. Modulation Strategy

Fig. 2 shows the phase-shift modulation strategy, where modulation signals $v_{\rm ms}$ and $-v_{\rm ms}$ are sinusoidal waveforms with a phase-shift of 180°, $v_{\rm cs}$ denotes fixed frequency saw-tooth carrier signal. The drive signals M_1 and M_2 are generated by comparing the carrier signal $v_{\rm cs}$ with the modulation signal $v_{\rm ms}$. Similarly, the drive signals M_3 and M_4 are obtained by com-

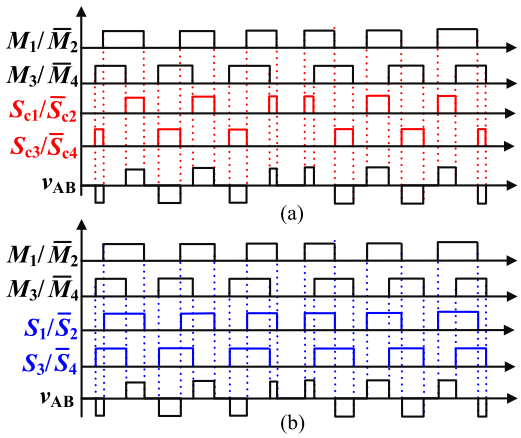


Fig. 3. Active voltage clamping strategy. (a) Conventional PWM clamping strategy. (b) Phase-shift clamping strategy.

paring the $v_{\rm cs}$ with the $-v_{\rm ms}$. When $v_{\rm ms} > 0$, the drive signals M_1 and M_2 lead to M_4 and M_3, respectively; therefore, the bridge leg consisting of switches M_1 and M_2 is defined as the leading leg and the one consisting of switches M_3 and M_4 as the lagging leg. When $v_{\rm ms} < 0$, the switches M_1 and M_2 form the lagging leg and the switches M_3 and M_4 form the leading leg. There is a phase-shift angle φ between the leading bridge leg and lagging bridge leg, which varies with the references $v_{\rm ms}$ and $-v_{\rm ms}$. The drive signals $M_5(M_6)$ and $M_7(M_8)$ are obtained from carrier signal $v_{\rm cs}$ by frequency divider circuit at trailing edge. The commutation overlap time t_s in [20] is adopted to enable natural commutation between the bidirectional switches $M_5(M_6)$ and $M_7(M_8)$ shown in Fig. 1.

As shown in Figs. 1 and 2, $v_{\rm AB}$ is the primary voltage of HF transformer T_x, d is the effective SPWM duty cycle, and the SPWM voltage v_G is modulated into a typical three-level waveform flowing through low-pass filter (L_oC_o) to output voltage v_o.

Yamato *et al.* [1] proposed an active voltage clamper with conventional PWM strategy to enable the CHFL inverter to be free of voltage spikes, as shown in Fig. 3(a), where the duty cycle of driving signals $S_{c1} - S_{c4}$ for switches $S_1 - S_4$ varies from 0 to 1 with the reference signals $v_{\rm ms}$ and $-v_{\rm ms}$ changing. Thus, the gate drive circuits for switches $S_1 - S_4$ are generally implemented with optocouplers to realize galvanic isolation, which limits the life time and the range of operating temperature. In this paper, a novel clamping strategy is proposed, as shown in Fig. 3(b), the drive signals $S_1 - S_4$ for switches $S_1 - S_4$ are the same with driving signals $M_1 - M_4$, respectively, which are nearly 50% fixed duty cycle square signals. Both the primary-side H-bridge and the secondary-side active full-bridge clamper network employ the phase-shift modulation strategy, which can be referred to as DPS modulation strategy.

It can be seen from Figs. 2 and 3(b) that all switches in the proposed DPS-CHFL inverter are driven with nearly 50% fixed duty cycle square signals and the switching period T_s of all switches is twice of the carrier signal cycle T_c, thus, making gate drive circuits for all switches easy to realize.

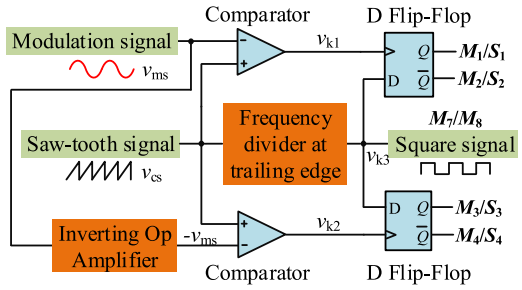


Fig. 4. Gating signal generation logic diagram of DPS-CHFL inverter.

C. Gating Signal Generation Logic

Fig. 4 presents the gating signal generation logic corresponding to the modulation strategy in Figs. 2 and 3(b).

As shown in Fig. 4, the square signal v_{k3} is obtained from the saw-tooth signal $v_{\rm cs}$ by frequency divider circuit at trailing edge, which is used as driving signal of switch M_7/M_8. The signals v_{k1} and v_{k2} are generated by comparing the signals $v_{\rm ms}$ and $-v_{\rm ms}$ with $v_{\rm cs}$, respectively, then the driving signals M_1/S_1 and M_2/S_2 (M_3/S_3 and M_4/S_4) are generated by capturing the value of the square signal v_{k3} at the rising edge of the signal v_{k1} (v_{k2}) with D flip-lop.

III. Operation Principles and ZVS Conditions of the DPS-CHFL Inverter

To simplify the analysis of operation mode of the proposed inverter, some assumptions are considered as follows:

1) All components in the proposed inverter are assumed ideal, except the parasitic capacitor C_p and junction diode D_p of power switches.
2) The switching frequency f_s is much greater than the output voltage frequency f. Thus, in one switching period T_s, the output voltage v_o and modulation signal $v_{\rm ms}$ remain constant.
3) C_{a1} and C_{a2} have equal capacitance value, thus, the v_E is equal to $V_i/2$.

A. Operation Principles of Primary-Side Auxiliary Inductor

As two switches on each leg of primary-side H-bridge are switched alternately and symmetrically with little dead time t_d in between, the auxiliary inductor L_a sees alternating positive, negative, and zero voltage for different intervals. Therefore, the steady-state current through L_a has a trapezoidal shape, which is shown in Fig. 5. The peak value I_{La} of the auxiliary inductor current $i_{La}(t)$ can be obtained as follows, where the leakage inductance L_{r1} and the dead time t_d are negligible

$$I_{La} = \frac{V_i(1-d)T_s}{8L_a}. \tag{1}$$

In system analysis, the physical transformer can be represented by an ideal transformer with a magnetizing inductance L_m. Thereby, the four-winding transformer T_x can be deformed and simplified as Fig. 6(a) for convenient analysis, where L_1 and L_2 referred as the magnetizing inductance are coupled

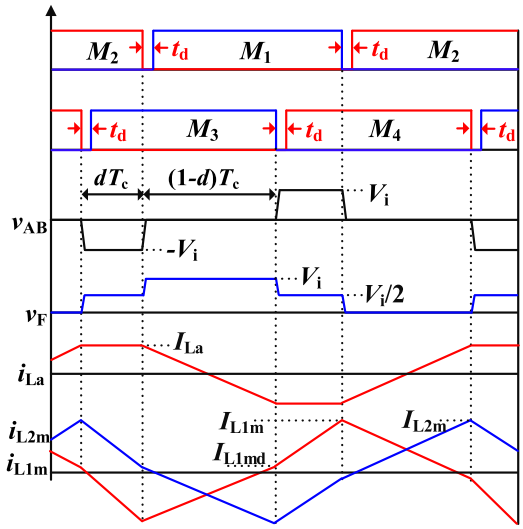


Fig. 5. Operation sequences and auxiliary inductor current waveforms.

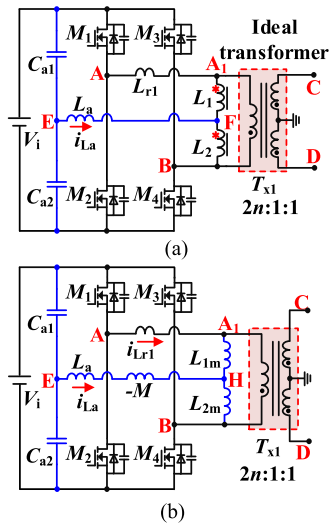


Fig. 6. Primary-side simplified circuit of DPS-CHFL inverter.

inductors in parallel with the primary side of ideal transformer T_{x1}. Considering that the primary-side winding turns $N_{P1} = N_{P2}$, then the coupled inductors $L_1 = L_2 = L_m/4$.

The decoupling equivalent circuit of coupled inductors L_1 and L_2 is shown in Fig. 6(b). It is assumed that the coupling coefficient between L_1 and L_2 is equal to 1, then the mutual inductor M, equivalent inductors L_{1m} and L_{2m} can be obtained as

$$M = \sqrt{L_1 L_2} = L_m/4 \tag{2}$$

$$L_{1m} = L_{2m} = L_1 + M = L_m/2. \tag{3}$$

According to Fig. 6(b), the variations of voltage $v_H(t)$ can be obtained by Kirchoff laws and derived as

$$\frac{v_A(t) - v_H(t)}{L_{1m}} = \frac{v_H(t) - v_B(t)}{L_{2m}} + \frac{v_H(t) - v_E(t)}{L_{ax}} \tag{4}$$

where $L_{ax} = L_a - M = L_a - L_m/4$.

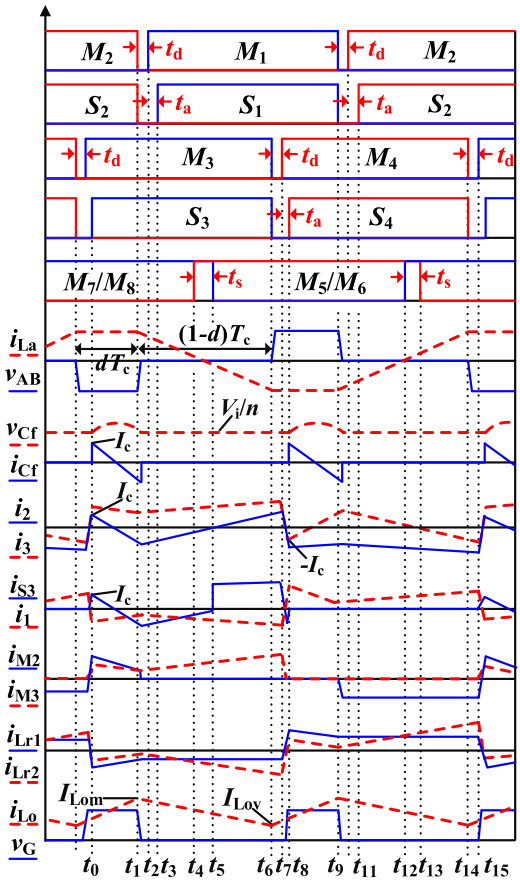


Fig. 7. Operation sequences and key waveforms of DPS-CHFL inverter.

Following the operation sequences shown in Fig. 5 and (4), the voltage $v_H(t)$ can be expressed as

$$v_H(t) = \begin{cases} V_i/2 & 0 \le t \le dT_c \\ V_i \dfrac{2 + k_{mx}/2}{2 + k_{mx}} & dT_c \le t \le T_c \\ V_i/2 & T_c \le t \le dT_c + T_c \\ V_i \dfrac{k_{mx}/2}{2 + k_{mx}} & dT_c + T_c \le t \le 2T_c \end{cases} \tag{5}$$

where the parameter $k_{mx} = L_m/2L_{ax}$.

In terms of voltages $v_A(t), v_B(t)$, and $v_H(t)$, the peak I_{L1m} (I_{L2m}) of current $i_{L1m}(t)$ ($i_{L2m}(t)$) and the defined specific value I_{L1md} of current $i_{L1m}(t)$ shown in Fig. 5 can be calculated as

$$I_{L1m} = I_{L2m} = \frac{V_i T_s}{16 L_a}(1 - d) + \frac{d V_i T_s}{4 L_m} \tag{6}$$

$$I_{L1md} = \frac{V_i T_s}{16 L_a}(1 - d) - \frac{d V_i T_s}{4 L_m}. \tag{7}$$

B. Operation Principles of DPS-CHFL Inverter

Fig. 7 shows the schematic waveforms and operation sequences of the DPS-CHFL inverter corresponding to positive output voltage and positive output current. There are 16 operation modes in one complete switching cycle T_s. The former

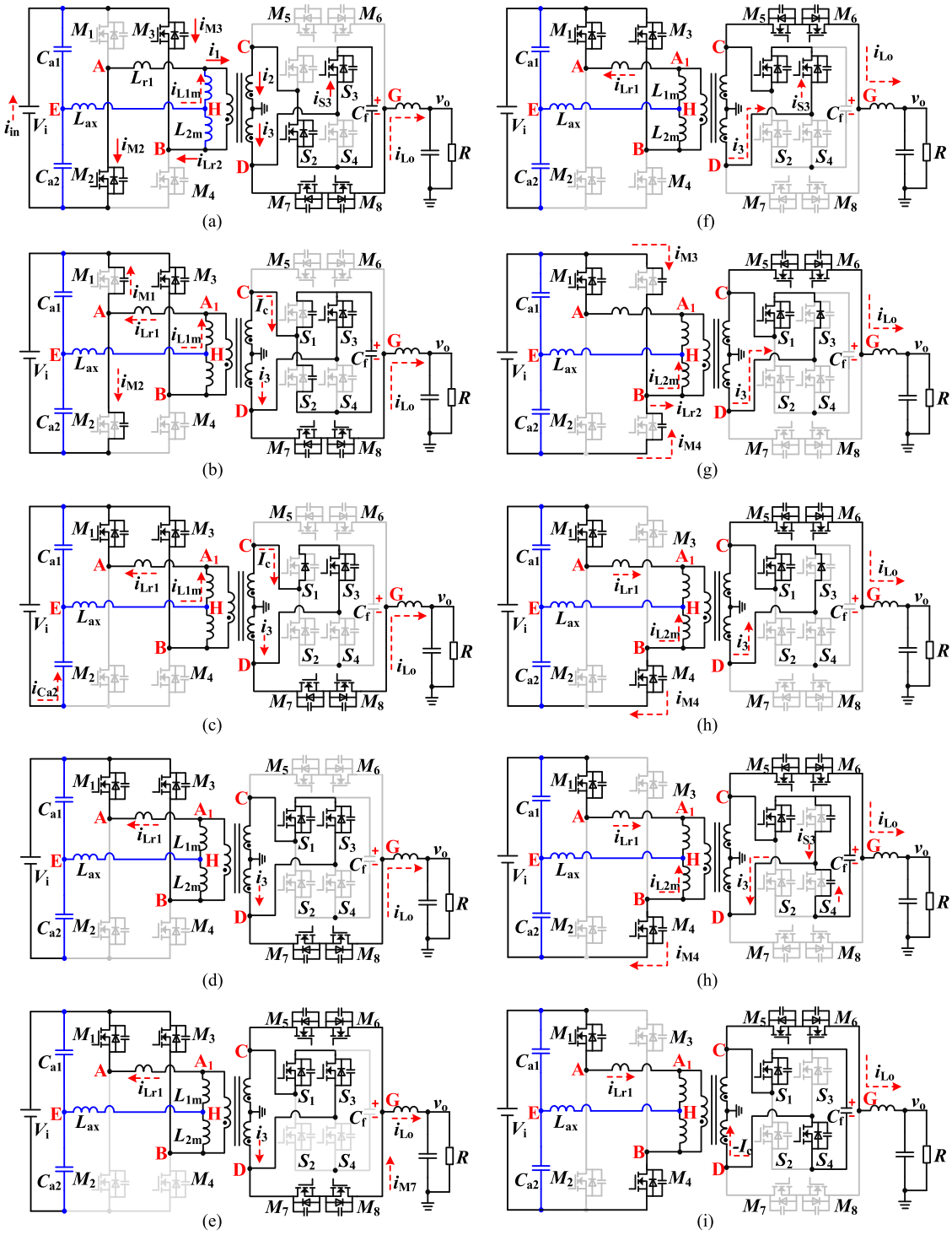


Fig. 8. Equivalent circuit for different modes in half switching cycle for DPS-CHFL inverter. (a) $t_0 - t_1$, (b) $t_1 - t_2$, (c) $t_2 - t_3$, (d) $t_3 - t_4$, (e) $t_4 - t_5$, (f) $t_5 - t_6$, (g) $t_6 - t_7$, (h) $t_7 - t_8$: stage I, (h) $t_7 - t_8$: stage II, (i) $t_8 - t_9$.

eight modes are discussed in detail later and the operation condition of the latter eight modes is symmetric with the former eight modes. The corresponding equivalent circuits for the former eight modes are depicted in Fig. 8.

For the low-pass filter, the steady-state current flowing through filter inductor L_o has the saw-tooth waveform as shown in Fig. 7, I_{Lom} and I_{Lov} are the peak and valley values, respectively, which are given below

$$I_{Lom} = \frac{V_i(1-d)dT_s}{8L_o n} + \frac{dV_i}{2nR} \tag{8}$$

$$I_{Lov} = -\frac{V_i(1-d)dT_s}{8L_o n} + \frac{dV_i}{2nR}. \tag{9}$$

Mode 1 [$t_0 - t_1$, Fig. 8(a)]: The switches M_2, M_3, S_2, S_3, M_7, and M_8 are conducting during this mode and the primary voltage v_{AB} is negative. Energy transfers from dc side to ac side through HF transformer. The clamping capacitor C_f begins to first accumulate charge, and then releases the energy during this mode. Assuming that the secondary current $i_2(t)$ [the definition of variables $i_1, i_2, i_3, i_{M2}, i_{M3}, i_{Lr2}, i_{S3}$ and their positive directions are given in Fig. 8(a)] and capacitor voltage $v_{cf}(t)$ at t_0 are equal to I_c and V_i/n, respectively. Then the variations of voltage $v_{Cf}(t)$ and current $i_2(t)$ can be obtained by Kirchoff laws during $t_0 - t_1$

$$\begin{cases} v_{Cf}(t) = \left(\dfrac{V_i}{n} - k\right)\cos\omega(t-t_0) + \dfrac{I_c}{\omega C_f}\sin\omega(t-t_0) + k \\ i_2(t) = -\omega C_f\left(\dfrac{V_i}{n} - k\right)\sin\omega(t-t_0) + I_c\cos\omega(t-t_0) \end{cases} \tag{10}$$

where ω is the resonant angular frequency and k is the defined factor, which can be obtained as

$$\begin{cases} \omega = \sqrt{\dfrac{L_m L_{r1} + 4L_o L_{r1} n^2 + 4L_o L_m n^2}{4L_o L_m L_{r1} C_f}} \\ k = \dfrac{2L_m(V_o L_{r1} + 2nV_i L_o)}{L_m L_{r1} + 4L_o L_{r1} n^2 + 4L_o L_m n^2} \end{cases}. \tag{11}$$

According to the law of capacitor amp-second balance, the clamping capacitor voltage $v_{cf}(t)$ and current $i_2(t)$ at t_1 can be approximately expressed by

$$\begin{cases} v_{Cf}(t_1) = v_{Cf}(t_0) \\ i_2(t_1) = -i_2(t_0) = -I_c \end{cases}. \tag{12}$$

By simplifying (10)–(12), the current I_c can be calculated as

$$I_c = \frac{\sin(\omega d T_c)}{1 + \cos(\omega d T_c)}\left(\frac{V_i}{n} - k\right)\omega C_f. \tag{13}$$

Mode 2 [$t_1 - t_2$, Fig. 8(b)]: At t_1, M_2 and S_2 are turned OFF simultaneously. In the secondary side, the current $i_2(t_1)\,(i_2(t_1) = -I_c)$ is negative and begins to discharge the parasitic capacitor C_{pS1} of switch S_1 and charge the parasitic capacitor C_{pS2} of S_2, the parasitic capacitor C_{pS1} will be discharged quickly, then the antiparallel diode D_{pS1} of S_1 conducts. In the primary side, the current i_{M2} starts to charge the parasitic capacitor C_{pM2} of M_2 and the current i_{M1} discharges the parasitic capacitor C_{pM1} of M_1. Provided that $C_{pM1} = C_{pM2}$, then i_{M1} is equal to i_{M2} that can be derived as

$$i_{M1}(t_1) = i_{M2}(t_1) = \frac{-2I_c + I_{Lom}}{4n} + \frac{I_{L1m}}{2}. \tag{14}$$

To achieve ZVS turn-on of switch M_1, the value of voltage v_A at t_2 must be clamped to V_i. Thus, the charging current i_{M2} should be enough to make sure the voltage v_{AB} drops to zero within the dead time period $t_d\,(t_1 - t_2)$. Therefore, the required charging current i_{M2} shall satisfy

$$i_{M2}(t_1) \geq V_i C_{pM2}/t_d. \tag{15}$$

Mode 3 [$t_2 - t_3$, Fig. 8(c)]: At t_2, the voltage v_A has been clamped to V_i, the switch M_1 is turned ON at ZVS mode. The antiparallel diode D_{pS1} of switch S_1 is conducting and the voltages $v_{AB,}\, v_C, v_D$, and v_G are clamped to zero guaranteeing ZVS turn-on of S_1.

Mode 4 [$t_3 - t_4$, Fig. 8(d)]: At t_3, switch S_1 is turned ON at ZVS mode. During this mode, the secondary voltages v_C, v_D, and v_G are zero; therefore, switches M_5 and M_6 can be turned ON at zero voltage at t_4 without incurring switching loss. Meantime, the primary voltages v_{A1B} and v_{AB} are zero correspondingly, thus, the voltage v_{Lr1} is clamped to zero and the current i_{Lr1} remains constant. The equivalent circuit of this mode is further simplified as Fig. 9(a), where the $i_{S3} = i_2$ and $i_3 = i_{Lo} + i_2$.

Mode 5 [$t_4 - t_5$, Fig. 8(e)]: At t_4, switches M_5 and M_6 are turned ON in ZVS. To avoid voltage spikes occurrence due to the interruption of continuous filter inductor current i_{Lo}, overlap commutation time $t_s\,(t_4 - t_5)$ is employed to enable natural commutation between bidirectional switches M_5/M_6 and M_7/M_8 in soft-switching mode.

Mode 6 [$t_5 - t_6$, Fig. 8(f)]: At t_5, switches M_7 and M_8 are turned OFF in ZVS condition. The equivalent circuit of this mode is further simplified as Fig. 9(b), where the $i_{S3} = i_3$ and $i_3 = i_{Lo} + i_2$. It can be seen from Fig. 7 that the current i_{S3} changes from $i_2(t_5)$ to $i_3(t_5)$ immediately, however, the primary currents i_{Lr1} and i_1 remain constant.

During the interval of $t_1 - t_6$, the voltage v_{Lr1} of leakage inductor L_{r1} is keeping to zero, thus, the leakage inductor current i_{Lr1} remains unchanged, which is given as

$$i_{Lr1}(t_1) = i_{Lr1}(t_6) = (2I_c - I_{Lom})/2n - I_{L1m}. \tag{16}$$

Additionally, during the interval of $t_1 - t_6$, the current i_{L1m} assures a linearly increase, which is equal to I_{L1md} at t_6, thus, the primary-side currents $i_1(t)$ and $i_{Lr2}(t)$ at t_6 are deduced as follows:

$$\begin{aligned} i_1(t_6) &= i_{Lr1}(t_6) - I_{L1md} \\ i_{Lr2}(t_6) &= i_1(t_6) - I_{L2m}. \end{aligned} \tag{17}$$

According to Fig. 9(b), the relationship between the primary current $i_1(t)$, secondary current $i_2(t), i_3(t)$, and the filter inductor current i_{Lo} at t_6 can be expressed as

$$\begin{cases} i_2(t_6) + i_3(t_6) = -2n^* i_1(t_6) \\ i_2(t_6) + I_{Lov} = i_3(t_6) \end{cases}. \tag{18}$$

Substitution of (16) and (17) into (18), leads to

$$i_3(t_6) = -I_c + (I_{Lom} + I_{Lov})/2 + n(I_{L1m} + I_{L1md}). \tag{19}$$

Mode 7 [$t_6 - t_7$, Fig. 8(g)]: At t_6, switches M_3 and S_3 are turned OFF simultaneously. In the secondary side, according to (19) and Fig. 7, the current $i_3(t_6)$ is positive and flows through the antiparallel diode D_{pS3} of switch S_3, thus, the voltages v_C, v_D, and v_G are still clamped to zero. In the primary side, the current i_{M3} starts to charge the parasitic capacitor C_{pM3} of M_3, and at the same time the current i_{M4} discharges the parasitic capacitor C_{pM4} of M_4. To achieve ZVS turn-on of switch M_4, the value of voltage v_B must be clamped to zero. Thus, the current i_{M4} is employed to make sure the voltage v_B drops to zero within the dead time period t_d, which can be

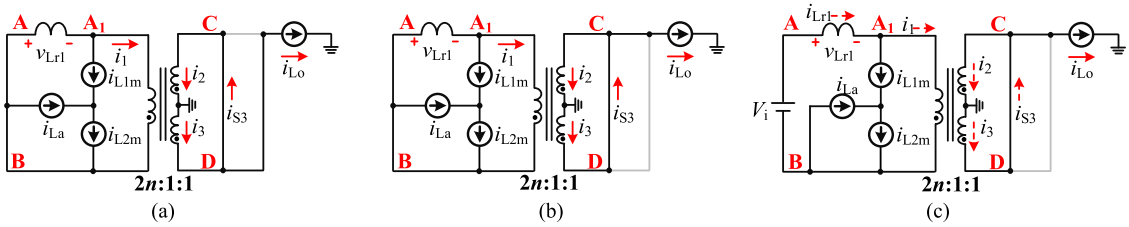


Fig. 9. Further simplified equivalent circuits of Fig. 8(d), (f), and (h) (stage I).

derived as

$$i_{M4}(t_6) \geq V_i C_{pM4}/t_d \tag{20}$$

where $i_{M4}(t_6) = i_{M3}(t_6) = -i_{Lr2}(t_6)/2$.

Mode 8 [$t_7 - t_8$, Fig. 8(h)]: At t_7, switch M_4 is turned ON at ZVS mode. The voltage v_{AB} is clamped to V_i and voltages v_C and v_D are still clamped to zero due to the positive current i_3. The equivalent circuit of this stage is further simplified as Fig. 9(c). It can be found that, since $v_{Lr1} = V_i$ ($V_{A1B} = 0$), this positive voltage forces current i_{Lr1} to increase linearly. If the increased value of current i_{Lr1} is ΔI ($\Delta I = V_i\, t/L_{r1}$), then the primary currents i_1 and i_{Lr2} will increase the same value ΔI and change their directions. According to (18), the changed value $\Delta i_2 + \Delta i_3$ of secondary currents i_2 and i_3 is equal to $-2n^*\Delta I$. At the same time, $(i_3 + \Delta i_3) - (i_2 + \Delta i_2) = i_{Lo}$, thus, both Δi_2 and Δi_3 are equal to $-n^*\Delta I$, i.e., the currents i_2 and i_3 will decay rapidly with the rate of nV_i/L_{r1}.

When current i_3 is decreasing to zero, the voltage v_C (v_D) begins to increase (decrease) quickly. The parasitic capacitor C_{pS4} of switch S_4 begins to discharge and the C_{pS3} of switch S_3 is charged. When the voltages v_C and v_D are clamped to $V_i/2$n and $-V_i/2$n, respectively, the parasitic capacitor voltage v_{CpS4} ($v_{CpS4} = v_{CD} - v_{Cf}$) is almost equal to zero, which guarantees ZVS turn-on of S_4 at t_8. The equivalent circuit is shown in Fig. 8(h) Stage II.

At t_8, the S_4 is turned ON at ZVS, as shown in Fig. 8(i). From t_8, the latter eight modes (*modes* 9–16) can be explained following the explanations for *modes* 1–8. Furthermore, the switching states of all power switches during different modes in one complete switching cycle T_s are listed in Table I.

C. ZVS Conditions of Switches $M_1 - M_8$ and $S_1 - S_4$

1) Switches $M_1 - M_4$: From the analysis presented in Section III-B, it can be seen that in order to achieve ZVS turn-on for switches $M_1 - M_4$, the parasitic capacitor in parallel with the incoming switch should be completely discharged and the parasitic capacitor in parallel with the outgoing switch in the same bridge leg should be fully charged.

According to (14) and (15), a factor called i_{ZVM1} given in (21) is defined to validate the ZVS conditions for switch M_1 (M_2). The ZVS turn-on transition for switch M_1 (M_2) is achieved only when $i_{ZVM1} > 0$

$$i_{ZVM1} = \frac{I_{Lom}}{4n} + \frac{I_{L1m}}{2} - \frac{I_c}{2n} - \frac{V_i C_{pM2}}{t_d} \tag{21}$$

where the peak value I_{L1m} of magnetizing current i_{L1m} is shown in Fig. 5 and the charging current I_c can be calculated as follows:

$$I_c = \frac{\sin(\omega d T_c)}{1 + \cos(\omega d T_c)} \left(\frac{V_i}{n} - k\right) \omega C_f \approx \frac{d\omega^2 T_c C_f}{2} \left(\frac{V_i}{n} - k\right). \tag{22}$$

By inserting (6), (8), and (22) into (21), the ZVS conditions of switches M_1 (M_2) are obtained as

$$i_{ZVM1} = \frac{V_i d}{8n^2 R} + \frac{V_i T_s}{32 L_a}(1-d) - \frac{V_i C_{pM2}}{t_d}. \tag{23}$$

Similarly, a factor called i_{ZVM4} given in (24) is defined to validate the ZVS conditions for switch M_4 (M_3) using mode 7 analysis and the ZVS transition for switch M_4 (M_3) can be achieved only when $i_{ZVM4} > 0$, where the i_{ZVM4} can be expressed as

$$i_{ZVM4} = \frac{V_i d}{8n^2 R} + \frac{3V_i T_s}{32 L_a}(1-d) - \frac{V_i C_{pM3}}{t_d}. \tag{24}$$

According to (6), (23), and (24), the auxiliary inductor L_a is designed to provide enough reactive current i_{L1m} and i_{L2m} to make sure the $i_{ZVM1} > 0$ and $i_{ZVM4} > 0$ under entire duty cycle range ($0 \leq d \leq 1$). The design considerations for the auxiliary inductor L_a are explained in the next Section IV.

2) Switches $M_5 - M_8$: By adopting the overlap modulation scheme, switches M_5/M_6 and M_7/M_8 have the overlap conduction time $t_4 - t_5$ and $t_{12} - t_{13}$, as shown in Fig. 7. It is evident that the ZVS turn-on and turn-off conditions of $M_5 - M_8$ can be satisfied.

TABLE I
SUMMARY OF CONDUCTING COMPONENTS OF THE DPS-CHFL INVERTER AT DIFFERENT MODES

Mode	Conducting Components
Mode 1 ($t_0 - t_1$)	$M_2, M_3, S_2, S_3, M_7, M_8$
Mode 2 ($t_1 - t_2$)	$M_3, D_{S1}, S_3, M_7, M_8$
Mode 3 ($t_2 - t_3$)	$M_1, M_3, D_{S1}, S_3, M_7, M_8$
Mode 4 ($t_3 - t_4$)	$M_1, M_3, S_1, S_3, M_7, M_8$
Mode 5 ($t_4 - t_5$)	$M_1, M_3, S_1, S_3, M_5, M_6, M_7, M_8$
Mode 6 ($t_5 - t_6$)	$M_1, M_3, S_1, S_3, M_5, M_6$
Mode 7 ($t_6 - t_7$)	$M_1, S_1, D_{S3}, M_5, M_6$
Mode 8 ($t_7 - t_8$)	M_1, M_4, S_1, M_5, M_6
Mode 9 ($t_8 - t_9$)	$M_1, M_4, S_1, S_4, M_5, M_6$
Mode 10 ($t_9 - t_{10}$)	$M_4, D_{S2}, S_4, M_5, M_6$
Mode 11 ($t_{10} - t_{11}$)	$M_2, M_4, D_{S2}, S_4, M_5, M_6$
Mode 12 ($t_{11} - t_{12}$)	$M_2, M_4, S_2, S_4, M_5, M_6$
Mode 13 ($t_{12} - t_{13}$)	$M_2, M_4, S_2, S_4, M_5, M_6, M_7, M_8$
Mode 14 ($t_{13} - t_{14}$)	$M_2, M_4, S_2, S_4, M_7, M_8$
Mode 15 ($t_{14} - t_{15}$)	$M_2, S_2, D_{S4}, M_7, M_8$
Mode 16 ($t_{15} - t_0$)	M_2, M_3, S_2, M_7, M_8

3) Switches $S_1 - S_4$: As shown in Fig. 8(c), before switch S_1 is turned ON, the voltages v_{AB}, v_C, v_D, and v_G have been clamped to zero, which guarantees the switch S_1 operating under the ZVS condition. Therefore, switches S_1 and S_2 can achieve ZVS easily.

For switch S_4, as shown in Fig. 8(h), the secondary-side current i_3 will decrease until the parasitic capacitor C_{pS4} of switch S_4 has been fully discharged. To achieve the ZVS conditions of S_4, the required increase value $\Delta I_{\rm req}$ of primary-side current i_{Lr1} shall satisfy

$$\frac{V_i t_a}{L_{r1}} \geq \Delta I_{\rm req} = \frac{i_3(t_6) + I_c}{n}. \tag{25}$$

A factor called i_{ZVS4} given in (26) is defined to validate the ZVS conditions for switch S_4. The ZVS turn-on transition for switch S_4 (S_3) is achieved only when $i_{ZVS4} > 0$. By inserting (19) and (22) into (25), the i_{ZVS4} can be expressed as

$$i_{ZVS4} = \frac{V_i t_a}{L_{r1}} - \Delta I_{\rm req} = \frac{V_i t_a}{L_{r1}} - \frac{V_i T_s}{8L_a} - \left(\frac{V_i P_o}{2n^2 V_{\rm orms}^2} - \frac{V_i T_s}{8L_a}\right) d > 0. \tag{26}$$

From inequality (26), it can be observed that the bigger t_a is preferred to achieve ZVS turn-on for switches S_3 and S_4 over the entire duty cycle range ($0 \leq d \leq 1$). However, an increase in t_a results in the higher harmonic distortion of output SPWM voltage. The design considerations for t_a are explained in the Section IV.

When output voltage $v_o < 0$, the driving signals for switches M_4 and M_3 will lead those for switches M_1 and M_2, respectively; for secondary-side active clamper network, the driving signals for switches S_4 and S_3 will lead those for switches S_1 and S_2, respectively; the operation modes and the ZVS conditions for switches $M_1 - M_4$ and $S_1 - S_4$ will be symmetrical to these of the positive output voltage. In practice, the load characteristic of the proposed DPS-CHFL inverter can be resistive, inductive, or capacitive. When the load is inductive or capacitive, the inverter still has similar operating states in one switching cycle. The soft-switching ranges of $M_1 - M_4$ are affected by the type of load because the primary current is closely related to load current. However, the switches $M_5 - M_8$ can achieve soft switching at different type of load.

IV. Design Guidelines and Process of Circuit Parameters

Circuit parameters design is one of the important parts for the proposed DPS-CHFL inverter that is applied in single-stage high-voltage audio power amplifier application [7]–[8], [30]–[31]. The design process is presented in this section and the design specifications are shown in Table II.

A. Design Considerations of Switching Frequency, the HF Transformer and Power Switches

For the audio power amplifier application, the signal frequency f is in the range of 20–20 kHz. Considering the frequency of the output SPWM voltage v_G is the double of the switching frequency f_s, the minimum frequency modulation ratio $m_{f\min}$ is $2f_s/f_{\max}$ and the f_s can be selected to be 200 kHZ.

TABLE II
Proposed Inverter Specifications

Components	Parameters
DC input voltage V_i	300 V
AC output voltage V_{orms}	110 Vac
Rated output power P_o	242 VA

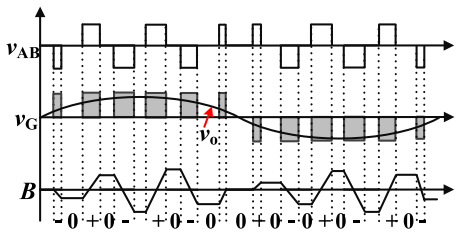


Fig. 10. Magnetizing states of HF transformer in the proposed DPS-CHFL inverter.

The turns ratio n of HF transformer T_x is designed for output peak voltage at maximum duty cycle $d_{\max}$, thus, the $V_{\rm orms}, d_{\max}, V_i$, and turns ratio n should meet the following inequality:

$$\sqrt{2} V_{\rm orms} \leq d_{\max} V_i / 2n \tag{27}$$

where the $d_{\max} = 0.9$, then the turns ratio $n \leq 0.86$, thus n can be selected to be 0.8.

The magnetizing states of HF transformer T_x is shown in Fig. 10, where "+" and "−" represent positive and negative magnetizing direction, respectively, and "0" represents unchanged direction. It can be seen that the operating flux density B is bipolar trapezoidal that can be obtained as

$$B = \frac{V_i d_{\max} T_c}{4 n_{p1} A_e} \leq B_m \tag{28}$$

where B_m is the maximum flux density.

Considering that the switching frequency f_s of the proposed inverter is 200 kHz, the DMEGC DMR50B is chosen as it is characterized by low losses at high frequencies in the range of 100–250 kHz and B_m is designed to be 0.1 T. At the same time, according to the principle of core area product, DMEGC PTS33 is chosen as the transformer magnetic core and its effective cross-sectional area A_e is $148.9\,{\rm mm}^2$. Therefore, the number of primary side turn n_{p1} for T_x is estimated from (28), which is selected as 16 and the actual B_m is calculated as 0.078T. Fig. 11 shows the three-dimensional (3-D) model of HF transformer T_x in finite element analysis simulation where the simulation result of equivalent leakage inductor L_{r1} is equal to $2.2\,\mu$H.

According to the switching frequency (200 kHz) and design cost, MOSFET is preferred for all power switches of the proposed DPS-CHFL inverter. The primary side switches $M_1 - M_4$ require MOSFET with a maximum blocking voltage of $V_{i\max}$ (300 V). Considering a safety margin of 30%, the drain-source breakdown voltage of the selected MOSFET,

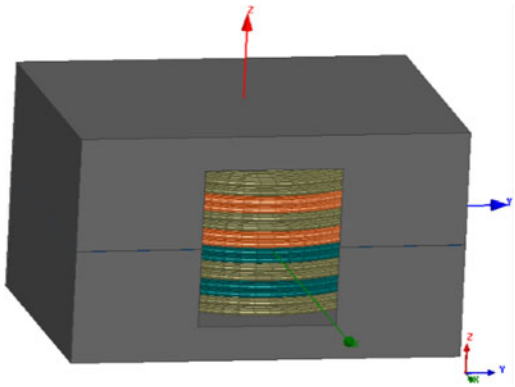


Fig. 11. 3-D model of HF transformer in finite element analysis simulation.

$V_{(\mathrm{BR})\mathrm{DSS}}$, should be at least 390 V. Meanwhile, the positive level value of secondary voltage v_C (v_D) is equal to $V_i/2n$ (188 V), thus, the drain-source breakdown voltage of the selected MOSFET for $M_5 - M_8$ and $S_1 - S_4$, $V_{(\mathrm{BR})\mathrm{DSS}}$, should be at least $(1 + 30\%)V_i/n$ (488 V). The FDPF20N50FT MOSFET from Fairchild [32] with drain-source breakdown voltage 500 V, typical output parasitic capacitance $C_p = 350$ pF, a lower on-state resistance (max. $R_{\mathrm{DS,on}} = 0.26\,\Omega$ at $V_{\mathrm{GS}} = 10$ V and $\mathrm{T}_j = 25\,^{\circ}\mathrm{C}$) in the TO-220 package, and a low reverse recovery charge ($0.5\,\mu c$) is selected for switches $M_1 - M_8$ and $S_1 - S_4$.

B. Design Considerations of the Auxiliary Inductor, Dead Time, Delay Time, and Clamping Capacitor

The ZVS operation of all switches is a significant factor for the efficiency-optimal design of the DPS-CHFL inverter. From (23) and (24), it can be seen that the ZVS conditions of primary switches $M_1 - M_4$ depend on the auxiliary inductor L_a and dead time t_d, thus, L_a and t_d should be selected to ensure that the available reactive current during switching transitions guarantees ZVS for switches $M_1 - M_4$ under the different duty cycle d. Owing to the factors $i_{ZVM4} > i_{ZVM1}$, the criterion considered here for achieving ZVS for switches $M_1 - M_4$ is to guarantee the $i_{ZVM1} > 0$ at any duty cycle $d\,(0 \le d \le 1)$. From (23), the i_{ZVM1} can be deduced as follows:

$$i_{ZVM1} = V_i\left[\left(\frac{P_o}{8n^2V_{\mathrm{orms}}^2} - \frac{T_s}{32L_a}\right)d + \frac{T_s}{32L_a} - \frac{C_{pM2}}{t_d}\right] > 0. \tag{29}$$

As we can see that there are two possible cases depending on the value of $\frac{P_o}{8n^2V_{\mathrm{orms}}^2} - \frac{T_s}{32L_a}$.

Case I: $\frac{P_o}{8n^2V_{\mathrm{orms}}^2} - \frac{T_s}{32L_a} > 0$. The minimum value of $i_{ZVM1}(d)$ is acquired at duty cycle $d = 0$, which can be expressed as

$$i_{ZVM1}(0) = V_i\left(\frac{T_s}{32L_a} - \frac{C_{pM2}}{t_d}\right) > 0. \tag{30}$$

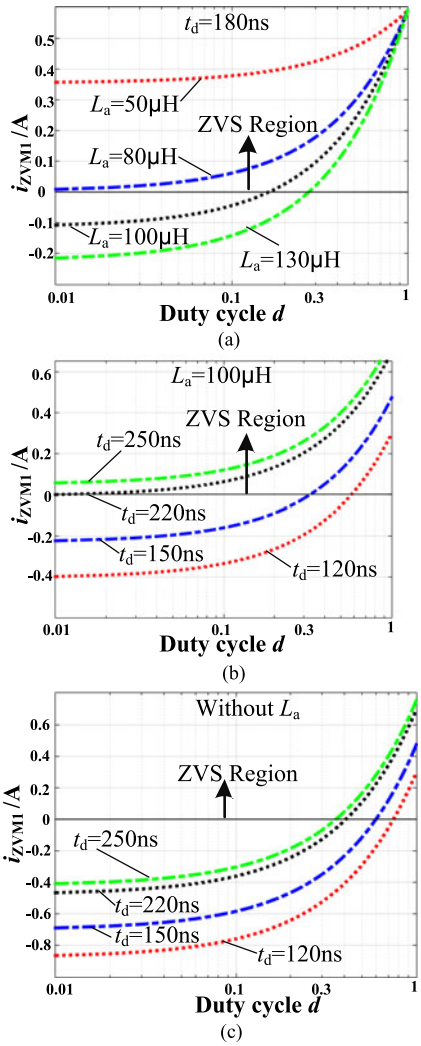


Fig. 12. i_{ZVM1} versus duty cycle d (a) at different auxiliary inductance L_a (b) at different dead time t_d with L_a (c) at different dead time t_d without L_a.

Case II: $\frac{P_o}{8n^2V_{\mathrm{orms}}^2} - \frac{T_s}{32L_a} < 0$. Then the minimum value of $i_{ZVM1}(d)$ can be acquired at duty cycle $d = 1$, thus

$$i_{ZVM1}(1) = V_i\left(\frac{1}{8n^2}\frac{P_o}{V_{\mathrm{orms}}^2} - \frac{C_{pM2}}{t_d}\right) > 0. \tag{31}$$

According to (30) and (31), L_a and t_d can be selected as

$$\begin{cases} \dfrac{n^2V_{\mathrm{orms}}^2T_s}{4P_o} < L_a \le \dfrac{T_st_d}{32C_{pM2}}\,(a) \\ \text{or} \\ L_a < \dfrac{n^2V_{\mathrm{orms}}^2T_s}{4P_o} \text{ and } t_d > \dfrac{8n^2V_{\mathrm{orms}}^2C_{pM2}}{P_o}\,(b) \end{cases}. \tag{32}$$

For the design specifications shown in Table II, the L_a and t_d can be calculated as

$$\begin{cases} 40\,\mu H < L_a \le 450t_d\ (a) \\ \text{or} \\ L_a < 40\,\mu H \text{ and } t_d > 90\,ns\ (b) \end{cases}. \tag{33}$$

Therefore, based on (29) and (33), i_{ZVM1} versus duty cycle d can be plotted in Fig. 12(a), showing that the smaller auxiliary

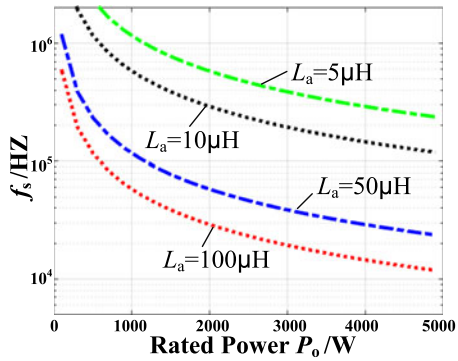


Fig. 13. Example design curves for the auxiliary inductor L_a at different switching frequency f_s and output power P_o.

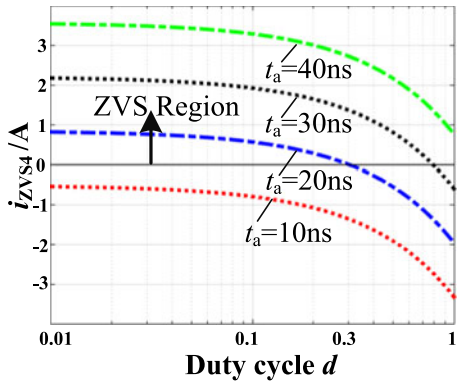


Fig. 14. i_{ZVS4} versus duty cycle d at different delay time t_a.

inductance L_a is a benefit to achieve the ZVS at whole range duty cycle from 0 to 1. Fig. 12(b) and 12(c) show the i_{ZVM1} versus duty cycle d at different dead time t_d for the proposed DPS-CHFL inverter and the conventional inverter, respectively. It can be seen that the ZVS range for switches $M_1 - M_4$ in the DPS-CHFL inverter is extended dramatically.

Ultimately, according to (33) and Fig. 12, L_a and t_d are selected as $100\,\mu$H and 220 ns, respectively.

Fig. 13 shows an example of the selection curves of the auxiliary inductor L_a as functions of rated output power P_o and the switching frequency f_s. It is seen that for a higher power DPS-CHFL inverter such as 5 KVA when switching frequency f_s is selected to be 20 kHz, the auxiliary inductor L_a shall be about $40\,\mu$H.

The delay time t_a significantly influences the ZVS region borders of switches $S_1 - S_4$. Inequality (26) shows the design methodology of t_a, which can be deduced as

$$i_{ZVS4} = V_i \left[\frac{t_a}{L_{r1}} - \frac{T_s}{8L_a} - \left(\frac{P_o}{2n^2 V_{\text{orms}}^2} - \frac{T_s}{8L_a} \right) d \right] > 0. \tag{34}$$

Similarly, there are two possible cases depending on the value of $\frac{P_o}{2n^2 V_{\text{orms}}^2} - \frac{T_s}{4L_a}$.

Case I: $\frac{P_o}{2n^2 V_{\text{orms}}^2} - \frac{T_s}{4L_a} > 0$. The minimum value of $i_{ZVS4}(d)$ is acquired at duty cycle $d = 1$, which can be expressed as

$$i_{ZVS4}(1) = V_i \left(\frac{t_a}{L_{r1}} - \frac{P_o}{2n^2 V_{\text{orms}}^2} \right) > 0. \tag{35}$$

Case II: $\frac{P_o}{2n^2 V_{\text{orms}}^2} - \frac{T_s}{4L_a} < 0$. Then the minimum value of $i_{ZVS4}(d)$ is acquired at duty cycle $d = 0$, thus

$$i_{ZVS4}(0) = V_i \left(\frac{t_a}{L_{r1}} - \frac{T_s}{8L_a} \right) > 0. \tag{36}$$

According to (35) and (36), then the required delay time t_a can be obtained as

$$\begin{cases} t_a \geq \dfrac{L_{r1} P_o}{2n^2 V_{\text{orms}}^2}, & \text{if } \dfrac{P_o}{2n^2 V_{\text{orms}}^2} - \dfrac{T_s}{8L_a} > 0 \text{ (a)} \\ t_a \geq \dfrac{T_s L_{r1}}{8L_a}, & \text{if } \dfrac{P_o}{2n^2 V_{\text{orms}}^2} - \dfrac{T_s}{8L_a} < 0 \text{ (b)} \end{cases}. \tag{37}$$

For the design specifications shown in Table II and the L_a value $(100\,\mu\text{H})$, the t_a can be calculated as

$$t_a \geq 34\,\text{ns}. \tag{38}$$

The i_{ZVS4} versus duty cycle d at different delay time t_a can be plotted in Fig. 14. It can be seen that the bigger delay time t_a is a benefit to achieve the ZVS for S_4 at whole range duty cycle from 0 to 1. According to (38) and Fig. 14, t_a is selected as 30 ns.

The design of clamping capacitor C_f should consider the resonant operation between capacitor C_f and the leakage inductance L_{r1}. According to the (13), the resonant frequency ω shall satisfy

$$1 + \cos(\omega d T_c) \neq 0 \Rightarrow \omega T_c < \pi. \tag{39}$$

Thus, the clamping capacitor C_f is obtained as

$$\omega \approx \sqrt{\frac{n^2}{L_{r1} C_f}} \Rightarrow C_f > \frac{n^2 T_s^2}{4\pi^2 L_{r1}} = 0.18\,\mu F. \tag{40}$$

Therefore, the value of capacitor C_f is selected to be $0.22\,\mu$F.

C. Design Considerations of DC Capacitor, Divider Capacitors, Filter Inductor, and Filer Capacitor

The proposed DPS-CHFL inverter is a typical single-phase inverter, the ac side instantaneous power contains both a dc component and a double line frequency power oscillation when the power factor is equal to 1 [33]. This power oscillation will then induce a significant current or voltage ripple on the dc side. To cope with this issue, the straightforward solution is to apply the bulky electrolytic capacitor (E-cap) as the energy buffer to passively decouple the power oscillation, which is shown in Fig. 15. The design constraints of the proposed DPS-CHFL inverter are that the input dc bus peak-to-peak current and voltage ripples should be $<20\%$ and 2% of the nominal values, respectively. Thereby, the E-cap C_{dc} can be obtained as

$$C_{\text{dc}} = \frac{(1 - 20\%/2) P_o}{2\omega V_i^{2*} 2\%} = 190.8\,\mu\text{F}. \tag{41}$$

Therefore, the E-cap capacitor C_{dc} can be selected as $200\,\mu$F. If the internal resistance R_s of the dc voltage source is small

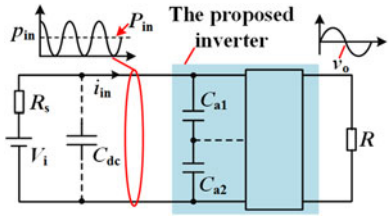


Fig. 15. Schematic showing the ripple power on the dc link.

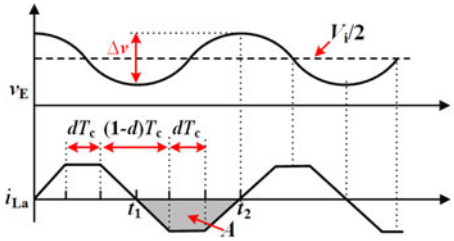


Fig. 16. Charging and discharging operation of capacitors C_{a1} and C_{a2}.

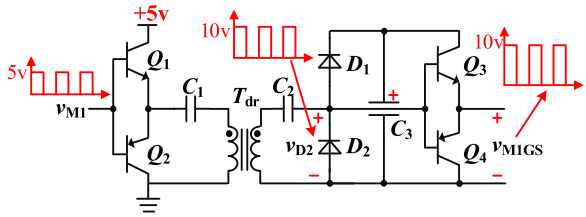


Fig. 17. TIGD circuit for all switches of the proposed DPS-CHFL inverter.

and can be ignored, the dc voltage source V_i will be the ideal voltage source and capacitor $C_{\rm dc}$ will be not required, however, the input current $i_{\rm in}$ will obtain significant second-order current ripple.

The two capacitors C_{a1} and C_{a2} should be employed to halve the input voltage V_i with little ripples over a single switching cycle. The permitted ripple voltage Δv on the capacitor C_{a2} is considered as 1% of v_{Ca2}. As shown in Fig. 16, the capacitor C_{a2} is charged by the auxiliary inductor current $i_{La}(\rm t)$ during the interval of $t_1 - t_2$, then the Δv shall satisfy

$$\frac{\left|\int_{t_1}^{t_2} i_{La}(t)dt\right|}{2C_{a2}} \le \Delta v = \frac{V_i}{2}^{*} 1\% \tag{42}$$

where the integral area A of the current $i_{La}(\rm t)$ during the interval of $t_1 - t_2$ can be obtained as follows:

$$\left|\int_{t_1}^{t_2} i_{La}(t)dt\right| = \frac{V_i {T_s}^2}{32L_a}(1-d^2). \tag{43}$$

Substituting the internal (43) into (42), then the C_{a1} and C_{a2} are expressed as

$$C_{a1} = C_{a2} \ge \frac{25{T_s}^2}{8L_a} = 0.78\,\mu\text{F}. \tag{44}$$

So the value of capacitor C_{a1} (C_{a2}) is selected to be $1\,\mu$F.

The output inductor L_o and capacitor C_o form a low-pass filter that filters out the high frequency components of output SPWM. The design of the L_o should take the ripple of harmonic current

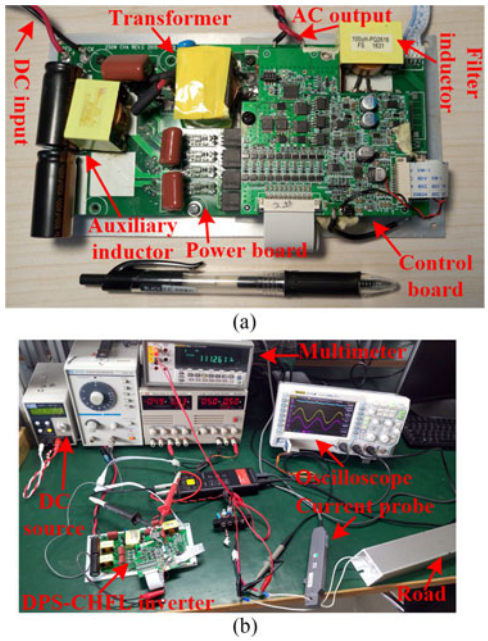


Fig. 18. Experimental prototypes. (a) Proposed DPS-CHFL inverter prototype. (b) Experiment setup of the system.

TABLE III
UTILIZED COMPONENTS AND PARAMETERS OF THE DPS-CHFL INVERTER

Components	Parameters
DC input voltage V_i	300 V
Power MOSFETs $M_1 - M_8$ and $S_1 - S_4$	FDPF20N50
Switching frequency f_s	200 kHz
Auxiliary capacitor $C_{a1} = C_{a2}$	$1\,\mu$F
The dead time t_d	220 ns
The delay time	30 ns
Auxiliary inductor L_a	$100\,\mu$H
HF transformer $T_{\rm x}$	$n_{p1} : n_{p2} : n_{p3} : n_{p4} = 16 : 16 : 20 : 20$
Leakage inductor L_{r1}	$2.2\,\mu$H
Clamping capacitor C_f	$2.2\,\mu$F
Output filter inductor L_o	$100\,\mu$H
Output filter capacitor C_o	$0.5\,\mu$F
Load resistance R	$50\,\Omega$
AC output voltage v_o	110 VAC
Rated output power P_o	242 VA

into considerations [34]. To limit the current ripple (40%) of harmonic current at the peak point of inductor current i_{Lo}, the lower limit of L_a should meet the following equation:

$$L_o \ge \frac{V_i V_{o\rm rms}}{16\sqrt{2}nf_s{*}40\%{*}P_o} = 94\,\mu\text{H}. \tag{45}$$

So the value of filter inductor L_o is selected to be $100\,\mu$H.

To get good high-frequency components attenuation, the cut off frequency is selected at $f_s/8$, thus, the output capacitor C_o can be obtained as

$$C_o = \frac{16}{\pi^2 f_s^2 L_o} = 0.41\,\mu\text{F}. \tag{46}$$

Therefore, a $0.5\,\mu$F output filter capacitor C_o is selected.

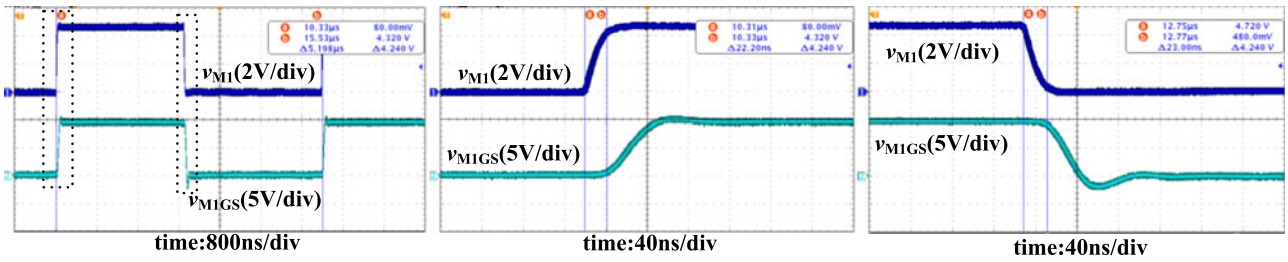


Fig. 19. Measured waveforms of the TIGD circuit for switch M_1. (a) Driving signal waveform. (b) Turn-on waveform. (c) Turn-off waveform.

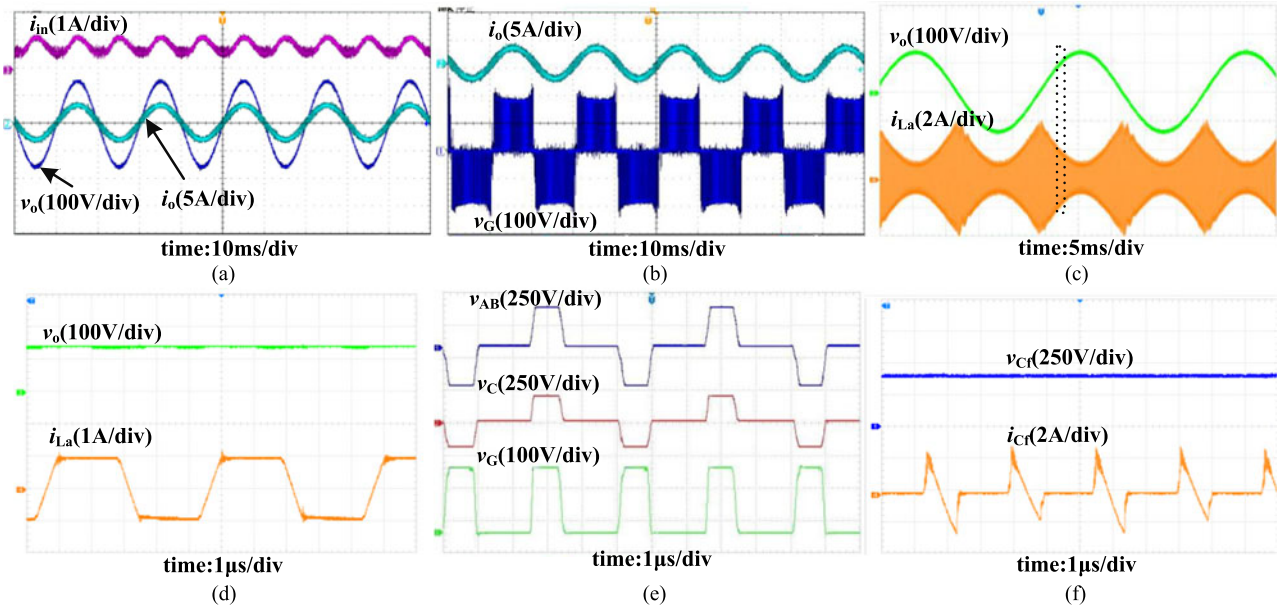


Fig. 20. Experimental waveforms for the proposed DPS-CHFL inverter under resistor load. (a) Input current $i_{\rm in}$, output SPWM voltage v_G, and output voltage v_o. (b) Output SPWM voltage v_G, output voltage v_o, and output current i_o. (c) Output voltage v_o and auxiliary inductor current i_{La}. (d) Expanded waveforms of v_o and i_{La}. (e) Primary-side voltage v_{AB}, secondary-side voltage v_C, and output SPWM voltage v_G. (f) Clamping capacitor voltage v_{cf} and current i_{cf}.

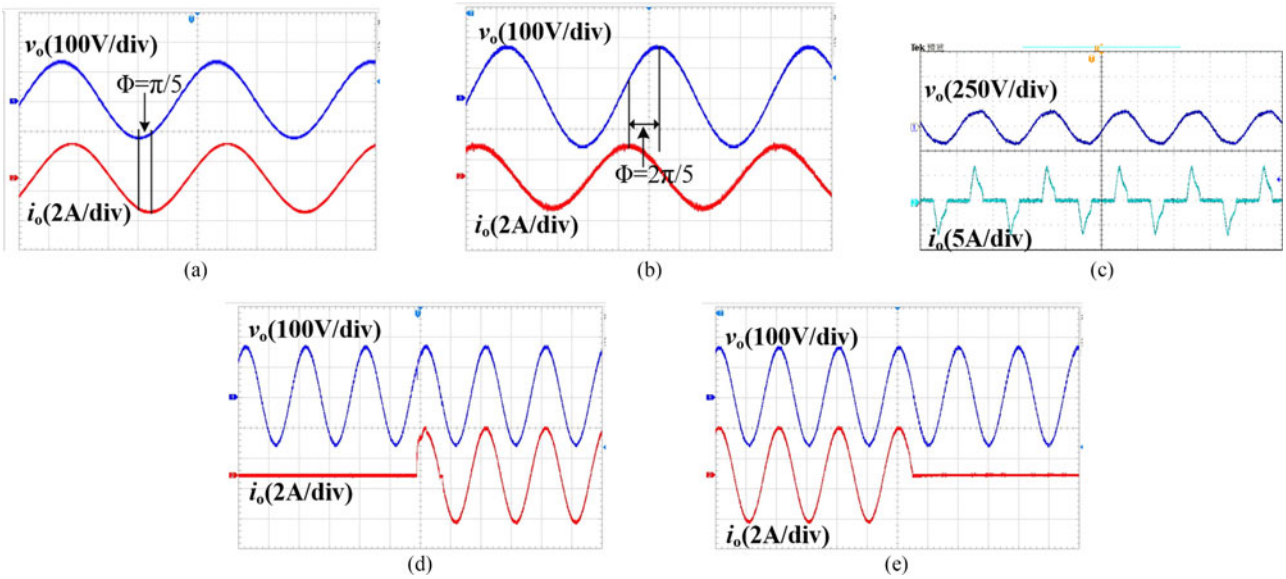


Fig. 21. Experimental waveforms for the proposed DPS-CHFL inverter. (a) Steady waveform under inductive load. (b) Steady waveform under capacitive load. (c) Steady waveform under diode rectifier load. (d) Transient waveforms from no-load to 50 Ω load. (e) Transient waveforms from 50 Ω load to no-load.

D. Design Considerations of Gate Drive Circuits

Gate drive circuits for switches $M_1 - M_8$ and $S_1 - S_4$ of the proposed DPS-CHFL inverter require electrical isolation to separate the low-voltage side (control circuit) from high-voltage side (power circuit). Because the driving signals for all switches are nearly 50% fixed duty cycle square signals, a TIGD circuit with small transmission delay for all switches is proposed, which is shown in Fig. 17. It consists of primary-side totem-pole transistors Q_1 and Q_2, a dc blocking capacitor C_1, drive transformer $T_{\rm dr}$ with turns ratio 0.5, voltage doubler circuit C_2, C_3, D_1, and D_2, and secondary-side totem-pole transistors Q_3 and Q_4. The TIGD circuit does not require an additional isolated secondary-side power supply. Both the gating signal and the gate drive power flow through the isolation transformer $T_{\rm dr}$. Meantime, the transformer cores can be reset at every half-cycle and the average volt-second of the transformer $T_{\rm dr}$ is zero to avoid core saturation.

V. Experiment Verification

In order to verify the theoretical analysis, gate driver technique, and the efficiency of the proposed DPS-CHFL inverter, an experimental prototype, as shown in Fig. 18(a), was built with the dimensions of 17 cm $\times$ 12 cm $\times$ 5 cm in the laboratory, where the proposed inverter is designed based on the well-established design considerations presented in the Section IV and the driving signals for all switches can be generated by a single DSP chip or the analog logic circuit. The experimental setup is shown in Fig. 18(b) in detail. According to Section IV, the detailed electrical parameters and utilized components are summarized in Table III.

A. Steady-State Results

Fig. 19(a) is the experimental waveforms of the input voltage v_{M1} and the gate-to-source voltage v_{M1GS} of switch M_1 for the TIGD circuit shown in Fig. 17. From the figure, it can be seen that the switching frequency is 200 kHz. Fig. 18(b) and (c) show that the rise and fall times of the TIGD circuit are less than 50 ns. The delay between input voltage v_{M1} and output voltage v_{M1GS} is approximately in the range of 25 ns, which validates that the TIGD circuit has better speed performance and small transmission delay.

Fig. 20 shows the stability waveforms of the proposed DPS-CHFL inverter when the equivalent load is a resistor. The experimental waveforms of input current $i_{\rm in}$, output voltage v_o, output current i_o, and output SPWM voltage v_G are shown in Fig. 20(a) and (b), respectively. Fig. 20(c) presents the waveforms of output voltage v_o and the auxiliary inductor current i_{La}, showing that the amplitude I_{La} of auxiliary inductor current i_{La} varies with the output voltage v_o. The expanded waveforms of v_o and i_{La} are given in Fig. 20(d), which shows that the current i_{La} has a trapezoidal shape verifying the theoretical results shown in Fig. 5. Fig. 20(e) indicates the waveforms of primary-side voltage v_{AB}, secondary-side voltage v_C, and output voltage v_G, where all waveforms are free of voltage spikes. Fig. 20(f) shows the waveforms of clamping capacitor voltage v_{Cf} and current i_{Cf}.

Fig. 21(a) shows the experimental waveforms with the inductive load, where the output voltage v_o leads the output current i_o. Fig. 21(b) is the result with the capacitive load, showing the output current i_o leads the output voltage v_o. Fig. 21(c) shows the experimental waveforms when the load is diode rectifier load. The above experimental results verify that the proposed DPS-CHFL inverter can operate well at the inductive load, capacitive load, and nonlinear load. Fig. 21(d) and (e) shows the transient waveforms when the resistor load (50 Ω) is pop-in and pop-out, respectively.

B. ZVS Waveforms

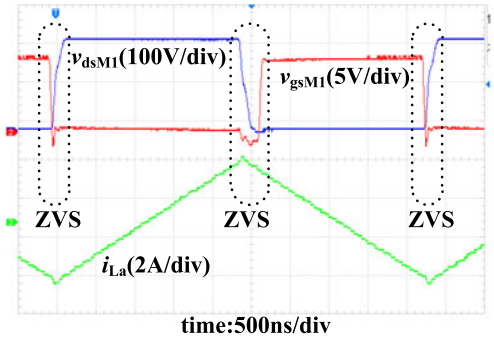
Fig. 22(a) and (b) show the overlapping gate-to-source and drain-to-source voltages of switch M_1 for different effective SPWM duty cycle d, illustrating that the drain-to-source voltage of the switch M_1 attains zero before the gating signal is applied. This phenomenon confirms ZVS turn-on of primary switches over wide duty cycle range. Fig. 22(c) shows the switching waveforms of switch S_1, showing that the switches of active clamper network can achieve ZVS due to the delay time t_a. In addition, the ZVS turn-off of switches M_1 and S_1 can be achieved as well due to the parasitic capacitor of power switches, as shown in Fig. 22 (a)–(c). The switching waveforms across switch M_8 are shown in Fig. 22(d). It can be seen that ZVS turn-on and ZVS turn-off of the cycloconverter switches are actually attained, which agrees with the ZVS predictions of theoretical analysis.

C. Experimental Efficiency and Harmonic Spectrums

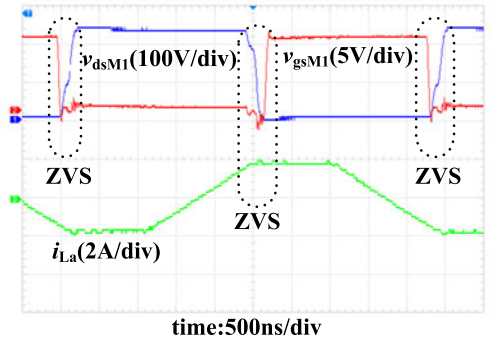
The measured efficiency versus output power is given in Fig. 23. The system was tested up to a peak power of 270 W, where the target system efficiency of 92.8% is achieved. An overall peak efficiency of 93.6% was measured at an output power of 190 W. The efficiency drops off at lower power levels; however, it is still greater than 91.9% at an output power of 100 W. Compared with the inverter in [20], it can be seen that the proposed DPS-CHFL inverter achieves higher efficiency over wide power range. The loss breakdown at 240 W is shown in Fig. 24. It can be seen that the conduction loss of power switches and the transformer loss are two major aspects of total loss, which take up around 36% and 33%, respectively. The switching loss only accounts for a minor proportion of total loss, which verifies the soft switching of the proposed inverter. Fig. 25(a) indicates the harmonic spectrums for the output voltage v_o at rated power. In addition, total harmonic distortion+noise (THD+N) against signal frequency f at 200 W output power in Fig. 25(b) shows the promising audio performance of DPS-CHFL inverter.

D. Comparison With Other CHFL Inverters

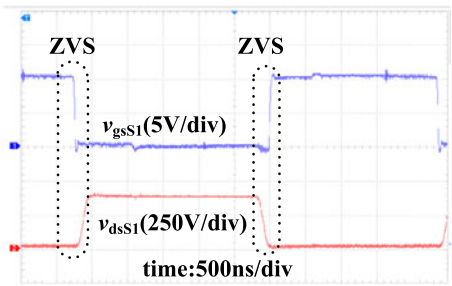
A comparison between the proposed DPS-CHFL inverter (A) and the other two CHFL inverters (B and C) are given in Table IV. One is a conventional primary-side H-bridge CHFL inverter (B) without the auxiliary inductor, where the active voltage clamper employs conventional PWM strategy [20]. The other is a recently developed push-pull CHFL inverter (C)



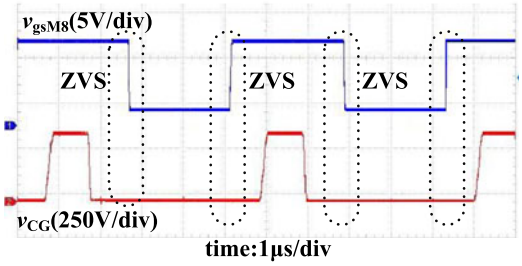
(a)



(b)



(c)



(d)

Fig. 22. Measured waveforms for the DPS-CHFL inverter. (a) Switching waveform of switch M_1 at $d = 0$. (b) Switching waveform of switch M_1 at $d = 0.4$. (c) Switching waveform of switch S_1. (d) Switching waveform of switch M_8.

without active clamper circuit [12]. Compared with inverters (B) and (C), both the modulation strategy and the isolated drive circuit for the proposed inverter (A) are simpler and more reliable. In addition, the wide range ZVS for primary-side switches, higher efficiency, and higher power density in the proposed DPS-CHFL inverter have been achieved.

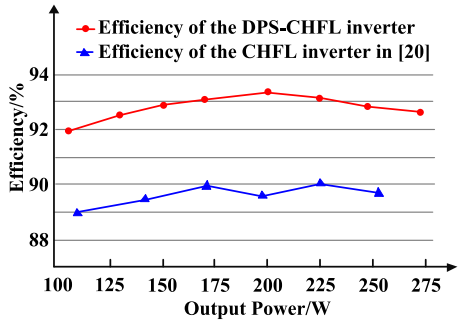


Fig. 23. Experimental efficiency curve for conventional CHFL inverter and proposed DPS-CHFL inverter.

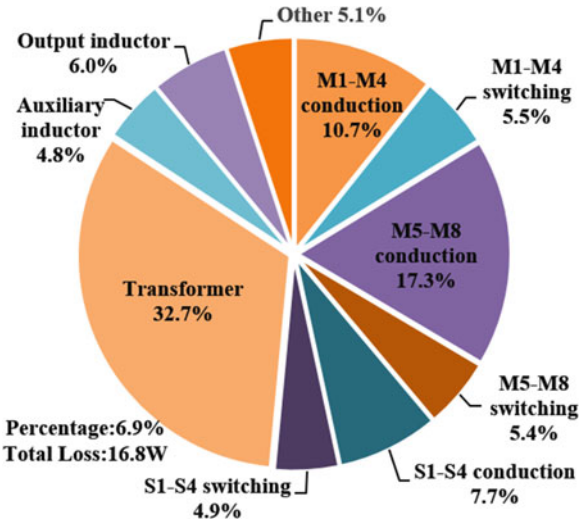
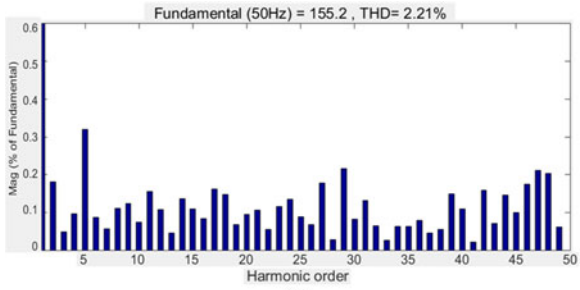
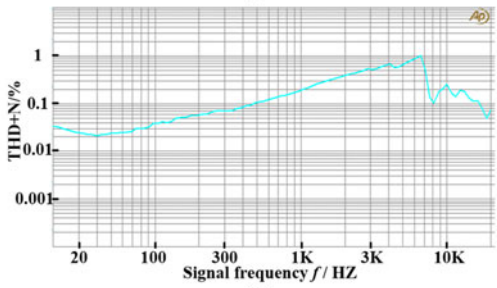


Fig. 24. Loss breakdown at rated output power 240 W.



(a)



(b)

Fig. 25. Harmonic spectrums under resistance load. (a) THD for the output voltage v_o at rated power. (b) THD + N against signal frequency at 200 W.

TABLE IV
COMPARISON OF THREE CHFL INVERTER

Components	A: The proposed DPS-CHFLI	B: Typical H- bridge CHFLI	C: Push-pull CHFLI
Main active switches	12 MOSFETs	12 Insulated gate bipolar transistor (IGBT)	3 MOSFETs +4 IGBTs
Number of diodes	0	2	1
Number of auxiliary inductor	1	0	0
Modulation strategy complexity	Easy (50% duty cycle)	Complex	Complex
Driving circuits	Transformer-isolated driver	OC-isolated driver	OC-isolated driver
Soft switching	Wide range ZVS for all switches	Partly ZVS	Partly ZVS
Max efficiency	93.6%	89%	91%
Power density	Highest	Low	Middle
Reliability	Very good	Good	Good

VI. CONCLUSION

In this paper, an isolated wide-range soft switching high-efficiency DPS-CHFL inverter has been proposed. Topology configuration, modulation strategy, operation principles, soft-switching conditions, and circuit parameters design of the proposed inverter have been presented in detail. The theoretical results have verified that the ZVS range for primary-side switches has been extended due to the auxiliary inductor and the center-tapped four-winding transformer structure; the voltage spikes on SPWM waveform have been suppressed by the secondary-side active clamper network. All switches in the proposed inverter are driven with nearly 50% duty cycle square signals, thus, a simple and reliable TIGD circuit with small transmission delay has been presented. Moreover, all switches achieve ZVS, which contributes to higher conversion efficiency. The features have been validated by the experimental results from the 200-kHz laboratory prototype, which is applied in high voltage audio amplifier and the efficiency results have proved the improved performance of the proposed DPS-CHFL inverter over the conventional CHFL inverters.

REFERENCES

[1] I. Yamato, N. Tokunaga, Y. Matsuda, H. Amano, and Y. Suzuki, "High frequency link DC-AC converter for UPS with a new voltage clamper," in *Proc. 21st Annu. IEEE Power Electron. Spec. Conf.,* 1990, pp. 749–756.

[2] M. Sarhangzadeh, S. H. Hosseini, and M. B. B. Sharifian, "Multiinput direct DC-AC converter with high-frequency link for clean power generation systems," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1777–1789, Jun. 2011.

[3] P. T. Krein, R. S. Balog, and X. Geng, "High-frequency link inverter for fuel cells based on multiple-carrier PWM," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1279–1288, Sep. 2004.

[4] A. Aganza-Torres, V. Cardenas, M. Pacas, and M. Gonzales, "An efficiency comparative analysis of isolated multi-source grid-connected PV generation systems based on a HF-link micro-inverter approach," *Solar Energy*, vol. 127, pp. 239–249, Apr. 2016.

[5] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen, and J. W. Kolar, "Optimal ZVS modulation of single-phase single-stage bidirectional DAB AC-DC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3954–3970, Aug. 2014.

[6] S. Vaishnav and H. Krishnaswami, "Single-stage isolated bi-directional converter topology using high frequency AC link for charging and V2G applications of PHEV," in *Proc. IEEE Veh. Power Propulsion Conf.*, 2011, pp. 1–4.

[7] P. Ljusev and M. A. E. Andersen, "Direct-conversion switching-mode audio power amplifier with active capacitive voltage clamp," in *Proc. IEEE Power Electron. Spec. Conf.*, 2005, pp. 2848–2854.

[8] S. Guo, J. Su, L. Guo, and X. Chen, "Phase-shifted modulation strategies for a single-stage isolated bi-directional power amplifier," in *Proc. IEEE Power Electron. Motion Control Conf.*, 2016, pp. 1206–1211.

[9] J. Kan, S. Xie, Y. Wu, Y. Tang, Z. Yao, and R. Chen, "High-frequency-link inverter using combined synchronous rectifiers," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6769–6777, Dec. 2014.

[10] D. De and V. Ramanarayanan, "A DC-to-three-phase-AC high-frequency link converter with compensation for nonlinear distortion," *IEEE Trans. Ind. Electron.*, vol. 57, no. 11, pp. 3669–3677, Nov. 2010.

[11] L. Jia and S. K. Mazumder, "A loss-mitigating scheme for DC/pulsating DC converter of a high-frequency-link system," *IEEE Trans. Ind. Electron.*, vol. 59, no. 12, pp. 4537–4544, Dec. 2012.

[12] Z. Chen, Q. Wu, and Y. Yuan, "A novel zero-voltage-switching push–pull high-frequency-link single-phase inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 421–434, Jun. 2016.

[13] S. K. Mazumder and A. K. Rathore, "Primary-side-converter-assisted soft-switching scheme for an AC/AC converter in a cycloconverter-type high-frequency-link inverter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 4161–4166, Sep. 2011.

[14] M. Wang, S. Guo, Q. Huang, W. Yu, and A. Q. Huang, "An isolated bidirectional single-stage DC–AC converter using wide-band-gap devices with a novel carrier-based unipolar modulation technique under synchronous rectification," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1832–1843, Mar. 2017.

[15] D. Chen and Y. Chen, "Step-up AC voltage regulators with high- frequency link," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 390–397, Jan. 2013.

[16] D. Sha, K. Deng, Z. Guo, and X. Liao, "Control strategy for input series-output-parallel high-frequency AC link inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4101–4111, Nov. 2012.

[17] Z. Yan, M. Jia, C. Zhang, and W. Wu, "An integration SPWM strategy for high-frequency link matrix converter with adaptive commutation in one step based on de-re-coupling idea," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 116–128, Jan. 2012.

[18] Z. Yan, S. Xu, X. Han, X. Sun, and J. Li, "A novel de-re-couple modulation strategy for full-wave mode single-phase high-frequency link inverter," in *Proc. IEEE Transp. Electrific. Asia-Pac. Conf. Expo.*, 2014, pp. 1–4.

[19] S. Guo, J. Su, X. Chen, and X. Yu, "Soft-switching single-stage three-level power amplifier for high-voltage audio distribution systems," *Electron. Lett.*, vol. 52, no. 21, pp. 1797–1799, Oct. 2016.

[20] W. Zhu, K. Zhou, and M. Cheng, "A bidirectional high-frequency-link single-phase inverter: Modulation, modeling, and control," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4049–4057, Aug. 2014.

[21] K. V. Iyer, R. Baranwal, and N. Mohan, "A high-frequency AC-link single-stage asymmetrical multilevel converter for grid integration of renewable energy systems," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5087–5108, Jul. 2017.

[22] K. Basu and N. Mohan, "A high frequency link single stage PWM inverter with common-mode voltage suppression and source based commutation of leakage energy," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3907–3918, Aug. 2013.

[23] S. Gandikota and N. Mohan, "A new leakage energy commutation technique for single stage high frequency link inverters," in *Proc. IEEE Int. Conf. Power Electron., Drives Energy Syst.*, 2014, pp. 1–6.

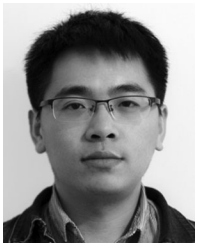
[24] K. S. Muhammad and D. D. Lu, "Magnetically isolated gate driver with leakage inductance immunity," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1567–1572, Apr. 2014.

[25] F. Qi, L. Xu, G. Zhao, and J. Wang, "Transformer isolated gate drive with protection for SiC MOSFET in high temperature application," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 14–18.

[26] C. H. Yu, S. R. Jang, H. S. Kim, and H. J. Ryoo, "Gate driving circuit with active pull-down function for solid-state pulsed power modulator," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 240–247, Jan. 2018.

[27] P. K. Jain, W. Kang, H. Soin, and Y. Xi, "Analysis and design considerations of a load and line independent zero voltage switching full bridge dc/dc converter topology," *IEEE Trans. Power Electron.*, vol. 17, no. 5, pp. 649–657, Sep. 2002.

[28] X. Ruan and Y. Yan, "A novel zero-voltage and zero-current-switching PWM full bridge converter using two diodes in series with the lagging leg," *IEEE Trans. Ind. Electron.*, vol. 48, no. 4, pp. 777–785, Aug. 2001.
[29] A. Safaee, P. Jain, and A. Bakhshai, "A ZVS pulse width modulation full bridge converter with a low-RMS-current resonant auxiliary circuit," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4031–4047, Jun. 2016.
[30] D. Bohn, "Constant-voltage audio distribution systems: 25, 70.7 & 100 volts," Rane Corporation, Mukilteo, WA, USA, 1997, Rep. no. 136.
[31] H. Ma, R. van der Zee, and B. Nauta, "Design and analysis of a high efficiency high-voltage class-D power output stage," *IEEE J. Solid-State Circuits*, vol. 49, no. 7, pp. 1514–1524, Apr. 2014.
[32] "Datasheet: FDP20N50F/FDPF20N50FT N-channel UniFETTM FRFET MOSFET from Fairchild Semiconductor Corporation," Mar. 2013. [Online]. Available:http://www.onsemi.com/pub/Collateral/FDPF20N50FT-D.pdf.
[33] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of AC and DC Active power decoupling circuits for second-order harmonic mitigation in kilowatt-scale single-phase inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 4, no. 1, pp. 15–25, Mar. 2016.
[34] C. Zhao *et al.*, "Design and implementation of GaN-based, 100 kHz, 102W/in3 single-phase inverter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 824–840, Sep. 2016.



Shilin Guo (S'16) was born in Shandong, China, in 1990. He received the B.S. degree in electrical engineering from the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei, China, in 2013, where he is currently working toward the Ph.D. degree in power electronics.

His current research interests include topology and design of high-frequency high-power density power converters, high-frequency magnetic design, single stage audio power amplifiers, and renewable energy generation.

Jianhui Su received the B.Sc., M.A.Sc., and Ph.D. degrees from the Hefei University of Technology, Hefei, China, in 1984, 1987, and 2003, respectively, all in electrical engineering.

He is currently a Full Professor in the School of Electrical Engineering and Automation, Hefei University of Technology and an Associate Director of the Research Center for Photovoltaic System Engineering, Ministry of Education, Hefei, China. His research interests include renewable power generation, special power supply, distributed power generation systems, and high-voltage transducer control technologies.

Jidong Lai received the B.Sc. degree in automatic engineering, and the M.Sc. and Ph.D. degrees in power electronics and power drives from the Hefei University of Technology, Hefei, China, in 2004, 2007, and 2012, respectively.

He is currently a Lecturer in the School of Electrical Engineering and Automation, Hefei University of Technology. His current research interests include distributed generation and microgrid control.

Xiang Yu was born in Jiangsu, China, in 1990. He received the B.S. degree in electrical engineering from the School of Electrical Engineering and Automation, Hefei University of Technology, Hefei, China, in 2013, where he is currently working toward the Ph.D. degree in power electronics.

His current research interests include novel soft-switching topologies, high-density dc–ac converters, and wide-band-gap power semiconductor devices.