An Ultralow Quiescent Current Power Management System With Maximum Power Point Tracking (MPPT) for Batteryless Wireless Sensor Applications

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(Highlighted Paper)

***Abstract*—This paper presents a chip-scale ultralow quiescent current power management system that interfaces with electromechanical energy harvester for enabling self-powering, batteryless wireless sensors. A piezoelectric transducer scavenges and transforms mechanical vibration energy into electricity in ac form, which is then converted into dc power by a full bridge rectifier and collected into a small filter capacitor. A buck–boost converter, as an impedance matching converter to achieve maximum power point tracking, further transfers the energy into a supercapacitor, from which a low-dropout (LDO) regulator powers an on-chip CMOS sensor with clean power supply. Additionally, the energy stored in the supercapacitor can be used to drive a radio frequency transmitter. These components form a complete wireless sensor node, applicable for the Internet of Things sensor networks. The chip is fabricated by using a standard 0.5 μm CMOS process. From measurements we have verified all the key merits of this design: first, a high voltage converting efficiency (up to 97.1%) of the rectifier; second, a minimum of 102 s charging time to charge a 1 mF supercapacitor from 0 to 3.3 V of the buck–boost converter with impedance matching method; and third, a 10 nA to 100 μA load current range and at least 85° phase margin LDO regulator with ultralow quiescent bias current as low as 750 pA.**

***Index Terms*—Buck–boost converter, full bridge rectifier, impedance matching, low-dropout (LDO) regulator, maximum power point tracking (MPPT), power management system, piezoelectric (PZE) energy harvester.**

I. Introduction

WIRELESS sensors are essential building blocks for facilitating interactions between human and environment; and they are becoming pervasive for enabling the Internet of Things (IoT). The rapidly emerging IoT applications and their advances increasingly demand high integration, ultrasmall volume, low cost, long lifetime, and maintenance-free operations [1]–[3]. Therefore, batteryless, self-powering solutions, such as scavenging vibration energy from environment [4]–[6], offer viable alternatives to today's mainstream wireless sensor networks powered by conventional energy sources, such as batteries, which require periodic replacement and maintenance. To realize such solutions, energy harvesting circuits are required to interface with these unconventional energy sources. One major challenge, however, is the ultra-low-power (ULP) consumption requirement in such energy harvesting circuits, energy storage unit, physical sensing element, and wireless communication, largely because of the limited availability of highly compact yet sufficient energy sources [7]–[9].

In order to enhance the energy scavenging, conversion, storage, distribution, and utilization, a number of approaches, including piezoelectric (PZE) transducers, ac–dc converters, dc–dc converters and other essential modules, have been proposed and studied in the last decade. Impedance modeling of PZE transducer has been developed for PZE energy harvesting systems with various interfacing circuits, including standard energy harvesting, parallel synchronized switch harvesting on inductor and series synchronized switch harvesting on inductor [10]. Systematic analysis and comparison of all the principal types of power extraction circuits that allow damping force to be increased, both under ideal conditions and with realistic constraints, have also been conducted [11]. For miniature vibration energy-powered PZE generators and analyzing modes of operation and control of a buck–boost converter for tracking the generator's optimal working point, a comprehensive model has also been developed [12].

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For rectifier design, a method for optimizing voltage conversion rate in full bridge rectifier has been proposed [13] by replacing the passive diodes with an operational amplifier-controlled active counterpart and adding a switch in parallel with the PZE transducer for vibration energy harvesting. This method solves the dc offset problem of the comparator-based active diode and minimizes the voltage drop along the conduction path. CMOS hybrid rectifier has also been studied [14], to simultaneously and efficiently scavenge energy from low-amplitude radio-frequency (RF) signals and low-frequency PZE transducers. An ac–dc converter employing an active-diode-based voltage doubler has also been theoretically and experimentally investigated for low-voltage vibrational energy harvesting systems [15], which has up to 80% energy efficiency for a wide range of load. A disk-shaped PZE transducer with several electrodes for increased energy harvesting from multiple mechanical resonances has been presented and tested by a full-wave rectifier with integrated peak selection [16]. To obtain more power from PZE transducers, a bias-flip rectifier circuit has been implemented [17], which can improve the power extraction capability from PZE harvesters beyond conventional full bridge rectifiers and voltage doublers by a factor of 4. The same method has also been introduced in [18] and [19]. An alternative resonance technique that can boost the PZE output swing as high as CMOS devices can sustain has been proposed [20] for low voltage applications. Another method that inverts energy from the battery into the transducer has been implemented [21], [22] to strengthen the electrostatic force against vibrational work, which leads to drawing more power from the transducer, over 3.6 times than a full-wave bridge rectifier with zero-volt diodes can deliver at its maximum power point.

For dc–dc converter design employed for energy transfer and storage, maximum power point tracking (MPPT) has been widely used as impedance matching method to maximize harvested energy [3], [23]–[25]. Besides, an adaptive on-time dc–dc controller with pulse skipping modulation has been employed in adaptive impedance matching MPPT technique to improve harvesting efficiency [8]. The method in this controller is partially similar to active power factor correction technique to broaden the current range and increase harvested energy. An efficient digital control circuit, instead of conventional comparator based zero current detector (ZCD), has been designed to reduce the quiescent power consumption [17]. Some other optimization methods, such as system optimization techniques [26]–[28] and multiple parallel harvesting energy source techniques [24], [29], [30], have been explored to improve the harvesting efficiency and energy level for sensor applications.

Other necessary components and relevant techniques, such as low quiescent current and low noise low-dropout (LDO) regulator [31], [32], high precision and low noise current bias, and reference voltage for analog front-end sensor nodes [33], can also be essential for the whole vibrational energy harvesting power management systems. To date, most of the aforementioned studies have been focused upon the individual components that make building blocks for enabling energy-scavenging and self-powering sensor nodes. There has been a clear lack, and thus a great need, to explore integration of these building blocks into fully functional systems, to close the technological gaps. Specifically, for sensor nodes powered by vibrational energy harvesters, although extensive efforts have been made on PZE-based energy harvesters, studies on application specific integrated circuits (ASIC) that interface with these harvesters have remained elusive, especially for ASIC that monolithically integrate both power management functions and physical sensors on the same chip. If we can realize the monolithic integration of the physical sensors, signal transduction for sensing, energy harvesting, and energy management on the same CMOS chip, a holistic, system-level view can be taken in optimizing the design parameters; and we expect this to lead to major improvement in overall performance and energy efficiency.

Meantime, while ultralow quiescent power design is generally desirable for all energy management ASIC, it is particularly crucial for energy-harvesting and self-powering wireless sensor nodes toward IoT applications. In the ASIC that monolithically integrate energy harvesting power management and physical sensors, ultralow quiescent power designs are especially essential. For self-powering wireless sensor nodes in IoT applications, even though the designs for each building block have been studied previously, new challenges are emerging given that the power input from the miniature vibrational energy harvesters can be as low as sub-nW level. To tackle such challenges, we have deliberated our considerations and design efforts in several aspects.

1) The ASIC not only need to be more adaptive to a wide range of possible energy input, but also should eliminate nonessential components as much as possible, in order to minimize standby power consumption.
2) We carefully engineer the important technical trade-offs between precision and speed, and others, to attain best possible reduction in power consumption.
3) We fully leverage the features of the chosen CMOS process for fabricating the ASIC, to approach the lowest possible power consumption set by the practical limits of this particular process.

Based on the above discussions, in this paper we design, implement, and demonstrate an ultralow quiescent current ASIC that integrates both the power management system and the physical sensor (in this case, a CMOS temperature sensor), for self-powering, wireless temperature sensing applications. Fig. 1 illustrates the block diagram of the whole architecture of harnessing vibrational energy for powering a wireless temperature sensor. The sensor system includes six parts: a PZE energy harvester, a power management system, a temperature sensor, an RF circuit, a wireless gateway, and a monitor.

The main body of this paper is organized as follows. In Section II, the architecture of the power management system is introduced, which includes operating principles and relationship among the circuit nodes and their voltages of the power management system. In Section III, analysis of the PZE transducer is presented, followed by the impedance matching design for a buck–boost converter in order to achieve MPPT. Design consideration and circuit implementation of the power management system are described in Section IV. Detailed description of the experimental studies and results demonstrating the designed ULP power management system are presented in Section V. Finally, the conclusions are drawn in Section VI.

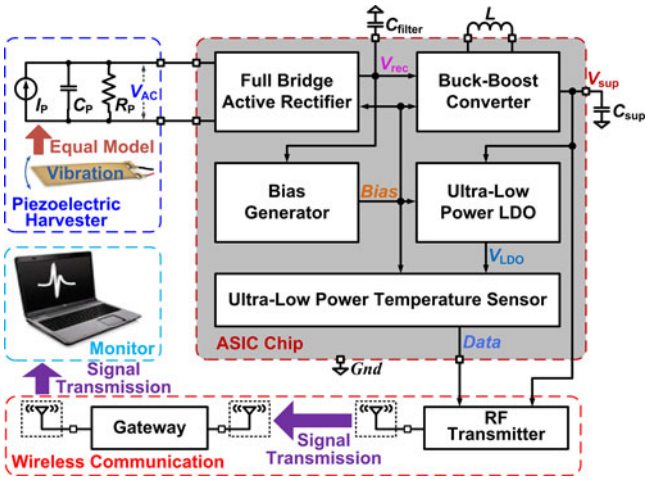

Fig. 1. Schematic illustration of the architecture of the self-powering sensor node with the proposed ASIC that monolithically integrates both the power management functions and the temperature sensor.

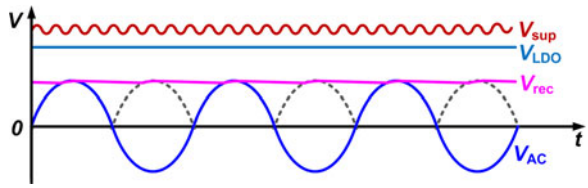

Fig. 2. Time evolution of voltage waveforms at the important nodes of the circuit.

II. Power Management System Architecture

The power management system, as shown in Fig. 1, includes a full bridge active rectifier, a hysteresis controlled buck–boost converter, and an ultralow quiescent current LDO regulator. The PZE transducer, which is equivalent to an ac current source at the vibration frequency in parallel to a capacitor and a resistor (see Fig. 1), transforms the mechanical vibrational energy into electricity. The current source provides a current proportional to the input vibration amplitude and generates an ac output voltage, $V_{\rm AC}$, at the same frequency as the ac current. A full bridge rectifier then converts this ac voltage to dc voltage, $V_{\rm rec}$ (the output voltage of the active rectifier), and store the energy into a small filter capacitor, $C_{\rm filter}$. A bias generator is directly powered by $V_{\rm rec}$, providing quiescent bias current and reference voltage for all other modules in the ASIC. A buck–boost converter further transfers the energy from the filter capacitor to a supercapacitor, $C_{\rm sup}$, with impedance matching to achieve MPPT. The stored energy in the supercapacitor ($E_{\rm sup} = 1/2 C_{\rm sup} V_{\rm sup}^2$, where $V_{\rm sup}$ is the voltage of the supercapacitor and also the output voltage of the buck–boost converter) powers the ultralow quiescent current LDO regulator and the RF module. The LDO regulator further provides clean and stable voltage supply, $V_{\rm LDO}$, to drive the on-chip temperature sensor, from which the environment temperature data is collected and sent by the RF transmitter. The RF gateway receives the environment temperature data and sends it to a PC or smart phone which displays the readings to users.

Fig. 2 schematically illustrates the evolution of the output voltage of each submodule in the power management system from the harvested energy, which shows the relations between the voltage signals on the ASIC ($V_{\rm AC}$, $V_{\rm rec}$, $V_{\rm sup}$ and $V_{\rm LDO}$, all defined in Fig. 2) in steady state.

The startup procedure of the ASIC is configured as the following: First, assume the ASIC starts in a completely powered-off state with no initial energy stored in all the capacitors and inductors. As energy input from the PZE transducer starts to charge $C_{\rm filter}$, $V_{\rm rec}$ starts increasing. Once $V_{\rm rec}$ exceeds a threshold voltage, the on-chip bias generator begins to work, providing bias current and reference voltage for the comparators and amplifiers of the entire ASIC; then the buck–boost converter and LDO regulator start operating; and then $V_{\rm sup}$ and $V_{\rm LDO}$ begin to increase with the same slope. Once $V_{\rm LDO}$ reaches a reference voltage (sufficient for powering the on-chip temperature sensor), it stops increasing. $V_{\rm sup}$ continues to rise until reaching a high reference voltage, which means the supercapacitor has sufficient energy to power the RF transmission module, then, the buck–boost converter operates in its steady state.

III. Impedance Matching Analysis

To achieve MPPT with simple control and low power consumption of the buck–boost converter, we first study the internal impedance feature of the PZE transducer, and then, we focus on discussing the impedance matching design of the buck–boost converter.

A. Impedance and Power Output of PZE Transducer

A PZE energy harvester is modeled by a current source in parallel to a capacitor and resistor (I_p, C_p and R_p, shown in Fig. 1). The current source provides current proportional to the input vibration amplitude. To simplify the following analysis, the input vibrations are assumed to be sinusoidal in nature, thus, the transient current is represented as $i_p(t) = I_p \sin(\omega_p t)$, where $\omega_p = 2\pi f_p$ and f_p is the frequency at which the PZE harvester is excited [3]. Normally R_p is large enough and can be considered as open circuit, thus, the value of internal impedance of the PZE cantilever, $Z_{\rm int}$, can be written as

$$Z_{\rm int} = \frac{1}{\omega_p C_p} = \frac{1}{2\pi f_p C_p}. \tag{1}$$

According to (1), $Z_{\rm int}$ is represented by the impedance of the internal plate capacitor, C_p, of the PZE material, and changes with the frequency of the variation f_p. Thus, $Z_{\rm int}\, f_p = 1/2\pi C_p$ is constant, which means that $Z_{\rm int}$ is inversely proportional to f_p. Each PZE transducer has its intrinsic resonant frequency and internal plate capacitor (determined by crystalline material, fabrication process, geometry, volume, and mass). For a random trigger or step or pulse excitation, the PZE transducer exhibits damped ring-down oscillations at its intrinsic resonant frequency, where it presents constant impedance in this circumstance. If ideal diode model is adopted (no voltage drop on *p-n* junction), according to Fig. 1, the output power, $P_{\rm rec}$, of the PZE transducer can be given by

$$P_{\rm rec} = V_{\rm rec} i_p = V_{\rm rec} \frac{(V_{\rm oc} - V_{\rm rec})}{Z_{\rm int}} = 2\pi f_p C_p V_{\rm rec} (V_{\rm oc} - V_{\rm rec}) \tag{2}$$

where the terms $V_{\rm oc}$ is the open-circuit voltage amplitude at the output of the PZE transducer, which can be represented as

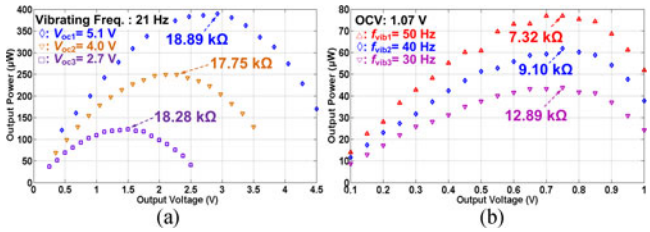

Fig. 3. Measured characteristics of the output power versus output voltage of the PZE transducer: (a) At fixed frequency with different vibration amplitude. (b) With fixed amplitude but at different vibrating frequency.

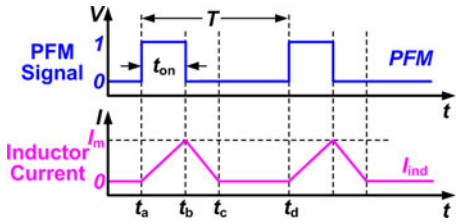

Fig. 4. Waveform variation of the inductor current in one switching period, *T*, of the PFM signal.

$V_{\rm oc} = I_p\,/2\pi f_p C_p$, and $V_{\rm rec}$ is the output voltage of the rectifier (see Fig. 1). Thus, the maximum output power can be obtained by

$$P_{\rm rec.max} = \frac{\pi f_p C_p V_{\rm oc}^2}{2}\left(\text{where } V_{\rm rec} = \frac{V_{\rm oc}}{2}\right). \tag{3}$$

In order to verify the features in (1) and (2), a 45 mm × 45 mm PZE transducer is measured. An adjustable dial resistance box is connected to the two ports of the PZE transducer as the external resistance load. We measure and record the root-mean-square value of the output voltage of the PZE transducer. Here, in order to guarantee the accuracy of the measured data, an LF357 amplifier with 10^{12} Ω input impedance is employed as a buffer, instead of directly connecting the testing points (nodes) and the probes (which have ∼10^6 Ω to ∼10^7 Ω input impedance) of the measuring equipment (e.g., Oscilloscope and Digital Multimeter). The same testing protocol has also been used and kept consistent throughout all the subsequent tests.

Fig. 3 demonstrates the measurement results. Fig. 3(a) displays the output power versus output voltage curves under fixed frequency (21 Hz) of the PZE transducer with different vibration amplitude, i.e., at different open-circuit voltage (OCV): $V_{\rm oc}$ = 2.7 and 5.1 V, respectively. When the output power reaches its maximum value, the calculated internal impedance under different OCV of the PZE transducer are $Z_{\rm int} = 18.89$, 17.75, and 18.28 kΩ, respectively, which are almost equal to each other. Fig. 3(b) depicts the output power versus output voltage characteristics under a fixed OCV ($V_{\rm oc} = 1.07$ V) of the PZE transducer at different vibrating frequency ($f_{\rm vib} = 30$, 40 and 50 Hz). At the maximum power points (MPP) of the measured curves in Fig. 3(b), the calculated internal impedance of the PZE transducer are $Z_{\rm int} = 12.89$, 9.10, and 7.32 kΩ, respectively. Therefore, based on (1), the calculated values of the internal plate capacitor, C_p, of the PZE transducer, are 412, 437, and 435 nF, respectively, which are also almost equal to each other.

B. Impedance Matching of Buck–Boost Converter

Based on (2), the output power of the PZE transducer also can be written by

$$P_{\rm rec} = \frac{V_{\rm rec}^2}{R_{\rm eq}} \tag{4}$$

where $R_{\rm eq}$ represents the external equivalent resistance which the PZE transducer drives. Thus, by combining (2) and (4), the relationship between equivalent resistance and the output voltage of the rectifier can be obtained by

$$R_{\rm eq} = \frac{V_{\rm rec}}{2\pi C_p f_p\,(V_{\rm oc} - V_{\rm rec})}. \tag{5}$$

According to (5), with the increase of $V_{\rm rec}$, $R_{\rm eq}$ increases rapidly. At low values of $V_{\rm rec}$, most of the charge available from the harvester flows into the output, but the output power is low. At high values of $V_{\rm rec}$, very little charge flows into the output, thus, the output power is still low. These opposite trends cause the output power of the full bridge rectifier to vary with $V_{\rm rec}$. When $V_{\rm rec} = V_{\rm oc}/2$, the output power reaches its peak value and MPPT is achieved; at this condition, the equivalent resistance, $R_{\rm eq.MPPT}$, can be written by

$$R_{\rm eq.MPPT} = \frac{1}{2\pi C_p f_p}. \tag{6}$$

In this circumstance, because $f_{\rm p}$ is equal to the intrinsic resonant frequency of the PZE transducer, $R_{\rm eq.MPPT}$ is constant, which means if the designed equivalent resistance of the impedance matching converter is equal to $R_{\rm eq.MPPT}$, the converter can transfer the maximum power to the supercapacitor without any complex tracking control circuit.

Considering the wide range of the output voltage and the low output power levels of the small-scale or even miniature PZE transducers of interest, we choose to employ a four-switch buck–boost converter under pulse frequency modulation (PFM) operating in the inductor current discontinuous conduction mode (DCM), as the impedance matching converter. Therefore, the waveform variation of the inductor current in one switching period, *T*, of PFM signal can be illustrated in Fig. 4.

Assuming the ideal diode model in used in the full bridge rectifier, and the buck–boost converter is connected with the rectifier in cascade. Thus, the input voltage of the buck–boost converter is the output voltage of the full bridge rectifier and is equal to $V_{\rm rec}$, as shown in Fig. 1. According to Fig. 4, inductor current, $i_{\rm ind}(t)$, of the buck–boost converter in the time interval $t_{\rm on}$ (from t_a to t_b, pulse width duration) is

$$i_{\rm ind}(t) = \frac{V_{\rm rec}}{L}t, t \in [0, t_{\rm on}] \tag{7}$$

where L is the inductance value of the inductor in the buck–boost converter. Thus, the input energy, $E_{\rm in}$, of the buck–boost converter during the interval $t_{\rm on}$ (from t_a to t_b) is obtained by

$$E_{\rm in} = \int_0^{t_{\rm on}} V_{\rm rec} i_{\rm ind}(t_1) dt_1 = \frac{V_{\rm rec}^2}{2L} t_{\rm on}^2. \tag{8}$$

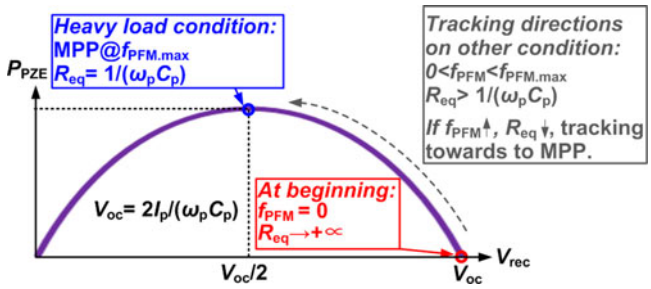

Fig. 5. Power point tracking under different loading conditions, with varying PFM frequency.

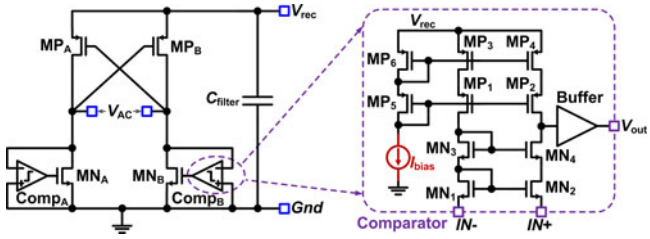

Fig. 6. Transistor implementation of the full bridge active rectifier.

For the buck–boost converter, the total input energy in one switching period T is just the input energy within $t_{\rm on}$ (see Fig. 4). According to the energy conservation law, the average input power, $P_{\rm in.avg}$, of the Buck–Boost converter is thus

$$P_{\rm in.avg} = \frac{E_{\rm in}}{T} = \frac{V_{\rm rec}^2}{2L}\frac{t_{\rm on}^2}{T}. \tag{9}$$

The output power of PZE transducer should equal the input power of the buck–boost converter in steady state. Thus, by combining (4) and (9), $R_{\rm eq}$ can be written as

$$R_{\rm eq} = \frac{2LT}{t_{\rm on}^2} = \frac{2L}{t_{\rm on}^2 f_{\rm sw}} \tag{10}$$

where the terms $t_{\rm on}$ is the pulse width duration (i.e., the time of inductor current increasing period, see Fig. 4) of the switching period time signal, T is the switching period cycle, and $f_{\rm sw}$ is the switching frequency of the buck–boost converter, as shown in Fig. 4, where $f_{\rm sw} = 1/T$.

According to (10), $R_{\rm eq}$ is inversely proportional to $f_{\rm sw}$, L and $t_{\rm on}$ are easy to design as constants. In order to achieve impedance matching to guarantee MPPT, $f_{\rm sw}$ should be adaptively regulated by the converter, to meet the requirement of the internal impedance of the PZE transducer. By combining (6) and (10), the switching frequency of the buck–boost converter at MPPT, $f_{\rm sw.MPPT}$, can be written by

$$f_{\rm sw.MPPT} = \frac{4\pi L C_p f_p}{t_{\rm on}^2}. \tag{11}$$

Towards ULP applications, hysteresis controlled dc–dc converters are widely explored because of their simple control circuit, low power consumption, and self-adjustable switching frequencies. In addition, normally one supercapacitor is adopted as the energy storage unit in batteryless sensor node applications. Therefore, only under heavy load conditions, the equivalent resistance of the buck–boost converter is required to match the internal impedance of the PZE transducer. In other loading ranges, the desired equivalent resistance should be as high as possible, so as to increase the output voltage while reducing the power consumption of the PZE transducer.

Based on the above analysis, a hysteresis controlled PFM mode buck–boost converter is adopted with the designed maximum PFM frequency, $f_{\rm PFM.max}$, being equal to $f_{\rm sw.MPPT}$ in (11). Fig. 5 demonstrates the diagram of the power point tracking under different loading conditions with varying PFM frequency.

IV. Circuit Implementation

The power management ASIC system (see Fig. 1) includes following four modules.

1) A full bridge active rectifier, which rectifies the ac input from the PZE vibrational energy harvester with high voltage conversion rate.
2) A hysteresis controlled buck–boost converter, which uses the rectified energy input to charge the supercapacitor, and maintains high charging efficiency.
3) An ultralow quiescent current LDO regulator, which provides clean and stable supply voltage with low ripples and noise for next stage sensor loads.
4) An ultralow quiescent current bias generator, which is directly powered by $V_{\rm rec}$, to provide the necessary quiescent bias current and reference voltage for other modules on the ASIC. The detailed circuit implementation is described in the following sections.

A. Full Bridge Active Rectifier

The complete transistor implementation of the full bridge active rectifier is shown in Fig. 6. The rectifier includes two NMOS and two PMOS power switches to form a full bridge rectification structure (see the left panel of Fig. 6). Because of the high peak-to-peak output voltage feature of the PZE transducer, the PMOS switches can be driven by a cross coupled connection, which can be adaptively tuned on the PMOS transistors, thus keeping the PMOS operation in the triode regime to cut down the drain-source voltage drop. In order to further decrease the internal body to drain drop voltage (*p-n* junction) of the NMOS switches, two comparators are adopted to achieve active gate driving of the NMOS by detecting the voltage difference between the drain and source of the switches all the time. The transistor implementation of the comparators is shown in the right panel of Fig. 6. Considering environmental low-frequency ambient vibrational energy harvesting scenarios of interest (e.g., with PZE transducers, often lower than 200 Hz in their resonance frequencies [3]), the typical telescopic common gate structure amplifier with subthreshold operating region is adopted, and totally only 40 nA quiescent bias current is consumed in the comparator, which has attained enough dc gain and nearly 10 kHz unit gain band-width (UGBW) in a wide supply voltage range to guarantee the turn-off of the NMOS on-time.

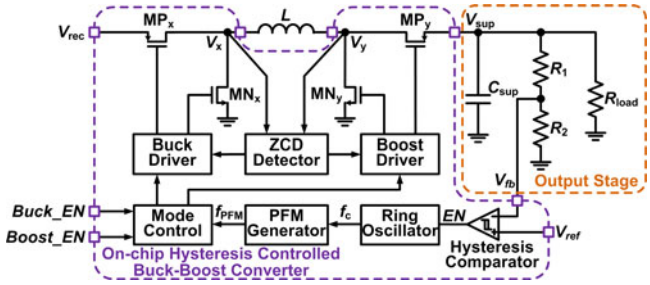

Fig. 7. Architecture of the hysteresis controlled Buck–Boost converter.

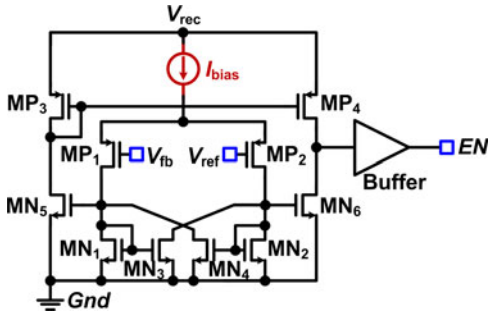

Fig. 8. Transistor implementation of the hysteresis comparator.

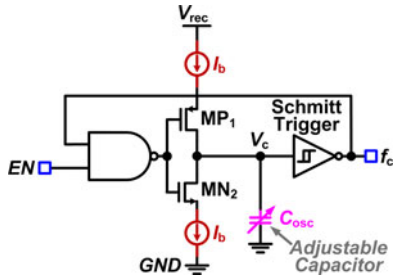

Fig. 9. Schematic of the ring oscillator.

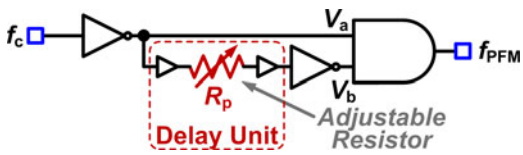

Fig. 10. Schematic of the PFM generator.

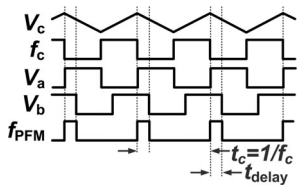

Fig. 11. Time diagram of the ring oscillator and PFM generator.

B. Buck–Boost Converter

Based on the discussions in Section III, as the impedance matching converter achieves MPPT, we implement a buck–boost converter with the hysteresis controlled PFM mode. The entire architecture of the buck–boost converter is shown in Fig. 7. A hysteresis comparator is employed to generate the enabling signal, EN, by comparing the feedback voltage, $V_{\rm fb}$, to the reference voltage, $V_{\rm ref}$, all the time, so as to control the operations of the ring oscillator. When $V_{\rm fb} > V_{\rm ref}$, the voltage on the supercapacitor, $V_{\rm sup}$, reaches the preset desired value; this leads to $\rm EN = 0$, thus $f_c = 0$, no $f_{\rm PFM}$ signal output and all the power switches are kept OFF. When $V_{\rm fb} < V_{\rm ref}$, the voltage on the supercapacitor is lower than the preset value, $\rm EN = 1$, thus f_c outputs as clock signal, $f_{\rm PFM}$ signal controls the ON/OFF states of the power switches of the Buck–Boost converter. A PFM generator is designed to provide $f_{\rm PFM}$ signal with proper pulse width from f_c. A mode control module is used to realize the buck, buck–boost, or boost topology modes in different input/output voltage ranges. A ZCD module is designed to control the OFF state of the synchronous rectifying switches ($\rm MN_{\it x}$ and $\rm MP_{\it y}$ in Fig. 7), so as to prevent formatting of the reverse inductor current after the inductor current decreases to zero. Both the buck driver and boost driver modules (including a level shifter to regulate the amplitude of the driving signal for $\rm MP_{\it y}$) are designed to generate the nonoverlap driving signals with enough drive capability to control the ON/OFF states of the power switches. A supercapacitor is connected to the output node of the buck–boost converter, which is employed as the energy storage unit to supply the LDO regulator and RF module. In order to further reduce the quiescent current consumption, an EN is employed to control the ON/OFF states of the bias current of other modules (e.g., the ring oscillator and the ZCD detector).

Fig. 8 shows the transistor implementation of the hysteresis comparator, which consumes merely 10 nA quiescent bias current with subthreshold operating region, and has a nearly 20 mV trigger window voltage to guarantee a UGBW of several hundred Hz, as well as an output voltage with as low as possible ripples, for the buck–boost converter.

Fig. 9 shows the schematic of the ring oscillator that includes a positive feedback loop involving a Schmitt trigger. In order to achieve impedance matching of the designed converter, according to (10), both the pulse width and frequency of the PFM signal, $f_{\rm PFM}$, should be adjustable. Because the frequency of the PFM signal equals that of the clock signal ($f_{\rm PFM} = f_c$), f_c needs to be adjustable. The variable capacitor in the ring oscillator, $C_{\rm osc}$, can easily modify the value of clock frequency f_c by

$$f_c = I_b / (2C_{\rm osc}\Delta V) \tag{12}$$

where $I_{\rm b}$ (5 nA) is the bias current, and ΔV is the trigger window voltage of the Schmitt trigger.

Fig. 10 shows the schematic of the PFM generator. The variable resistor, R_p, in PFM generator can be easily used to adjust the delay time of V_b. The pulse width frequency of $f_{\rm PFM}$ is established by the comparison between V_a and V_b.

Fig. 11 depicts the timing diagram of the ring oscillator and the PFM generator.

Finally, based on the above discussions, an 820 μH inductor is selected, and 10 μs pulse width with maximum 1 kHz switching frequency for the buck–boost converter is designed, to match a nearly minimum value of 16 kΩ impedance for MPPT.

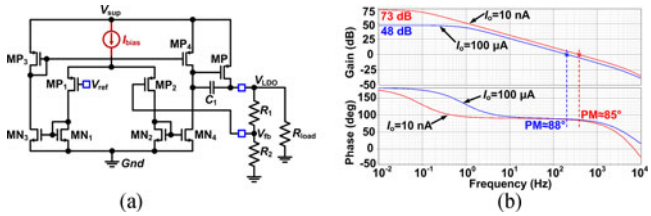

Fig. 12. LDO regulator: (a) Transistor implementation. (b) Open loop frequency response under extreme load conditions.

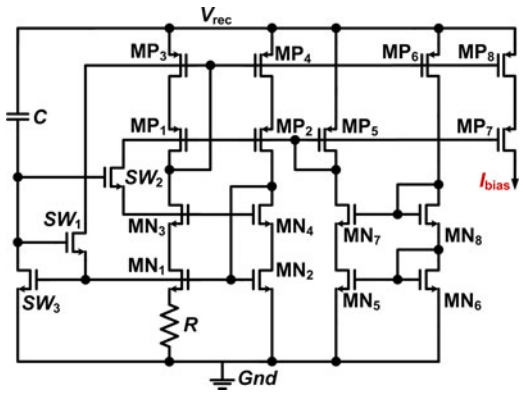

Fig. 13. Transistors implementation of the bias generator.

C. LDO Regulator

Fig. 12(a) shows the transistor implementation of the cap-less LDO regulator, which is a typical two-stage common-source amplifier by employing an on-chip capacitor, C_1, as the compensation capacitor to guarantee loop stability. The total quiescent current consumption of the designed LDO is only 750 pA (250 pA for $I_{\rm bias}$, and 500 pA for $\rm MP_3$ and $\rm MP_4$) to realize subthreshold operating regime with high dc gain and to achieve load current range from 10 nA to 100 μA. The Cadence post-simulation results of the open loop frequency response under extreme load conditions are given in Fig. 12(b). The simulation results exhibit good stable stability with at least 85° phase margin (PM).

D. Bias Generator

In order to guarantee the valuable operating with ultralow quiescent current of the power management system, an auxiliary on-chip bias generator circuit, which provides quiescent bias current and reference voltage for the comparators and amplifiers of the entire ASIC, is designed on chip [33]. Fig. 13 shows the full transistors implementation of the bias generator.

E. ULP Design Challenge

Towards self-powering systems using PZE vibrational energy harvesters for IoT applications, the level of energy scavenged and power generated from the environment can be often limited. Thus, reducing power consumption and improving power conversion efficiency of the power management system are critical for extending operation time and broadening the application scope of the PZE vibrational harvesting systems. Compared to the conventional design, in order to achieve high energy conversion efficiency in very light load range of the power management ASIC system, both quiescent and dynamic power consumption need to be reduced by optimizing the design. Our detailed design considerations are discussed below:

1) *Quiescent power optimization*: Quiescent power is a product of the sum of the quiescent bias currents of the bias generator, amplifier, comparator, oscillator, and the feedback resistance network (buck–boost converter and LDO regulator). Thus, reducing the usage of the above mentioned components or modules and decreasing the value of bias current can lower quiescent power consumption significantly. The designed bias current in this ASIC is 10 nA and below, toward making the maximum quiescent power consumption as low as possible. The minimum quiescent power consumption is achieved when only one bias generator, one hysteresis comparator, one oscillator, and two feedback networks are operating. Besides, for hysteresis controlled buck–boost converter, when the output voltage is higher than the desired value, all the quiescent currents in the buck–boost converter module except hysteresis comparator can be eliminated, thus further reducing the quiescent power consumption.
2) *Dynamic power optimization*: Dynamic power consumption is mainly generated by the oscillator, PFM signal generator, drivers, conduction loss of the power switches in buck–boost converter and rectifier, and active control of the full bridge rectifier. Thus, optimization of the buck–boost converter and active full bridge rectifier design will reduce the dynamic power effectively. For buck–boost converter design, the key parameters for optimizing are the turn-ON period of the power switches, peak inductor current and frequency of the PFM signal. For self-powering PZE vibration harvester applications, the buck–boost converter is usually operating in DCM. In this condition, The PFM conducting time is fixed, and in stable operations, the energy through buck–boost converter is discretized into equal amount. Without considering the quiescent power consumption, the energy conversion efficiency of the buck–boost converter is constant. Therefore, optimization of dynamic power consumption within a single PFM period is essential for improving the energy conversion efficiency of the buck–boost converter. For the full bridge rectifier, because of the low frequency of the PZE harvester, the variation rate of the current is very small, even in reverse. Thus, the precision of turn-off time of the active control can be reduced, which decreases both quiescent bias current of the comparators and the drive ability. All these can further improve the energy conversion efficiency of the power management system.

F. Quiescent Current Summary

Upon completion of the ASIC design, the individual quiescent current performance of each module of the power management system is summarized in Table I. A 1.2 V reference voltage is generated for buck–boost converter and LDO regulator by

TABLE I
SUMMARY OF QUIESCENT CURRENT CONSUMPTION IN THE ASIC

Bias Generator	50 nA	bias current: 40 nA, ref. voltage:10 nA
Full Bridge Rectifier	0 nA 40 nA	without active diode driving with active diode driving
Buck-Boost Converter	15 nA* 95 nA	without ZCD control with ZCD control
LDO Regulator		0.75 nA

15 nA*: 10 nA for hysteresis comparator, 5 nA for ring oscillator, when $EN = 0$, just 10 nA consumed.

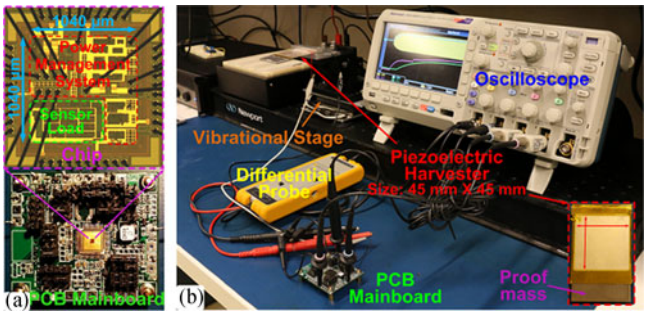

Fig. 14. Experimental testing apparatus and results: (a) Micrograph of the ASIC chip and photo of the circuit board after wire bonding and integration onto the PCB. (b) Testing platform of the entire ASIC and self-powering sensor node.

flowing a 10 nA quiescent bias current through a 120 MΩ resistor to *Gnd*. Therefore, we can see that as low as 65.75 nA (50 nA+15 nA+0.75 nA) quiescent current is required for the entire power management system, which is very small and much suitable for ULP energy harvesting applications.

V. EXPERIMENTAL RESULTS

The ASIC chip has been fabricated by using a standard 0.5 μm CMOS process. Fig. 14(a) displays the chip micrograph after wire bonding with an active core area of 1.04 mm × 1.04 mm and the printed circuit board (PCB) mainboard with area of 50 mm × 55 mm for chip test. Fig. 14(b) shows the actual test platform including the vibrational stage (an environmental ambient vibration simulator), PZE harvester, PCB mainboard, ASIC chip, oscilloscope, and probes.

For minimum startup voltage requirement of the bias generator of the ASIC chip, the range of valid voltage supply from the PZE transducer is between 1.8 to 5.0 V. When $V_{\rm rec}$ exceeds the 1.8 V minimum cold-start voltage, the bias generator begins to work and provides the necessary current bias for the entire ASIC, then the power management system (active driving of rectifier, buck–boost converter and LDO) and on-chip temperature sensor all start operating. The output voltage of the buck–boost converter $(V_{\rm sup})$ can be set as a tunable voltage range between 3.1 to 5 V, and the output voltage of the LDO regulator $(V_{\rm LDO})$ is set as 3.0 V to drive the on-chip temperature sensor. The bias generator provides 1.2 V reference voltage to the Buck–Boost converter and LDO regulator, each feedback resistance network consumes as low as 10 nA quiescent current. $C_{\rm filter}$ is 10 μF, L is 820 μH, $t_{\rm on}$ period time is designed as 10 μs and the maximum

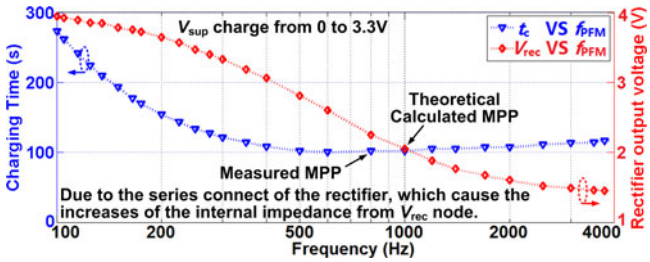

Fig. 15. Charging time and output voltage versus PFM frequency.

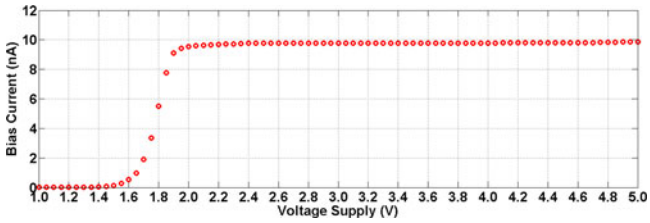

Fig. 16. Measured bias current versus voltage supply of the current bias generator at room temperature.

PFM switching frequency is set to 1 KHz. $C_{\rm sup}$ is chosen as 10 μF for transient test and 1 mF for charging test and long time operation.

To verify the impedance matching design of the buck–boost converter, a set of tests are taken and we have thus obtained the measured data on the charging time of the supercapacitor and output voltage of the rectifier versus different PFM frequency under the same test platform condition, the same PZE transducer and its operating condition (30 Hz, 4.1 V open circuit voltage), the same pulse width of PFM signal (10 μs), the same charging supercapacitor (1 mF). The measured results are shown in Fig. 15, which very well match the design.

Since the bias generator provides bias current and reference voltage for all other modules of the ASIC chip, it is essential to test the performance of the designed circuit in detail. We conduct detailed measurement of the bias current at room temperature in ambient environment. Fig. 16 shows the perfect performance of the bias generator, with a dynamic error below 1% when the voltage supply is larger than 2.0 V.

To quickly measure the transient response of the presented power management system, a 10 μF capacitor is adopted instead of the supercapacitor as the energy storage unit. Considering the slow increase of the reference voltage after the cold start, an on-chip RC charging circuit using one branch of the bias current is designed to obtain a low supply voltage control signal, so as to guarantee boost control mode before bias generator operating at startup period with no quiescent and dynamic power consumption. Fig. 17 displays the measured transient waveforms of the full bridge rectifier. In Fig. 17(a), the startup period is measured, we can see that once $V_{\rm rec}$ exceeds a threshold voltage, the active diodes start working because of the on-chip bias generator begins to work and provides the necessary current bias for the comparators of the rectifier. Fig. 17(b) shows the measured waveform of the full bridge rectifier with/without active diode control in steady state. Fig. 18 demonstrates the measured voltage conversion rate under different load conditions

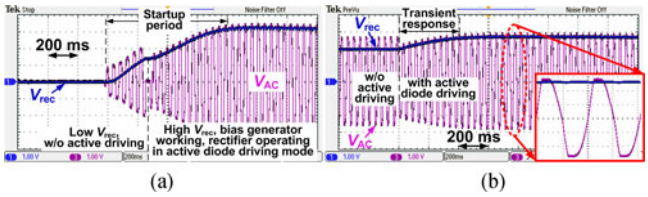

Fig. 17. Measured waveforms of the full bridge rectifier: (a) In startup period with active diode control. (b) With and without active diode control in steady state.

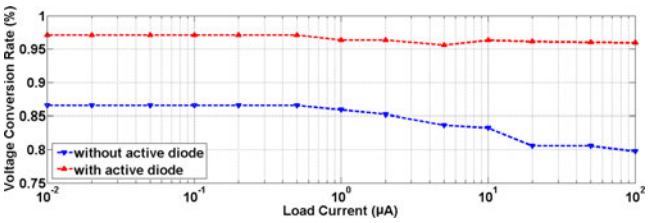

Fig. 18. Measured voltage conversion efficiency under different load conditions with and without active diode control of the full bridge rectifier.

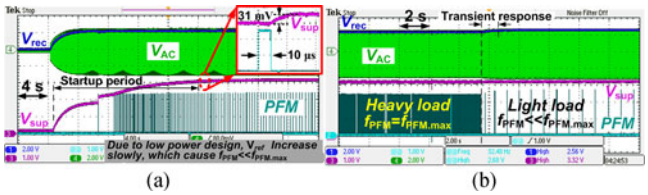

Fig. 19. Measured waveforms of the Buck–Boost converter powered by PZE transducer: (a) In startup period. (b) Under extreme load conditions.

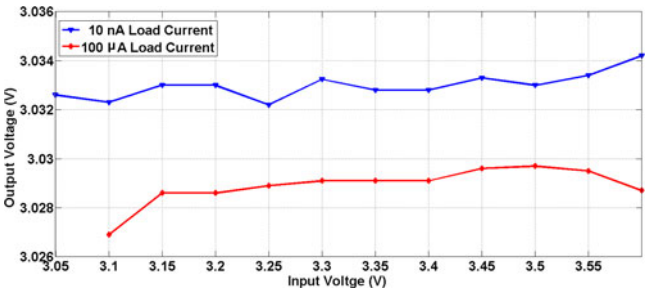

Fig. 20. Measured line regulation of the LDO regulator.

with/without active diode control of the full bridge rectifier; and the measured maximum voltage conversion rate is up to 97.1% when the active diode control is enabled.

Fig. 19(a) shows the measured output waveforms of the active rectifier, buck–boost converter and PFM signal in startup period, due to the low power design, the reference voltage increases very slowly, the PFM controller also needs a long setup time period to start working, then $V_{\rm sup}$ is boosted to the desire value. Fig. 19(b) exhibits the measured waveforms of the buck–boost converter under extremely load condition. The frequency of the PFM signal is adaptive adjusted very well by the hysteresis control loop of the buck–boost converter.

In order to evaluate the performance of the LDO regulator, the line regulation, load regulation, and transient response of the LDO regulator are measured. The results of line regulation and load regulation are shown in Figs. 20 and 21, respectively,

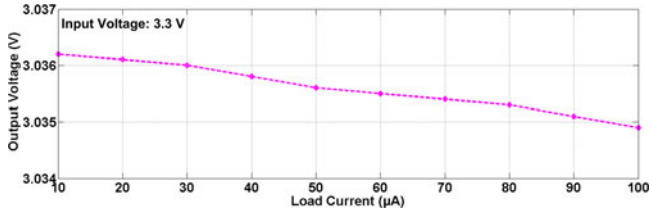

Fig. 21. Measured load regulation of the LDO regulator.

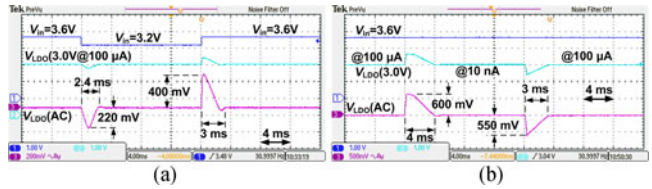

Fig. 22. Measured waveforms of the LDO regulator: (a) In line transient response. (b) In load transient response.

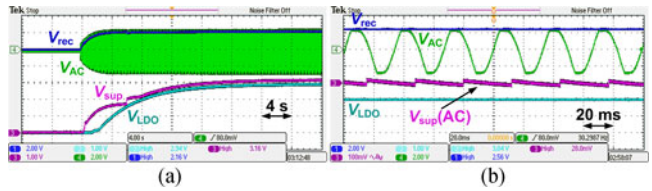

Fig. 23. Measured waveforms of the power management system: (a) In startup period. (b) In steady state.

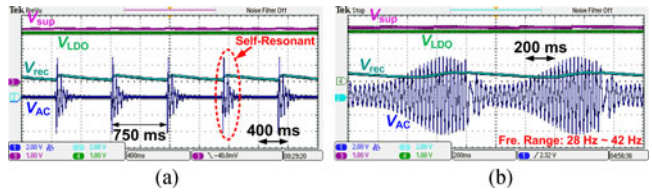

Fig. 24. Measured transient response of the whole power management system: (a) In pulse trigger. (b) In linear frequency sweep.

which reflect dc characteristics of LDO regulator. Fig. 20 shows that the variations of the output voltage are 2.0 and 2.8mV when the input voltage changes from 3.1 to 3.6 V under the current conditions of 10 nA and 100 μA, respectively. The calculated line regulations are 4.0 and 5.6 mV/V, respectively. Fig. 21 shows the variation of the output voltage is 1.3 mV under 3.3 V input voltage when load current changes from 10 to 100 μA. The calculated load regulation is 0.014 mV/μA.

Fig. 22(a) shows the experimental results of line transient response. When the input voltage step changes between 3.2 V and 3.6 V with transient time of 100 ns, the settling time and spick voltage are 2.4 ms with 220 mV undershoot and 3.0 ms with 400 mV overshoot, respectively. Fig. 22(b) demonstrates the measurement waveforms of load transient response. When the load current step changes between 10 nA and 100 μA with step-change time of 100 ns, the settling time and spike voltage are 3.0 ms with 550 mV undershoot and 4.0 ms with 600 mV overshoots, respectively. The ultralow quiescent current enables low UGBW of the LDO regulator, which in turn leads to a little longer response period time. Even though, the designed LDO

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY PUBLISHED WORKS

	Sankman's [8]	Aktakka's [18]	Sanchez's [19]	Yuk's [20]	Kwon's [22]	This work
Process	0.25 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	**0.5 μm CMOS**
Chip area	4.00 mm^2	0.25 mm^2 (active area)	N/A	5.52 mm^2	2.34 mm^2 (active area)	**2.25 mm^2**
Architecture	Rectifier+ Boost converter	Rectifier	Rectifier	Rectifier	Rectifier	**Rectifier+ Buck–Boost converter + LDO**
Input voltage	N/A	N/A	N/A	N/A	2.6 V	**1.8–5.0 V**
Cold-start voltage	N/A	N/A	0.54 V	N/A	N/A	**1.8 V (limited by Bias Gen.)**
PZE transducer frequency	60 Hz	155 Hz	134.6–229.2 Hz	100 Hz	143 Hz	**28–42 Hz**
PFM frequency	50 kHz	–	–	–	–	**$\leq$ 1 kHz**
Inductor	330 μH	–	–	–	–	**820 μH**
Storage unit	4.7 mF supercapacitor	70 mF supercapacitor	N/A	N/A	N/A	**1 mF supercapacitor**
Output voltage	N/A	N/A	0.7–5 V	4 V	N/A	**3.0 V (for on-chip sensor load)**
Quiescent current	450 nA	N/A	N/A	N/A	N/A	**65.75 nA (incl. bias and ref. volt.)**
MPPT	Yes	No	No	No	No	**Yes**
Input power range	12 μW–1.1 mW	95 μW	4 μW–1 mW	81 μW	79 μW	**100 nW–330 μW**

still satisfies the loading requirement of the on-chip sensor, which needs to transduce the environmental temperature data per minute.

The measured results of the whole power management system are shown in Fig. 23. The measured waveforms of the full bridge rectifier, buck–boost converter and LDO regulator in startup period are shown in Fig. 23(a), when PZE transducer start vibrating, $V_{\rm rec}$ increases first, then $V_{\rm LDO}$ increases with the increasing of $V_{\rm sup}$, until achieve the desire value, then $V_{\rm LDO}$ keeps stable, as clean voltage supply with low noise and ripple, to drive the next stage sensor load. Fig. 23(b) shows the detailed waveforms in steady state, due to the active driving of the full bridge rectifier and hysteresis control of the buck–boost converter, $V_{\rm rec}$ has very high voltage conversion rate, $V_{\rm sup}$ has a very small ripple ($\sim$20 mV), while $V_{\rm LDO}$ is still clean, which shows high power supply rejection ratio performance of the designed LDO regulator.

Fig. 24 shows the measured transient response of the whole power management system. The measured response of the power management system with pulse trigger of the PZE transducer is shown in Fig. 24(a). A period pulse signal with less than 5 ms pulse width and 750 ms period time is employed to trigger the PZE transducer, then the transducer operates in its damped ring-down oscillations to generate ac electricity. In steady state, $V_{\rm sup}$ is regulated to the desired value with very small ripples, and $V_{\rm LDO}$ remains unchanged. In Fig. 24(b), the transient response of the power management system powered by linear frequency sweeping of the PZE transducer is measured. The sweeping frequency range is from 28 to 42 Hz. $V_{\rm rec}$ changes with the variation of PZE transducer, while $V_{\rm sup}$ and $V_{\rm LDO}$ remain unchanged.

Furthermore, to demonstrate a fully functional system toward wireless temperature sensor node applications, we have built and characterized the full senor node testing platform (Figs. 1 and 14) including the temperature sensor and the RF module. The on-chip temperature sensor consumes static power of 600 nW (caused by 200 nA quiescent current) and dynamic power of much lower than the static power, to provide a data rate of nearly 1 min per conversion of temperature data, with 0.5 °C resolution, in the 0 °C–75 °C temperature range. In the RF module, a CC2531 hardware and a custom-engineered ZigBee protocol are employed for the RF transmitter to optimize the power consumption. The period time of data exchange can be preset at a large scale. In this paper, nearly 15 min per data transmission has been set to send the on-chip temperature data.

The tested waveforms confirm the excellent performance of the ultralow quiescent current power management system for enabling the PZE transducer self-powered temperature sensor node. Finally, Table II summarizes the performance comparison of this work with previously published works. The merits of ultralow quiescent current, batteryless, and small die active area (including the on-chip sensor) with the high performance of the power management system demonstrate clear suitability and potential for a variety of emerging ULP IoT applications.

VI. CONCLUSION

In summary, a self-powering, batteryless, ultralow quiescent current, multiple-stage architecture power management ASIC system for vibrational energy harvesting and monolithically incorporating an on-chip physical sensor, has been presented. The merit of this design is that it consumes as low as 65.75 nA quiescent current to achieve the energy conversion, storage, transfer and regulation with MPPT to supply the on-chip sensor load. In addition, configurable impedance of the converter and simple periphery circuit of the system benefit from the large scale

integration design of the chip. All these have made it possible to apply this ASIC design to low-cost, maintenance-free, and miniature sensors for pervasive IoT sensor networks.

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