A Temperature-Dependent SPICE Model of SiC Power MOSFETs for Within and Out-of-SOA Simulations

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***Abstract*—This paper presents a temperature-dependent SPICE model for SiC power MOSFETs. The model describes the static and dynamic behavior and accounts for leakage current and impact ionization. The technology-dependent MOSFET parameters are extracted from characterization measurements and datasheets. SPICE standard components and analog behavior modeling blocks are adopted for the model implementation. The model ensures a good agreement with experimental data over a wide temperature range, even under out-of-safe-operating-area (SOA) conditions close to the failure occurrence.**

***Index Terms*—Avalanche, electrothermal (ET) simulation, short-circuit (SC), silicon carbide (SiC) power MOSFET, SPICE, unclamped inductive switching (UIS).**

I. Introduction

NOWADAYS, silicon carbide (SiC) power devices are expanding among several application areas, such as energy distribution, automotive, aircraft, and spacecraft by virtue of their excellent features. Since SiC devices often operate under harsh conditions, reliable simulations including electrothermal (ET) effects are highly needed for design optimization.

In the last years, several papers have focused on the modeling of SiC MOSFETs; a review of the models presented in literature is discussed in [1]. Many works start from models developed for Si MOSFETs and enrich them with various parameters and empirical functions to reproduce the characteristics of the SiC counterparts [2]–[7]. However, models based on an empirical formulation of the device behavior result in an onerous and prone-to-error calibration procedure. Recently, some models have been published with the aim to describe the specific mechanisms occurring in SiC MOSFETs. Effects caused by interface traps, their influence on the threshold voltage and the variation of the electron mobility are considered in [8]. In [8]–[10], the nonlinear drain resistance is also modeled. Various sophisticate physical models have been developed for device simulations [11]–[15], but in many cases they are too resource-hungry to be exploited for the analyses of complex circuits. A surface-potential-based model for circuit simulation is proposed in [16]. An analytical temperature-dependent model implemented in PSPICE that covers static and dynamic behavior, leakage current, and breakdown voltage characteristics is proposed in [17]. This model was shown to ensure a favorable matching of the R_{ON} at different temperatures, as well as of the low-current static avalanche *I–V* characteristic, but its accuracy in describing the pinch-off behavior and high-temperature out-of-safe-operating-area (SOA) conditions was not validated. In addition, like other physical models, it is based on many parameters that are unknown to the users, thus leading to a cumbersome and painstakingly onerous calibration procedure.

Although several models have been proposed in the last ten years, a validated SPICE model suitable for SiC power MOSFETs under extreme operating conditions, where very high temperatures are reached, is still missing in the literature.

In this paper, starting from a first attempt proposed in [18], an accurate, yet simple enough, physics-based model is conceived and developed, which is associated to a straightforward parameter extraction methodology. The proposed model is oriented to ET simulation in real applications (e.g., power converters) with the possibility to enable physical phenomena occurring close to the device failure. The model extends the version in [18] by including:

1) improved formulations for the nonlinear bias-dependent components of the drain resistance and for threshold voltage;
2) the thermally generated leakage current;
3) the parasitic npn transistor;
4) the nonlinear C_{ds} and C_{GD} capacitances;
5) the mobility degradation dictated by high electric fields.

The proposed model is suited to cover a wider temperature range, and is validated through comparison with static and dynamic experimental data even in out-of-SOA operations (avalanche and short-circuit (SC) conditions).

The model is implemented as a subcircuit fully compatible with most commercial SPICE-like software suites and can be solved by their powerful engines with low computational effort. An equivalent electrical network is coupled to the circuit to account for the dynamic heat propagation. Consequently, it is

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easy to monitor the evolution of the MOSFET temperature, as well as of the temperature-sensitive parameters.

The remainder of this paper is articulated as follows: in Section II, details are given on the model equations; in Section III, the developed subcircuit is shown and explained; in Section IV, the calibration procedure for the proposed model is described; in Section V, the model is validated through comparison with experimental data measured under static and dynamic conditions; conclusions are then drawn in Section VI.

II. Model Equations

The proposed model is based on the partitioning of the device into an "intrinsic" conventional MOSFET, which describes the channel region, a bias-dependent resistance for the accumulation and JFET regions, and a constant resistance for the epitaxial lightly doped drift region (also referred to as epilayer in the following). All the physical quantities are temperature dependent; in the following we will denote as T and T_0 the temperature of the transistor (assumed uniform within the whole device) and the reference temperature (300 K), respectively.

The drain resistance is modeled with the series of two nonlinear resistors with the following expression:

$$R_D\left(V_{GS}, V_{\mathrm{drift}}, T\right) = R_{AJ}\left(V_{GS}, V_{\mathrm{drift}}, T\right) + R_{\mathrm{EPI}}\left(T\right) \quad (1)$$

where

$$R_{AJ}\left(V_{GS}, V_{\mathrm{drift}}, T\right) = \frac{V_{\mathrm{drift}}}{V_1 + V_{\mathrm{drift}}} \cdot \left[R_{AJ1}\left(T\right) + R_{AJ2}\left(T\right)\left(1 + \frac{V_{GS}}{V_2}\right)^{-\eta}\right]. \quad (2)$$

The bias-insensitive R_{EPI} describes the resistive contribution of the epilayer, while R_{AJ} accounts for the current path through the accumulation and JFET regions [19]. $V_{\mathrm{drift}} = V_{DS} - V_{\mathrm{ch}}$ is the voltage drop across R_D, V_{ch} being the drop across the channel, while V_1, V_2, and η are fitting parameters. This formulation improves the one reported in [18] in the high-current triode region and is derived on the basis of simple arguments. First, the resistance of the accumulation region reduces with gate voltage due to the increased concentration of attracted electrons; second, under high V_{drift} values, the high electric field occurring in the JFET region tends to saturate the electron velocity, thus degrading the mobility.

The temperature dependences are modeled with the following expressions:

$$R_{\mathrm{EPI}}\left(T\right) = R_{\mathrm{EPI0}}\left(\frac{T}{T_0}\right)^{r_0} \quad (3)$$

$$R_{AJ1}\left(T\right) = R_{AJ10}\left(\frac{T}{T_0}\right)^{r_1} \quad (4)$$

$$R_{AJ2}\left(T\right) = R_{AJ20}\left(\frac{T}{T_0}\right)^{r_2}. \quad (5)$$

R_{EPI0}, R_{AJ10}, R_{AJ20}, r_0, r_1, and r_2 being fitting parameters. These dependences are found to ensure a good alignment between model and measurements up to about 500 K. To extend the model validity to higher temperatures with respect to [18], a slight modification of the above formulations is required, which can be explained as follows. As discussed in [20] and [21], the following expression can be used to describe the temperature dependence of the "bulk" electron mobility even for $T > 500$ K:

$$\mu_L\left(T\right) = \mu_{L0}\left(\frac{T}{300}\right)^{-r+\alpha T/300}. \quad (6)$$

Therefore, the exponents in (3)–(5) become

$$r_i\left(T\right) = r_i - \alpha_i \frac{T}{300}. \quad (7)$$

The threshold voltage (V_{TH}) in SiC MOSFETs exhibits a strong temperature dependence for low-temperature values that can be attributed to the very high density of states located at the SiO_2/SiC interface [22]. It has been reported that the interface states distribution within the bandgap increases exponentially toward the conduction band edge. As the temperature increases, less interface states are occupied [23], thus leading to more electrons in the depletion region. This effect could allow for stable operation at high temperatures where the I_D increase caused by the V_{TH} shift can be compensated by the reduced carrier mobility. The V_{TH} reduction with temperature was described with the classical linear law in [18], while in [24] a piecewise linear function was proposed. However, the latter approach suffers from a discontinuity that can lead to convergence issues in a SPICE implementation. We then propose the following exponential analytical expression:

$$V_{TH}\left(T\right) = \left[V_{TH}\left(T_0\right) - \beta_{TH}\right] e^{-\varphi_{TH}\left(T - T_0\right)} + \beta_{TH} \quad (8)$$

where the temperature coefficient φ_{TH} and the voltage β_{TH} are fitting parameters.

To model the temperature dependence of the electron channel mobility μ_n, many physical concurrent phenomena must be considered. For low-temperature values, μ_n exhibits a weak positive temperature coefficient (PTC), whereas a negative temperature coefficient (NTC) takes place at high temperature. This can be directly attributed to the presence of interface traps [25], [26]. The temperature coefficient of μ_n in a SiC power MOSFET is indeed the result of an interplay between 1) the Coulomb scattering with the filled traps, leading to a PTC induced by the trap discharging with increasing temperature; and 2) the acoustic-phonon scattering yielding an NTC, where 1 and 2 prevail at low and high temperatures, respectively. In the proposed model, such a behavior is accurately described through the power relationship shown in (9), where exponent *m* is temperature dependent

$$\mu_n\left(T\right) = \mu_n\left(T_0\right)\left(\frac{T}{T_0}\right)^{-m(T)}. \quad (9)$$

Parameter *m(T)*, usually considered positive and temperature independent for Si MOSFETs that are not subject to mechanism 1, is modeled with the following expression:

$$m\left(T\right) = -a_m + \left(a_m + b_m\right)\left[1 - c_m \exp\left(-d_m \frac{T}{T_0}\right)\right]. \quad (10)$$

with a_m, b_m, c_m, and d_m are fitting parameters.

Impact-ionization (II) effects are activated by multiplying the II-unaffected drain current by the avalanche factor [27]

$$M = 1 + a_{II} \tan\left[f_I\left(I_D\right)\frac{\pi}{2}\left(\frac{V_{DS}}{BV_{DS}\left(T\right)}\right)^{b_{II}}\right]. \quad (11)$$

The breakdown voltage BV_{DS} and the f_I term are given by

$$\begin{aligned} BV_{DS}\left(T\right) &= BV_{DS0}\exp\left[c_{II}\left(T - T_0\right)\right] \\ f_I\left(I_D\right) &= 1 - b_{AV} I_D \end{aligned} \quad (12)$$

where f_I is a nondimensional term needed to account for the current dependence of *M*; a_{II}, b_{II}, and c_{II} are fitting parameters.

The thermally generated leakage current I_{Therm} is modeled with the current contribution associated to the drain-body junction, which is reverse biased. I_{Therm} can be then expressed with the following equation [28]:

$$I_{\text{Therm}} = \frac{qW_D n_i}{\tau_H} + qn_i^2 f\left(N_D, N_A\right). \quad (13)$$

In (13), it is possible to identify two terms: in the first (drift) term, W_D and τ_H are the depletion layer width and the carrier generation lifetime in the depletion region of the collector–base junction, respectively. In the second (diffusion) term, *f* describes an involved function defining the diffusion components of the electrons and holes based on acceptor N_A and donor N_D concentrations, on the carrier lifetime of holes τ_p and electrons τ_n, as well as on the diffusivity of holes D_p and electrons D_n. Moreover, for 4H-SiC, the intrinsic carrier concentration is given by [29]

$$n_i\left(T\right) = 1.7 \times 10^{16} T^{3/2} e^{\left(2.08\times 10^4/T\right)}. \quad (14)$$

Using (12) and (13), the following simplified equation is adopted in the proposed model:

$$I_{\text{Therm}} = A_{\text{Therm}} n_i(T)^{\alpha_{\text{Therm}}} \quad (15)$$

where A_{Therm} and α_{Therm} are fitting parameters.

The dynamic behavior of the MOSFET model is described with three parasitic capacitances, namely, C_{GS}, C_{GD}, and C_{DS}. As discussed in detail in [30], these capacitances have considerable impact on the transient characteristics during the switching process. However, it has been proved that the nonlinearity of C_{GS} plays a minor role, especially for positive gate voltage, so that it be reasonably considered constant [31]. Conversely, experiments show that there will be a significant deviation between simulation and actual device switching behavior if C_{DS} and C_{GD} are assumed constant. Differently from [18], where the embedded formulations were exploited, in the proposed model

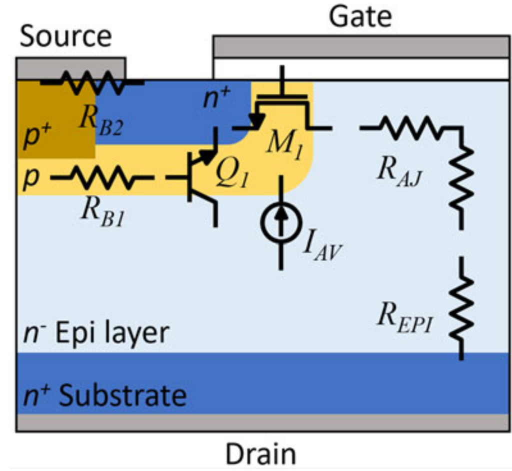


Fig. 1. Structure of the SiC power MOSFET and main equivalent circuit components.

these nonlinear capacitances are expressed as

$$C_{DS}\left(V_{ds}\right) = \frac{C_{DS0}\left[\frac{\pi}{2} + \arctan\left(-\frac{V_{ds}}{V_{ds}^*}\right)\right]}{\pi/2} + C_{DSMIN} \quad (16)$$

$$C_{GD}\left(V_{gd}\right) = \left(C_{GD0} - C_{GDMIN}\right)\left[1 + \frac{2}{\pi}\arctan\left(\frac{V_{gd}}{V_{gd}^*}\right)\right]. \quad (17)$$

The voltage-dependent behavior of C_{DS} was modeled with the function reported in (16) for $V_{ds} > 0\,\text{V}$, while it is kept constant for $V_{ds} < 0\,\text{V}$ [32]. Similarly, for $V_{gd} < 0\,\text{V}$ the C_{GD} capacitance asymptotically decreases down to a minimum value C_{GDMIN} according to (17), while for $V_{gd} \geq 0\,\text{V}$ it is equal to C_{GD0} [33]. Parameters V_{ds}^* and V_{gd}^* are used to fit experimental data for different switching voltages.

III. Subcircuit

The schematic structure of a basic SiC VDMOS is shown in Fig. 1. In this picture, the most relevant equivalent circuit elements are illustrated for the different device regions. A sketch of the implemented subcircuit is represented in Fig. 2. In addition to the electrical terminals (*drain*, *source*, and *gate*), the subcircuit receives as an input the device temperature *T*, evaluated by the equivalent thermal network, and the reference temperature T_0.

It is worth noting that the proposed implementation can in principle be applied to *any* power MOSFETs regardless of technology, provided that the equations and/or parameter values included through the additional components are properly modified. A behavioral voltage controlled voltage source, denoted as ΔV_{TH}, is connected in series with the intrinsic gate terminal to activate the temperature-induced V_{TH} reduction described by (8).

The controlling voltage is the difference between the nodal voltages representing *T* and T_0, while the outcome is the V_{TH}

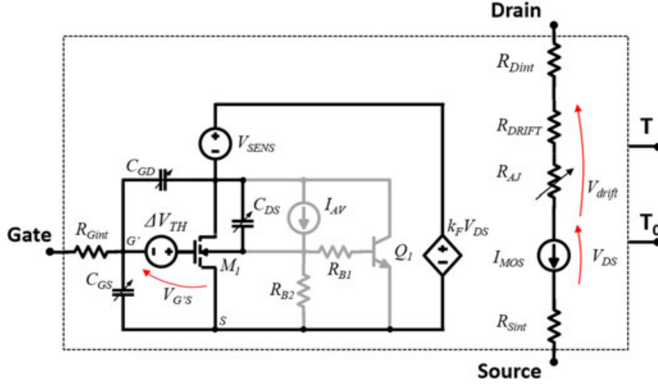


Fig. 2. Developed SPICE subcircuit, with electrical and thermal nodes. The elements in gray are needed to model the out-of-SOA operation.

variation given by

$$\Delta V_{TH} = (V_{TH0} - \beta_{TH})\, e^{-\varphi_{TH}(T-T_0)} - \beta_{TH} + V_{TH0}. \tag{18}$$

In this way, a proper voltage is added to the external gate voltage, leading to the desired temperature-dependent overdrive voltage given by

$$V_{G'S} - V_{TH0} = V_G + \Delta V_{TH} - V_S - V_{TH0} = V_{GS} - V_{TH}(T). \tag{19}$$

The total output MOSFET current I_{MOS} is evaluated starting from the current of the zero-voltage source V_{SENS} used as a current monitor. The term $I(V_{\mathrm{SENS}})$ includes the current of the MOSFET M_1, the currents through the capacitances, the thermally generated leakage current, the avalanche-induced current, and the current through Q_1. Then, the complete expression for I_{MOS}, valid for both linear and saturation regions, is given by

$$I_{\mathrm{MOS}} = \frac{I(V_{\mathrm{SENS}}) \cdot f_\mu(T)}{[1+\theta_1(V_{GS} - V_{TH}(T))](1+\theta_2 \cdot V_{DS})}(1+\lambda \cdot V_{DS}) \tag{20}$$

where f_μ being a function accounting for the temperature dependence of the electron mobility in the channel

$$f_\mu(T) = \left(\frac{T}{T_0}\right)^{-m(T)}. \tag{21}$$

Expression (20) of the MOSFET current includes the reduction in channel mobility due to the high transverse electric field dictated by high gate voltages through parameter θ_1. This results in a linear increase in the saturation current with $V_{GS} - V_{TH}$, instead of the classical quadratic function [33].

The bias-independent λ parameter accounts for the channel modulation effect. In order to include the impact of the nonuniform channel doping density on the current, two different current factor have to be adopted for the linear and saturation regions, respectively; to implement this effect into SPICE, a parameter K_F is multiplied by V_{DS}, as reported in [33]. The effect of the carriers velocity saturation at high V_{DS} (high parallel electric field) is modeled with parameter θ_2 [34].

Avalanche effects are included by adding a behavioral current source I_{AV} with the following expression:

$$I_{AV} = (M-1)\, I_{D(M_1)} + M \cdot I_{\mathrm{Therm}} \tag{22}$$

where $I_{D(M1)}$ is the II-unaffected drain current, M is given by (11), and I_{Therm} accounts for the thermally generated leakage current.

A network is also added to account for the parasitic *npn* BJT formed by the body, source, and drift regions, which represent the base, emitter, and collector, respectively. The potential difference between base and emitter depends on two resistors: R_{B1} and R_{B2}. The presence of the parasitic BJT improves the model in [18] and allows the modeling of a possible failure during out-of-SOA operation (as an example, during avalanche conditions, the BJT activation can be triggered if the I_{AV} current induces sufficient voltage across the device internal base resistance).

IV. Model Calibration Procedure

In this section, the procedure to calibrate the model parameters is described. The complete model with all the temperature dependences is based on 38 parameters, some of which have a physical meaning and can be directly extracted from measured data. However, depending on the application of the model and the required accuracy, a subset of parameters can be excluded (e.g., if the description of the parasitic *npn* BJT is not required, the related four parameters are unnecessary). In the following, we will refer to experimental data of the device under test (DUT) used in this paper, which is a 1.2 kV–36 A (at $T = T_0$) 4H-SiC power MOSFET, part number C2M0080120D, manufactured by Wolfspeed [35] and chosen as a case study. The MOSFET current factor *K* and threshold voltage V_{TH} were directly extracted from the highest-slope portion (medium V_{GS}) of the isothermal $I_D - V_{GS}$ transfer characteristics measured at various baseplate temperatures using the *quadratic extrapolation method* (QEM) [36], [37].

The parameters in (8) needed to model the temperature dependence of the threshold voltage can be evaluated from the best-fit procedure of the extracted values. Moreover, since the temperature dependence of factor *K* is only attributed to the electron mobility, the extracted *K* values were used to calibrate the parameters of exponent (10) employed in (21).

In Fig. 3, the extracted current factor *KP* normalized to the value at T_0 is shown as a function of temperature, along with the model with optimized parameters. Fig. 4 reports the threshold voltage against temperature. It can be inferred that the QEM technique leads to high values for $V_{TH}(T_0)$ (=5.05 V) and φ_{TH} (=4.12 mV/K) compared to similarly rated Si power MOSFETs. Both findings were attributed to the high density of SiO_2/SiC interface traps [38], [39]. The fast V_{TH} reduction with temperature—due to the emission of inversion electrons from the traps—entails a severe PTC for I_D, which in turn exacerbates the ET feedback [40]. Moreover, the $V_{TH}(T_0)$ value obtained with the QEM is rather higher than that reported on the device datasheet (=2.6 V), which is evaluated with the *constant current method* with $V_{GS} = V_{DS}$ at the reference $I_D = 5$ mA. However, in our approach, the main element is the standard Level 1 component M_1 (see Fig. 2) and the correct value to be used for the threshold voltage parameter [V_{TH0} in (18) and (19)] is the one obtained with the QEM. As an overwhelming evidence of the accuracy of the $V_{TH}(T)$

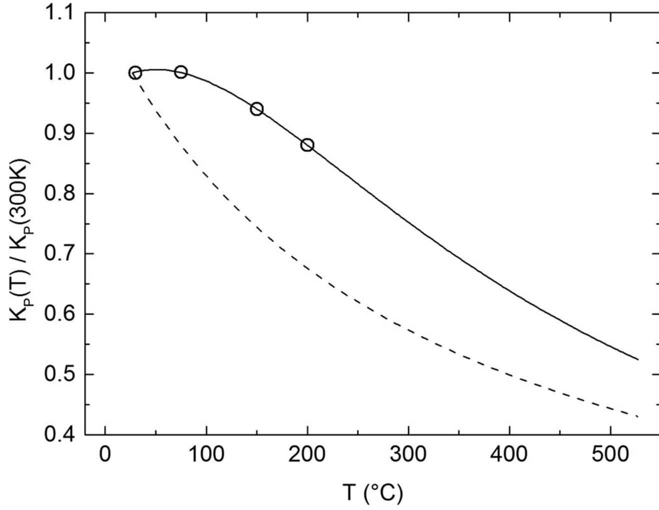


Fig. 3. Normalized MOSFET transconductance as a function of temperature. Circles are data extracted from isothermal $I_D - V_{GS}$ curves, the dashed line corresponds to a typical Si power law, while the continuous line is the new model fitted on experimental data.

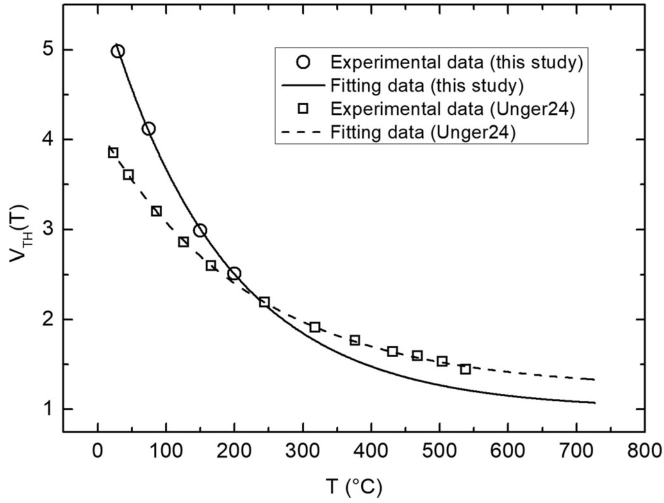


Fig. 4. Threshold voltage as a temperature function. Solid line and circles refer to the DUT analyzed in this paper. Dashed line and squares refer to the data extracted from [24].

expression at very high temperatures, Fig. 4 also reports the favorable alignment with experimental data from [24]. Parameter λ was extracted from an isothermal $I_D - V_{DS}$ curve at low V_{GS} (e.g., 7–8 V) in the pinch-off region ($V_{DS} >> V_{GS} - V_{TH}$). The nonlinear drain resistances (R_{AJ}, R_{EPI}) in (4) and (5), together with parameters θ_1 and K_F, were determined comparing the model with: 1) isothermal $I_D - V_{DS}$ output characteristics for different V_{GS}; and 2) the transfer characteristic at fixed $V_{DS} = 20$ V. More specifically, an automatic multistep calibration routine was implemented using the MATLAB Optimization Toolbox [42]. In the first step, the procedure evaluates six parameters minimizing the error between the simulated and measured $I_D - V_{GS}$ curve at ambient temperature: R_{EPI0}, R_{J10}, R_{J20}, V_2, θ_1, and η. Afterward, using the numerical and experimental output curves $I_D - V_{DS}$ at the reference temperature T_0, parameters K_F and V_1 are determined with the best-fit procedure.

TABLE I
CALIBRATED MODEL PARAMETERS

Symbol	Quantity	Value
*KP*0	Current factor	1.01 A/V^2
V_{TH0}	Zero-bias threshold voltage	5.05 V
Θ_1	Transverse electric field factor	0.01 V^{-1}
Θ_2	Parallel electric field factor	0.014 V^{-1}
λ	Channel-length modulation factor	0.046 V^{-1}
K_F	Nonuniform channel doping factor	0.846
R_{AJ10}	R_{AJ1} at reference temperature T_0	0.18 Ω
R_{AJ20}	R_{AJ2} at reference temperature T_0	0.57 Ω
R_{EPI0}	R_{EPI} at reference temperature T_0	7.7 mΩ
V_1	Drain resistance parameter	10.75 V
V_2	Drain resistance parameter	0.074 V
η	Drain resistance coefficient	1.88
BV_{DS0}	V_{ds} breakdown voltage at low current	1642 V
b_{II}	Multiplication factor coefficient	4 -
C_{GD0}	Zero-bias gate-to-drain capacitance	0.6 nF
C_{GDMIN}	Minimum gate-to-drain reverse-biased capacitance	0.01 nF
V_{gd}^*	Gate-to-drain capacitance parameter	2.0 V
C_{DS0}	Zero-bias drain-to-source capacitance	2 nF
C_{DSMIN}	Minimum gate-to-drain reverse-biased capacitance	0.06 nF
V_{ds}^*	Drain-to-source capacitance parameter	10 V
C_{GS}	Gate-to-source capacitance	1.05 nF
a_m	μ_n temperature parameter	1.12
b_m	μ_n temperature parameter	0.86
c_m	μ_n temperature parameter	1.34
d_m	μ_n temperature parameter	0.96
φ_{TH}	V_{TH} temperature coefficient	5.34 mK^{-1}
β_{TH}	V_{TH} temperature parameter	0.85 V
r_0	R_{EPI} temperature coefficient	5.02
r_1	R_{AJ1} temperature coefficient	4.34
r_2	R_{AJ2} temperature coefficient	0.34
c_{II}	BV temperature coefficient	0.22 mK^{-1}
b_{AV}	BV current coefficient	−0.1 mA^{-1}
A_{therm}	I_{therm} parameter	18 × 10^{-9}
α_{therm}	I_{therm} parameter	0.65
α_i	μ_n temperature coefficient	0.1

Finally, with the $I_D - V_{DS}$ at higher temperature (in our case $T = 470$ K) the automatic procedure determines parameters r_0, r_1 and r_2.

The parameters involved in the expression of the capacitances were tailored to match the experimental gate and drain voltage waveforms during an inductive load switching (ILS) turn-off and turn-on transient operated at different supply voltages. The starting guess values for the optimization procedure were extracted from the *C–V* curves reported on the DUT datasheet. The remaining parameters, used to model additional effects, were calibrated to favorably match experimental data during out-of-SOA operation. Parameter θ_2 is used to fit the drain peak current during SC operation (very high V_{DS}). In a similar fashion, the avalanche multiplication factor was tailored using the experimental waveforms obtained during an unclamped inductive switching (UIS) experiment. Furthermore, the parameters in (15) used to model the leakage current were calibrated using 2D-TCAD simulations up to very high temperature ($T = 2000$ K). The temperature coefficients in (7) can be optimized to ensure the best agreement with the current drain waveform during the SC test, when the temperature increase exceeds 500 K. All the model parameters corresponding to the DUT are reported in Table I.

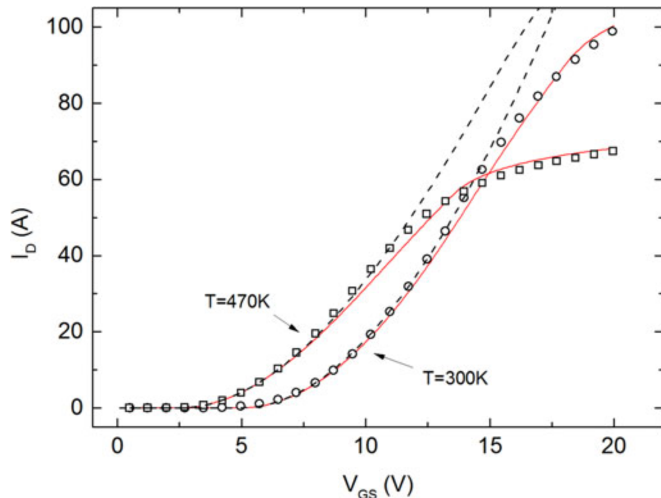


Fig. 5. Transfer characteristics under isothermal conditions, at $T = T_0 = 300$ K and $T = 470$ K. Solid lines are SPICE numerical results; symbols refer to the experiments on the DUT analyzed in this paper; dashed lines correspond to the curves obtained with the previous model version presented in [18].

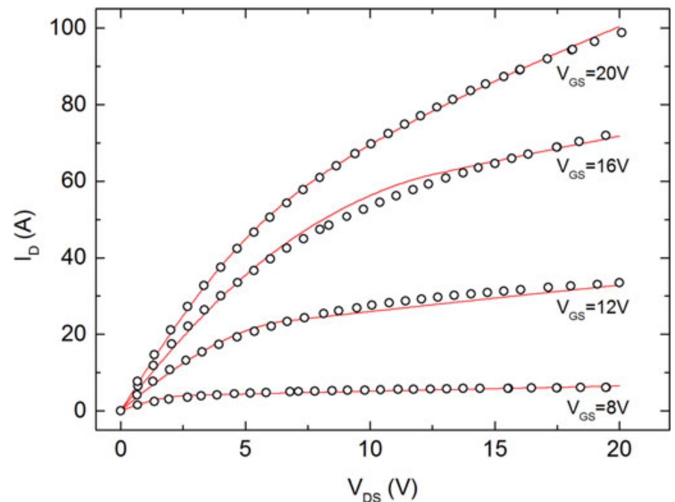


Fig. 6. MOSFET output characteristics at $T = T_0$. Solid lines are SPICE numerical results; symbols refer to the experiments on the DUT analyzed in this paper.

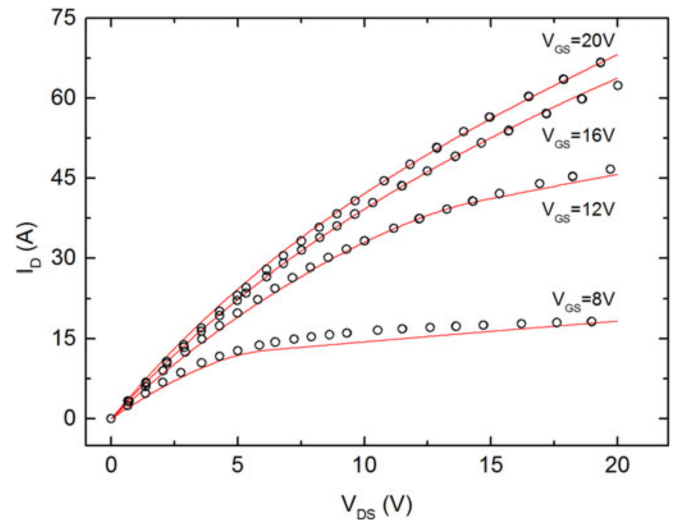


Fig. 7. MOSFET output characteristics at $T = 470$ K. Solid lines are SPICE numerical results; symbols refer to the experiments on the DUT analyzed in this paper.

V. Model Validation

The proposed model was validated comparing SPICE simulation results with experiments; in this section, we report a broad set of results with a focus on harsh working conditions where a large amount of energy is dissipated by the device causing high ET stress. All simulations were performed within the environment of the tool SIMetrix [41]; nonetheless, the model can be used in any SPICE simulator as a standard sub-circuit.

A. Static Validation

Isothermal measurements of *I–V* characteristics of the DUT were performed by means of an in-house 250-A-rated curve tracer suited to apply down to 1-μs-wide current pulses, the device baseplate being set to assigned temperatures *T* through the thermochuck. In Fig. 5, the experimental $I_D - V_{GS}$ curves at $T = T_0$ and $T = 470$ K are compared with simulation results. $I_D - V_{GS}$ characteristics derived with the model version in [18] are also reported. The calibrated SPICE model can predict with a high accuracy the device behavior for a wide range of V_{GS}, including the transition of the drain current from the standard quadratic region to a sublinear region. It is worth noting that the improved description of the drain resistance with respect to [18] allows extending the validity range of the model also in the high-current triode region. Figs. 6 and 7 depict the output curve family at $T = T_0$ and $T = 470$ K, respectively. In addition, in this case, it is evident how the model can describe with a high accuracy the device behavior, including the gradual transition from linear to saturation region, typical of SiC power MOSFETs.

B. Dynamic Validation

To investigate the device switching behavior, a half-bridge converter board has been used as test circuit (see Fig. 8) configured to operate as a standard ILS test [43].

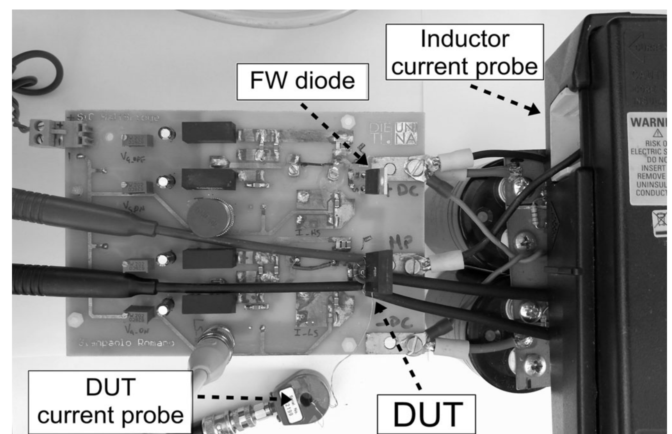


Fig. 8. Circuit used to evaluate the DUT switching waveforms.

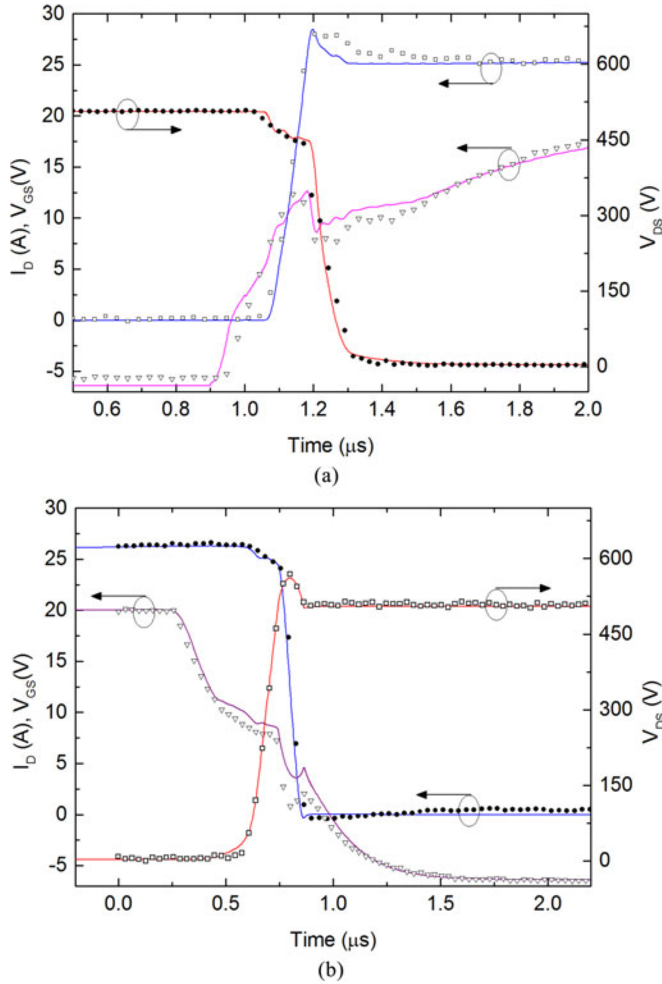


Fig. 9. Inductive switching waveforms (I_D, V_{DS}, V_{GS}): (a) turn on and (b) turn off. Solid lines are SPICE numerical results; symbols refer to the experiment.

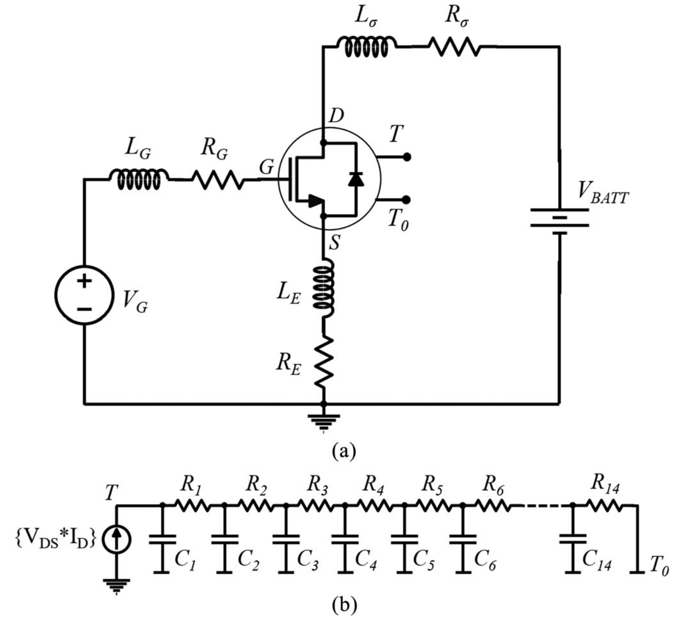


Fig. 10. SPICE equivalent schematics of SC test setup: (a) electrical network and (b) thermal network.

The DUT was placed as low-side switch of the half bridge, while the high side was replaced by an inductive load of 1.9 mH with a 1.2 kV SiC Schottky diode connected in parallel (free-wheeling diode).

An Agilent waveform generator (33220A) provided the logic signal for the DUT driver (IXYS IXDD609SI). The driving circuit (optically isolated) was designed to supply adjustable ON-state and OFF-state voltages, set to +20 V and –6 V for this experiment. A current transformer was used to measure the drain current. The turn-on and turn-off dynamics of the SiC MOSFET were obtained with double-pulse tests.

In the simulated circuit, the parasitic inductances of the device packages and the connections between the circuit components, as well as the parasitic capacitance of the inductive load, are taken into account. The gate drive is represented with a pulsed voltage source and a gate resistor. For the Schottky diode, a model provided by Wolfspeed was used [44]. Fig. 9 shows the waveforms of gate-source voltage, drain–source voltage, and drain current, which are obtained by measurements and by simulations of turn-on and turn-off of the SiC-MOSFET during a double-pulse test operated at a drain current of 26 A and T_0.

The main test parameters are as follows: supply voltage of 500 V, drain stray inductance equal to 200 nH, bipolar gate driver –6 V/+20 V [45], rise-time and fall-time of the driving gate signal of 100 ns, first pulse duration of 99 μs (conduction time before turn-off transient), second pulse after 20 μs (off-state before turn-on transient). Good agreement between simulation and measurements is achieved: the model fairly well predicts the drain voltage overshoot (∼580 V), and the drain current and voltage slopes.

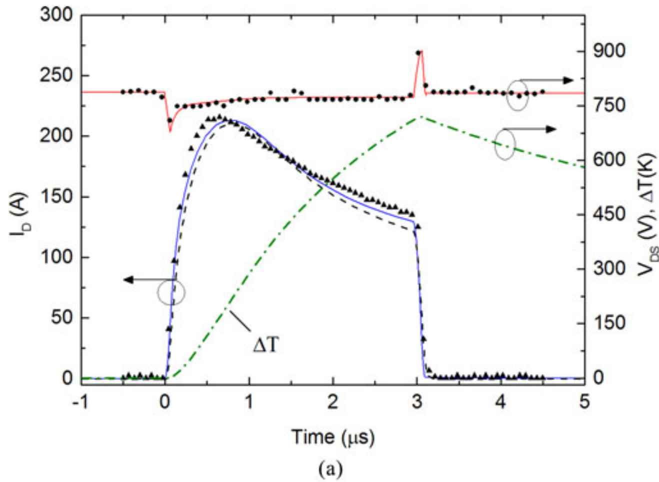
C. Out-of-SOA Validation

The proposed model is suited to describe the device behavior even under harsh working conditions, when the high dissipated power within the device causes a critical and potentially harmful temperature increase. In this section, the model validation during out-of-SOA conditions is presented for SC and UIS tests. In both cases, the operating limits are dictated by the temperature value. In the SC test, the transistor is turned on when a load SC already exists, i.e., the full dc-link voltage is applied. The *di/dt* of the drain current is determined by the driver parameters (driver voltage, gate resistor) and the transfer characteristic of the device. The schematic of circuit used for ET simulations is depicted in Fig. 10. A Cauer equivalent thermal network [see Fig. 10(b)] provided by the device manufacturer on the datasheet was used to evaluate the transient temperature evolution. The values of *RC* elements of the thermal network are reported in Table II.

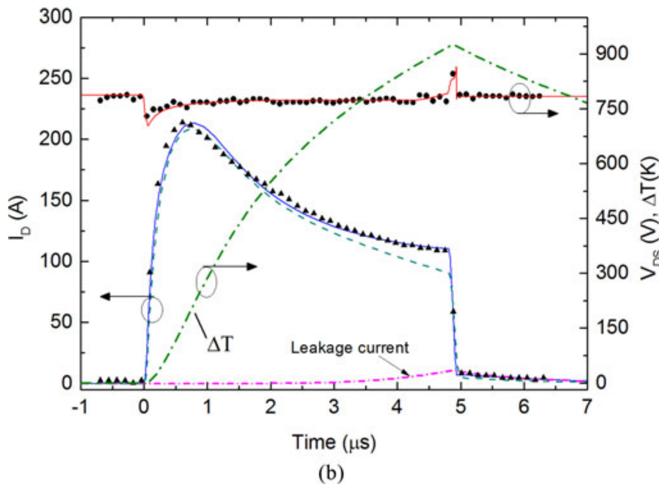
The description of the circuit used to perform the SC tests is reported in [46]. An HVdc power supply applies the voltage on the DUT, which is held by a 2.2-mF capacitors bank. A field-programmable gate array-based digital circuit provides a single pulse of the desired duration to the driving circuit. The test conditions are as follows: $V_{GS} = 0/18$ V, $R_G = 15\,\Omega$,

TABLE II
THERMAL NETWORK PARAMETERS

Node	1	2	3	4	5	6	7	8	9	10	11	12	13	14
$R_i\,(\mathrm{mK/W})$	13.3	13.3	37.8	36.9	83.6	58.4	43.2	51.2	51.9	47.5	46.6	58.7	40.8	10.4
$C_i\,(\mathrm{J/K})$	0.424 m	0.341 m	1.32 m	1.58 m	1.88 m	2.64 m	8.5 m	14.2 m	26 m	47.8 m	0.102	0.165	0.282	2.41



(a)



(b)

Fig. 11. SC electrical waveforms (I_D, V_{DS}) and temperature increase (ΔT) for both (a) 3 μs and (b) 5 μs pulse length cases. Solid lines are SPICE numerical results; symbols refer to the experiments on the DUT analyzed in this paper. The graph (b) also reports the leakage current.

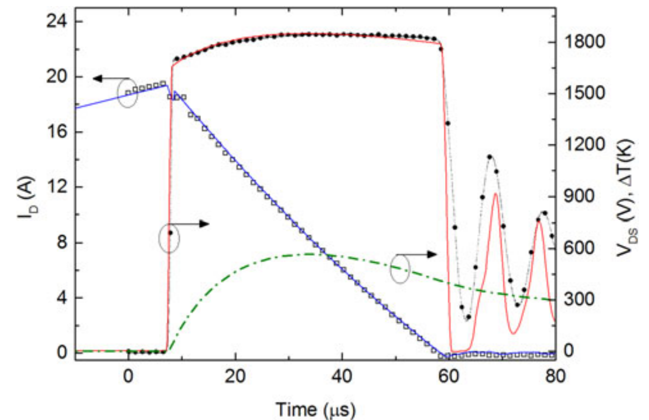


Fig. 12. UIS waveforms (I_D, V_{DS}) and temperature increase (ΔT). Solid lines are SPICE numerical results; symbols refer to the experiments on the DUT analyzed in this paper.

$V_{BATT} = 758$ V. Fig. 11 reports the comparison between experimental waveforms of DUT drain current and drain-to-source voltage during two SC pulses with duration of 3 and 5 μs, respectively. The device temperature increase ΔT, evaluated by the thermal network during the simulation run, is reported against the conduction time. Besides favoring the physical interpretation of the SC behavior, widely addressed in literature [47]–[52], the model correctly describes the effect of an extremely high temperature increase on the device current, as confirmed by the good agreement between experiments and simulations. In Fig. 11(b), the drain current evaluated with the temperature dependence of [18] is also reported for comparison purposes; for temperature exceeding 450 K, it is evident how the new model predicts with higher accuracy the ET device behavior. In addition, as stated in [51], the SC failure mechanisms of SiC MOSFETs can be driven by thermal runaway induced by temperature-generated current or high-temperature-related gate oxide damage. Fig. 11(b) shows the effect of the leakage when the device temperature approaches 1000 K, with the presence of a current tail in the drain current, correctly predicted by the ET simulation. This extremely high temperature value was first estimated by Huang in [53], and confirmed by finite-element ET simulations in [50]–[52]. In these papers, it is also demonstrated by means of simulations and experiments that the state-of-art SiC power MOSFETs cannot sustain a standard 10 μs SC pulse (with $\mathrm{V_{BATT}} = 2/3 \times \mathrm{V_{DSMAX}}$), with a reduced ruggedness under SC conditions if compared with similarly rated silicon devices.

The last validation was performed with an UIS test [54]. Under this working condition, the proper modeling of the avalanche multiplication factor *M* is of paramount importance. The schematic of the circuit adopted for the ET simulation is the same as in Fig. 10, where an inductance L_{load} is used instead of parasitic inductance L_σ. In the test circuit described in [55], a 3.3 kV IGBT was used as parallel switch to charge the load inductor, kept in ON-state for a time long enough to reach the desired $I_{\max}$. Moreover, the test circuit is also equipped with a series switch used to disconnect the power supply so as to prevent the DUT destruction in case of failure.

The test conditions are as follows: $V_{GS} = 0/18$ V, $R_G = 15\,\Omega$, $V_{BATT} = 400$ V, and $L_{\mathrm{load}} = 4.6$ mH. In Fig. 12, the comparison between experimental and numerical waveforms during an UIS test at $I_{\max} = 20$ A is shown. It is found that the device is plagued by a temperature reaching about 600 K above

T_0 during the avalanche time; nevertheless, also in this case, the model correctly describes the measured current and voltage.

VI. Conclusion

In this work, a temperature-dependent model for SiC power MOSFETs has been presented, which can be exploited for dynamic ET simulations within a broad range of voltages, currents, and temperatures, including out-of-SOA conditions. The model is based on a mathematically simple formulation associated with a straightforward parameter extraction procedure, and can be implemented with a SPICE-compatible subcircuit including a standard MOSFET and additional resistors, controlled capacitors, and controlled nonlinear sources to account for specific physical mechanisms and temperature dependences. The influence of SiO_2/SiC interface traps on threshold voltage and channel mobility, the dependence on biasing of the drain resistance, impact ionization, and capacitance nonlinearity are accounted for. The model has been adopted to analyze the behavior of a 4H-SiC power MOSFET rated 1200 V–36 A. Excellent agreement has been obtained with the experimental transfer and output *I–V* characteristics, despite the smooth triode-saturation transition occurring in SiC transistors. Both the turn-on and turn-off current and voltage evolutions have been fairly well predicted, including the drain voltage overshoot in the latter. Moreover, the calibrated model has been found to ensure a good alignment with the measured waveforms under harsh out-of-SOA conditions dictated by SC and UIS tests, where the temperature can reach several hundreds of Kelvin degrees. As a result, the model can be suggested to support the thermal-aware design of SiC power MOSFETs.

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