A Modular-Designed Three-Phase High-Efficiency High-Power-Density EV Battery Charger Using Dual/Triple-Phase-Shift Control

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***Abstract*—In this paper, an enhancement-mode GaN high-electron mobility transistor (HEMT)-based 7.2-kW single-phase charger was built. Connecting three such single-phase modules to the three-phase grid, respectively, generates a three-phase ∼22-kW charger with the $>97\%$ efficiency and $>3.3-\mathrm{kW/L}$ power density, superior to present Si-device-based chargers. In addition to GaN HEMTs with fast-switching transitions yielding high efficiency, the proposed charger employs the dc/dc stage to control the power factor and power delivery simultaneously, yielding little dc-bus capacitance and thereby high power density. To secure the soft switching for all switches within full voltage and power ranges, a variable switching frequency control with dual phase shifts was adopted at high power, and a triple phase shift was employed to improve the power factor at low power. Both control strategies accommodated the wide input range (80–260 VAC) and output range (200–450 VDC). A closed-loop control for the three-phase charger was realized to minimize the output current ripple and balance the power among three single-phase modules. Experimental results validated this design.**

***Index Terms*—Battery charger, dual active bridge (DAB), electric vehicle (EV), wide-bandgap (WBG) semiconductor, zero-voltage switching (ZVS).**

I. Introduction

THERE is a growing interest in high-power-density and high-efficiency battery chargers for electric vehicles (EVs) [1], [2], most of which adopt a three-stage design [3], [4], [5], i.e., an ac/dc stage to convert the grid voltage to a dc voltage and realize the power factor correction (PFC), a dc/ac stage to transform the dc to the high-frequency ac (hundreds of kilohertz) on the primary side of the transformer, and an ac/dc stage to rectify the induced high-frequency ac to dc voltage to charge the battery. Shown in Fig. 1(a) is a typical single-phase charger using resonance technology. The grid-side ac/dc employs the totem-pole boost-type PFC circuit. L_r and C_r form a resonance circuit to realize the zero-voltage switching (ZVS) [6]. Shown in Fig. 1(b) is a three-phase charger using the full-bridge LLC resonance [7]. When MOSFETs are used, all switches have body diodes.

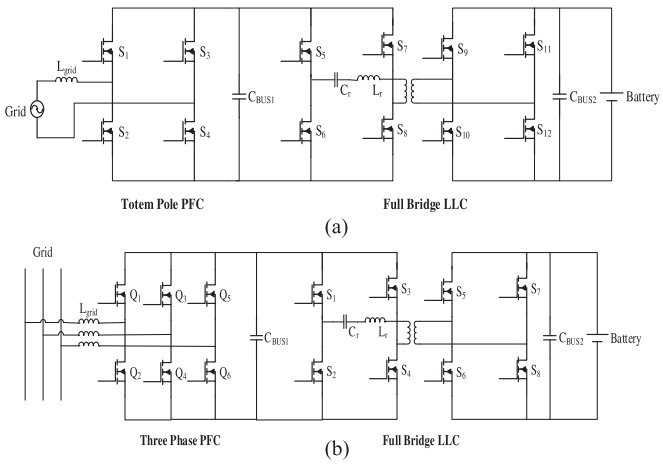

Fig. 1. (a) Conventional single-phase isolated charger. (b) Conventional three-phase isolated charger.

All chargers above need bulky dc-bus capacitors and have relatively high power loss. Assume each stage (ac/dc, high-frequency dc/ac, transformer, and ac/dc) has 1–2% power loss. This yields ∼94% efficiency and ∼2-kW/L power density, such as a Brusa 22-kW charger (NLG664) based on Si devices. To further enhance the performance, various isolated ac/dc converters were investigated in previous publications [8]–[10]. In [8], a single-phase bidirectional isolated ZVS ac–dc converter was proposed, as shown in Fig. 2(a). Such a topology reduces the stage number and eliminates the massive dc-bus capacitor. By using back-to-back switches, the transformer's primary voltage follows the envelope of the grid voltage. It needs to vary the phase shift and switching frequency to secure the power delivery and the power factor simultaneously. To avoid back-to-back switches, a circuit in [11] and [12] is a better candidate. As shown in Fig. 2(b), the front-end rectifier stage ($R_1 - R_4$, where *R* stands for "rectifier") is operated at the line frequency,

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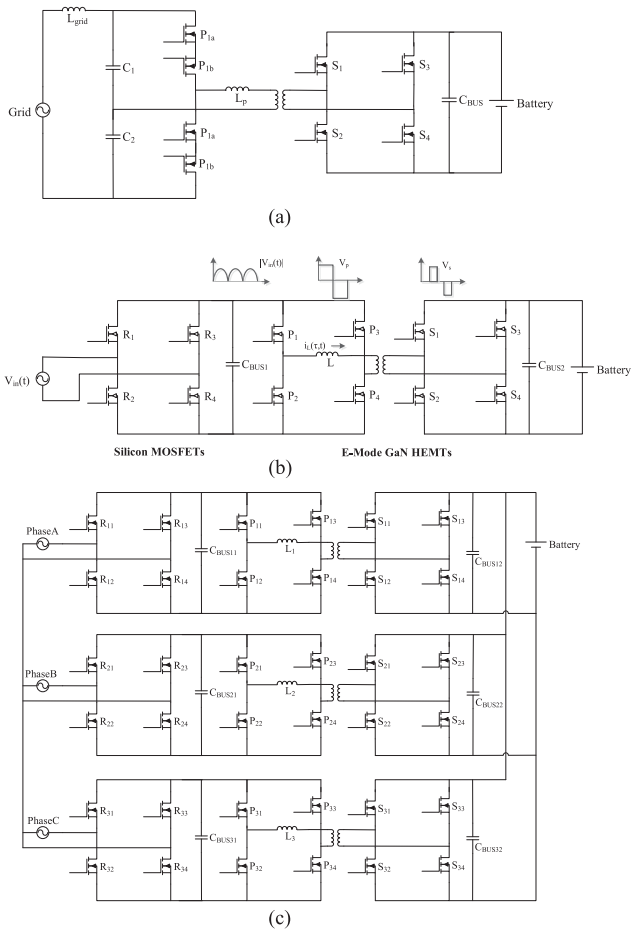


Fig. 2. (a) Single-phase single-stage bidirectional isolated ZVS ac–dc converter [8]. (b) Single-phase charging module adopted in this paper [11], [12]. (c) Proposed three-phase charger using a modular design.

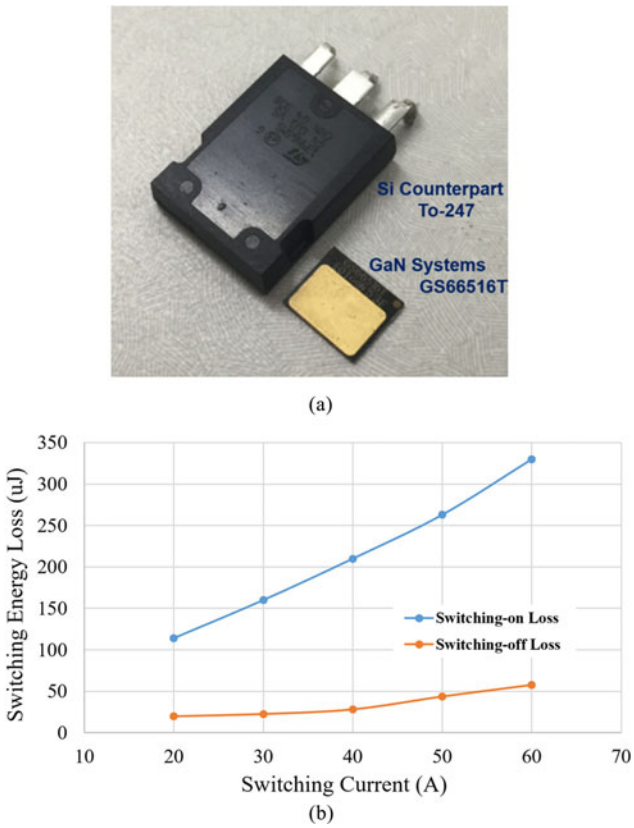


Fig. 3. (a) Leadless top-cooled package of GaN HEMTs (GS66516T). (b) Switching energy of GS66516T.

simply converting the sinusoidal waveform to a double-line-frequency dc voltage. Therefore, for the grid-side H-bridge, using a conventional Si MOSFET is sufficient. It meanwhile saves back-to-back switches, eliminates the switching loss, and shrinks the dc-bus capacitance to $\sim\mu$F levels, given there is no need to keep the dc-bus voltage constant. The dual-active-bridge (DAB) stage needs to realize both PFC and battery charging. To build a three-phase charger, e.g., 380 VAC/20 kW for European and Asian markets, three such single-phase modules could be connected, as shown in Fig. 2(c). The overall charger follows the exact power density and efficiency of each single-phase charging module and offers high fault tolerance, i.e., providing the power even when two phases fail.

For the DAB stage $(P_1 - P_4, S_1 - S_4)$, wide-bandgap (WBG) devices such as GaN HEMTs and SiC MOSFETs are excellent candidates to enhance the efficiency and power density, due to their ultrafast switching transitions and ultralow gate-drive power [13]. Some attempts have been carried out for EV chargers using GaN for high-switching-frequency applications [14], [15], [16], showing superior efficiency or power density. Different from the previous literature mostly using cascode GaN devices, this paper adopts enhancement-mode (E-mode) GaN HEMTs, GS66516T from GaN Systems Inc., as shown in Fig. 3(a). Its no-lead and top-cooled package significantly facilitates the parasitics reduction. Compared to Si and other GaN counterparts, its much smaller size makes it more appealing. Along with the topology shown in Fig. 2(b) and (c), we expect a high-efficiency and high-power-density EV onboard charger.

It is also possible to use SiC devices [17], [18], which represent another type of the WBG device. Whatever devices are preferred, the following issues need to be resolved: 1) ZVS turn-on needs to be true within the full output-voltage range (200–450 VDC), given that both SiC and GaN have much higher switching-on losses than switching-off losses, as shown in Fig. 3(b); and 2) a systematic integration of the three single-phase charging modules needs to be carried out, not only at the package level but also at the control level, e.g., a *closed-loop* control to balance each phase power even when the grid voltage is imbalanced. Section II will discuss control algorithms for the single-phase charging module, to realize the ZVS for all battery voltage and power. Section III forms the three-phase charger with the current *closed-loop* control. In Section IV, the overall charger is prototyped to verify the proposed design. Section V presents the conclusion.

II. Control Algorithms of the Single-Phase Charging Module

Each single-phase module receives the 80–260-VAC single-phase input, charges a 200–450-VDC battery, and delivers the

TABLE I
DEFINITION OF SYMBOLS

Symbol	Definition
$i_L(\tau,t)$	Transformer current of the primary side
$V_{\rm in}(t)$	The instantaneous grid voltage
L	Leakage inductance of the transformer reflected to the primary side
n	Turn ratio of the transformer (primary side versus secondary side)
$V_{\rm out}$	Battery voltage
$f_s(t)$	Switching frequency of the DAB stage
$g(t)$	Phase shift defined in Fig. 4
$g\max(t)$	Upper limit of the phase shift
$g\min(t)$	Lower limit of the phase shift
$w(t)$	Phase shift defined in Fig. 4
$P(t)$	Output instantaneous power
$I\text{neg\_min}(t)$	The minimum switching-off current for ZVS

charging power up to 7.2 kW. Before the detailed discussion of control strategies, all symbols are given in Table I.

A. Secondary Dual Phase Shift (SDPS)

When the battery voltage is higher than the reflected peak voltage of the grid, i.e., $|V_{\rm in}(t)| < nV_{\rm out}$, adding one extra phase shift on the secondary side will secure ZVS for all switches, as shown in Fig. 4(a). With the large magnetization inductance of the transformer, the excitation current is ignored. The overall DAB waveform within one line period is shown in Fig. 4(b). Since such control adopts two phase shifts, with one of which between two legs of the secondary H-bridge, we call it the SDPS control.

The primary-side current of the transformer is

$$i_L(\tau,t)=\begin{cases}\frac{V_{\rm in}(t)+nV_{\rm out}}{L}\tau+i_L(\tau_0(t),t), & \tau_1(t)\le\tau\le\tau_2(t)\\ \frac{V_{\rm in}(t)}{L}(\tau-\tau_1(t))+i_L(\tau_1(t),t), & \tau_2(t)\le\tau\le\tau_3(t)\\ \frac{V_{\rm in}(t)-nV_{\rm out}}{L}(\tau-\tau_2(t))+i_L(\tau_2(t),t), & \tau_2(t)\le\tau\le\tau_3(t)\\ \frac{-V_{\rm in}(t)-nV_{\rm out}}{L}(\tau-\tau_3(t))+i_L(\tau_3(t),t), & \tau_3(t)\le\tau\le\tau_4(t)\\ \frac{-V_{\rm in}(t)}{L}(\tau-\tau_4(t))+i_L(\tau_4(t),t), & \tau_4(t)\le\tau\le\tau_5(t)\\ \frac{-V_{\rm in}(t)+nV_{\rm out}}{L}(\tau-\tau_5(t))+i_L(\tau_5(t),t), & \tau_5(t)\le\tau\le\tau_6(t).\end{cases}\tag{1}$$

Here

$$i_L(\tau_0,t)=-\frac{V_{\rm in}(t)+nV_{\rm out}}{2Lf_s(t)}g(t),$$

$$i_L(\tau_1,t)=\frac{V_{\rm in}(t)+nV_{\rm out}}{2Lf_s(t)}g(t)$$

$$i_L(\tau_2,t)=\frac{V_{\rm in}(t)(1-g(t)-2w(t))+nV_{\rm out}g(t)}{2Lf_s(t)},$$

$$i_L(\tau_3,t)=\frac{V_{\rm in}(t)+nV_{\rm out}}{2Lf_s(t)}g(t)$$

$$i_L(\tau_4,t)=-\frac{V_{\rm in}(t)+nV_{\rm out}}{2Lf_s(t)}g(t),$$

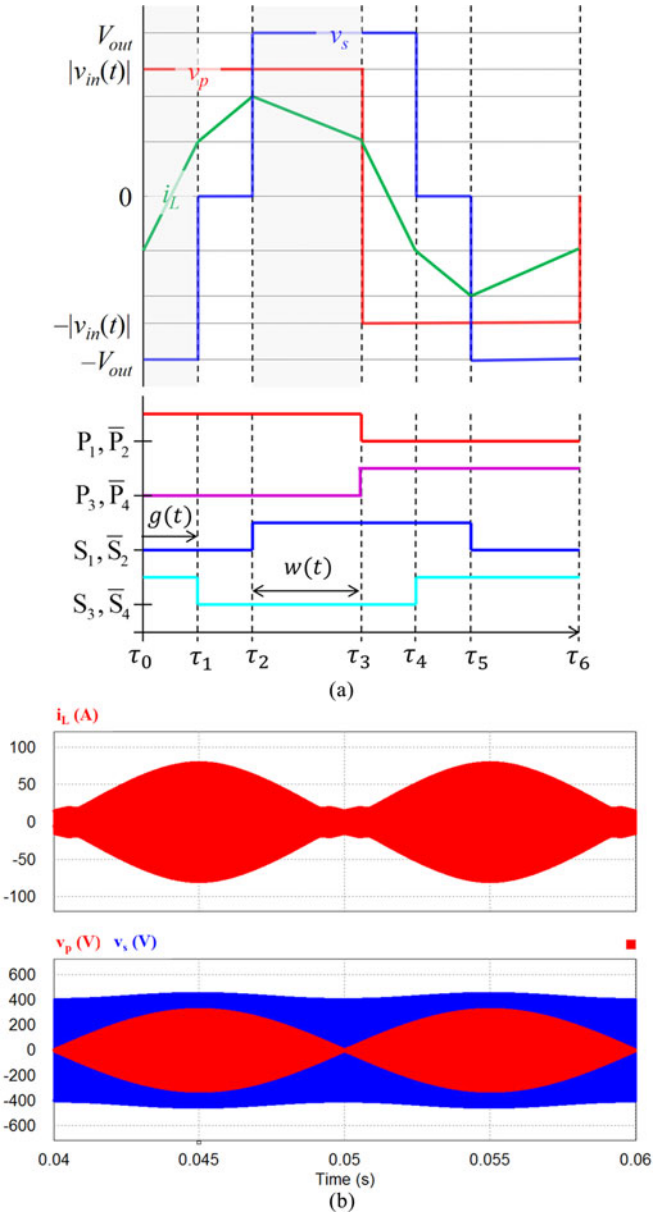


Fig. 4. (a) Output voltage of the DAB primary side and secondary side, current of the primary inductor, and gate signals of all switches (zoomed in at a randomly selected switching period). (b) Current of the primary inductor (top) and output voltage of the DAB primary side and secondary side (bottom) (within one line period).

$$i_L(\tau_5,t)=-\frac{V_{\rm in}(t)(1-g(t)-2w(t))+nV_{\rm out}g(t)}{2Lf_s(t)}.$$

To maintain $i_{L(\tau_1)}=i_{L(\tau_3)}$ and $i_{L(\tau_4)}=i_{L(\tau_6)}$, we need

$$w(t)=\frac{1-2g(t)}{2nV_{\rm out}}V_{\rm in}(t).\tag{2}$$

The average power during one switching period is

$$P(t)=2V_{\rm in}(t)\frac{(1-2w(t))V_{\rm in}(t)+2ng(t)V_{\rm out}}{4Lf_s(t)}(0.5-g(t)).\tag{3}$$

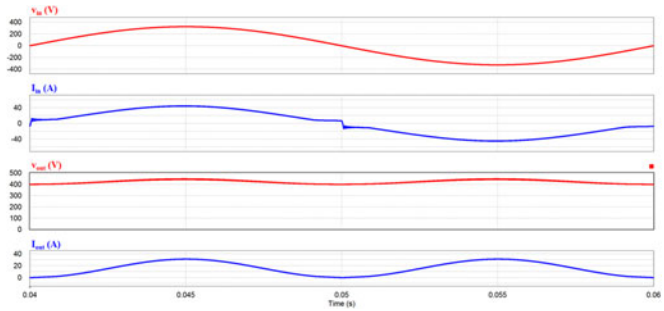


Fig. 5. Simulated input and output of a single-phase module using the SDPS control.

Substituting (2) into (3), we have

$$P(t)=\frac{V_{\text{in}}(t)}{2Lf_s(t)}\left\{\left(2nV_{\text{out}}+2\frac{V_{\text{in}}(t)^2}{nV_{\text{out}}}\right)g(t)^2+g(t)\left[nV_{\text{out}}+V_{\text{in}}(t)\left(\frac{V_{\text{in}}(t)}{nV_{\text{out}}}-1\right)+\frac{V_{\text{in}}(t)^2}{nV_{\text{out}}}\right]-0.5V_{\text{in}}(t)\left(\frac{V_{\text{in}}(t)}{nV_{\text{out}}}-1\right)\right\}. \quad (4)$$

Once $g(t)$ is selected, $w(t)$ will be determined by (2) and $f_s(t)$ will be determined by (4). Simulation results of the PFC function are shown in Fig. 5. Here, the grid voltage is 208 VAC, the battery voltage is 400 V, the charging average power is 7.2 kW, and the ceiling switching frequency is 500 kHz. It shows the output current of each single-phase charger contains the 120-Hz ripple. An extra active filter is necessary for a single-phase module [19], however, not necessary for the three-phase charger. This will be validated in Section IV, given such ripple will be neutralized by another two phases when running in the three-phase mode.

B. Primary Dual Phase Shift (PDPS)

When the battery voltage is low, i.e., $|V_{\text{in}}(t)|>nV_{\text{out}}$,. using the SDPS control will not result in the intended $i_{L(\tau_1)}=i_{L(\tau_3)}$ and $i_{L(\tau_4)}=i_{L(\tau_6)}$. This could further yield losing ZVS or increasing the current stress. Here, we propose adding an extra phase shift $v(t)$ on the primary-side voltage (PDPS for simplicity) and keeping the secondary voltage as square waveforms, as shown in Fig. 6

$$v(t)=\frac{|V_{\text{in}}(t)-V_{\text{out}}|}{|V_{\text{in}}(t)|}(0.5-g(t)) \quad (5)$$

and the switching frequency is

$$f_s(t)=\frac{V_{\text{out}}}{PLV_{\text{in}}(t)}\left[-V_{\text{out}}|V_{\text{in}}(t)|-\frac{V_{\text{out}}^3}{|V_{\text{in}}(t)|}\right)g(t)^2+\left(0.5V_{\text{out}}|V_{\text{in}}(t)|-0.5V_{\text{out}}^2+\frac{V_{\text{out}}^3}{|V_{\text{in}}(t)|}\right)g(t)+0.25V_{\text{out}}^2-\frac{0.25V_{\text{out}}^3}{|V_{\text{in}}(t)|}\Bigg]. \quad (6)$$

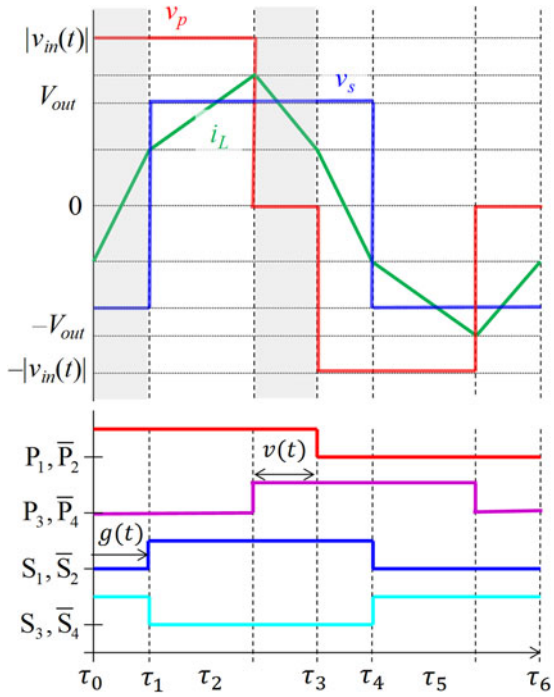


Fig. 6. Output voltage of the DAB primary side and secondary side and current of the primary side and gate signals.

After examining all switching points, it is validated that ZVS turn-on is still true for all switches. When $|V_{\text{in}}(t)|=nV_{\text{out}}, v(t)=0$, and $w(t)=0.5-g(t)$, the dual phase shift (DPS) evolves into the conventional single-phase-shift control.

C. Triple Phase Shift (TPS)

For A&B, it is obvious that the control has to switch between PDPS and SDPS frequently when the battery voltage is less than the peak value of the ac input voltage. Meanwhile, f_s and the phase shifts are tightly coupled and need to vary at all times. More importantly, (2)–(6) show that when the power is low, $f_s(t)$ must be quite high, which is usually not possible due to switching limitations. Setting an upper limit of f_s causes a lower limit on the power transfer, thereby distorting the grid current. In Fig. 5, when the grid voltage is close to zero, f_s is clamped to the ceiling frequency (500 kHz), resulting in the distorted input current. Such distortion becomes worse at light load, which cannot be resolved by either PDPS or SDPS.

To enhance the light-load performance by removing the grid-current distortion, a TPS algorithm is proposed here, which maintains ZVS down to the zero power. In such a control, rising edges of P_1 and S_3 in Fig. 2(b) maintain a phase shift of ϕ_r. Meanwhile, a second phase shift, ϕ_p, is placed between $P_1\&P_3$ and a third phase shift, ϕ_s, is placed between $P_1\&S_1$. This makes both the primary and secondary voltages of the transformer three-level waveforms. Both ϕ_r and ϕ_p work to regulate the near-zero switching current, I_r, which is responsible for maintaining ZVS during four of the eight switching-on cycles within a period. The switching waveforms and the transformer voltages and current are shown in Fig. 7.

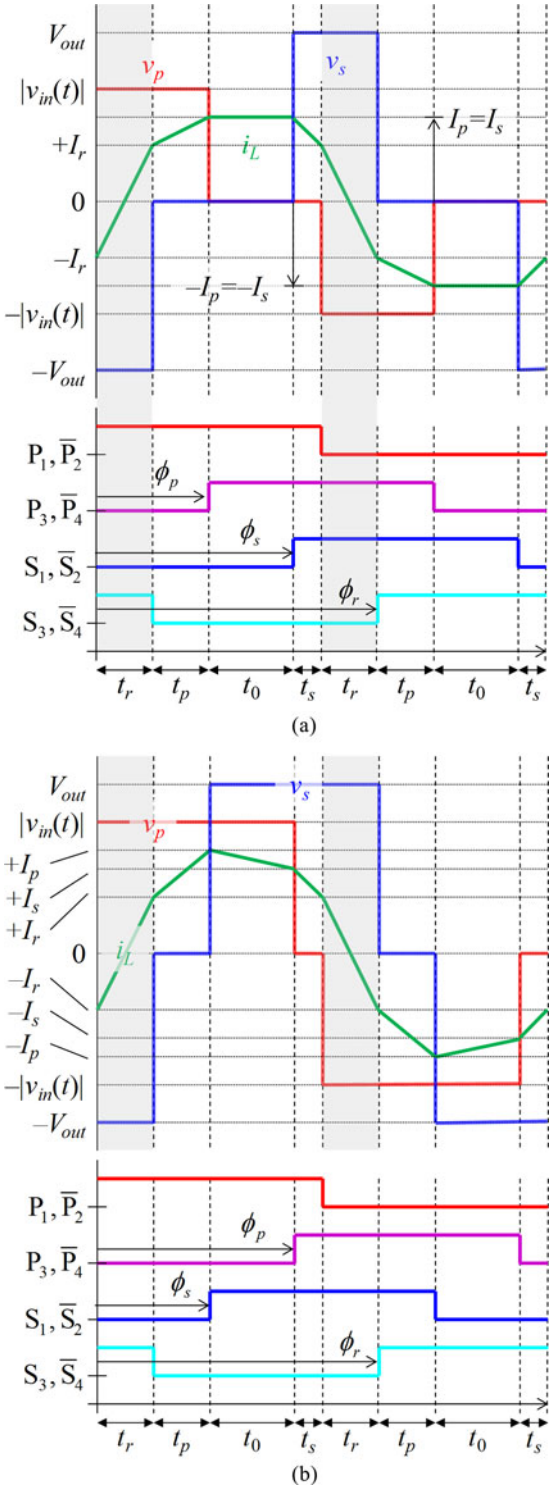


Fig. 7. (a). Voltage, current, and switching waveforms of TPS (nonoverlap). (b). Voltage and current waveforms of TPS (overlap).

The power is regulated by ϕ_p and ϕ_s. Note that since the three phase shifts are independent of each other, it is possible that $\phi_p < \phi_s$ or $\phi_p > \phi_s$; the former case is denoted as the "nonoverlap condition," as shown in Fig. 7(a), and the latter is denoted as the "overlap condition," as shown in Fig. 7(b). The variables t_p, t_s, t_r, t_0, and t_o are denoted as the primary-active,

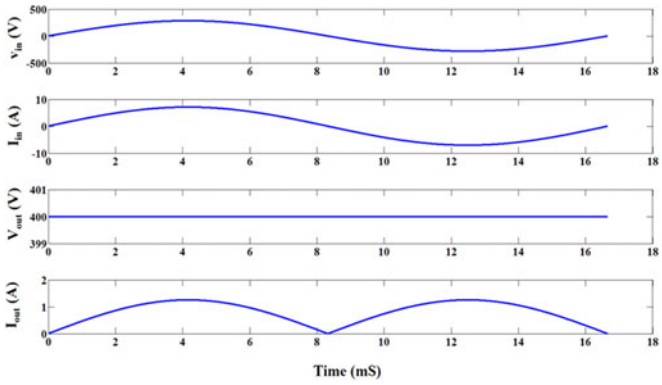


Fig. 8. TPS control within one line period at 200 W.

secondary-active, reactive, inactive, and overlap time intervals, where

$$\varphi_p = \begin{cases} (t_r + t_p)/T, & \text{nonoverlap} \\ (t_r + t_p + t_o)/T, & \text{overlap} \end{cases} \tag{7.1}$$

$$\varphi_s = \begin{cases} \left(\frac{T}{2} - t_s\right)/T, & \text{nonoverlap} \\ \left(\frac{T}{2} - t_s - t_o\right)/T, & \text{overlap} \end{cases} \tag{7.2}$$

$$\varphi_r = \left(\tfrac{T}{2} + t_r\right)/T \tag{7.3}$$

and the value T is the switching period. The value I_r is the magnitude of the current during the reactive power transfer interval when P_1, S_4, P_2, and S_3 turn ON. We can describe this value as

$$I_r = \frac{t_r\left(v_{\text{in}} + V_{\text{out}}\right)}{2L}. \tag{8}$$

To realize ZVS turn-on, the magnitude of I_r must be sufficient enough to completely discharge the drain–source capacitances of the upper and lower switching devices during dead time

$$I_r \geq \sqrt{2C_{\text{oss}}V^2/L_r} \tag{9}$$

where the voltage V could be the primary-side voltage or the secondary-side voltage, whichever side is larger. ZVS turn-on of the other four switching events (P_3, P_4, S_1, and S_2) is guaranteed, since the transformer current will be larger than I_r. C_{oss} is the equivalent output capacitance of each switching module, which in this paper is made of four paralleled switches.

The value I_p is the transformer current magnitude during the primary active-power-transfer interval when $v_p \neq 0$ and $v_s = 0$. Similarly, I_s is the current magnitude during the secondary active-power-transfer interval when $v_s \neq 0$ and $v_p = 0$, where

$$I_p = I_r + \frac{|v_{\text{in}}|\, t_p}{L} \tag{10.1}$$

$$I_s = I_r + \frac{V_{\text{out}} t_s}{L}. \tag{10.2}$$

To guarantee that the value of I_r remains constant at the P_1, S_4, P_2, and S_3 turn-on points (and that the i_L waveform is balanced), the two active-time intervals must be proportional to the primary and secondary side voltages, i.e.,

$$\frac{|v_{\text{in}}|}{V_{\text{out}}} = \frac{t_s}{t_p}. \tag{11}$$

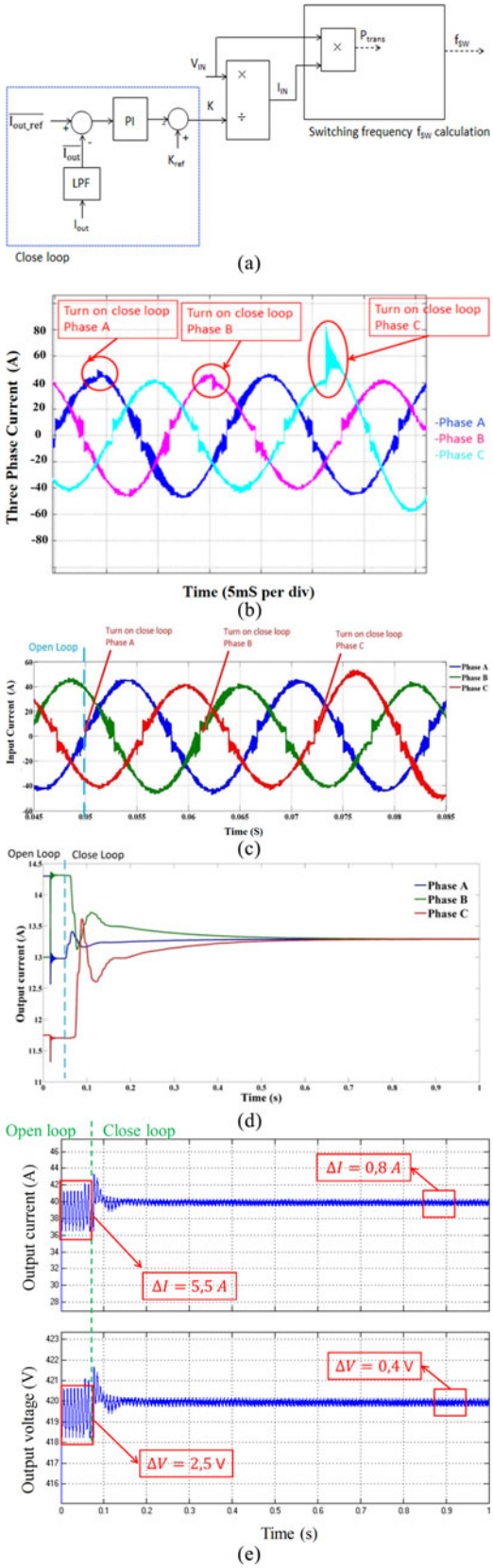


Fig. 9. (a) Proposed closed-loop control. (b) Switching from open loop to closed loop at the peak voltage. (c) Switching from open loop to closed loop at zero-crossing points. (d) Output current of each module before and after the closed-loop control. (e) Overall output current and voltage before and after the closed-loop control.

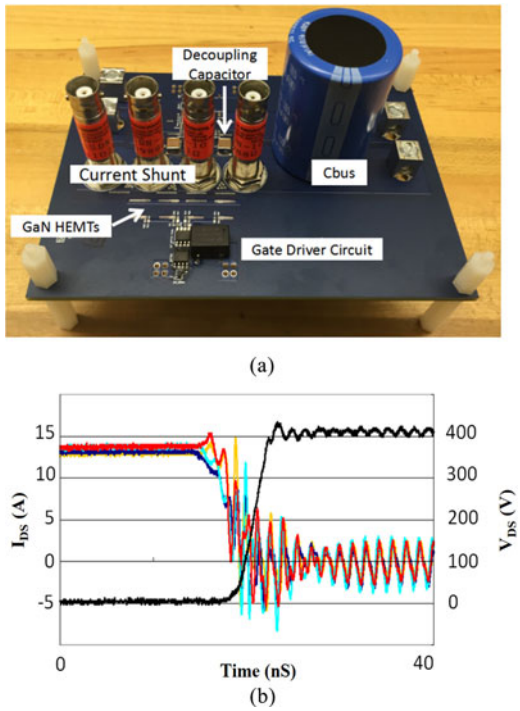


Fig. 10. (a) DPT with four GaN HEMTs in parallel. (b) Current sharing among paralleled HEMTs @ 400 V/56 A during the turn-off process.

The power transfer of the DAB operating under the TPS control in the nonoverlap case can be described as

$$p(t) = V_{\text{out}}(I_r + I_s)\, t_s f_s \tag{12}$$

which, after substituting (12) and rearranging, gives us

$$p(t) = (2V_{\text{out}} I_r f_s)\, t_s + \left(\frac{{V_{\text{out}}}^2 f_s}{L}\right) {t_s}^2. \tag{13}$$

In other words, by using TPS, the instantaneous power could be exactly zero once $t_s = 0$. The limitation of the switching frequency is gone. Another merit is, while the output power depends on I_r, f_s, and t_p or t_s, the value of I_r is independently controlled by only t_r, the voltage magnitudes, and leakage inductance, L. Thus, I_r could be set to a constant desired value, determined by the switching device's output capacitance and maximum voltage, while the power can be set by varying either f_s and/or the time intervals. Here, the ZVS condition is totally decoupled from the power delivery, unlike the DPS control shown in A&B. Thus, from a control standpoint, there is no need to vary f_s at the light load, which resolves the grid-current distortion problem of the VSF DPS control at light loads, as shown in Fig. 8.

However, the efficiency of the nonoverlap TPS will be low, since a majority of the transformer current is simply circulating during the t_0 period, leading to excessive conduction losses. For the high power transfer, the system still needs switch back to DPS.

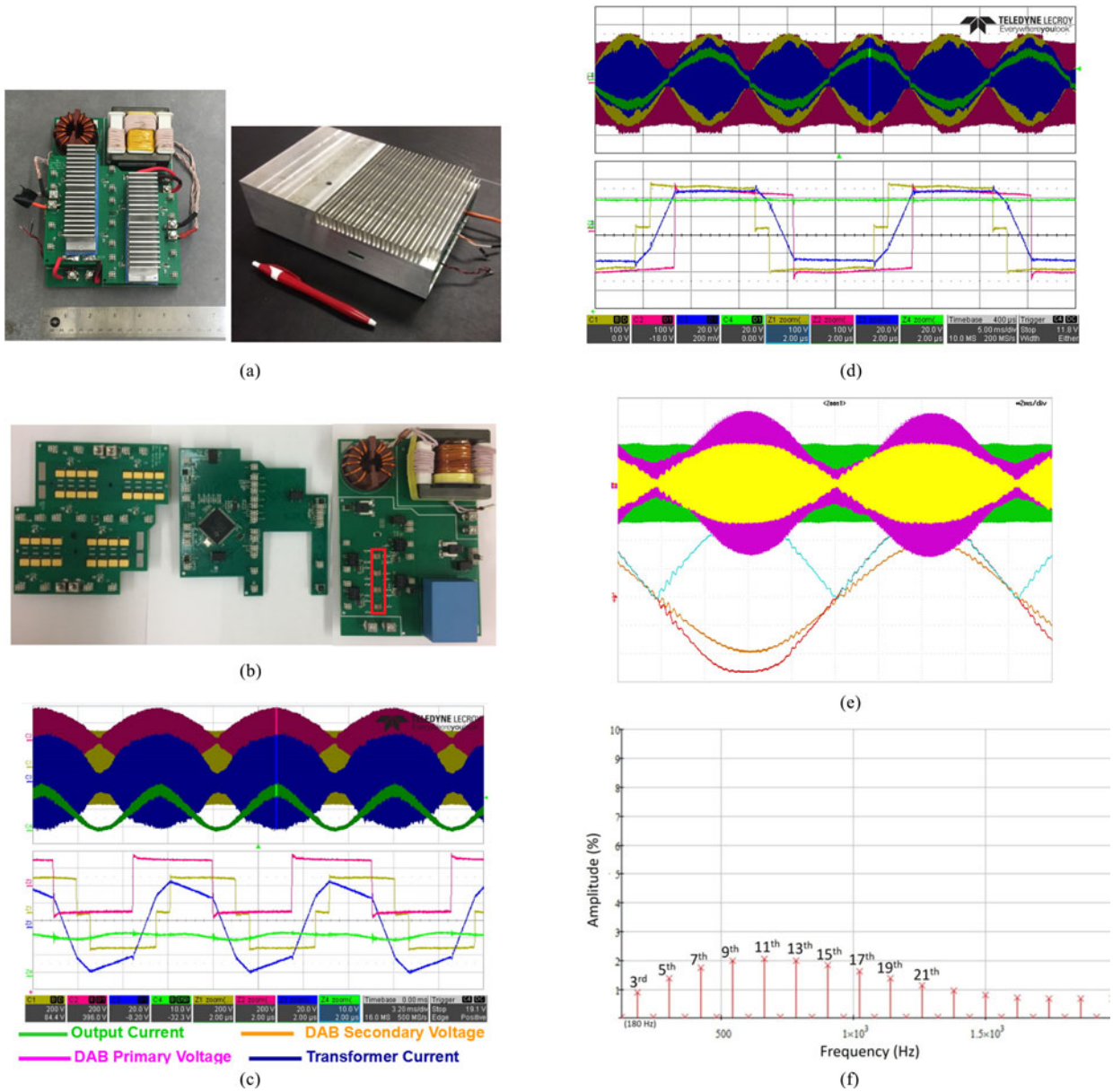
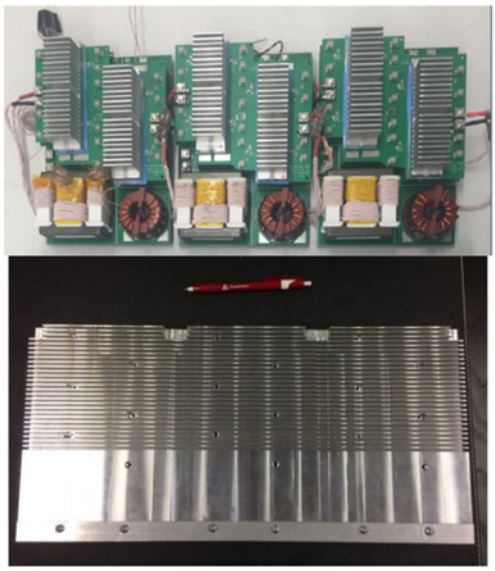


Fig. 11. (a) Prototype of the single-phase charger (left—the charger, right charger with the enclosure). (b) PCBs of the single-phase charger (from left to right: GaN HEMT PCB, control PCB, and rectifier PCB). (c) DAB waveform of the charger @ $V_{\rm o} = 400$ V, $P = 7.2$ kW. (d) DAB waveform of the charger @ $V_{\rm o} = 200$ V, $P = 4$ kW (yellow-DAB primary voltage, 100 V/div; purple-DAB secondary voltage, 100 V/div; blue-transformer current, 20 A/div; green-grid-side current, 20 A/div). (e) TPS control at 100 W (yellow-transformer primary voltage, 100 V/div; purple-transformer current, 1 A/div; green-transformer secondary voltage, 100 V/div; red-grid voltage 100 V/div; brown-grid current 1 A/div). (f) Grid-current-harmonics distribution (experiments).

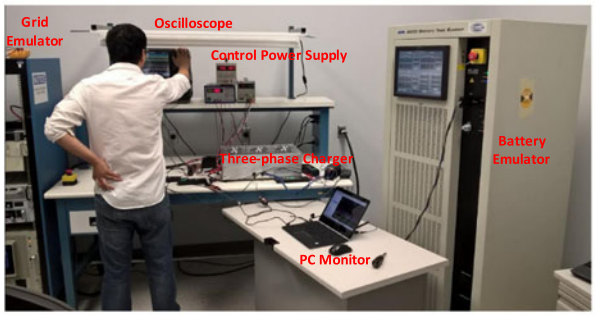
III. Forming the Three-Phase Charger

A closed-loop control for the output current is usually required for the battery charging, as shown in Fig. 9(a). Each charging module samples its output current and uses the average value to compare with the target current. To shorten the dynamic process, a $K_{\rm ref} = V_{\rm battery}/I_{\rm out\_ref}$ is assigned to form the feedforward control loop. The calculated power then will be used to determine the switching frequency. Here, $V_{\rm IN}$ is the instantaneous value of the grid voltage. Simulation results are shown in Fig. 9(b)–(e).

In Fig. 9(b), the control was switched from the open loop to closed loop at the peak voltage of the grid. Kicking PI and feedforward controller in will bring a sudden change of K, which results in a current overshoot. To avoid that, in Fig. 9(c), each phase closes the loop at voltage zero-crossing points, where $I_{\rm IN}$ and P are both zero. It sets a smooth transition from the open-loop to the closed-loop control. To test the effectiveness of the closed-loop control, we set Phase-C voltage 10% lower than Phases A and B, which under the open-loop control will bring the lower output power. The closed-loop control will generate the higher phase current to maintain the same power per phase, as shown in Fig. 9(b) and (c). Fig. 9(d) and (e) compares the open-loop control and closed-loop control, with a $\pm 5\%$ grid imbalance. It indicates that the proposed closed-loop control



(a)



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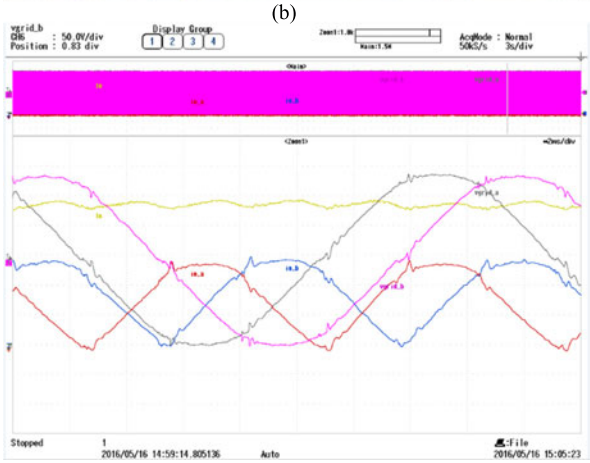

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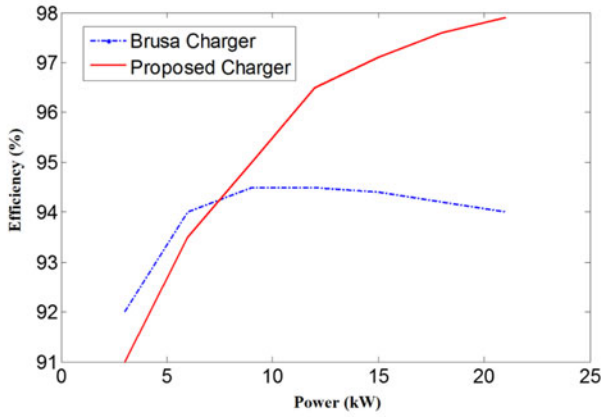

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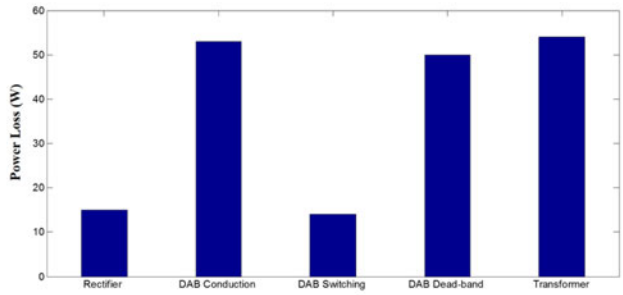

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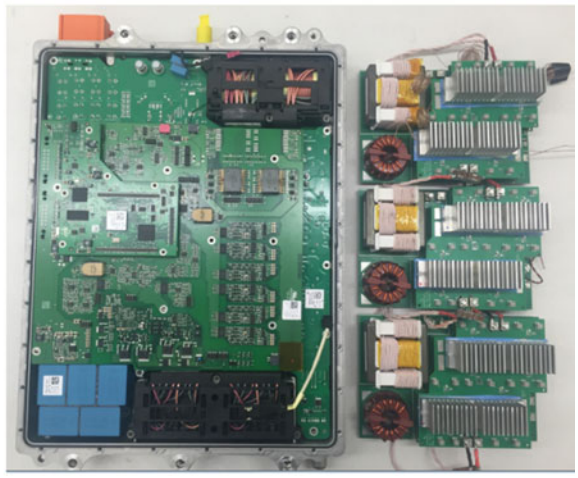

(f)

Fig. 12. (a) Three-phase charger using three single-phase modules (top) and its enclosure (bottom). (b) Test bench for the charger. (c) Three-phase-charger test result @5 kW (yellow-I_o: 3A/div; I_{oa}, I_{ob}, I_{oc}: 3 A/div; grey&purple-grid phase voltage $V_{\mathrm{grid\_a\&b}}$: 100 V/div). (d) Efficiency comparison (GaN versus Si). (e) Power loss breakdown (per phase). (f) Power density comparison (left—Si Charger of 2 kW/L, right—GaN charger of 3.3 kW/L).

not only balances the output power of each-phase charging module, but also reduces the output current ripple significantly. Simulation indicates that such a modular design using three single-phase chargers to form one three-phase charger could control each phase separately, which is the effective way to deal with the grid imbalance. Such a feature does not exist in the conventional three-phase design like Fig. 1(b).

IV. Prototype and Experiments

A. Switch Test

As shown in Fig. 10(a), a DPT system with four GaN HEMTs in parallel was built with exactly the same parasitics as the final charger. Additional current shunt resistors are applied to measure the switching off current. The experimental waveform @

TABLE II
KEY PARAMETER VALUES

Symbol	Definition	Values
$C_{\rm oss}$	Switch equivalent capacitance	2 nF
C_{BUS11}, C_{BUS21} and C_{BUS31}	DC-bus capacitance of each module	10 μF
L	Transformer leakage inductance reflected to the primary	11.5 μH
n	Transformer turn ration	1:1
f_{sa}	Ceiling switching frequency	500 kHz
$V_{\rm in}$	Nominal input voltage	208 VAC
$V_{\rm out}$	Output voltage	200–450 VDC
P	power	0–7.2 kW
$I_{\rm o}$	Nominal output current of each module	20 A

$I_{\rm off} = 56$ A&$V_{\rm DC} = 400$ V is shown in Fig. 10(b), indicating the currents are balanced well with a small voltage spike.

B. Single-Phase Module Test

A single-phase on-board charger was prototype [see Fig. 11(a) and (b)]. The system key parameters are shown in Table II. The red block in Fig. 11(b) is the dc-bus capacitor, which is much smaller than dc links in other chargers. All three printed circuit boards (PCBs) are stacked to form a compact package. The overall module includes the input EMC choke and output capacitor as well. The charger has the dimension of $22 \times 15 \times 6.5$ cm^3, yielding a power density of 3.3 kW/L with the enclosure and heatsink. The system input and output waveform at 7.2 kW is shown in Fig. 11(c). The measured power factor $= 0.997$. The waveform of the DAB stage at battery voltage of 400 and 200 V is shown in Fig. 11(c) and (d), respectively. Each bottom plot shows the zoomed-in highlighted area. At the high output voltage, the secondary-side voltage becomes three level, while at the low output voltage, the primary-side voltage is three level, which is aligned with the SDPS and PDPS design in Section II. Fig. 11(e) shows the TPS control at the light-load condition, where the grid-voltage distortion disappears, validating its effectiveness. Fig. 11(f) shows the distribution of the grid-side current harmonics. The overall current total harmonic distortion is $\sim$6%, slightly higher than the requested 5%, which should be the focus of the future optimization.

C. Three-Phase Charger Test

The overall three-phase charger was prototyped, as shown in Fig. 12(a). The overall efficiency, power factor, and power density are the same as the single-phase charger. A 5-kW test shown in Fig. 12(c) indicates the overall current ripple is small (yellow line), even though the output current I_{oa}, I_{ob}, and I_{oc} have 120-Hz ripples. Such results validate the design of the charger. Fig. 12(d) compares the experimental efficiency between the proposed charger and an Si-version charger. Fig. 12(e) shows the loss breakdown, indicating that the transformer and switch conduction loss is more dominant. Given the grid-side ac/dc part has low switching frequency and low channel resistance, the rectifier loss is negligible. Fig. 12(f) shows the head-to-head comparison of the power density.

V. CONCLUSION

The main contribution of this paper is not only demonstrating effectively applying paralleled GaN HEMTs to EV chargers, but also realizing ZVS for all switches at any power. Such design efforts result in a three-phase 20-kW charger with superior power density (3.3 kW/L) and efficiency ($>97\%$). The size reduction is mostly attributed to the selected topology, making the dc-bus capacitor and grid-side inductor negligible compared to the conventional three-phase charger. The efficiency increment is mainly due to the adoption of E-mode GaN HEMTs. All such efforts make it possible to fit the charger in the car.

The building block of such a charger is a GaN HEMT-based single-phase 7.2-kW charger. By using a variable switching frequency and a phase-shift control strategy, ZVS turn-on for all the switches is secured. The phase shifts will be adjusted based upon the grid and battery voltage to cover 200–450-VDC output. To further enhance the system's light-load performance, a TPS control is utilized to eliminate the grid-current distortion. With three such single-phase charging modules connected to the three-phase grid, respectively, a 22-kW charger was built yielding the same power density and efficiency. A closed-loop control is also proposed to minimize the output current ripple when grid imbalance occurs. Future work will include running the charger long term and examining the thermal capability using different cooling methods, e.g., air cooling or liquid cooling. Meanwhile, since the overall charger is essentially bidirectional, testing its bidirectional capability for vehicle-to-grid is another pending task.

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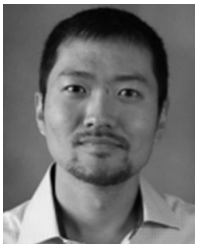

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