A 96.5% Efficiency Current Mode Hysteretic Buck Converter With 1.2% Error Auto-Selectable Frequency Locking

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***Abstract*—This paper proposes a current mode hysteretic buck converter with auto-selectable frequency locking. In this work, the hysteresis of the hysteretic comparator and the resistance of the feedback network are adjusted simultaneously to fix the switching frequency. The proposed switching frequency locking scheme can improve the power efficiency and fix the spectral components of the output at specific frequencies by suitably lowering the switching frequency under light load conditions. Implemented in a 65 nm complementary metal oxide semiconductor (CMOS), the proposed converter achieves peak efficiency of 96.5% for a 3.3 V input with less than 1.2% frequency error while locking at 1, 0.5, and 0.25 MHz.**

***Index Terms*—Auto-selectable frequency locking, current mode hysteretic buck converter, hysteresis and resistance control, light load condition.**

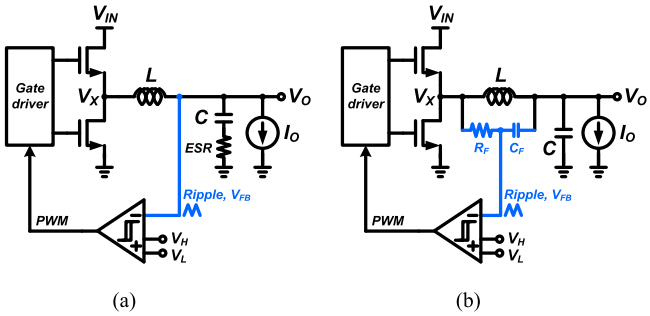

Fig. 1. Hysteretic buck converter. (a) Voltage mode hysteretic control. (b) Current mode hysteretic control.

I. Introduction

With the rapid spread of the internet of things (IoT) services, demand for portable devices, such as wearable devices and smartphones, which are important components of the IoT, has been rapidly increasing. Since the batteries of portable devices have a limited capacity, the need for a highly efficient power management integrated circuit (IC) to supply devices with the desired voltage from the battery continues to increase [1]–[4]. Improving the light load efficiency of the power management ICs is crucial, since portable devices mostly operate in standby mode [5]. Meanwhile, dynamic voltage scaling (DVS) is the most widely used power management technique for reducing the power loss of the system on chip (SoC) in portable devices [6]. Hence, the transient response performance of the dc – dc converters is an important design consideration for good dynamic performance while simultaneously ensuring the regulator's stability [7]. The hysteretic dc – dc converters are considered as low cost architecture with fast transient response because they do not require additional circuitry, such as error amplifiers for stability compensation. Therefore, these converters are widely used for power management of portable devices.

In a hysteretic buck converter, a feedback ripple signal is generated from the output voltage or the inductor current. The power switches of the hysteretic buck converter are controlled by comparing the feedback ripple voltage with the hysteretic voltages of the hysteretic comparator. Depending on the generation method of the feedback ripple, the hysteretic buck converter is categorized as voltage or current mode hysteretic control. Fig. 1 shows the basic architectures of the two hysteretic control-based buck converters. The voltage mode hysteretic buck converter shown in Fig. 1(a) obtains the ripple signal V_{FB} from the output voltage V_O. Assuming that the equivalent series resistance (ESR) of the output capacitor dominates the ripple, the switching frequency of the voltage mode hysteretic buck converter is given by [8]

$$f_{S\_\mathrm{VM}} = \frac{(V_{\mathrm{IN}} - V_O)\, V_O \cdot ESR}{L\,(V_H - V_L)\, V_{\mathrm{IN}}} \tag{1}$$

where V_{IN} is the input voltage of the converter and V_H and V_L are the upper and lower threshold voltages of the hysteretic comparator, respectively. The voltage mode hysteretic control determines the switching frequency by tuning the ESR of the output capacitor. However, if the amplitude of the feedback ripple signal from the output voltage is smaller than the hysteresis amplitude of the hysteretic comparator, the ripple signal cannot be compared with the hysteresis signals properly and the PWM signal will not be generated. Thus, capacitors with a large ESR

Manuscript received May 25, 2017; revised August 14, 2017; accepted October 20, 2017. Date of publication October 25, 2017; date of current version June 22, 2018. This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean Government (MSIP) (Grant NRF–2015R1A5A1036133). Recommended for publication by Associate Editor P. S. Shenoy. *(Corresponding author: Jeong-Il Seo.)*

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Digital Object Identifier 10.1109/TPEL.2017.2766691

are required to produce a feedback ripple signal for a proper comparison, and capacitors with a low ESR, such as ceramic capacitors, are not suitable for voltage mode hysteretic control [9]–[10]. Fig. 1(b) shows the fundamental architecture of the current mode hysteretic buck converter. The current mode hysteretic buck converter generates the feedback ripple signal $V_{\rm FB}$ through an RC network connected in parallel with the inductor [11]. In the current mode hysteretic control, the slope of the feedback ripple signal is determined by the RC time constant of the feedback network. Accordingly, the switching frequency of the current mode hysteretic buck converter is given by [12]

$$f_{S\_\rm CM} = \frac{(V_{\rm IN} - V_O)\, V_O}{R_F C_F\, (V_H - V_L)\, V_{\rm IN}} \tag{2}$$

where R_F and C_F are the resistance and capacitance of the feedback network, respectively. According to (2), the current mode hysteretic scheme can easily set the switching frequency by the appropriate adjustment of R_F and C_F. Unlike the voltage mode hysteretic control, since the feedback ripple signal of the current mode hysteretic control is not affected by the ESR of the output capacitor, capacitors with a low ESR can be used and a clean output voltage can be obtained. Accordingly, current mode hysteretic control has been widely adopted in recent years. However, as shown in (2), the switching frequency of current mode hysteretic control is changed by other factors as well, such as the input voltage, the output voltage, and the threshold voltages of the hysteretic comparator. The variable switching frequency, which is an unavoidable problem of hysteretic control, creates an unpredictable electro-magnetic interference (EMI) spectrum and leads to difficulty in designing filters to suppress EMI [13]–[14]. The EMI is strictly regulated because it degrades the sensitivity and can cause malfunctions in applications, such as RF communication systems.

To address the EMI issues, locking the switching frequency has been proposed [15]–[22]. This achieves a constant switching frequency by constructing an additional loop to regulate the switching frequency to the desired frequency through a phase-locked loop (PLL). In current mode hysteretic control, three main factors can be adjusted to lock the switching frequency: delay, hysteresis, and resistance. Fig. 2 shows simplified schematics of the frequency locking method that control each factor. The structure shown in Fig. 2(a) changes the hysteresis band of the hysteretic comparator to obtain a constant switching frequency [15]–[17]. This method requires precise hysteresis level selection considering the switching noise and the locking range of the switching frequency. Fig. 2(b) shows the frequency stabilization technique by adjusting the delay [18]–[20], where an additional delay is inserted into the control loop to fix the switching frequency. However, the internal delay of the control loop can degrade the transient response of the hysteretic converter. In the method proposed in [21]–[22], as presented in Fig. 2(c), the feedback resistance is configured as a switch-controlled resistance and its value is digitally controlled to fix the switching frequency. The resistance control method has a tradeoff between the settling time of the switching frequency and the resolution of the switch-controlled resistance. The resolution is closely related to the frequency error.

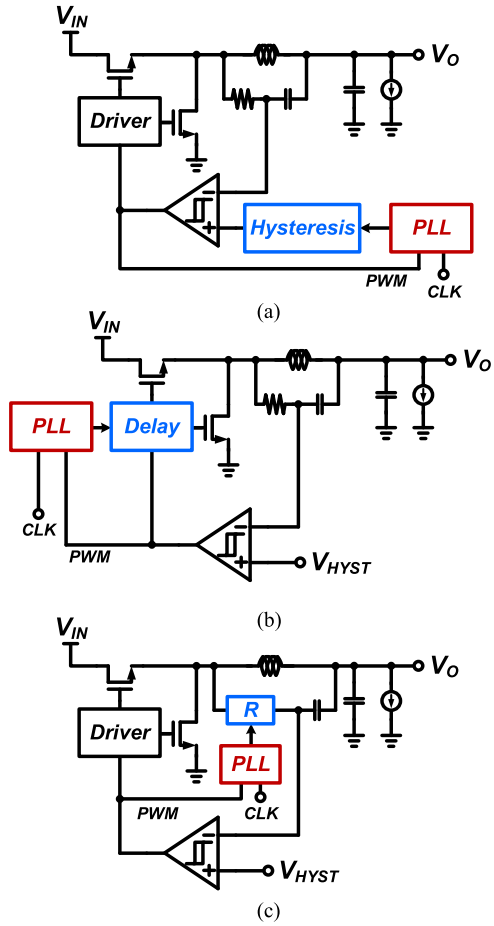


Fig. 2. Simplified structure of the frequency locking method. (a) Hysteresis control. (b) Delay control. (c) Resistance control.

Previous frequency stabilization techniques have reported a low switching frequency error. However, under light load conditions, previous techniques fix the switching frequency to a constant value or neglect the locking of switching frequency entirely. For a buck converter with a constant switching frequency, the power efficiency is drastically reduced due to the switching losses and gate driving losses under light load conditions [23]–[25]. In order to reduce these losses, techniques, such as pulse frequency modulation (PFM) [26]–[27], pulse skipping modulation (PSM) [28]–[30], and auto-selectable-frequency PWM [31] to lower the switching frequency under light loads, have been proposed. While PFM and PSM produce an unpredictable EMI spectrum composition due to the load current or other factors, the output spectrum of the auto-selectable-frequency PWM technique is predictable because it appears as the harmonic of the lowest switching frequency.

This paper proposes a current mode hysteretic buck converter with a novel technique that combines frequency reduction and stabilization methods through the feedback resistance and the hysteresis of the comparator for high power efficiency under light loads and a predictable EMI spectrum. Section II presents an analysis of the switching frequency of the current mode hysteretic buck converter under discontinuous conduction mode op-

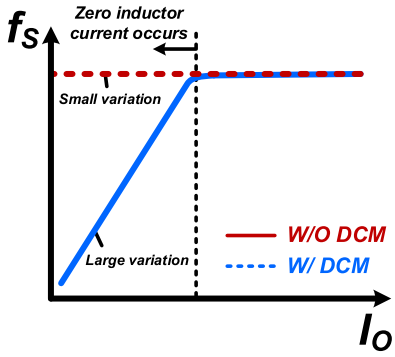


Fig. 3. Switching frequency of the current mode hysteretic buck converter versus load current with and without DCM.

eration and the operational principle for the proposed switching frequency locking technique. In Section III, schematic diagrams and implementation details of the proposed technique are presented. Experimental results are shown in Section IV. Finally, the conclusion of this paper is given in Section V.

II. Operation Principle

A. Switching Frequency of Current Mode Hysteretic Control

In a buck converter, low-side power switches can be implemented with a MOSFET or a diode depending on whether is a synchronous or asynchronous type. For low current applications, a synchronous buck converter is used to reduce the conduction losses. However, in synchronous buck converters, inadvertent losses occur due to the reverse inductor current under light load conditions. To eliminate the reverse current, the diode emulation mode (DEM) can be adopted in which the low-side MOSFET turns off when the inductor current becomes zero [32]–[33]. Since the synchronous buck converter without a DEM operates as a continuous conduction mode (CCM) over the entire load section, the switching frequency equation is given by (2). When the DEM is applied, the converter operates under discontinuous conduction mode (DCM) with the load current declining to zero. Following the same approach as in [34], the switching frequency of the current mode hysteretic buck converter under the DCM can be given by

$$f_{S\_CM\_DCM} = \frac{2I_O L\,(V_{IN} - V_O)\,V_O}{{R_F}^2 {C_F}^2 (V_H - V_L)^2 V_{IN}} \tag{3}$$

As shown in (2), the switching frequency of the CCM is mathematically unrelated to the load current. In practice, there is a slight variation in f_{S_CM} due to the internal delay of the control loop, the voltage drop across the on-resistance of the power switches, and the DCR of the inductor when the load current changes. On the other hand, according to (3), the switching frequency of the DCM is greatly affected by the load current. Equation (3) is valid only in the load current section where the inductor current reaches zero. Fig. 3 shows the switching frequency of the current mode hysteretic buck converter as a function of the load current with and without the DCM, where V_O is constant. Fig. 4 shows the feedback voltage and inductor

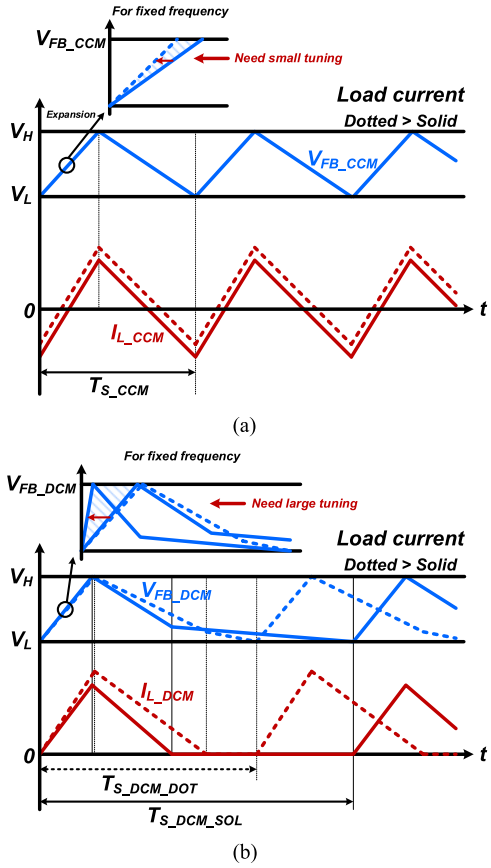


Fig. 4. Feedback voltage and inductor current waveforms of the current mode hysteretic buck converter for resistance control. (a) CCM. (b) DCM.

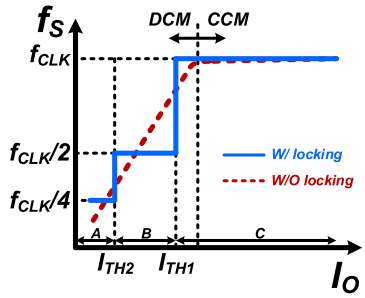


Fig. 5. Concept of the proposed switching frequency locking technique.

current waveforms of the current mode hysteretic buck converter for resistance control in the case of CCM and DCM. In Fig. 4, the dotted line represents the reference and indicates the feedback voltage and inductor current when the load current is higher than the solid line. Fig. 4(a) shows the case of CCM, where I_{L_CCM} and T_{S_CCM} are the inductor current and switching period, respectively. In the CCM, to fix the switching frequency, only a small range of feedback resistance adjustment is required because the feedback ripple voltage V_{FB_CCM} varies only slightly due to the load current. The frequency locking with resistance control in DCM is shown in Fig. 4(b), where I_{L_DCM} is the inductor current and $T_{S\_DCM\_DOT}$ and $T_{S\_DCM\_SOL}$ are the switching periods of the dotted and the solid lines, respectively. In the DCM, when the inductor current is zero and the

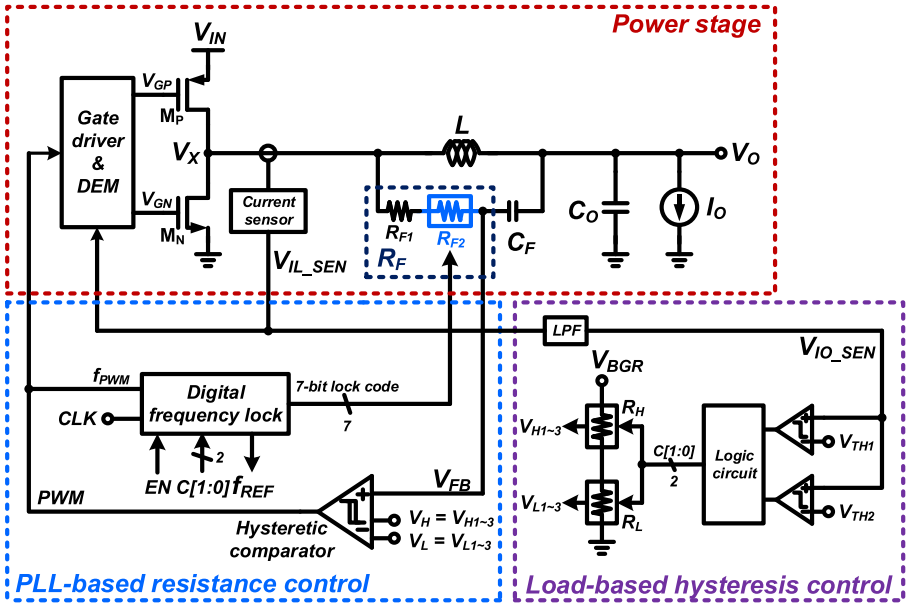


Fig. 6. Block diagram of the proposed current mode hysteretic buck converter with auto-selectable frequency locking technique.

power switches are turned off, the feedback capacitor, which forms the slope of the ripple in $V_{\mathrm{FB\_DCM}}$, is discharged by the load current. Therefore, if the load current decreases, the switching frequency decreases, as in (3). As a result, a wide range of feedback resistance adjustment is required, and it is difficult to fix the switching frequency with the adjustment range required in the CCM.

B. Principle of Proposed Switching Frequency Locking Technique

To lock the switching frequency in consideration of light load power efficiency, a new frequency locking technique is proposed in this paper. The proposed technique adopts a DEM to eliminate the reverse inductor current. As shown in Fig. 3, the switching frequency of the current mode hysteretic buck converter is constant in the CCM, whereas the switching frequency in the DCM decreases as the load current decreases. Fig. 5 shows the concept of the proposed frequency locking technique, where the switching frequency increases in a staircase pattern with an increase of the load current. The proposed method fixes the switching frequency constantly in the normal load current where CCM occurs. In the low load section where DCM occurs, the fixed switching frequency is lowered to improve the light load efficiency. The reduced switching frequency follows the frequency behavior of the auto-selectable-frequency PWM, which reduces the frequency while producing predictable output harmonics to meet the original purpose of the frequency locking. In Fig. 5, I_{TH1} and I_{TH2} are the two threshold currents, and the three sections of load currents, A, B, and C, are divided by the threshold currents. f_{CLK} is the frequency of the external clock, and the switching frequency is fixed at different frequencies, $f_{\mathrm{CLK}}/4$, $f_{\mathrm{CLK}}/2$, and f_{CLK} in each load current section. In section C, the switching frequency is locked at the same frequency as f_{CLK}, which is the reference. When the load current falls into Section B, the switching frequency is fixed at $f_{\mathrm{CLK}}/2$. The switching frequency is locked at $f_{\mathrm{CLK}}/4$ at the lowest load current, Section A. Through auto-selectable frequency locking, the output harmonics of all cases are included in the harmonics of the lowest locked frequency $f_{\mathrm{CLK}}/4$, and thus predictable spectral components of the output can be obtained while lowering the switching frequency.

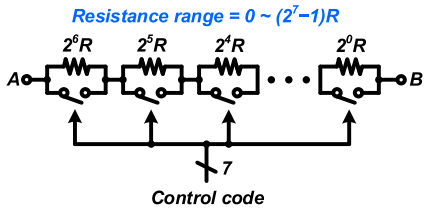


Fig. 7. 7-bit switch-controlled resistor.

III. Implementations

The circuit schematic of the proposed current mode hysteretic buck converter with the auto-selectable frequency locking technique is shown in Fig. 6. In Fig. 6, the proposed converter consists of a power stage, PLL-based resistance control, and load-based hysteresis control blocks. In the power stage, a synchronous buck converter is adopted in which P- and N-MOSFETs (M_P and M_N) are used for the high- and low-side switches, and the feedback resistance R_F is configured in series with a predefined resistance R_{F1} and a 7-bit switch-controlled resistor R_{F2}. Fig. 7 shows the schematic of the binary-weighted 7-bit switch-controlled resistor. In Fig. 6, the current sensor is adopted to sense the inductor current, and the DEM is applied to turn off the low-side switch M_N when the inductor current is zero. The inductor current sense signal $V_{\mathrm{IL\_SEN}}$ is fed to the low-pass filter (LPF) to obtain the load current information $V_{\mathrm{IO\_SEN}}$, and

TABLE I
OPERATION MECHANISM OF THE PROPOSED FREQUENCY LOCKING TECHNIQUE

Load Current	Load Detection Signal		Hysteretic Voltages		Hysteresis Band	Reference Frequency
I_o	C[1]	C[0]	V_H	V_L	$V_H - V_L$	f_{REF}
High	0	0	V_{H1}	V_{L1}	Narrow	f_{CLK}
↑	0	1	V_{H2}	V_{L2}	↓	$f_{CLK}/2$
Low	1	0	V_{H3}	V_{L3}	Wide	$f_{CLK}/4$

the 2-bit load detection code $C[1:0]$ is obtained by comparison with the threshold voltages V_{TH1} and V_{TH2}. The values of the switch-controlled resistors R_H and R_L are determined by the $C[1:0]$. The band-gap reference voltage V_{BGR} is divided by R_H and R_L to generate the upper and lower threshold voltages of the hysteretic comparator, $V_{H1\sim3}$ and $V_{L1\sim3}$. In the PLL-based resistance control part, a digital frequency lock block determines the reference frequency f_{REF} with the $C[1:0]$ code and the external clock signal CLK. A 7-bit lock code is produced by comparing the switching frequency f_{PWM} with f_{REF}. f_{PWM} is adjusted by changing the value of the switch-controlled resistor according to the 7-bit code. As shown in Fig. 3, since the switching frequency variation in DCM is larger than that of CCM, the range of required R_F must be widened. Therefore, the number of bits or the unit step size of the switch-controlled resistor must be increased for an extended R_F range. However, as the number of bits increases, the mismatch of switch-controlled resistors increases and the digital frequency lock block becomes more complex. Alternatively, if the unit step size is increased, the frequency error of the switching frequency with respect to the reference frequency increases.

Instead of transforming the switch-controlled resistor, load-based hysteresis control is added to ensure the R_F value required for the proposed frequency locking shown in Fig. 5. In the load-based hysteresis control, V_H and V_L of the hysteretic comparator are produced from the reference voltage V_{BGR} through voltage division using the switch-controlled resistors R_H and R_L, which are controlled by the $C[1:0]$ code. R_H and R_L are similar to the switch-controlled resistor shown in Fig. 7. The operation mechanism of the proposed frequency locking technique is shown in Table I. Under the heaviest load conditions $[C[1:0] = 00]$, f_{CLK} is selected as f_{REF}, and the upper and the lower hysteretic threshold voltages are selected as V_{H1} and V_{L1}, respectively. If the load current decreases and $C[1:0] = 01, f_{CLK}/2$ is selected as f_{REF} and the hysteretic voltages become V_{H2} and V_{L2} to expand the hysteresis band. Fig. 8 shows the frequency locking scenarios of the proposed frequency locking technique in the case of load transitions. In Fig. 8(a), when the load current I_O falls below $I_{TH1}, C[1:0] = 01$ and f_{REF} becomes $f_{CLK}/2$ after a delay by the current sensor and LPF. According to $C[1:0], V_H$ and V_L become V_{H2} and V_{L2}, respectively. Assuming no dithering, the value of the switch-controlled resistor R_{F2} varies over four regions from A_L to D_L. In the region A_L, the frequency locking at f_{CLK} is completed and R_{F2} is fixed. In the region B_L, R_{F2} is reduced by the decrease in the load current and the

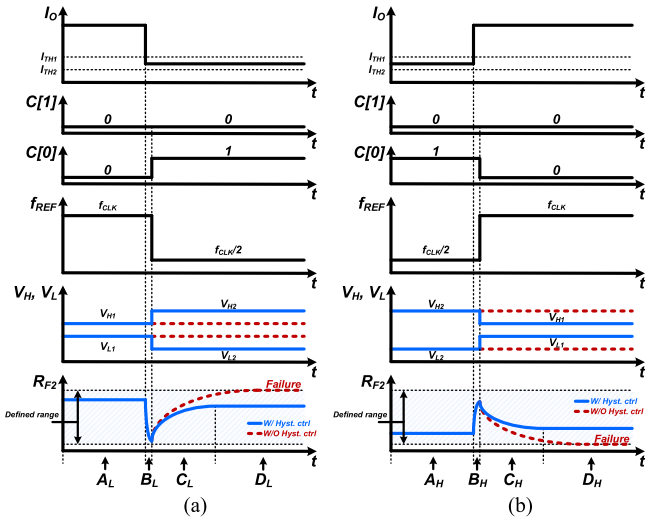


Fig. 8. Locking scenarios of the proposed frequency locking technique with and without load-based hysteresis control. (a) When entering a lighter load. (b) When entering a heavier load.

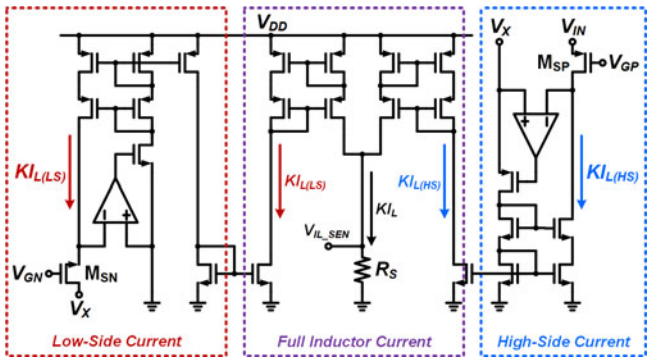


Fig. 9. Schematic of the current sensor.

switching frequency is rapidly lowered compared to f_{CLK}. After the delay, $C[1:0]$ changes and f_{REF} becomes $f_{CLK}/2$. In the region C_L, if there is no load-based hysteresis control [red dotted line], R_{F2} becomes too large to fix the switching frequency to $f_{CLK}/2, R_{F2}$ reaches the upper limit of the defined range, and the frequency locking fails. In the case where the hysteretic control is applied [blue solid line], V_H and V_L become V_{H2} and V_{L2} by $C[1:0]$, respectively, and R_{F2} required for locking is reduced. Thus, R_F for locking the switching frequency to $f_{CLK}/2$ is within the defined range. When the frequency locking is completed with respect to the changed f_{REF}, the operation state enters region D_L from region C_L and R_{F2} becomes constant. Fig. 8(b) shows the operation in the case of a transition to a heavier load condition. In the transition to a high load condition, there are four regions from A_H to D_H, and the frequency locking is completed through the operation opposite to that shown in Fig. 8(a).

A. Current Sensor

The typical current sensor shown in Fig. 9 is used to sense the full inductor current [35]. The current sensor consists of a high-

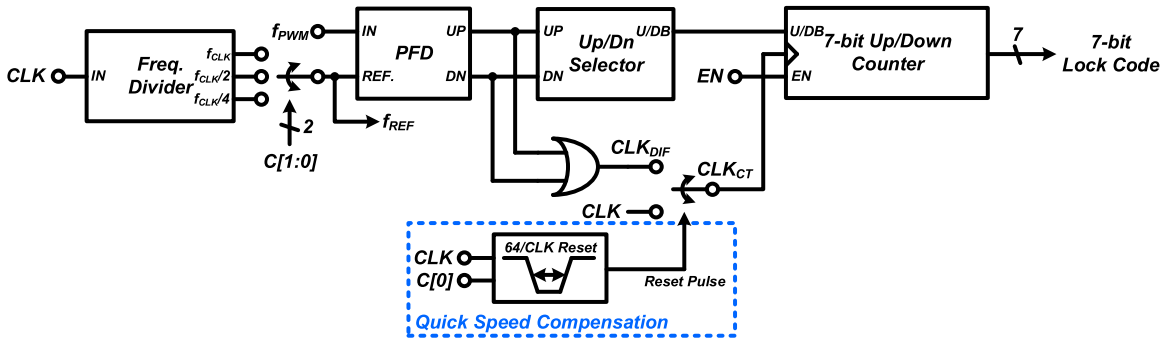


Fig. 10. Block diagram of the digital frequency lock block.

side current sensing part, a low-side current sensing part, and a current adder. The sensing switches $M_{\rm SP}$ and $M_{\rm SN}$ of the current sensor are K times smaller than M_P and M_N of the power stage in Fig. 6. In the high-side current sensing part, the V_X voltage is copied through the feedback using the amplifier. All the nodes of $M_{\rm SP}$ are then applied with the same voltages as all the nodes of the M_P, and the high-side current $KI_{L(\rm HS)}$ is detected. In the same manner, the low-side current $KI_{L(\rm LS)}$ can be sensed in the low-side current sensing part. The full inductor current KI_L is obtained by summing the sensed currents into the current mirrors and a corresponding voltage $V_{\rm IL\_SEN}$ is generated from a resistor R_S. In the design of the proposed hysteretic converter, the K value is 1/1400, and folded cascode amplifiers are used for feedback.

B. Digital Frequency Lock

Fig. 10 shows a block diagram of the digital frequency lock block applied to the proposed frequency locking technique. The digital frequency lock block includes a frequency divider, a phase-frequency detector (PFD), a 7-bit up/down counter, and quick speed compensation. The frequency divider divides the external clock signal CLK by 1/4, 1/2, and 1 times. One of the divided signals is selected at the reference $f_{\rm REF}$ of the PFD according to the C[1:0] code reflecting the load condition. In PFD, the switching frequency $f_{\rm PWM}$ during operation is compared to $f_{\rm REF}$ and an up or down pulse is produced depending on the difference. The generated pulse $CLK_{\rm DIF}$ is applied to the clock $CLK_{\rm CT}$ of the 7-bit up/down counter and the up/down signal U/DB required for the counter is set by the up/down selector similar to the latch. As a result, a 7-bit lock code is generated at the counter and the lock code adjusts R_{F2} of the feedback network in the power stage to lock the switching frequency. Unfortunately, in the case of locking the switching frequency at low frequencies, such as $f_{\rm CLK}/4$ and $f_{\rm CLK}/2$, the number of up or down pulses generated in the PFD is remarkably reduced. Therefore, since the output code of the counter changes slowly, the time taken to fix the frequency becomes longer. As shown in Fig. 8, when the load current section is changed, R_{F2} changes substantially. In other words, the frequency locking time becomes too large because the 7-bit lock code changes significantly. To improve the locking time, quick speed compensation is added, which reduces the time required for locking by driving the fastest frequency signal to $CLK_{\rm CT}$ for a specific

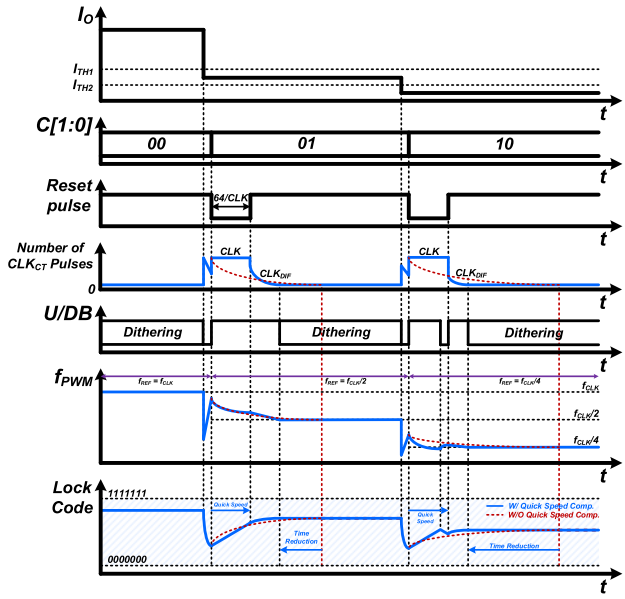


Fig. 11. Operation waveforms of the digital frequency lock block with and without quick speed compensation under light load conditions.

time. Fig. 11 shows the operation waveforms with and without quick speed compensation in the lighter load conditions. In the absence of quick speed compensation [red dotted line], $f_{\rm PWM}$ and $f_{\rm REF}$ according to $C[1:0]$ are compared in the PFD and the corresponding up/down signal and $CLK_{\rm DIF}$ are generated. The U/DB is set in the up/down selector, and the $CLK_{\rm DIF}$ is driven to the 7-bit up/down counter to generate the appropriate 7-bit lock code according to $f_{\rm PWM}$. When $f_{\rm PWM}$ approaches $f_{\rm REF}$, the number of $CLK_{\rm DIF}$ pulses becomes significantly smaller. Therefore, frequency locking is much slower at lower $f_{\rm REF}$. The quick speed compensation consists of a reset pulse generator and a multiplexer. The reset generator generates a reset pulse of $64/CLK$ intervals whenever $C[0]$ is changed. When a reset pulse is generated, CLK is set to $CLK_{\rm CT}$ instead of $CLK_{\rm DIF}$ in the multiplexer. Thus, with quick speed compensation [blue solid line], when the load section changes, the 7-bit up/down counter is driven for the time of $64/CLK$ at the fastest frequency CLK, $f_{\rm PWM}$ quickly reaches $f_{\rm REF}$, and $CLK_{\rm DIF}$ is then applied to the counter. Through the compensation, the time required to lock the switching frequency can be considerably shortened.

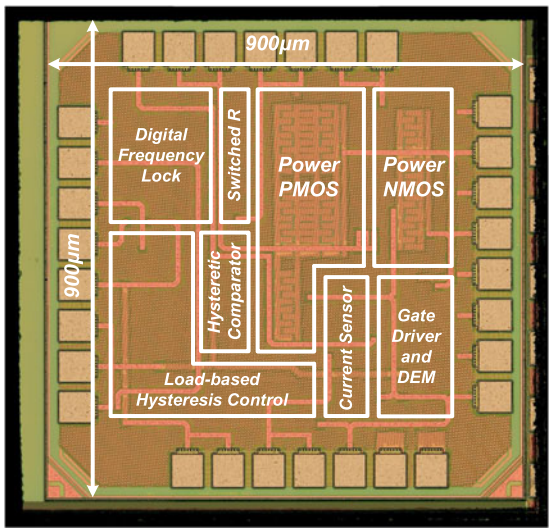


Fig. 12. Chip micrograph of the proposed converter.

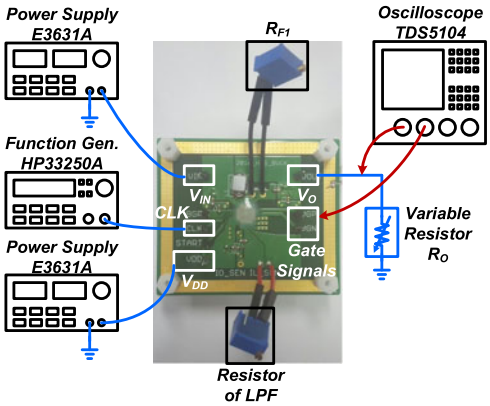


Fig. 13. Measurement setup of the proposed converter.

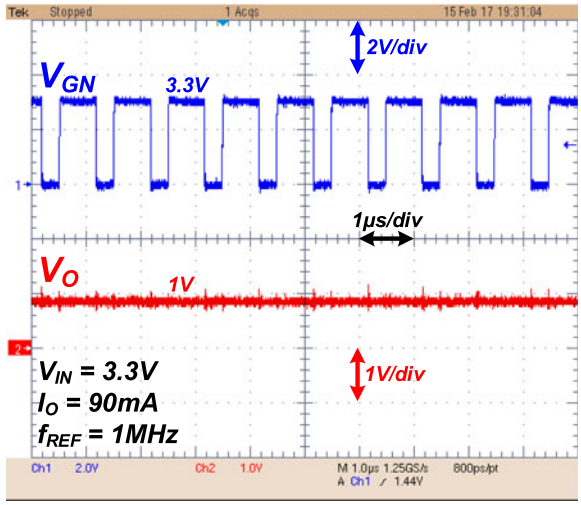


Fig. 14. Gate voltage of the N-MOSFET and output voltage waveforms at $I_O = 90$ mA.

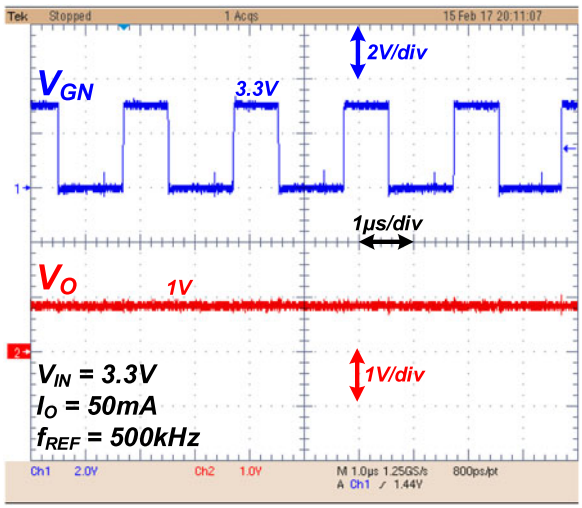


Fig. 15. Gate voltage of the N- MOSFET and output voltage waveforms at $I_O = 50$ mA.

IV. Experimental Results

The proposed current mode hysteretic buck converter with an auto-selectable frequency locking technique is implemented in a 65 nm CMOS technology. Fig. 12 shows the chip micrograph. The chip area including the pad is around 900 μm $\times$ 900 μm. The proposed converter covers an input voltage $V_{\rm IN}$ of 2.7 to 3.3 V and can drive load current of up to 150 mA. Fig. 13 shows the measurement setup of the proposed converter. External capacitors and resistors are used in the LPF and feedback networks for measuring. The proposed converter is measured at $V_{\rm IN} = 3.3$ V, $V_O = 1$ V, $L = 4.7$ μH, and $C_O = 10$ μF. This paper presents specific measurement results when the external clock is 1 MHz and the load current is changed by using a variable resistor R_O. The locking performance of the proposed frequency locking technique is verified by observing the gate signal $V_{\rm GN}$ of the N-MOSFET in the power stage under a specific load condition.

The operation waveforms of the proposed converter at $I_O = 90$ mA is shown in Fig. 14. In the digital frequency lock block, $f_{\rm REF} = f_{\rm CLK}$, and the switching frequency is fixed at 1 MHz. Fig. 15 shows the operation waveforms at IO = 50 mA. $f_{\rm REF}$ becomes $f_{\rm CLK}/2$, and a switching frequency locked to 500 kHz is observed. The switching frequency of the proposed converter at $I_O = 30$ mA is fixed at 250 kHz, as shown in Fig. 16. Fig. 17 shows the measured load transient response for the load current changes from 130 to 40 mA and vice versa. Fig. 18 shows the line transient response of the proposed converter with 0.6 V input voltage step (from 2.7 to 3.3 V) at a load current of 70 mA. The transient response may be degraded because the feedback RC time constant is continuously adjusted to fix the switching frequency at the transition. After the transition, the voltage error occurs due to the dithering of the feedback resistance and the changes in the threshold voltages of the load-based hysteresis control block and the reference frequency for locking. However, the proposed technique focuses on improving the switching frequency and light load efficiency. The switching frequency and frequency error of the proposed converter at different load conditions are presented in Fig. 19. As plotted in Fig. 19(a), the

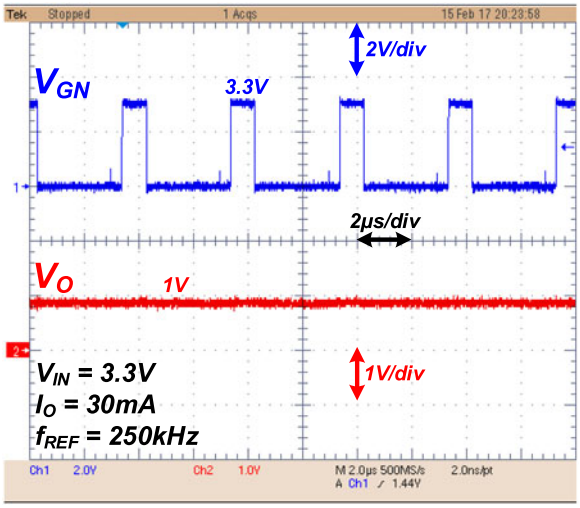
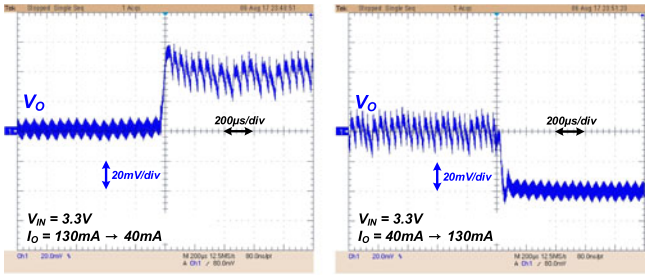
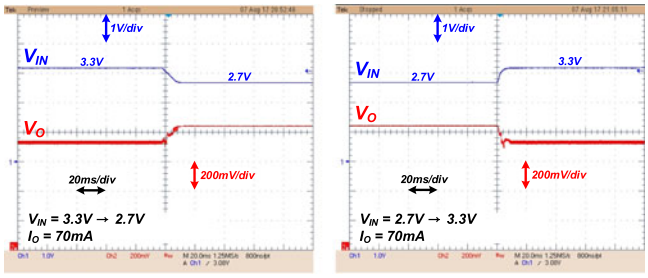


Fig. 16. Gate voltage of the N- MOSFET and output voltage waveforms at $I_O = 30$ mA.



(a) (b)

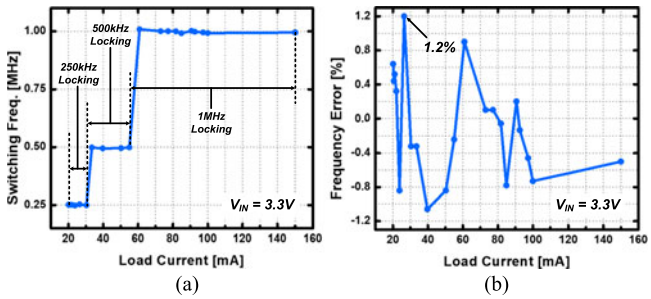
Fig. 17. Load transient response for the load current changes (a) from 130 to 40 mA and (b) from 40 to 130 mA.



(a) (b)

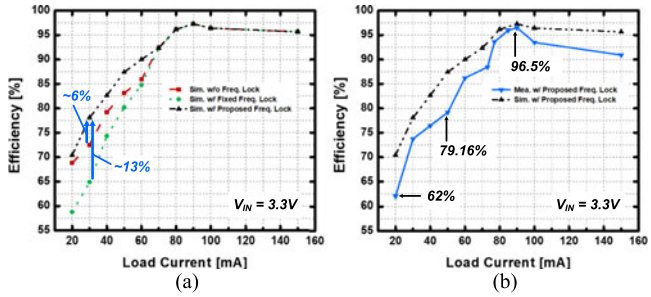
Fig. 18. Line transient response for the input voltages (a) from 3.3 to 2.7 V and (b) from 2.7 to 3.3 V.

switching frequency is locked at 1 MHz at a load current of 60–150 mA, 500 kHz at a load current of 33–60 mA, and 250 kHz at a load current of 20–33 mA. The frequency error for the reference frequency is within $\pm 1.2\%$, as shown in Fig. 19(b). Fig. 20 shows the power efficiency of the proposed converter at different conditions. The simulated efficiency at different frequency locking conditions is presented in Fig. 20(a). According to the simulation results, at a light load current of 30 mA, the efficiency of the proposed frequency locking condition shows 13% improvement over that of the fixed switching frequency condition at the same frequency. In addition, the efficiency of



(a) (b)

Fig. 19. Measured (a) switching frequency and (b) frequency error at different load conditions.



(a) (b)

Fig. 20. (a) Simulated efficiency at different frequency locking conditions and (b) comparison of the efficiency at the proposed frequency locking condition.

TABLE II
POWER CONSUMPTION BREAKDOWN OF THE PROPOSED CONVERTER AT $I_O = 50$ MA

	Item	Power [mW]	Percentage [%]
Measurement	Input Power	62.7	100
	Output Power	49.63	79.16
Simulation	Gate Driver & DEM (Gate Driving Loss)	4.42	7.05
	Power Switches (Switching & Conduction Loss)	3.73	5.95
	PWM Control Circuit (Hysteretic Comparators & Logics)	0.12	0.19
	Digital Frequency Lock	0.01	0.02
	Load-based Hysteresis Control	0.37	0.59
	Current Sensor	0.48	0.76
Estimation	Device Parasitics & PCB	3.94	6.28

TABLE III
SPECIFICATION SUMMARY OF THE PROPOSED CONVERTER

Technology	65 nm CMOS
Chip Area	900 μm × 900 μm
Input Voltage, V_{IN}	2.7–3.3 V
Output Voltage, V_o	1 V
Load Current, I_o	20–150 mA
Switching Frequency	1 MHz @I_o > 60 mA 500 kHz @I_o = 33 − 60 mA 250 kHz @I_o < 33 mA
Frequency Error	$\pm 1.2\%$
Inductor / Capacitor	$\mathbf{L} = 4.7\ \mu$H/$C_o = 10\ \mu$F
Peak Efficiency	96.5% @ $V_{IN} = 3.3$ V, $I_o = 90$ mA

TABLE IV
PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER

	This Work	[19] JSSC 2008	[16] TVLSI 2012	[21] SOVC 2012	[22] ISSCC 2015	[26] TCASI 2007	[31] ISSCC 2008	[27] JSSC 2011
Technology	65 nm CMOS	350 nm CMOS	350 nm CMOS	130 nm CMOS	350 nm BCDMOS	500 nm CMOS	350 nm CMOS	45 nm CMOS
Frequency Locking Technique	Resistance & Hysteresis	Delay	Hysteresis	Resistance	Resistance	None	None	None
Input Voltage	2.7–3.3 V	3 V	2.4–4.2 V	2.5 V	2.7–4.5 V	1.4–4.2 V	1.8–3 V	2.8–4.2 V
Output Voltage	1 V	0.5–2.5 V	1.8 V	0.7–1.8 V	2 V	0.5 V	0.9 V	0.4–1.2 V
Switching Frequency	1, 0.5, 0.25 MHz	850 kHz	1 MHz	1 MHz	1 MHz	∼140 kHz	2, 1, 0.5, 0.25 MHz	2 MHz
Frequency Error	±1.2%	±2.5%	±1%	±0.5%	±0.2%	None	None	None
Output Current	20–150 mA	30–500 mA	–500 mA	350–900 mA	–700 mA	–250 mA	–500 mA	0.2–100 mA
Inductor/ Capacitor	4.7 μH/10 μF	4.7 μH/10 μF	4.7 μH/4.7 μF	$1-5$ μH/ 10 μF	4.7 μH/10 μF	1 μH/20 μF	2.2 μH/2.2 μF	10 μH/2 μF
Peak Efficiency	96.5%	94.5%	95%	93%	95.5%	83%	∼90%	87.4%
Efficiency @50 mA Load	79.16%@ $V_{IN} = 3.3$ V	$>88\%$	N/A	N/A	N/A	76% @$V_{IN} =$ 3 V	$\sim 80\%$@ $V_{IN} = 3$ V	84%@ $V_{IN} = 3$ V
Light Load Technique	YES (ASFPWM)	NO	YES (PFM)	NO	NO	YES (PFM)	YES (ASFPWM)	YES (PFM)
Output Spectrum @Full Load	Predictable	Predictable	Unpredictable	Predictable	Predictable	Unpredictable	Predictable	Unpredictable
Note	Freq. Lock & Light Load Eff.	Freq. Lock	Freq. Lock & Light Load Eff.	Freq. Lock	Freq. Lock	Light Load Eff.	Light Load Eff.	Light Load Eff.

the proposed solution improves by about 6% compared to the condition where there is no locking mechanism while the switching frequency changes naturally. The measured efficiency of the proposed converter, reasonably agrees with the simulation result, is shown in Fig. 20(b). For a given condition, the peak efficiency reaches 96.5% at a load current of 90 mA. Greater than 62% efficiency is measured with the use of the proposed locking technique at load currents of less than 40 mA. To show the cost/benefit tradeoff of the proposed solution, the measured input/output power and the simulated power consumption of each block at a load current of 50 mA are described in Table II. It can be seen that more than 13% of the input power is consumed by the gate driver, power switches, and PWM control circuit. About 6% of the input power is dissipated by the device parasitics associated with the converter including PCB. On the other hand, the total power consumption of the remaining blocks, including the digital frequency lock and load-based hysteresis control blocks, occupies a small portion of about 1.4%. A performance summary of the proposed converter is presented in Table III.

Table IV shows a performance comparison between the proposed hysteretic buck converter and previous hysteretic buck converters. The performance comparison table is divided into two categories depending on the design focus of the prior works. The first category is the fixed switching frequency. The second category is the light load efficiency. [16], [19], [21] and [22] are included in the first category. In the second category, [26]–[27] and [31] with the switching frequency scaling method are listed. In the comparison table, compare to the prior works of the first category, the frequency error of the proposed converter is 1.2%, which is relatively larger than the state-of-the-art technique. However, considering the fact that the purpose of switching frequency locking is predictable output spectrum, the switching frequency with an error of 1.2% would produce a sufficiently predictable output spectrum. Meanwhile, the proposed converter achieves the efficiency of 79.16% at a 50 mA load current. Since the proposed scheme has the lower limit on the switching frequency, the light load efficiency of the proposed scheme may be lower than that of the PFM scheme which can drop the switching frequency to near the audible frequency without frequency limit when the load current reduces. However, the proposed converter achieves comparable light load efficiency compare to that of the converters presented in the second category. Compare to [16], which considers both the fixed switching frequency and light load efficiency, the proposed converter provides predictable output spectrum over the full load range. The proposed technique has a value in terms of suggesting a way to achieve both a predictable output spectrum independent of the load current and enhanced light load efficiency.

V. CONCLUSION

A current mode hysteretic buck converter with an auto-selectable frequency locking technique is proposed in this paper. The proposed switching frequency locking technique can improve the power efficiency and fix the spectral components of the output by appropriately lowering the switching frequency under a light load condition. In the proposed converter, the hysteresis of the hysteretic comparator and the resistance of the feedback network are controlled simultaneously to lock the switching frequency. The proposed converter has been implemented in a 65 nm CMOS technology. The switching frequency of the proposed converter is locked at 1, 0.5, and 0.25 MHz according to the load current, and the measured frequency error is within 1.2%. The measured peak efficiency is 96.5% at an input voltage of 3.3 V.

REFERENCES

[1] B. Sahu and G. A. Rincon-Mora, "A low voltage, dynamic, noninverting, synchronous buck-boost converter for portable applications," *IEEE Trans. Power Electron.*, vol. 19, no. 2, pp. 443–452, Mar. 2004.

[2] Y.-J. Lee, A. Khaligh, A. Chakraborty, and A. Emadi, "Digital combination of buck and boost converters to control a positive buck-boost converter and improve the output transients," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1267–1279, May 2009.

[3] P.-C. Huang, W.-Q. Wu, H.-H. Ho, and K.-H. Chen, "Hybrid buck-boost feedforward and reduced average inductor current techniques in fast line transient and high-efficiency buck-boost converter," *IEEE Trans. Power Electron.*, vol. 25, no. 3, pp. 719–730, Mar. 2010.

[4] W.-C. Chen, C.-C. Chen, C.-Y. Yao, and R.-J. Yang, "A fast-transient wide-voltage-range digital-controlled buck converter with cycle-controlled DPWM," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 1, pp. 17–25, Jan. 2016.

[5] W.-R. Liou, M.-L. Yeh, and Y. L. Kuo, "A high efficiency dual-mode buck converter IC for portable applications," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 667–677, Mar. 2008.

[6] H.-H. Huang, C.-L. Chen, and K.-H. Chen, "Adaptive window control (AWC) technique for hysteresis DC-DC buck converters with improved light and heavy load performance," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1607–1617, Jun. 2009.

[7] C.-Y. Hsieh and K.-H. Chen, "Adaptive pole-zero position (APZP) technique of regulated power supply for improving SNR," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2949–2963, Nov. 2008.

[8] B. C. Bao, J. Yang, J. P. Xu, X. Zhang, and G. H. Zhou, "Effect of output capacitor ESR on dynamic performance of voltage-mode hysteretic controlled buck converter," *Electron. Lett.*, vol. 49, no. 20, pp. 1293–1294, Sep. 2013.

[9] L. K. Wong and T. K. Man, "Steady state analysis of hysteretic control buck converters," in *Proc. 13th IEEE Int. Power Electron. Motion Control Conf.*, Sep. 2008, pp. 400–404.

[10] Linear Technology Corporation, "Ceramic input capacitors can cause overvoltage transients," Application Note 88, Linear Technology Corporation, Milpitas, CA, USA, Mar. 2001.

[11] M. Castilla, L. G. de Vicuna, J. M. Guerrero, J. Miret, and N. Berbel, "Simple low-cost hysteretic controller for single-phase synchronous buck converters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1232–1241, Jul. 2007.

[12] T. Nabeshima, T. Sato, S. Yoshida, S. Chiba, and K. Onda, "Analysis and design considerations of a buck converter with a hysteretic PWM controller," in *Proc. IEEE Power Electron. Specialists Conf.*, 2004, vol. 2, pp. 1711–1716.

[13] J. Balcells, A. Santolaria, A. Orlandi, D. Gonzalez, and J. Gago, "EMI reduction in switched power converters using frequency modulation techniques," *IEEE Trans. Electromagn. Compat.*, vol. 47, no. 3, pp. 569–576, Aug. 2005.

[14] Power Integrations, Inc., "TOPSwitch power supply design techniques for EMI and safety," Application Note 15, Power Integrations, Inc., San Jose, CA, USA, Apr. 2005.

[15] S. C. Huerta, P. Alou, J. A. Oliver, O. Garcia, J. A. Cobos, and A. Abou-Alfotouh, "Non-linear control for DC-DC converters based on hysteresis of the COUT current with a frequency loop to operate at constant frequency," *IEEE Trans. Ind. Electron.*, vol. 58, no. 3, pp. 1036–1043, Mar. 2011.

[16] Y. Zheng, H. Chen, and K. N. Leung, "A fast-response pseudo-PWM buck converter with PLL-based hysteresis control," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 20, no. 7, pp. 1167–1174, Jul. 2012.

[17] Z. C. Sun, L. Siek, R. P. Singh, and M. Je, "A fixed-frequency hysteretic controlled buck DC–DC converter with improved load regulation," in *Proc. IEEE Int. Symp. Circuits Syst.*, Jun. 2014, pp. 954–957.

[18] C.-H. Tso and J.-C. Wu, "A ripple control buck regulator with fixed output frequency," *IEEE Power Electron. Lett.*, vol. 1, no. 3, pp. 61–63, Sep. 2003.

[19] F. Su, W.-H. Ki, and C.-Y. Tsui, "Ultra fast fixed-frequency hysteretic buck converter with maximum charging current control adaptive delay compensation for DVS application," *IEEE J. Solid State Circuits*, vol. 43, no. 4, pp. 815–822, Apr. 2008.

[20] P. Li, D. Bhatia, L. Xue, and R. Bashirullah, "A 90–240 MHz hysteretic controlled DC-DC buck converter with digital phase locked loop synchronization," *IEEE J. Solid State Circuits*, vol. 46, no. 9, pp. 2108–2119, Sep. 2011.

[21] Q. Khan, A. Elshazly, S. Rao, R. Inti, and P. Hanumolu, "A 900 mA 93% efficient 50 μA quiescent current fixed frequency hysteretic buck converter using a highly digital hybrid voltage- and current-mode control," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2012, pp. 182–183.

[22] S.-H. Lee *et al.*, "A 0.518 mm^2 quasi-current-mode hysteretic buck DC-DC converter with 3 μs load transient response in 0.35 μm BCDMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[23] O. Abdel-Rahman, J. A. Abu-Qahouq, L. Huang, and I. Batarseh, "Analysis and design of voltage regulator with adaptive FET modulation scheme and improved efficiency," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 896–906, Mar. 2008.

[24] J. Sun, M. Xu, Y. Ren, and F. C. Lee, "Light-load efficiency improvement for buck voltage regulators," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 742–751, Mar. 2009.

[25] Y. Jang and M. M. Jovanovic, "Light-load efficiency optimization method," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 67–74, Jan. 2010.

[26] B. Sahu and G. A. Rincon-Mora, "An accurate, low-voltage, CMOS switching power supply with adaptive on-time pulse-frequency modulation (PFM) control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 2, pp. 312–321, Feb. 2007.

[27] S. Bandyopadhyay, Y. K. Ramadass, and A. P. Chandrakasan, "20 μA to 100 mA DC-DC converter with 2.8–4.2 V battery supply for portable applications in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2807–2820, Dec. 2011.

[28] H.-W. Huang, K.-H. Chen, and S.-Y. Kuo, "Dithering skip modulation, width and dead time controllers in highly efficient DC-DC converters for system-on-chip applications," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2451–2465, Nov. 2007.

[29] S. Angkititrakul and H. Hu, "Design and analysis of buck converter with pulse-skipping modulation," in *Proc. IEEE Power Electron. Specialists Conf.*, 2008, pp. 1151–1156.

[30] S. Kapat, A. Patra, and S. Banerjee, "Achieving monotonic variation of spectral composition in DC-DC converters using pulse skipping modulation," *IEEE Trans. Circuits Syst. I, Reg. Paper*, vol. 58, no. 8, pp. 1958–1966, Aug. 2011.

[31] T. Y. Man, P. K. T. Mok, and M. Chan, "An auto-selectable-frequency pulse-width modulator for buck converters with improved light-load efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 440–626.

[32] C. Chun, Q. Weihong, and N. Dequina, "Adaptive zero-current switching control scheme for diode emulation operation," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2011, pp. 871–876.

[33] Y. Chen, P. Asadi, and P. Parto, "Comparative analysis of power stage losses for synchronous buck converter in diode emulation mode vs. continuous conduction mode at light load condition," in *Proc. 25th IEEE Annu. Appl. Power Electron. Conf. Expo.*, 2010, pp. 1578–1583.

[34] Texas Instruments, Inc., "AN-1487 Current mode hysteretic buck converter," Application Report, Texas Instruments, Inc., Dallas, TX, USA, 2006.

[35] C.-W. Chen and A. Fayed, "A low-power dual-frequency SIMO buck converter topology with full-integrated outputs and fast dynamic operation in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 9, pp. 2161–2173, Sep. 2015.

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