Variable Switching Frequency PWM Strategy of Two-Level Rectifier for DC-Link Voltage Ripple Control

Qiao Li and Dong Jiang, *Senior Member, IEEE*

***Abstract*—The switching frequency is an important control parameter of pulse-width-modulation (PWM) rectifier to reduce switching losses and electromagnetic interference noise. This paper proposed a variable switching frequency PWM (VSFPWM) strategy for dc-link voltage ripple control in two-level rectifier. DC-link voltage ripple is determined by the dc-link current directly, and can be predicted synchronously with PWM signals. A real-time prediction model of dc-link voltage ripple is derived for a common voltage-oriented control PWM rectifier. Then, VSFPWM control is introduced, which changes the switching frequency cycle to cycle with a restriction of dc-link voltage ripple peak value. Furthermore, the dynamic behavior is also observed when the proposed VSFPWM control scheme is adopted. Detail simulation and experimental comparisons are carried out between VSFPWM and normal constant switching frequency PWM, which demonstrate the advantages of the proposed method.**

***Index Terms*—Electromagnetic interference (EMI), prediction, pulse-width-modulation (PWM) rectifier, switching losses, variable switching frequency, voltage ripple.**

I. Introduction

THREE-PHASE voltage source rectifiers (VSR) with pulse width modulation (PWM) are widely accepted and used in industrial applications owing to its high performance, such as controllable power factor, bidirectional power flow, reduced input harmonics [1]–[3], etc. The most popular control strategies for PWM rectifier are [4]–[8]: 1) Vector-oriented current control, which adjusts the power flow via internal current control loop, including voltage-oriented control (VOC) and virtual-flux-oriented control (VFOC); (2) Direct power control, which regulates the power flows via instantaneous power control loops, including voltage-based direct power control (V-DPC) and virtual-flux-based power control (VF-DPC). The VOC and VFOC employ the traditional PWM module to track the reference under the revolving *d-q* reference frame. Different from vector-oriented control, V-DPC and VF-DPC select the switching state through a lookup table or hysteresis loop. In addition, model predictive control is another kind of high-performance control strategy for PWM rectifier without traditional PWM module, attracting wide attention currently. This paper is still based on the VOC strategy, but the PWM generation is optimized according to the real-time dc-link voltage prediction model.

In a two-level PWM rectifier system, various PWM methods are employed to adjust the output voltage, such as space-vector PWM (SVPWM) and discontinuous PWM (DPWM). The dc-link capacitor is utilized to bypass the current ripple and generates the voltage ripple that is usually limited in a certain range. The dc-link current ripple and voltage ripple are determined by PWM method; ac-side current, load current, and capacitor value, and are important for capacitor selection simultaneously. In [9], Ayhan and Hava analyzed current ripple characteristics with several common PWM methods, which are beneficial for the loss calculation of dc-link capacitor. Hava *et al*. [10] gave a dc-link capacitor design method, mainly considering voltage ripple and losses caused by the flowing current.

Voltage ripple in the dc-link capacitor is a key factor for the design of dc-link capacitor. Many research works have been done for the optimization of dc-link capacitor. In the view of PWM, the variation of dc-link voltage ripple gives an opportunity to make variation of switching frequency that can control the dc-link voltage ripple distribution. Then, with the same dc-link voltage ripple requirement, the average switching frequency and the switching losses can be reduced. In addition, the variation of switching frequency can reduce the electromagnetic interference (EMI) noise of the PWM rectifier from constant switching frequency PWM (CSFPWM) whose EMI noise is focusing around the harmonics of constant switching frequency. These two benefits (reduction of losses and EMI) are only with software modification and without any change in hardware, that is, so-called variable switching frequency PWM (VSFPWM).

VSFPWM was proposed for three-phase PWM converters with the target of ac-side current ripple initially, with the ac-side current ripple prediction models [11]–[17]. In order to achieve a better control over the ac-side current ripple, the time-domain-based analysis has been reported in previous literatures. Jiang and Wang [11] first proposed a current ripple prediction method using the Thevenin equivalent circuit for the three-phase inverter, and similar evaluation is also shown in [12]. The comparison and analysis of peak-to-peak current in

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Q. Li is with the Department of Electrical and Electronics, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: liqiao@hust.edu.cn).

D. Jiang is with the School of Electrical and Electronics Engineering, Huazhong University of Science and Technology, Wuhan 430074, China (e-mail: jiangdong.tsinghua@gmail.com).

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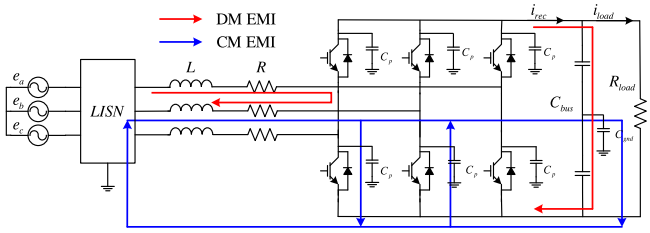

Fig. 1. Equivalent circuit for AFE rectifier as well as EMI mode path.

multiphase and multilevel inverter have been summarized in [13] and [14]. For simplifying the calculation of current ripple in multiphase inverter, a general current ripple prediction method is given in [15]. Furthermore, VSFPWM has been implemented in the three-phase inverter for current ripple peak value and rms value control, in [16] Jiang and Wang pointed out that VSFPWM has a better performance in switching losses and EMI noise under the same current ripple criterion, comparing with the CSFPWM. Yang *et al.* [17] used the *d-q* transformation to realize the current prediction in interior permanent magnet motors. Extended work has been carried out for PWM torque ripple control [18] and optimal switching losses reduction [19].

However, the physical principle of dc-link voltage ripple and ac-side current ripple are different. Without understanding the dc-link voltage ripple model, which is associated with PWM, the DC-link voltage ripple based VSFPWM is not possible. Note that the existing VSFPWM control is limited to the ac-side current ripple of the inverter; here the VSFPWM for dc-link voltage ripple control of the rectifier will be introduced. Jiang and Li [20] presented a real-time prediction method of dc-link current considering the ac-side current ripple, but the analysis of dc-link voltage ripple is not given in the paper. This paper focuses on the dc-link voltage ripple peak, and adopts the VSFPWM method to reduce the switching losses and EMI noise of the VSR system.

The rest of this paper is organized as follows. In Section II, a rigorous real-time prediction of dc-link voltage ripple is provided first. In Section III, based on the prediction model, the VSFPWM strategy is carried out in a two-level rectifier through the MATLAB/Simulink, the steady-state performance of it is compared with the CSFPWM in detail. In Section IV, assuring the dc-link required voltage ripple, the experimental results are given to verify the superiority of the proposed method. Meanwhile, the switching frequency has influence on the control loop bandwidth [21], the dynamic state performance should be analyzed in the results. Finally, the conclusions are summarized in Section V.

II. DC-Link Voltage Ripple Prediction

The active-front-end (AFE) rectifier is considered here as shown in Fig. 1, which consists of a three-phase two-level converter, three inductors inserted in the ac side, and a capacitor connected to the dc side. The line impedance stabilization network (LISN) is used here to prevent external conductive noise on the power system, and the EMI path mode is also depicted in Fig. 1. The voltage-oriented current control method is adopted

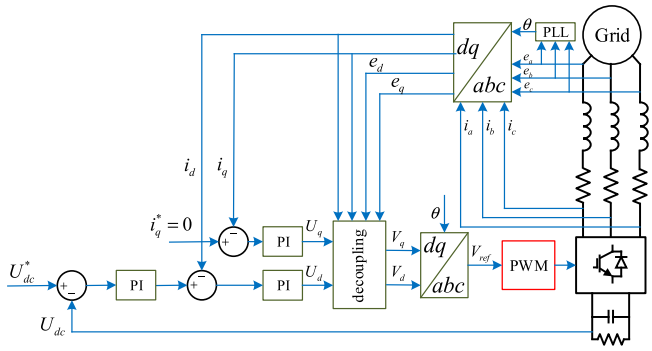

Fig. 2. Control structure of AFE rectifier.

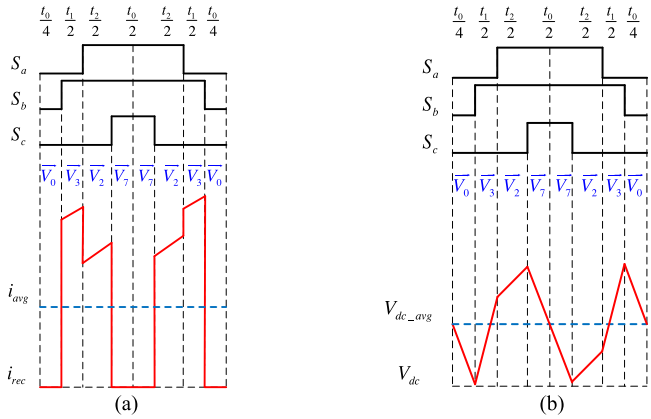

Fig. 3. Rectifier structure and dc-link current/voltage ripple in one switching frequency: (a) dc-link current and (b) dc-link voltage ripple.

based on the revolving *d-q* reference frame. For the output current control, the terminal voltage of the converter is adjusted according (1). Fig. 2 gives the basic control structure of a two-level rectifier, including the voltage and current double-loop control, as well as PWM module. The grid voltage vector is oriented to *d*-axis and the *q*-axis of it is forced to be zero in phase locking loop tracking controller. In *d-q* axis, coupling terms are added to the u_{d} and u_{q}, respectively, in the internal current loop, using two conventional proportional-integral (PI) controller to regulate the output current. For dc voltage control, a voltage PI controller is used here, and delivers the *d-q* axis current reference. The unity power factor is analyzed in this paper, thus, i_q^* is set to 0

$$\begin{cases} V_d = -L\frac{di_d}{dt} - Ri_d + \omega Li_q + e_d \\ V_q = -L\frac{di_q}{dt} - Ri_q - \omega Li_d + e_q. \end{cases} \tag{1}$$

With typical SVPWM, Fig. 3(a) shows the dc-link current in one switching cycle, a function of switching state, and ac-side current (2) determined by the ac-side voltage/current vectors. With three-phase duty cycles (d_a, d_b, d_c), the action time of each sectors shown in Fig. 3(a) can be calculated in (3). By computing the integral of the current difference through the capacitor in each sector, the dc-link voltage ripple is obtained with (4). The dc-link current is a ladder-like distribution if ac current ripple is ignored, and voltage ripple peak is simply proportional to the

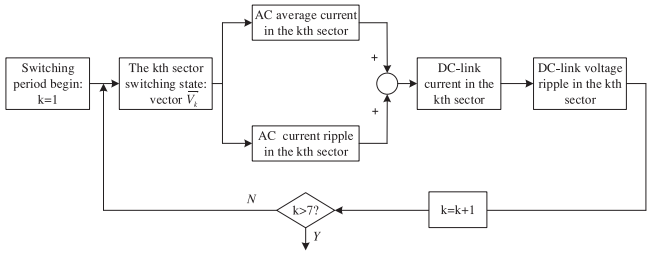

Fig. 4. DC-link voltage ripple prediction: (a) calculation process in one switching cycle.

switching period (T_s) as shown in Fig. 3.(b)

$$i_{\rm rec} = S_a i_a + S_b i_b + S_c i_c \tag{2}$$

$$\begin{cases} t_0 = (1 - d_b)T_s \\ t_1 = (d_b - d_a)T_s \\ t_2 = (d_a - d_c)T_s \end{cases} \tag{3}$$

$$V_{\rm ripple} = \frac{\int (i_{\rm rec} - i_{\rm load})dt}{C_{\rm bus}} \tag{4}$$

where i_d and i_q are the phase current in *d-q* axis; V_d and V_q are the terminal voltage of rectifier in *d-q* axis; *L* and *R* are the inductance and the equivalent resistance, respectively; e_d and e_q are the projection of grid voltage vector in *d-q* axis; ω is the electrical angular velocity; S_a, S_b, and S_c are the switching state of three phase determined by the three-phase duty cycles; i_a, i_b, and i_c are the three-phase current; t_0, t_1, t_2 are the action time of zero vectors and active vectors shown in Fig. 3(a); $i_{\rm rec}$ is the dc-link current and $i_{\rm load}$ is the load current; $C_{\rm bus}$ is the dc-link capacitance; and $V_{\rm ripple}$ is the dc-link voltage ripple.

Thanks to the DC-link current prediction method [20], its time-domain-based prediction is realized in each switching cycle. Combining the equation (3) and (4), the prediction process of DC-link voltage ripple is shown in Fig. 4. There are seven sectors in one switching cycle with typical SVPWM, and the calculation is executed one by one. In the *k*th sector, the dc-link current ripple is composed of two parts: 1) ac average current which is given by the controller; 2) ac current ripple which can be predicted with three-phase duty cycles. Next, the three-phase switching states are at work for ac-side phase current selection. Then, the dc-link voltage ripple is achieved with (4).

Taking voltage vector $\overrightarrow{V_3} = 010$ as an example, it is the second sector as shown in Fig. 3(a). In this sector, the dc-link current is selected as $i_{\rm b}$, the slope of dc-link voltage ripple is $(i_{\rm load} - i_b)/C_{\rm bus}$, and the action time is $(d_b - d_a)T_s/2$. With the slope and action time of each sector, the locus of dc-link voltage ripple can be depicted as shown in Fig. 3(b). Obviously, the dc-link current is not a ladder-like distribution when active voltage vectors turn to work, and actually the voltage ripple is a quadric relationship with switching period. The prediction program repetitively acts in next switching cycle when the last sector has finished the calculation. In addition, the prediction process is also valid for other PWM methods with minor change. For example, the number of sectors turns into five in each switching cycle if the DPWM is used.

TABLE I
RECTIFIER PARAMETERS

Parameter	Value
Rated power	2.7 kW
DC-link voltage	200 V
Line-to-line voltage	182 V
Inductance	1 mH
Equivalent resistance	0.5 Ω
Grid frequency	50 Hz
Constant switching frequency	10 kHz
DC-link capacitor	17.5 μF

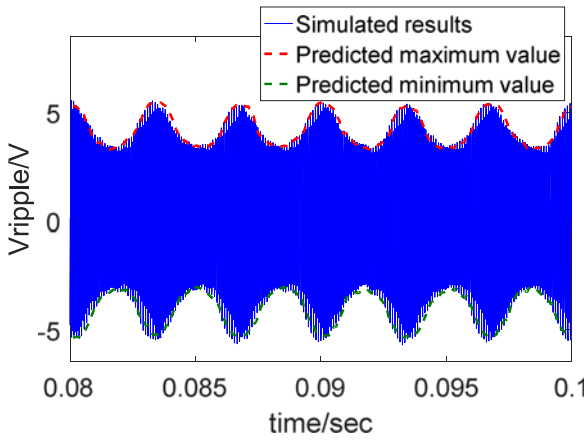

Fig. 5. Comparison between the prediction and the simulation results of the dc-link voltage ripple in one line cycle.

In order to verify the prediction method, an AFE rectifier has been simulated by MATLAB/Simulink, having parameters shown in Table I.

With typical SVPWM, Fig. 5 shows the dc-link voltage ripple comparison between predicted results and the simulated. In a fundamental period, the dc-link voltage ripple is rising and falling with the peak value (±5.5 V), matching well with the predicted envelope, which illustrates the correctness of the prediction method. It can be observed that the voltage ripple reaches the peak value only in several time points. The requirement of dc-link voltage ripple for an AFE rectifier is usually with the peak value requirement. Then, if with (±5.5 V) voltage ripple requirement, the performance is over-qualified in most of the periods, which means the switching frequency could be reduced in those periods, thus, the space limited by the peak value is not fully utilized with CSFPWM. The periodic variation of dc-link voltage ripple can be well predicted by the proposed method in real-time, which provides a tool for VSFPWM for dc-link voltage ripple control.

III. VSFPWM FOR VOLTAGE RIPPLE CONTROL

Based on the real-time dc-link voltage ripple prediction method, the VSFPWM strategy is developed for voltage ripple control in an AFE rectifier. In [22], Zhou and Wang have proved that SVPWM is equivalent to carrier-based PWM essentially, here carrier-based PWM method is adopted for easy application. From Fig. 6(a), PWM signals are generated by comparing

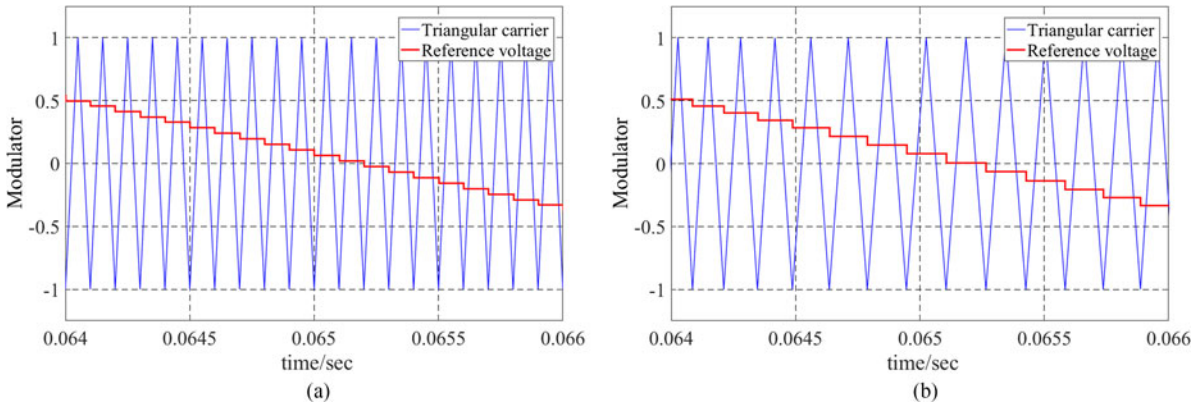

Fig. 6. Carrier and reference in modulator of (a) CSFPWM and (b) VSFPWM.

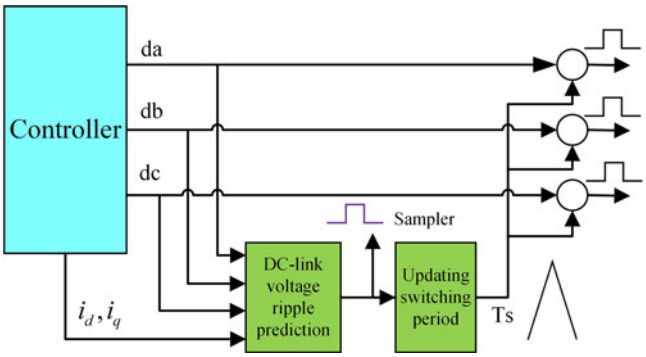

Fig. 7. VSFPWM control diagram.

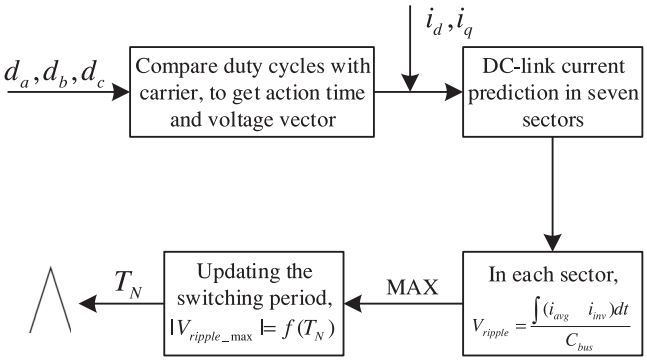

Fig. 8. Voltage ripple prediction diagram.

duty cycles with the triangular carrier in CSFPWM. Since the switching cycle is constant, the sampled reference voltage is also with constant frequency. When applying VSFPWM in the modulator, the carrier triangles are with variable cycles and the sampled reference voltage is also synchronous with the triangular carrier, as shown in Fig. 6(b). Then, the PWM signals generated in modulator in Fig. 6(b) will also be with variable cycles.

Fig. 7 shows the VSFPWM control diagram, mainly including dc-link voltage ripple prediction module and switching period updating module. In each interrupt cycle, the prediction module reads three-phase duty cycle and load current from the controller after receiving a sampling signal. Based on the dc-link voltage ripple prediction method, the locus of dc-link voltage ripple can be achieved. In the switching period updating module, the voltage ripple peak can be controlled equal to the requirement in the way of adjusting the slope of triangular carrier. A sampling signal will be generated when an integrated updating carrier waveform has been sent to the controller, and the next control cycle is coming.

Fig. 8 gives the voltage ripple prediction process in detail. The duty cycles in three phases and the *d-q* axis current in the controller are sent to the prediction diagram to estimate the dc-link voltage ripple V_{ripple} in (4) with nominal switching cycle T_{N0}. With the predicted maximum voltage ripple ($V_{\mathrm{ripple\_max}}$) of one switching cycle, the updating switching period T_{N} can be calculated and acts by the means of controlling the slope of updating triangular carrier. In that way, the actual dc-link voltage ripple in this switching cycle will be exactly equal to the required dc-link voltage ripple. By continuously doing that, the dc-link voltage ripple will be controlled equally with the required value with variable T_N.

In order to study the proposed strategy, VSFPWM and CSFPWM have been, respectively, carried out with the target of dc-link voltage ripple peak in MATLAB/Simulink. With the simulation parameters given in Section II, the requirement of voltage ripple is sure to be ±5.5 V. Fig. 9 shows the dc-link voltage ripple comparison of VSFPWM and CSFPWM, both of them can still be controlled within the identical limitation (±5.5 V). Comparing with the voltage ripple of CSFPWM, VSFPWM can reach the requirement almost in every switching cycle. It means that the switching frequency is decreased in the area, where the voltage ripple peak for CSFPWM is lower than the requirement.

Fig. 10 shows the comparison of switching frequency. Comparing with the classical CSFPWM whose switching frequency is always a constant (10 kHz), switching frequency of VSFPWM varies between 6.1 and 10 kHz resulting in ∼23% average switching frequency reduction. With the similar ac-side current and dc-link voltage, the reduction of average switching frequency directly brings the lower switching losses.

For a two-level rectifier, each switching loss can be calculated in (5). The device voltage is fixed to dc-link voltage and instant current value is set as sinusoidal waveform. Considering the

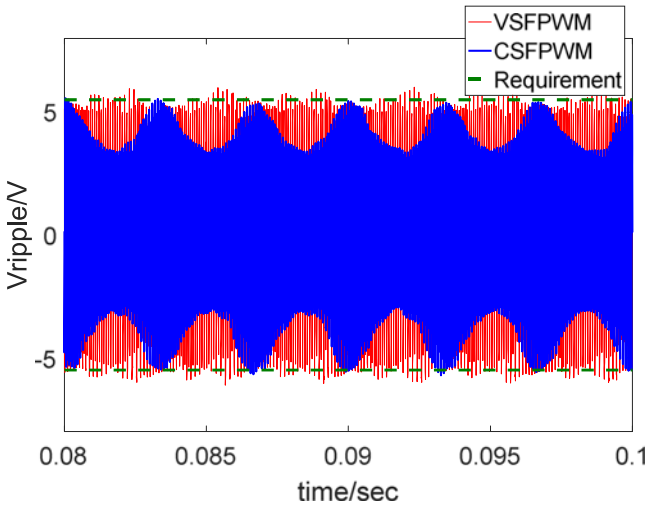

Fig. 9. DC-link voltage ripple comparison.

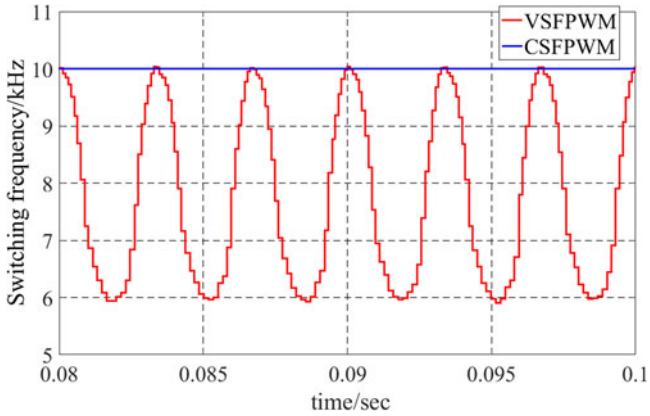

Fig. 10. Switching frequency comparison.

switching frequency and the output fundamental frequency, a whole line cycle can be divided into N switching cycles. With SVPWM, there are two commutations for each phase in one switching cycle. Combining switching instant current value and the switching cycles determined by PWM strategy, a switching losses parameter is defined in (6) over a whole period [16]. Thus, the switching loss saving obtained by VSFPWM can be calculated as (7). Add the phase-a sampling current of each switching cycle within a whole line cycle and then put them into (7). Comparing with conventional CSFPWM, 21.6% reduction of switching losses is achieved by VSFPWM in this case

$$P_{\mathrm{sw,loss}}(\theta) = K \cdot V_{\mathrm{dc}} \cdot i(\theta, \varphi) \tag{5}$$

$$E_{\mathrm{sw}} = \sum_{a,b,c} \sum_{k=1}^{N} |i(t_k)| \cdot e_{\mathrm{unit}} \tag{6}$$

$$\begin{aligned} \text{Loss Saving} &= \left(1 - \frac{E_{\mathrm{sw,VSFPWM}}}{E_{\mathrm{sw,CSFPWM}}}\right) \cdot 100\% \\ &= \left(1 - \frac{\sum_{k=1}^{N1} |i(t_k)|}{\sum_{k=1}^{N2} |i(t_k)|}\right) \cdot 100\% \end{aligned} \tag{7}$$

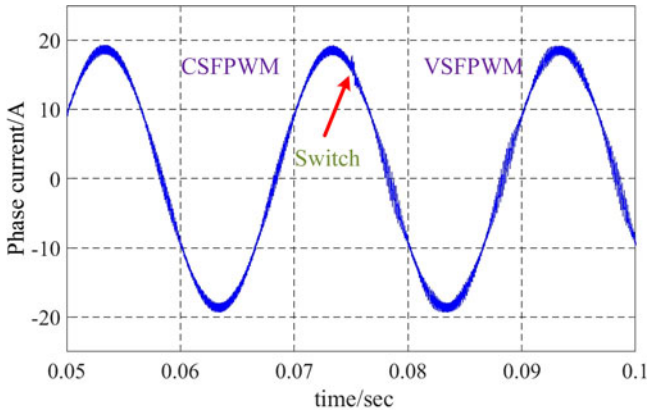

Fig. 11. AC-side current.

where K is the switching transition times, V_{dc} is the dc-link voltage, i is the load current related to phase angle (θ) and load angle (φ), $i(t_k)$ is kth switching instant current value, and e_{unit} represents the switching losses with unit ac-side current for one phase per switching cycle.

Note that the rms current for different PWM methods on the dc-link capacitor is basically the same (7.1 A), which validates the result proposed in literature [23]. It means that the VSFPWM strategy has no obvious harm to the rms current value stress on the dc-link capacitor. On the ac side, the phase current smoothly turns into VSFPWM control from CSFPWM as shown in Fig. 11. The total harmonic distortion of ac-side current rises from 3.31% to 4.89%, getting a little worse by the decrease of average switching frequency. This is a tradeoff between average switching frequency and rms value of the ac-side output current ripple [16].

Due to the variation of switching frequency, both the ac-side current and the dc-link current for VSFPWM get a much wider distribution in the frequency domain. As shown in Fig. 12, harmonic current peak value for CSFPWM has been dramatically reduced with VSFPWM control. Thus, the conductive EMI can be effectively improved with VSFPWM, especially in the dc-link.

Meanwhile, in order to compare the dynamic property, 30 V step change is carried out for two types of PWM methods and the PWM module switches from CSFPWM to VSFPWM at 0.35 s. The voltage ripple limitation for VSFPWM is always kept to ± 3.5 V in the whole process. In Fig. 13(a), it can be found that both of them have the similar dynamic response speed, and the voltage ripple of CSFPWM presents the zigzag appearance around the reference voltage. For CSFPWM with 10 kHz switching frequency, the voltage ripple peak increases from 3.5 to 6.8 V since the current difference through the capacitor becomes lager. In fact, 19 kHz switching frequency is needed for CSFPWM to control the voltage ripple within ± 3.5 V when the dc-link voltage is set to 170 V. However, the voltage ripple of VSFPWM is perfectly controlled under the limitation and distributes more homogeneously from the perspective of the envelope. Fig. 13(b) shows the change of switching frequency in VSFPWM, the average switching frequency will ascend or

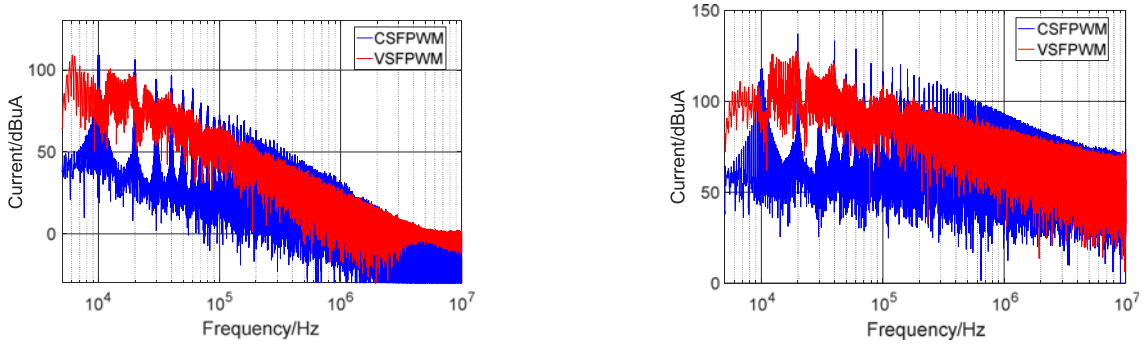

Fig. 12. Spectrum comparison (a) ac side and (2) dc-link.

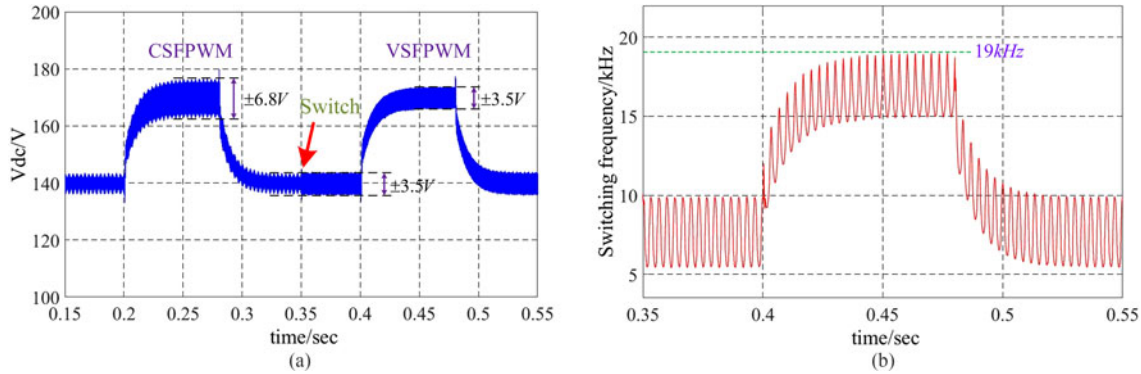

Fig. 13. Step response: (a) step response of dc-link voltage and (b) change of switching frequency with VSFPWM.

descend along with the dc-link voltage reference to meet the requirement of voltage ripple.

IV. Experimental Verification

First, the steady-state performance of VSFPWM strategy is carried out in an AFE rectifier platform with parameters shown in Table I, using a commercial 6MBP20RH060 three-phase converter produced by Fuji connected to filter inductors, and ac power supplied by Pacific Power source. The R&S oscilloscope is used to record the dc-link voltage ripple and the EMI noise is monitored by R&S EMI test receiver. A current probe with the measurement frequency range of 20 Hz–200 MHz is used here to capture the conductive current, and then transfers it to the EMI test receiver though the RF input 50 Ω connector. The physical map of each part of the rectifier system is presented in Fig. 14. In this experiment, the control program is computed based on the digital signal processor (DSP) of TMS320F28335. When the dc-link voltage has achieved the voltage reference with CSFPWM, the control program is turn into VSFPWM strategy. During the implementation process of CSFPWM, a switching frequency of 10 kHz for traditional SVPWM, and the requirement of dc-link voltage ripple can be obtained (±5.5 v) as a control target for the later VSFPWM.

In this case, the switching frequency is stored in the DSP interruption, compared in Fig. 15. The switching frequency of VSFPWM varies from 6 to 10 kHz, always below the selected constant switching frequency. ∼22.5% reduction of the average switching frequency can be achieved with VSFPWM, so the

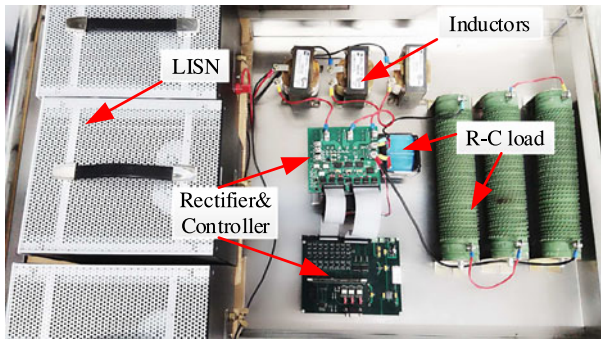

Fig. 14. Picture of experimental setup.

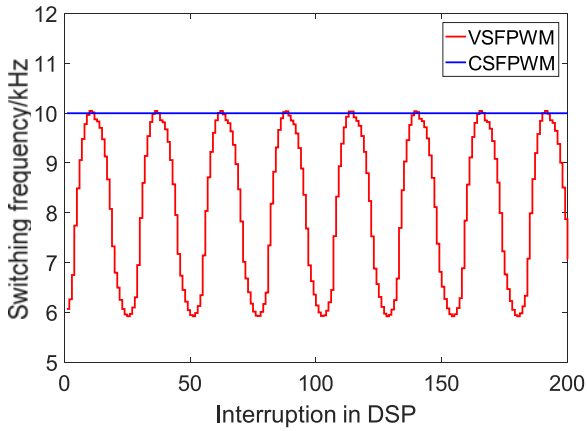

Fig. 15. Experimental result: switching frequency comparison.

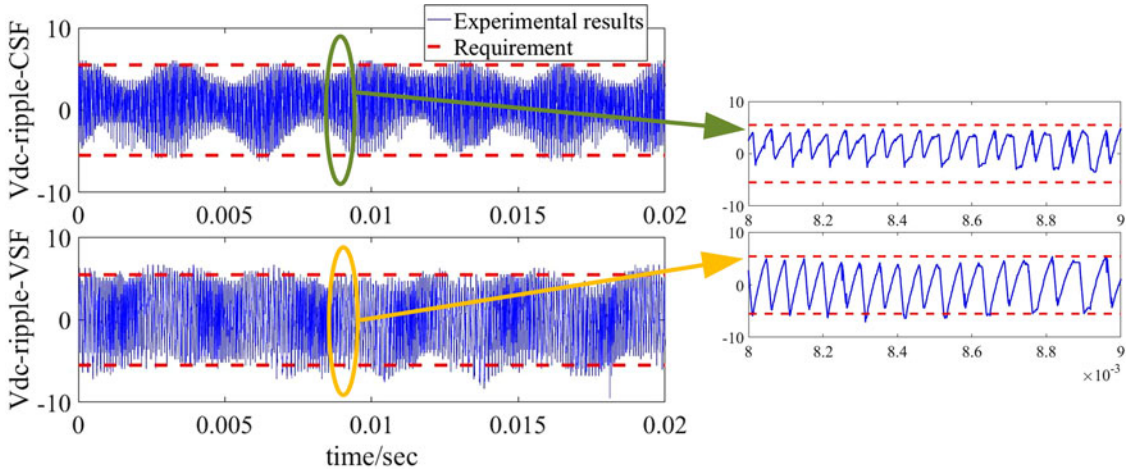

Fig. 16. Experimental result: dc-link voltage ripple comparison.

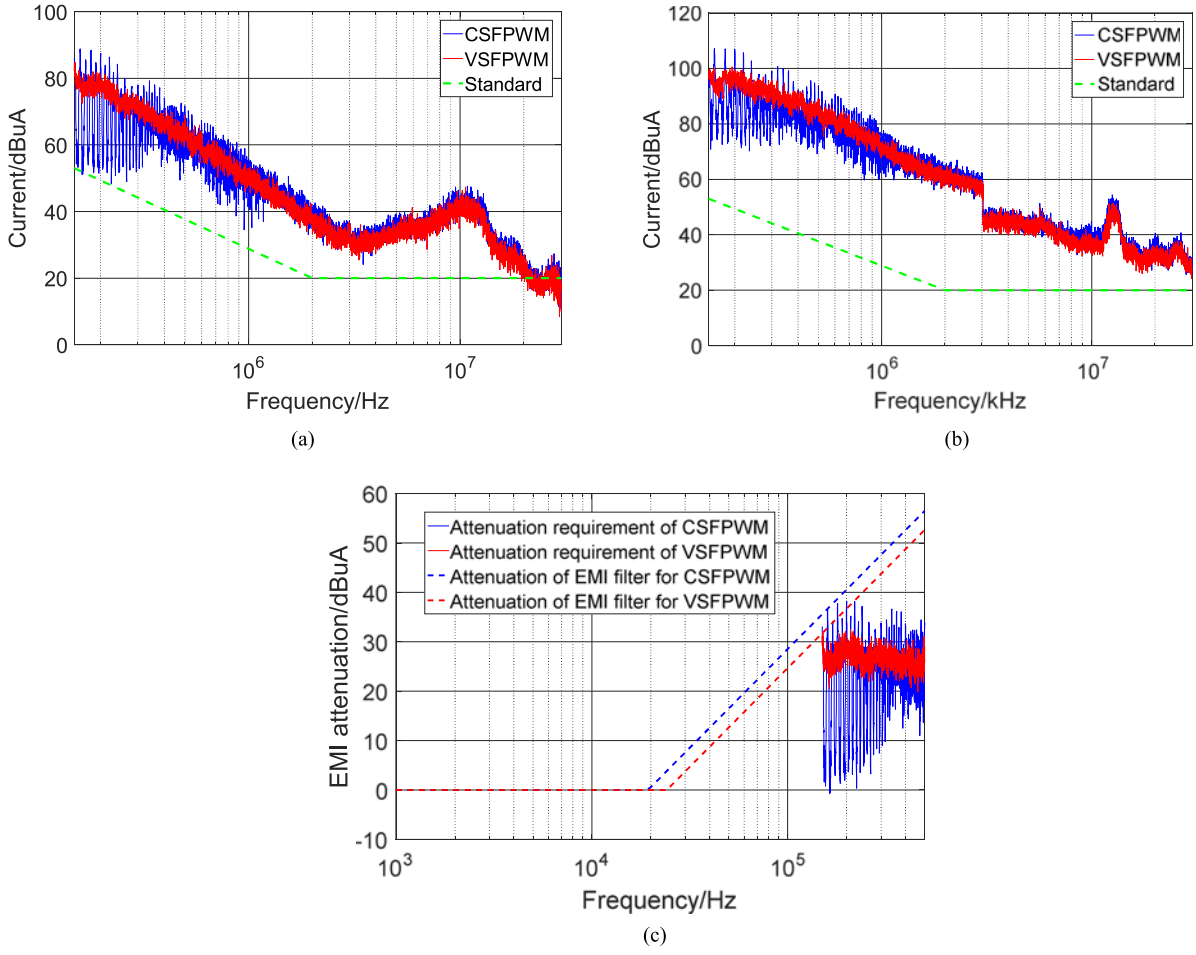

Fig. 17. Experimental results of: (a) measured EMI in ac side, (b) measured EMI in dc side, and (c) EMI attenuation.

switching losses are directly reduced. The comparison of dc-link voltage ripple has been depicted in Fig. 16 as well as enlarged detail view. With respect to CSFPWM, the ripple for VSFPWM is still controlled within the limitation, but nearly covering all areas between the red lines. In this case, the VSFPWM need to take up extra computing time in each interruption, around 2.6 μs.

Since continuously variable switching frequencies are obtained in VSFPWM, the current harmonic of it will not concentrate in the multiple switching frequency shown in CSFPWM. From Fig. 17(a) and (b), the measured EMI of both ac side and dc side can be suppressed with VSFPWM, and a reduction of 10 dB can be seen in the 150 kHz—1 MHz range. There is no obvious advantage of using VSFPWM at higher spectral range

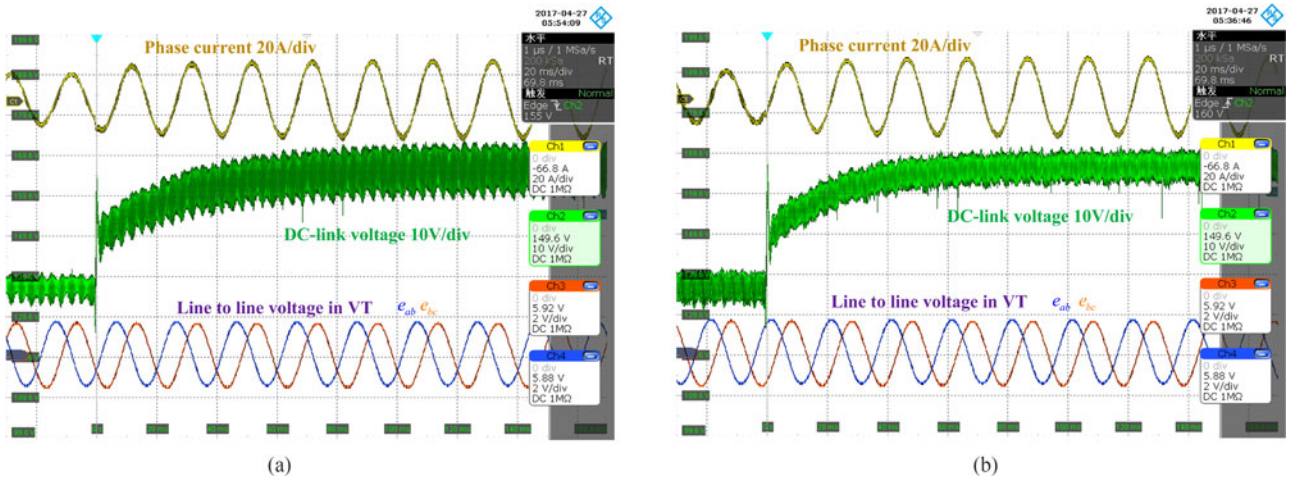

Fig. 18. Experimental results of dynamic state: (a) voltage step-up with CSFPWM and (b) voltage step-up with VSFPWM.

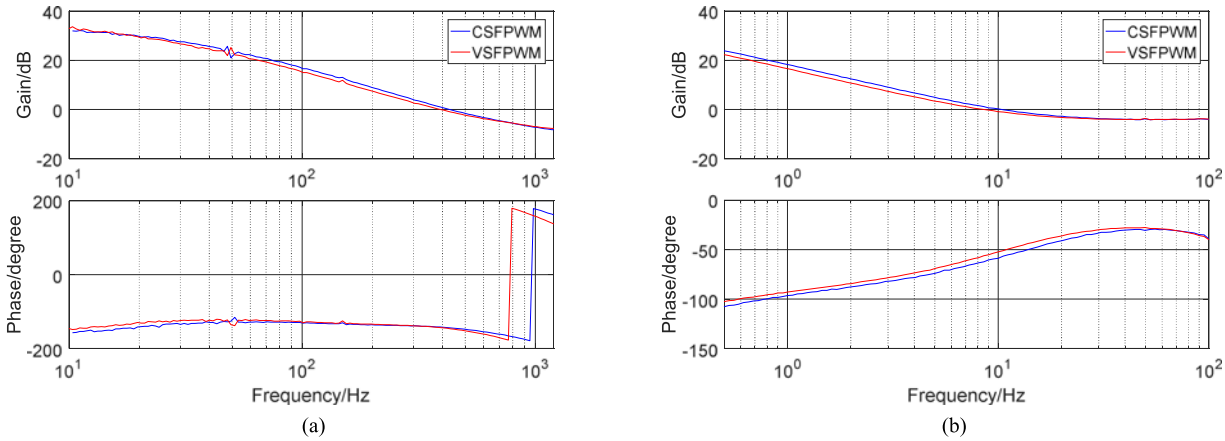

Fig. 19. Experimental results of dynamic state: (a) open-loop Bode plots comparison of the current loop and (b) open-loop Bode plots comparison of the voltage loop.

because of the other nonideal factors. For a passive EMI filter, the corner frequency determines the required capacitance and inductor value [25]. That is, a higher corner frequency makes it possible to use smaller passive component for EMI filter. Considering EMI standard based on DO-160E [26], the corner frequencies of CSFPWM and VSFPWM for ac-side DM EMI are compared in Fig. 17(c) using an ideal one-stage *LC* filter. In this case, the one-stage EMI filter corner frequency has been increased from 19.3 to 24.2 kHz with VSFPWM strategy. Thus, the proposed VSFPWM can help to lower the EMI filter cost and component sizes in a two-level rectifier.

For a better evaluation of the proposed method, the system behaviors under the condition of step change in dc-link voltage have been tested also by using VSFPWM and CSFPWM control, respectively. The line-to-line voltage is set to 130 V, and 30 V step command is applied here. As shown in experimental screenshots, Fig. 18(a) and (b) compares the rectifier behaviors under conditions of step change in dc-link voltage, using CSFPWM and VSFPWM, respectively. As clearly observed, the dynamic response time of VSFPWM behaves similarly with regard to CSFPWM in the time domain. In CSFPWM, when the dc-link reference voltage is step-up changed, the voltage ripple rise rapidly along with the dc-link voltage. In the VSFPWM process, the ripple is always limited in ± 3.5 V, which is the ripple peak value of CSFPWM on 140 V dc-link voltage reference.

Besides, in order to further compare the dynamic behavior of the rectifier system with different PWM method, the dynamic response of each control loop is tested by a frequency response analyzer of PSM1700. The dc-link voltage reference is set to 155 V in the whole process. A small disturbance-sinusoidal-signal varying frequency from 10 Hz to 1 kHz is added to the reference of i_{q} to investigate the current loop first. Then, the closed-loop Bode plot is given from the machine by calculating the ratio of the measured to input i_{q} disturbance. Similarly, the closed-loop Bode plot of outer voltage loop can be achieved with a small disturbance-sinusoidal-signal varying frequency from 1 to 100 Hz. It should be noted that all the disturbance tests are carried out in a normal closed-loop experiment, using the identical PI parameters. For better understanding of the control bandwidth, the open-loop Bode plot is further derived from the closed-loop Bode plots, given in Fig. 19(a) and (b). In theory, the switching frequency is usually associated with the delay of signal sampling and low inertial property of PWM control, so the reduction of switching frequency for VSFPWM will decrease

the bandwidth of control loop. It can be observed that the current loop bandwidth decreases 30 Hz and the voltage loop bandwidth decreases 1.7 Hz slightly.

V. Conclusion

The contribution of this paper is to develop the VSFPWM strategy for dc-link voltage ripple control. Different from the previous work on the ac-side current ripple or torque ripple, the dc-link voltage ripple is nearly not affected by the PWM current ripple of ac side. In a rectifier system, the dc-link voltage ripple is determined by the PWM method and load current, and its peak value is important for dc-link capacitor design or selection. The proposed VSFPWM fully utilizes the freedom of switching frequency, which is often neglected in the PWM module. However, the proposed VSFPWM is different from the random PWM [24], which changes the switching frequency based on the statistics and no prediction model is used. It should be noted that the proposed technique can be applied to a different power factor than the unitary one and not can be applied direct to the rectifier with neutral wire (four wire). Few conclusions can be derived as follows.

1) DC-link voltage ripple prediction model can be built in the time-based-domain. With the three-phase duty cycles, ac-side current, and load current measured by the current sensors, the dc-link voltage ripple peak can be predicted for updating the switching frequency in next cycle. The prediction method also applies to other PWM methods, and also be used for design and analysis of dc capacitors and dc battery reliability.
2) In a whole line period, the switching frequency of VSFPWM continuously varies below the designed constant switching frequency, keeping the dc-link voltage ripple always under the requirement. Using the proposed VSFPWM strategy, the switching losses decrease significantly, and EMI noise reduces markedly.
3) The dynamic property of VSFPWM is first investigated in a typical closed-loop control system. In fact, VSFPWM still has a good dynamic response, without nearly impairing the tracking performance shown in common CSFPWM. The open-loop Bode plot indicates the VSFPWM methods just decrease a little bit of bandwidth of both voltage control loop and the current in CSFPWM because of the reduction of average switching frequency.

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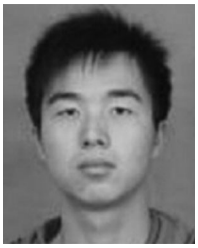

Qiao Li received the B.S. in electrical engineering degree from Huazhong University of Science and Technology, Wuhan, China, in 2015. He is currently working toward the Ph.D. degree in electrical engineering at Huazhong University of Science and Technology, Wuhan.

His research interests include pulse width modulation strategy, converter control, and power hardware-in-the-loop.

Dong Jiang (S'05–M'12—SM'16) received the B.S and M.S degrees in electrical engineering from Tsinghua University, Beijing, China, in 2005 and 2007, respectively. He began Ph.D. study at Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA, in 2007, and was transferred to the University of Tennessee, Knoxville, TN, USA, with his advisor in 2010. He received the Ph.D. degree in electrical engineering from the University of Tennessee, in Dec. 2011.

From Jan. 2012 to Jul. 2015, he was with United Technologies Research Center, Connecticut, as a Senior Research Scientist/Engineer. In Jul. 2015, he joined Huazhong University of Science and Technology, China as a Professor. His major research area is power electronics and motion control, with more than 50 published journal and conference papers and 20 patents/patent applications in this area.

Dr. Jiang is an Associate Editor of IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS. He received two best paper awards from IEEE conferences.