Sine-Reference Band (SRB)-Controlled Average Current Technique for Phase-Cut Dimmable AC–DC Buck LED Lighting Driver Without Electrolytic Capacitor

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***Abstract*—This paper presents a phase-cut dimmable ac–dc buck LED driver for electrolytic capacitor-less LED lighting applications. In the driver, the sine-reference band (SRB)-controlled average current technique is proposed to perform rectified sine-average current control and phase-cut dimming control. The rectified sine-average current control can regulate the average value of sine-wave LED current, maintaining a high power factor (PF) over a wide range of ac input voltage and output LED load. The phase-cut dimming control not only makes the LED driver compatible with two types of phase-cut dimmers, namely, leading-edge and trailing-edge dimming types, but also eliminates visible dimming flicker at the ac line frequency. Fabricated in a 0.35 μm CMOS process, experimental results show the line regulation of $\pm$2.36% over 90 to 260 V_{AC} and the load regulation of $\pm$0.65% within the load range of 10 to 36 LEDs. The PF exceeds 0.95 under all conditions, and the peak efficiency of 90.7% is achieved. The analysis of the flicker frequency verifies that the proposed dimmable LED driver completely eliminates visible flicker owing to the phase dimming variations without an output electrolytic capacitor.**

***Index Terms*—AC–DC, buck LED driver, current regulation, dimming compatibility, electrolytic capacitor (E-Cap), phase-cut dimming control, power factor (PF), rectified sine-average (RSA) current control, visible flicker.**

I. Introduction

With the development of high-power and high-brightness light-emitting diode (LED) technologies, LED lighting systems have been used in various applications, such as indoor and outdoor lighting, display backlighting, automotive lighting and signaling, light therapy, etc. LED lighting systems have gradually replaced the traditional incandescent and fluorescent lighting technologies because of the main benefits of LEDs, which are high efficiency (luminous efficacy of over 100 lm/W), extremely long lifetime (up to 100 000 h), and environmental friendliness (gas- and mercury-free solution) [1]–[4]. An LED light source typically consists of a series connection of single LED cells, which usually require a current of few hundreds milliamps in off-line lighting applications. Since its brightness is proportional to the average conduction current flowing through the series-connected LED string, a driver that controls the LED current is always required to obtain a constant luminous intensity. Among the various topologies of ac-powered off-line LED drivers [5]–[7], a nonisolated buck converter, as shown in Fig. 1, is widely used for the LED current control because of its simplicity and low cost [8]–[15]. However, there are a lot of problems to be solved in the design of a single-stage off-line buck LED driver for LED current control.

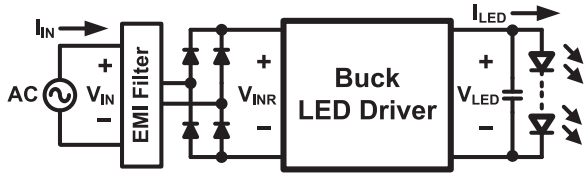

Fig. 1. Buck converter in the LED driving system.

The key issues of the LED current ($I_{\rm LED}$) control method in an ac-powered buck driver are power factor (PF) correction and current regulation [16]–[21]. The conventional dc current control method [8]–[12], which uses a dc supply voltage on a bulky capacitor from the rectified ac input, can easily regulate the average $I_{\rm LED}$ regardless of external conditions, such as the input voltage and the number of LEDs, as shown in Fig. 2(a). The conventional dc current control method, however, cannot avoid a low PF less than 0.5 since the input bulky capacitor results in a large peak input current [20]. Although a two-stage off-line LED driver with a PF correction converter can improve the low PF, the two-stage driver still has critical weak points

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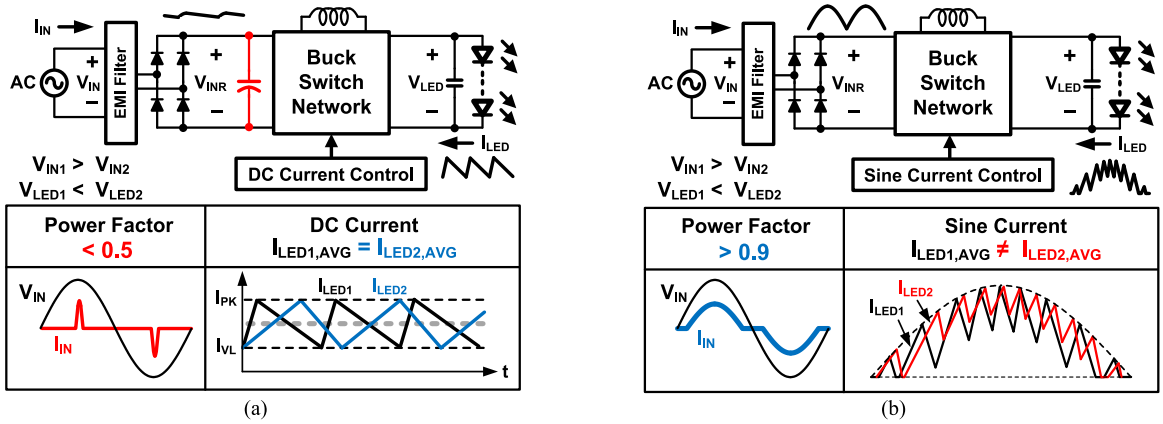

Fig. 2. Conventional LED current control for PF and current regulation. (a) DC current control. (b) Sine current control.

caused by the extra stage, which degrades the power efficiency and cost effectiveness [4], [6], [10].

To achieve a high PF without using an extra stage, a single-stage ac–dc buck LED driver has been recently developed [13]–[15]. In this driver, the sine-peak current control method can significantly improve the PF, raising it to more than 0.9 [13]. This control method generates a sine-wave $I_{\rm LED}$, as shown in Fig. 2(b), directly drawn from the ac input source. Therefore, the conventional sine current control method can perform the PF correction function. However, the average value of the sine output current varies substantially under various input and output conditions because the sine-wave $I_{\rm LED}$ cannot be regulated by the peak current control (PCC) scheme [21]. It can be identified by Fig. 2(b). In this figure, two LED currents ($I_{\rm LED1}$ and $I_{\rm LED2}$), which are obtained under different conditions, have different average values ($I_{\rm LED1,AVG}$ and $I_{\rm LED2,AVG}$), even though the peak levels of $I_{\rm LED1}$ and $I_{\rm LED2}$ are the same. Consequently, the previous current control methods [12]–[15] have a tradeoff between high PF and good current regulation in the single-stage off-line buck LED driver.

Apart from the PF and current regulation for the LED current control, there is another important feature in LED drivers, namely, the dimming technique. Dimming systems, which allow the user to adjust the brightness of light to the desired level, potentially improve energy savings, system lifetime, visual comfort, and productivity at work place [22]. The majority of dimming devices installed today in residential applications are based on phase-cut dimmers [23]. The phase control devices were originally designed for use with incandescent light sources and have a variety of dimming properties for each product [24]–[28]. The dimmers are also widely utilized for flexibility and versatility in the LED lighting system, because the demand for replacing the incandescent lamps with the LED lamps is increasing rapidly and it takes a lot of time and cost to change the previously installed dimmers to other dimming devices [22], [23]. However, serious problems, such as flickering and audible noise could occur when those dimmers are used for driving LEDs. Therefore, a phase dimming control circuit is additionally required to avoid potential issues in the LED dimming operation [24].

Fig. 3(a) describes a phase-cut dimmable ac–dc buck LED lighting system. In this system, there are two main parts, a phase-cut dimmer and a buck LED driver. The phase-cut dimmer determines the energy delivered from an ac power source to the buck LED driver, and the driver adjusts $I_{\rm LED}$ in response to its dimming operation by using a phase dimming control scheme.

The main challenges of phase dimming control in LED lighting systems are the dimming compatibility and the removal of the visible dimming flicker. There are two major types of phase-cut dimmers [25], [26] as shown in Fig. 3(b). The leading-edge dimmer delays the firing angle following the zero point (ZP), cutting out the initial portion of the ac half-cycle (off-time, α) and conducting its end portion (conduction angle, θ). The trailing-edge dimmer operates in the opposite manner, conducting the initial portion of the ac half-cycle and turning off its end portion. When an LED driver is not compatible with both dimming types, the driver cannot work with either of them. Thus, end-users would have the inconvenience of needing to know whether their fixture is controlled by a leading-edge or trailing-edge dimmer, and manufacturers would have unnecessary costs to develop and provide different drivers for two dimming types.

In Fig. 3(c), the principle of the visible light flicker caused by phase-cut dimmers is illustrated [27]. The dimmer has different turn-on thresholds for positive and negative conductions of the ac input ($V_{\rm IN}$). This difference gives rise to phase dimming variations that are defined as the deviations of voltage magnitude (V_+, V_-) and conduction angle (θ_+, θ_-) of the rectified input voltage $V_{\rm INR}$ at the ac line frequency below 60 Hz. The variations result in unbalanced $I_{\rm LED}$, causing the critical problem of visible dimming flicker, especially at low conduction angles [29]. The visible dimming flicker caused by phase dimming variations can be eliminated when an electrolytic capacitor (E-Cap) is used in parallel with the LED string, but use of the E-Cap results in negative effects on lifetime and volume of the LED driver [6], [13], [30], [31].

To resolve all of the problems mentioned above and improve the performance of the LED driver at the same time, a new control scheme: sine-reference band (SRB)-controlled average current technique is proposed in this paper. The proposed control technique can achieve both 1) rectified sine-average (RSA)

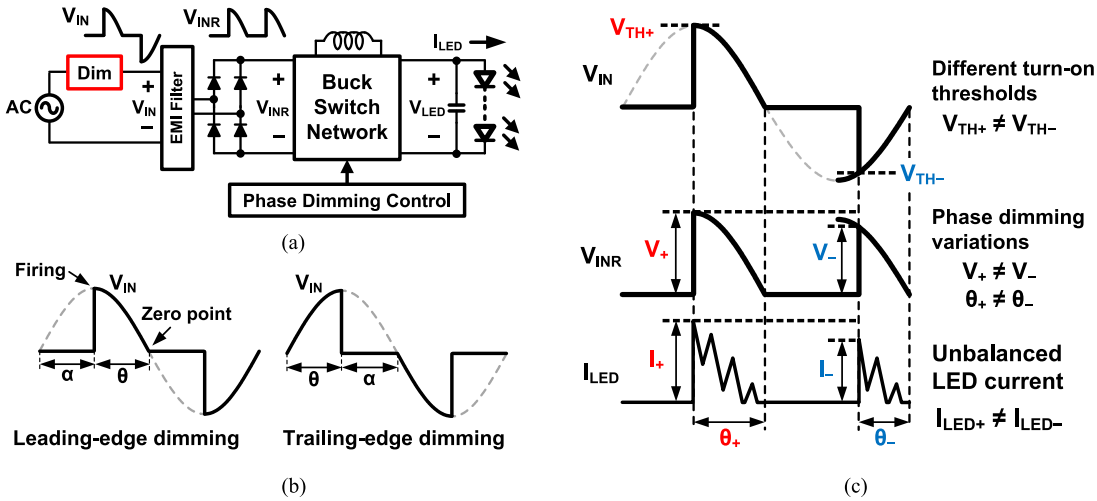

Fig. 3. Phase-cut dimmable buck LED lighting system. (a) Structure with phase dimming control. (b) Two types of phase-cut dimmers. (c) Principle of the visible dimming flicker due to the phase dimming variations at the ac line frequency.

current control to accurately regulate the average value of the sine-wave LED current while maintaining a high PF regardless of external conditions and 2) phase-cut dimming control to not only provide compatibility with two types of phase-cut dimmers but also to eliminate the visible dimming flicker at the ac line frequency without output capacitors. Furthermore, it is possible to achieve compact size and low cost of the LED driver because the proposed driver is designed as a buck LED driver that uses a small number and small size of external components.

This paper is organized as follows. In Section II, the overall architecture, control scheme, and design considerations for the proposed SRB-controlled LED driver are described and discussed. Section III presents the circuit implementations of the SRB-controlled average current technique in detail. Experimental results presented in Section IV demonstrate the performance of the proposed control scheme. Finally, conclusions are given in Section V.

II. Proposed SRB-Controlled LED Driver

A. Overall System Architecture

Fig. 4 shows the overall architecture of the proposed SRB-controlled buck LED driver [32]. There are several parts in the proposed LED driver, namely, the start-up circuit, the dynamic bleeder sensing and control circuit, the power stage, and the proposed SRB-controlled average current controller, which is a key block of the proposed work. When ac power is available at the input, the rectified input voltage $V_{\rm INR}$ on the ac line can be represented as

$$V_{\rm INR}(\Phi) = V_{\rm INR,PK} \cdot \sin\Phi \tag{1}$$

where $V_{\rm INR,PK}$ is the peak voltage of $V_{\rm INR}$, and the phase $\Phi = \omega_{\rm AC} \times t$ changes periodically from 0 to π [rad].

To make the driver start its operation, the operating voltage ($V_{\rm CC}$) of the driver should be supplied. The $V_{\rm CC}$ can be supplied by the $V_{\rm INR}$ by using the external start-up circuit [33]. The start-up circuit consists of a high-voltage MOSFET ($M_{\rm HV}$), a resistor, and a zener diode. The zener diode, which is biased by the resistor, sets the gate voltage of $M_{\rm HV}$ to V_Z, and $M_{\rm HV}$ supplies current to charge up the capacitor $C_{\rm VCC}$ through the diode. As a result, $V_{\rm CC}$ is approximately equal to the source voltage of $M_{\rm HV}$ minus the diode forward voltage ($V_{\rm CC} = V_{\rm Z} - V_{\rm GS,HV} - V_{\rm F}$), which is less than the maximum voltage rating of the driver from $V_{\rm INR}$. Once $V_{\rm CC}$ becomes greater than the starting threshold voltage, the driver eventually starts the operation to control $I_{\rm LED}$.

The phase-cut dimmer needs two minimum levels of input current to be flowing through it: the latching current ($I_{\rm LAT}$) at firing and the holding current ($I_{\rm HLD}$) during the conduction angle after firing [24], [26]. If those current requirements are not met, the input voltage of the driver is seriously distorted due to the abnormal operation of the dimmer. The dynamic bleeder sensing and control circuit in the driver draws extra input current to ensure the $I_{\rm LAT}$ and $I_{\rm HLD}$ requirements when $I_{\rm LED}$ is not enough [28], [34]. In Fig. 4, $I_{\rm LAT}$ is determined to be $(V_{\rm CC} + V_F)/(R_{\rm LAT} + R_B)$ when the bleeder MOSFET M_B is fully turned ON. On the other hand, $I_{\rm HLD}$ is regulated to be $(R_{\rm SEN} \times I_{\rm SEN})/R_{\rm HLD}$ by controlling the gate voltage of M_B. This regulation point, which is adjustable by using the external resistor $R_{\rm HLD}$, is the threshold value of the minimum $I_{\rm HLD}$. Hence, the dynamic bleeder control circuit quickly stops drawing $I_{\rm HLD}$ from the input when the input current flowing into the LED load is above the threshold value by sensing the current across $R_{\rm HLD}$. This approach reduces the extra power dissipation by the holding current to be minimized.

The power stage adopts the floating buck (also called inverted buck) topology [8]–[14] with a high-side freewheeling diode ($D_{\rm FW}$) and a low-side power MOSFET (M_N). When M_N is turned ON, $I_{\rm LED}$ flows through the inductor toward the current sensing resistor $R_{\rm CS}$ connected between M_N and ground. During the on-time, $I_{\rm LED}$ linearly increases with the slope of $(V_{\rm INR}(\Phi) - V_{\rm LED})/L$, where $V_{\rm LED}$ is the total forward voltage of the LEDs, and L is the inductance used in the power stage. To obtain the information of the current passing through the LEDs,

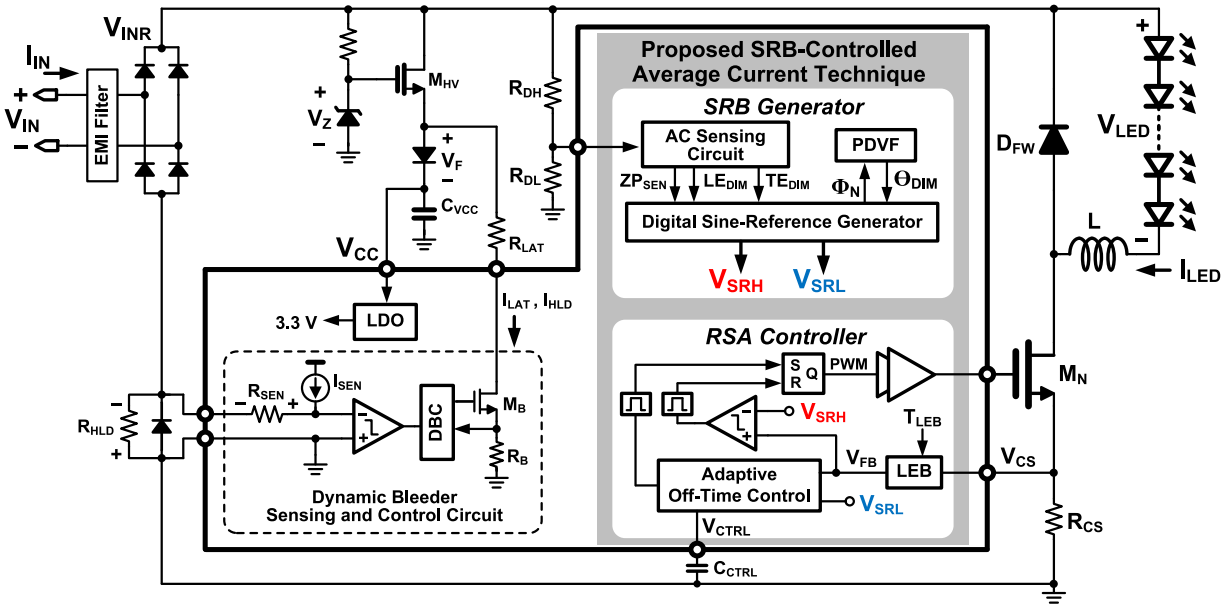

Fig. 4. Overall system architecture of the proposed SRB-controlled LED driver.

the sensed voltage $V_{\rm CS}$ is fed back to the controller. When M_N is turned OFF, on the other hand, $I_{\rm LED}$ is circulated through $D_{\rm FW}$. During the off-time, $I_{\rm LED}$ is discharged with the slope of $(-V_{\rm LED})/L$, and its current cannot be sensed.

The integrated on-chip LED controller, which implements the proposed SRB-controlled average current technique, controls the switching operation mentioned above to achieve both the RSA current control and the phase-cut dimming control. This controller is explained in detail in part B of this section. Owing to this proposed controller, the LED driver can accurately regulate the phase-cut dimmable $I_{\rm LED}$ and completely remove the visible dimming flicker at the ac line frequency without using any output capacitor, which could be a great advantage from the viewpoint of cost. In addition, the proposed LED driver can avoid the lifetime shortening and volume increasing caused by a bulky capacitor because it does not use an E-Cap of several hundred μF at the output terminal [6]. Even though the visible flicker is removed by the proposed LED controller, the invisible flicker at twice the ac line frequency (100 or 120 Hz) still exists due the fact that there is no capacitor. However, this invisible flicker could be tolerated in most case because its flicker at the twice the ac line frequency is not perceivable by a human viewer [13], [29].

B. SRB-Controlled Average Current Technique

The proposed control system of the SRB-controlled average current technique is composed of two parts, the SRB generator and the RSA controller, as shown in Fig. 4. The phase-cut dimmable SRB generator only receives a signal from an external resistor divider ($R_{\rm DH}$ and $R_{\rm DL}$) to scale down $V_{\rm INR}$, and it generates two sine-reference voltages, $V_{\rm SRH}$ and $V_{\rm SRL}$, as the SRB signal (see Fig. 5). The RSA controller regulates $I_{\rm LED}$ as the middle value of the sine current window generated by $V_{\rm SRH}$ and $V_{\rm SRL}$, as illustrated in Fig. 6.

In the SRB generator, the ac sensing circuit detects the dimming type and ZP of the ac input by sensing the slope of $V_{\rm INR}$ based on the zero-crossing detection. According to the $V_{\rm INR}$ waveform, three dimming modes exist: nondimming (nonDIM), leading-edge dimming (LEDIM), and trailing-edge dimming (TEDIM), as shown in Fig. 5. Considering the derivative of $V_{\rm INR}$ with respect to phase at $V_{\rm INR} \approx 0$ V in Fig. 5, the nonDIM mode has $dV_{\rm INR}/{\rm d}\Phi = \pm m$ V/rad, where $m \leq V_{\rm INR,PK}$. This means that $V_{\rm INR}$ changes slowly at the ZP. In contrast, the dimming points of the leading-edge and trailing-edge are ideally $dV_{\rm INR}/d\Phi = +\infty$V/rad and $dV_{\rm INR}/d\Phi = -\infty$V/rad, respectively. In this way, the ac input slope sensing at the $V_{\rm INR} \approx 0$ V can distinguish each of the dimming modes. The digital sine-reference generator processes one cycle time of the ZP, denoted by $T_{\rm ZP}$, to obtain the sine-wave phase Φ from 0 to π [rad], and then creates the SRB signals using the predefined pattern table for the sine-wave [see Fig. 5(a)]:

$$
\begin{aligned}
0 \leq \Phi &= \left(\frac{\pi}{T_{\rm ZP}}\right) \cdot t \leq \pi \\
V_{\rm SRH}(\Phi) &= V_{\rm SRH,PK} \cdot \sin\Phi \\
V_{\rm SRL}(\Phi) &= V_{\rm SRH}(\Phi) - \Delta V_G \geq 0
\end{aligned} \tag{2}
$$

where $V_{\rm SRH,PK}$ and ΔV_G are the peak voltage of $V_{\rm SRH}$ and the voltage gap between $V_{\rm SRH}$ and $V_{\rm SRL}$, respectively. These values are fixed in the pattern table. Therefore, the SRB signals are generated in phase with the ac input, but they are independent from its magnitude. If the driver is on dimming operation, it is necessary to apply the conduction angle of the ac input to the sine-reference generation. In the process, the phase dimming variation filter (PDVF) generates the steady dimming angle $\Theta_{\rm DIM}$ (from $\Phi_{\rm A}$ to $\Phi_{\rm B}$) for the SRB waveform so that the phase-cut dimmable SRB signals remain unchanged completely

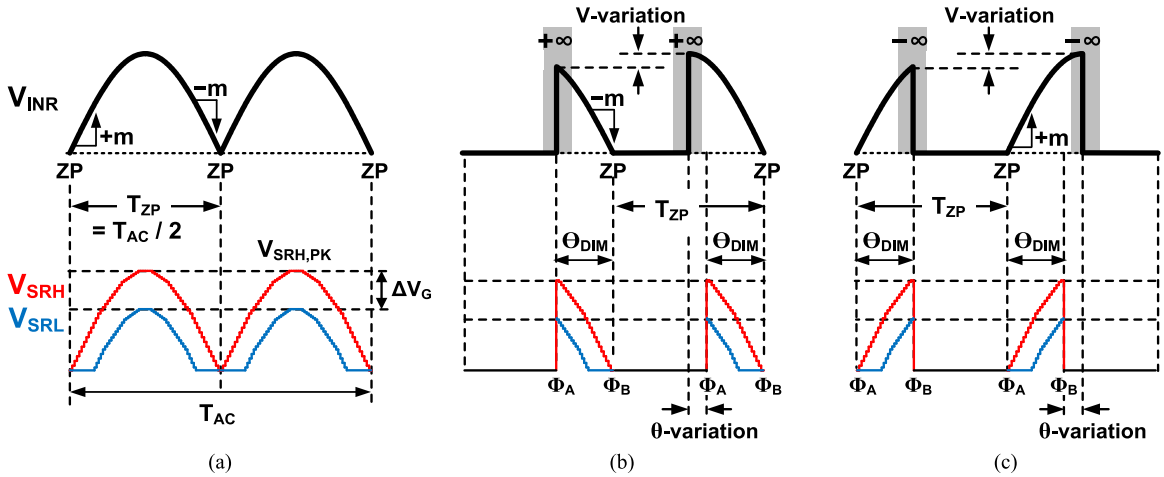

Fig. 5. SRB generator. (a) Non-DIM. (b) LEDIM. (c) TEDIM.

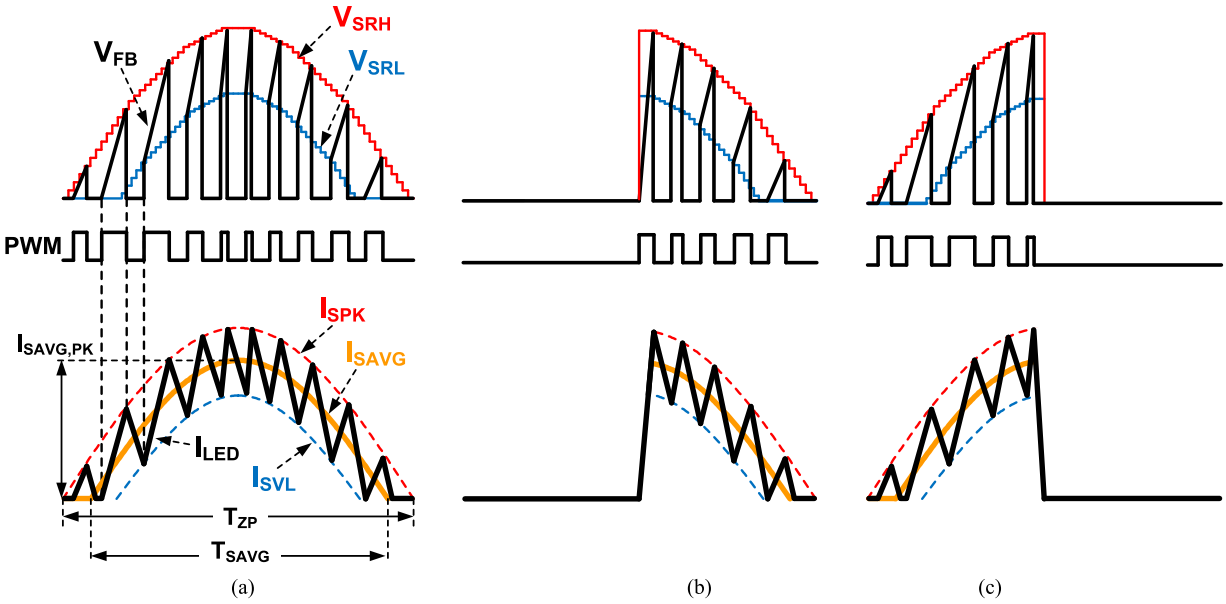

Fig. 6. RSA controller. (a) Non-DIM mode. (b) LEDIM mode. (c) TEDIM mode.

in spite of the phase dimming variations, as shown in Fig. 5(b) and (c).

The RSA controller regulates the peak level ($I_{\rm SPK}$) and valley level ($I_{\rm SVL}$) of $I_{\rm LED}$ to let the shape of $I_{\rm LED}$ be identical to the SRB waveform, as shown in Fig. 6. Here, $I_{\rm SPK}$ is regulated by the PCC method, and $I_{\rm SVL}$ is adjusted by the proposed adaptive off-time control (AOTC) method. When M_N is turned ON, the feedback voltage $V_{\rm FB}$ shown in Fig. 4 appears after the leading-edge blanking time ($T_{\rm LEB}$) to filter out the switching current spike noise on $R_{\rm CS}$. In the PCC, $V_{\rm FB}$ is compared with $V_{\rm SRH}$ to turn M_N OFF. At this moment, the rectified sine-peak current $I_{\rm SPK}$ is defined as

$$I_{\rm SPK}(\Phi) = \frac{V_{\rm SRH}(\Phi)}{R_{\rm CS}}. \tag{3}$$

For the valley LED current $I_{\rm SVL}$, the duration of the pulse width modulation (PWM) off-time needs to be adaptively controlled since the $I_{\rm LED}$ information is not available from $V_{\rm FB}$ during the off-time [8]–[10]. The AOTC automatically adjusts the PWM off-time depending on the control voltage $V_{\rm CTRL}$ so as to regulate $I_{\rm SVL}$, which will be explained in detail in Section III-D. According to this sequence, $I_{\rm SVL}$ is regulated to the following desired value:

$$I_{\rm SVL}(\Phi) = \frac{V_{\rm SRL}(\Phi)}{R_{\rm CS}}. \tag{4}$$

After the off-time duration, PWM is set to logic high, and then M_N is turned ON again. From (3) and (4), the RSA LED current $I_{\rm SAVG}$ is represented as [see Fig. 6(a)]

$$I_{\rm SAVG}(\Phi) = \frac{I_{\rm SPK}(\Phi) + I_{\rm SVL}(\Phi)}{2} = \frac{1}{2}\left(\frac{V_{\rm SRH}(\Phi) + V_{\rm SRL}(\Phi)}{R_{\rm CS}}\right). \tag{5}$$

This implies that the waveform and value of I_{SAVG} are determined by the SRB signals as illustrated in Fig. 6. That is, I_{SAVG} can be regulated to the constant sine-wave in phase with the ac input, regardless of external conditions and variations, related to input voltage, LED load, and phase-cut dimming. The regulated average value of the LED current $I_{\mathrm{LED,AVG}}$ can be expressed mathematically as

$$I_{\mathrm{LED,AVG}} = \left(\frac{1}{\pi}\int_0^{\pi} I_{\mathrm{SAVG}}(\Phi)\cdot d\Phi\right)\cdot\left(\frac{T_{\mathrm{SAVG}}}{T_{\mathrm{ZP}}}\right) = \left(\frac{2}{\pi}I_{\mathrm{SAVG,PK}}\right)\cdot\left(\frac{T_{\mathrm{SAVG}}}{T_{\mathrm{ZP}}}\right) \tag{6}$$

where $I_{\mathrm{SAVG,PK}}$ is the peak value of I_{SAVG}, and T_{SAVG} is equivalent to one cycle time of I_{SAVG} from 0 to π [rad]. Therefore, the RSA current control of the proposed LED driver can simultaneously achieve excellent current regulation and a high PF over a wide range of ac input voltage V_{IN} and the number of output LEDs. In addition, the SRB-controlled dimmable driver including the phase-cut dimming control is compatible with the different types of dimmers and enables the dimming current to be controlled uniformly without an output capacitor.

Fig. 7 shows the zoomed-in waveforms of PWM at the same phase point under different input line voltages (V_{INR1}, V_{INR2}) and LED load voltages (V_{LED1}, V_{LED2}). The on-time (T_{ON}) and the off-time (T_{OFF}) of PWM for the proposed SRB-controlled LED driver are, respectively, given by

$$T_{\mathrm{ON}}(\Phi) = \frac{L\cdot\Delta I_R}{V_{\mathrm{INR}}(\Phi) - V_{\mathrm{LED}}} \tag{7}$$

$$T_{\mathrm{OFF}} = \frac{L\cdot\Delta I_R}{V_{\mathrm{LED}}} \tag{8}$$

where

$$\Delta I_R = I_{\mathrm{SPK}}(\Phi) - I_{\mathrm{SVL}}(\Phi) = \frac{\Delta V_G}{R_{\mathrm{CS}}}. \tag{9}$$

Note that the ripple current of I_{LED} (ΔI_R), which is determined by ΔV_G, is held constant. Given $V_{\mathrm{INR1}}(\Phi) \neq V_{\mathrm{INR2}}(\Phi)$ in Fig. 7(a), the PCC still maintains the level of I_{SPK}, and yet it inevitably results in the variable T_{ON} from (7). Similarly, if $V_{\mathrm{LED1}} \neq V_{\mathrm{LED2}}$, as shown in Fig. 7(b), the AOTC adjusts T_{OFF} correspondingly to (8), and the regulation of I_{SVL} is guaranteed. Consequently, both T_{ON} and T_{OFF} are essentially controlled for the line and load regulations, while ΔI_R is kept constant.

C. Design Considerations for Current Ripple and Power Loss

The ripple current of I_{LED}, ΔI_R, has a great influence on the switching frequency and the power losses in the driver design. In the proposed control method, the LED current ripple ratio (CRR) is defined as

$$\mathrm{CRR} = \frac{\Delta I_R}{I_{\mathrm{SAVG,PK}}} = \frac{\Delta V_G}{V_{\mathrm{SRH,PK}} - \Delta V_G/2}. \tag{10}$$

The value of the CRR can be kept constant by the SRB. Therefore, the SRB generation should be designed to reflect the CRR considered in relation to the switching frequency and the power losses.

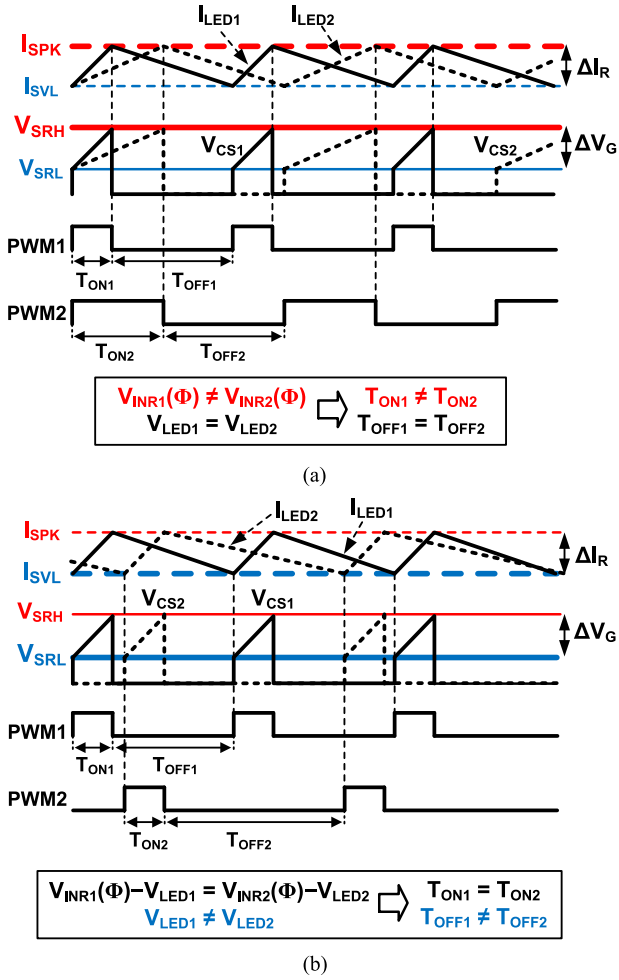

Fig. 7. Zoomed-in waveforms for the current regulation and PWM. (a) Rectified sine-peak current regulation and PWM on-time under different input line voltages. (b) Rectified sine-valley current regulation and PWM off-time under different output load voltages.

The instantaneous switching frequency varies in the sine-wave phase because T_{ON} is a function of the phase Φ, as expressed in (7) (see Fig. 6). For this reason, the average switching frequency $f_{\mathrm{SW,AVG}}$ is more suitable to find out the relation between the current ripple and the switching frequency. From (7) and (8), $f_{\mathrm{SW,AVG}}$ is approximately calculated as

$$f_{\mathrm{SW,AVG}} = \frac{1}{\pi}\int_0^{\pi}\frac{1}{T_{\mathrm{ON}}(\Phi)+T_{\mathrm{OFF}}}d\Phi = \frac{V_{\mathrm{LED}}}{L\cdot\Delta I_R}\left(1-\frac{1}{\pi}\int_0^{\pi}\frac{V_{\mathrm{LED}}}{V_{\mathrm{INR}}(\Phi)}d\Phi\right) \approx \frac{V_{\mathrm{LED}}\,(1-D_{\mathrm{AVG}})}{L\cdot\Delta I_R} \tag{11}$$

where D_{AVG} is the approximate value of the average duty ratio and it is equal to

$$D_{\mathrm{AVG}} = \frac{V_{\mathrm{LED}}}{V_{\mathrm{INR,AVG}}} = \frac{V_{\mathrm{LED}}}{2/\pi\cdot V_{\mathrm{INR,PK}}}. \tag{12}$$

Thus, $f_{\mathrm{SW,AVG}}$ is inversely proportional to ΔI_R.

To analyze the power losses associated with the CRR, two major power losses caused by operation of the MOSFET M_N, which are the switching and conduction losses, are taken into account in the proposed LED driver. The power losses of the freewheeling diode D_{FW} are negligible, because the diode conduction and reverse-recovery switching losses for changes of CRR are small and constant compared with the power losses of M_N. The switching loss P_{SW} is dissipated at the drain node of M_N, and P_{SW} is given as

$$\begin{aligned} P_{\mathrm{SW}} &= \frac{1}{2} C_{\mathrm{OSS}} V_D^2 f_{\mathrm{SW}} \\ &\approx \frac{1}{2} C_{\mathrm{OSS}} \left(\frac{1}{\pi} \int_0^{\pi} V_{\mathrm{INR}}^2(\Phi) d\Phi \right) f_{\mathrm{SW,AVG}} \\ &= \frac{1}{4} C_{\mathrm{OSS}} V_{\mathrm{INR,PK}}^2 f_{\mathrm{SW,AVG}} \end{aligned} \tag{13}$$

where C_{OSS} and V_D are the output capacitance and drain voltage of M_N, respectively. Substituting (10) and (11) into (13), P_{SW} can also be expressed as

$$P_{\mathrm{SW}} = \frac{C_{\mathrm{OSS}} V_{\mathrm{INR,PK}}^2 V_{\mathrm{LED}} \left(1 - D_{\mathrm{AVG}}\right)}{4L \cdot I_{\mathrm{SAVG,PK}}} \cdot \frac{1}{\mathrm{CRR}}. \tag{14}$$

The conduction loss P_C that is power dissipated by resistors is calculated to

$$\begin{aligned} P_C &\approx D_{\mathrm{AVG}} I_{\mathrm{LED,RMS}}^2 \cdot (R_{\mathrm{ON}} + R_{\mathrm{CS}}) \\ &= D_{\mathrm{AVG}} \left(\frac{I_{\mathrm{SAVG,PK}}^2}{2} + \frac{1}{3} \cdot \frac{\Delta I_R^2}{4} \right) \cdot (R_{\mathrm{ON}} + R_{\mathrm{CS}}) \\ &= \frac{D_{\mathrm{AVG}} I_{\mathrm{SAVG,PK}}^2 \left(R_{\mathrm{ON}} + R_{\mathrm{CS}}\right)}{12} (6 + \mathrm{CRR}^2) \end{aligned} \tag{15}$$

where $I_{\mathrm{LED,RMS}}$ and R_{ON} are the rms value of the LED current and equivalent on-resistance of M_N, respectively. According to (14) and (15), a small CRR increases P_{SW}, whereas it reduces P_C. In contrast, a large CRR results in decrement of P_{SW}, but it increases P_C. Thus, the value of the CRR should be optimized to minimize the total power loss P_T $(= P_{\mathrm{SW}} + P_C)$ in the tradeoff between P_{SW} and P_C.

Fig. 8 plots the power losses that result from variation of CRR at 110 and 220 $\mathrm{V_{AC}}$. To verify (14) and (15), the calculated outputs are compared with the simulation results, using $C_{\mathrm{OSS}} = 100\,\mathrm{pF}$, $L = 3.3\,\mathrm{mH}$, $V_{\mathrm{LED}} = 40\,\mathrm{V}$, $I_{\mathrm{SAVG,PK}} = 400\,\mathrm{mA}$, $R_{\mathrm{ON}} = 5\,\Omega$, and $R_{\mathrm{CS}} = 2.5\,\Omega$. Furthermore, it demonstrates that the P_C is dominant at 110 $\mathrm{V_{AC}}$ [see Fig. 8(a)], while P_{SW} is dominant at 220 $\mathrm{V_{AC}}$ [see Fig. 8(b)]. In other words, the effect of P_{SW} on P_T becomes greater than P_C as V_{IN} increases. To ensure that the LED driver has a small current ripple with little power loss, one of the CRR points at which P_T is insensitive to the current ripple over a wide input voltage ranges should be determined as the optimized value. As a result, the designed point of the CRR is 0.4, as shown in Fig. 9, and its value can also be used to determine ΔV_G in (10).

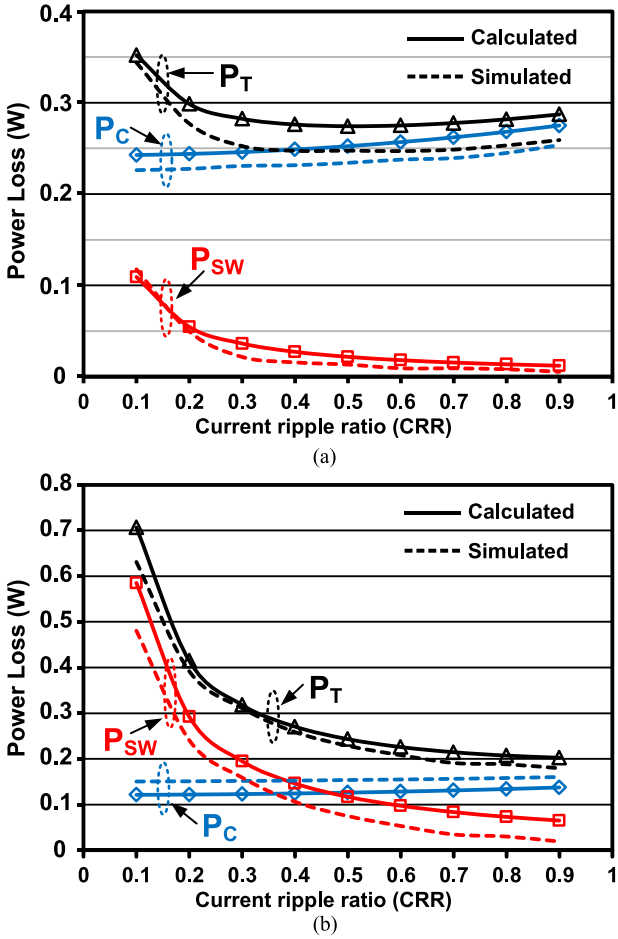

Fig. 8. Relation between the CRR and power loss. (a) 110 $\mathrm{V_{AC}}$. (b) 220 $\mathrm{V_{AC}}$.

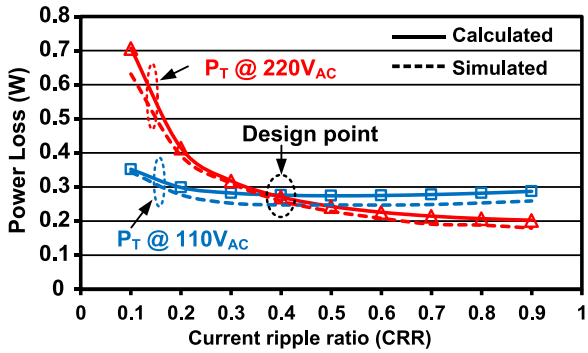

Fig. 9. Design point of the CRR when considering power losses over a wide input voltage range.

III. Circuit Implementations

A. AC Sensing Circuit

Fig. 10 shows the ac sensing circuit and its operating waveforms by each dimming mode. For two levels of zero-crossing detection, two comparators generate ZCL and ZCH from the reference voltages, V_{ZCD} and $2V_{\mathrm{ZCD}}$, respectively. Then, the filtered output of the XOR gate, ZCX, indicates that the V_{INR} slope is either steep or not at around $V_{\mathrm{INR}} = 0\,\mathrm{V}$. The rising and

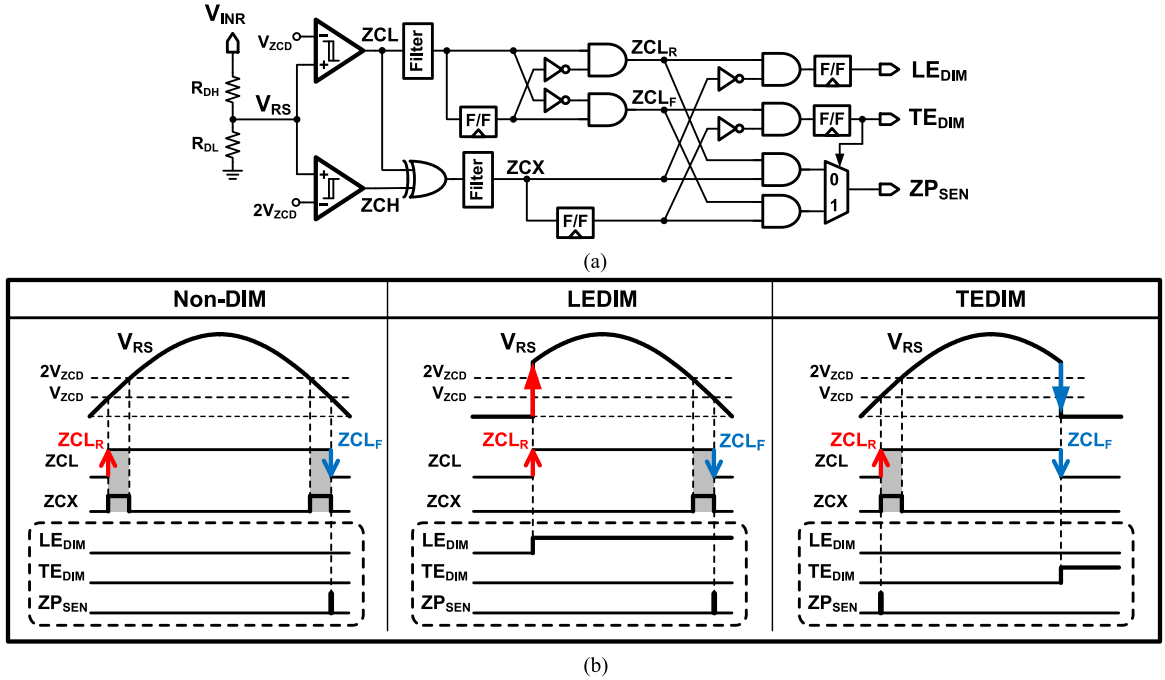

Fig. 10. AC sensing circuit. (a) Schematic. (b) Operating waveforms by each dimming mode.

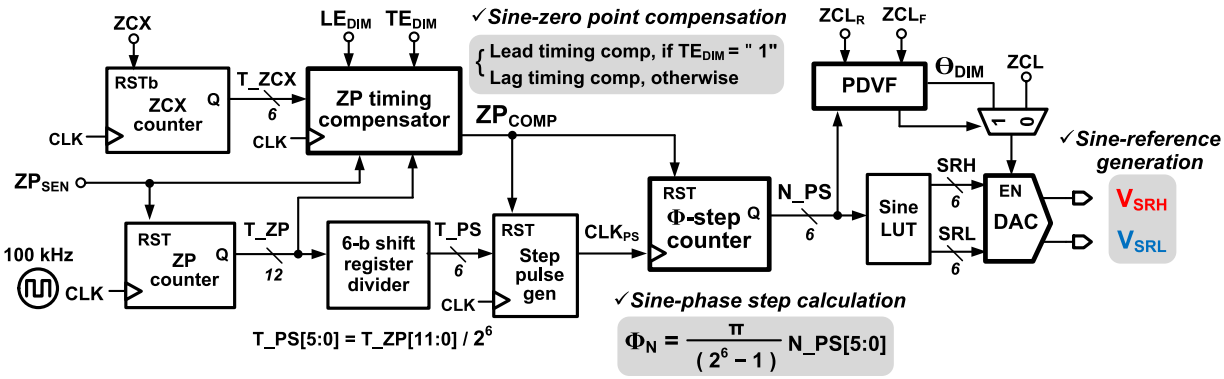

Fig. 11. Block diagram of the digital sine-reference generator.

falling edges of ZCL, denoted by ZCL_R and ZCL_F, represent the positive and negative signs of the V_INR transition, respectively. For example, in the case of the LEDIM mode, ZCL_R is detected during $\mathrm{ZCX} = ''0''$ when V_INR rises sharply, while ZCL_F is detected during $\mathrm{ZCX} = ''1''$ when V_INR falls slowly. Thus, the dimming mode signals (LE_DIM and TE_DIM) and the sensed ZP signal (ZP_SEN) can be logically expressed as

$$\begin{aligned}
\mathrm{LE}_\mathrm{DIM} &= \overline{\mathrm{ZCX}}\,\&\,\mathrm{ZCL}_R \\
\mathrm{TE}_\mathrm{DIM} &= \overline{\mathrm{ZCX}}\,\&\,\mathrm{ZCL}_F \\
\mathrm{ZP}_\mathrm{SEN} &= \begin{cases} \mathrm{ZCX}\&\mathrm{ZCL}_R & ;\mathrm{TEDIM} \\ \mathrm{ZCX}\,\&\,\mathrm{ZCL}_F & ;\mathrm{Otherwise}. \end{cases}
\end{aligned} \tag{16}$$

When $\mathrm{LE}_\mathrm{DIM} = \mathrm{TE}_\mathrm{DIM} = ''0''$, the LED driver is operating in the non-DIM mode.

B. Digital Sine-Reference Generator

The block diagram of the digital sine-reference generator is shown in Fig. 11. In this generator, the counter-based timing processor, the sine lookup table (LUT), and 6-bit digital to analog converter (DAC) are implemented to perform three main functions: the sine-zero point compensation, sine-phase step calculation, and sine-reference generation. The sine-zero point compensation cancels the timing offset of ZP_SEN to find the more precise ZP. The sine-phase step calculation is designed to represent the sine-wave phase in the discrete phase steps N_PS[5:0]. The sine-reference generation outputs the digital SRB with 6-bit resolution, based on the sine LUT.

The operation of the sine-zero point compensation is shown in Fig. 12. In this figure, there is a timing difference between the sensed ZP and the ideal ZP, and its timing offset is very similar to the ZCX on-time, T_ZCX. The ZCX counter is used to quantify the duration of T_ZCX to T_ZCX[5:0] using the internal

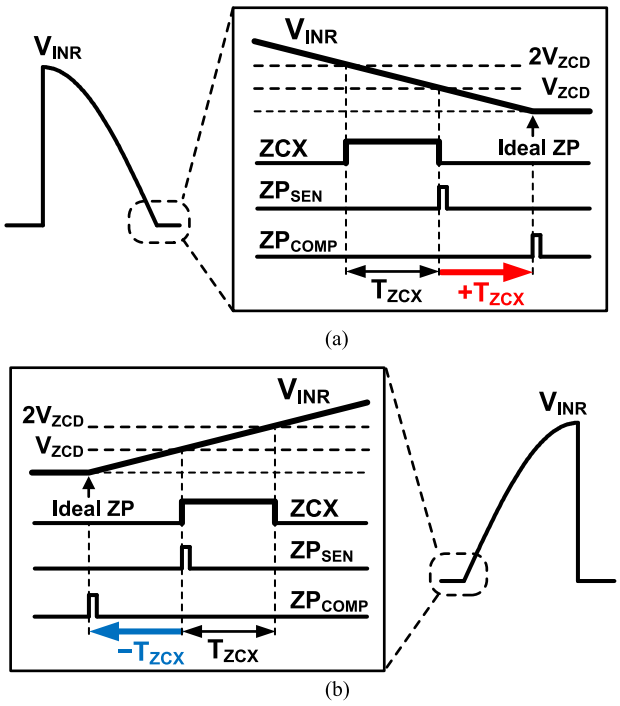

Fig. 12. Sine-zero point compensation. (a) Lag timing compensation. (b) Lead timing compensation.

clock of 100 kHz. Specifically, it counts up for ZCX = "1" and holds the counting value for ZCX = "0" after resetting the value by the rising edge of ZCX. Then, the lag or lead timing compensation by T_ZCX[5:0] is applied to $\mathrm{ZP_{SEN}}$, depending on the dimming mode. As a result, the output of the ZP timing compensator, $\mathrm{ZP_{COMP}}$ is close to the ideal ZP in Fig. 12.

In the sine-phase step calculation, the ZP counter measures one cycle time of the ZP and stores its value into T_ZP[11:0]. To uniformly make the 64-phase steps in the ZP cycle, the period of one-phase step, T_PS[5:0] is calculated by dividing T_ZP[11:0] by 64. The division operation is performed by the 6-bit LSB-side shifted register instead of an arithmetic unit that occupies a large chip area and consumes too much power. Thus, T_PS[5:0] corresponds to T_ZP[11:6], which is the 6-bit MSB of T_ZP[11:0] (i.e., T_PS[5:0] = T_ZP[11:6]). The pulse of the phase-step clock $\mathrm{CLK_{PS}}$ is generated every T_PS[5:0] × (1 / 100 kHz), starting from $\mathrm{ZP_{COMP}}$ as the reference point. Accordingly, the value of N_PS[5:0], which is reset to 0 at $\mathrm{ZP_{COMP}}$, increases by one on each $\mathrm{CLK_{PS}}$ cycle until N_PS[5:0] = 63 (= $2^6 - 1$). Therefore, the discrete phase Φ_N can be expressed as

$$\Phi_N = \frac{\pi}{(2^6 - 1)} \cdot \mathrm{N\_PS}[5:0]. \tag{17}$$

In the sine-reference generation the sine LUT contains the 6-bit sine pattern values, SRH[5:0] and SRL[5:0], that are matched with Φ_N for V_{SRH} and V_{SRL}, respectively. These values are loaded into the 6-bit DAC in response to N_PS[5:0]. As shown in Fig. 13, the DAC has two sets of 64 switches to generate two outputs using one shared resistor-string. The DAC reference voltage is set to 1.2 V for the peak voltage of

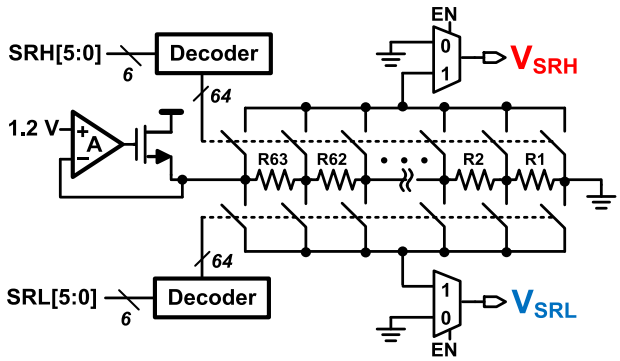

Fig. 13. Implementation of the DAC for the sine-reference generation.

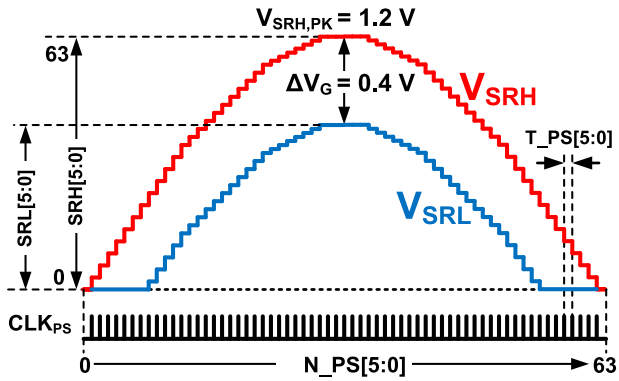

Fig. 14. Detailed waveform of the SRB.

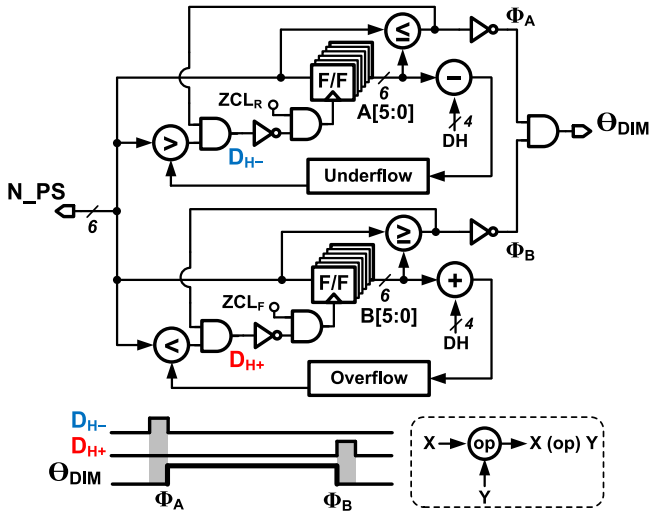

Fig. 15. Schematic circuit of the PDVF.

V_{SRH} ($V_{\mathrm{SRH,PK}}$). Hence, ΔV_G can be calculated as

$$\Delta V_G = \frac{1.2V}{(2^6 - 1)} \cdot (\mathrm{SRH}[5:0] - \mathrm{SRL}[5:0]). \tag{18}$$

To satisfy the optimum CRR (CRR = 0.4) explained previously in Section II, ΔV_G is determined to be 0.4 V from (10) and implemented adopting SRH[5:0] − SRL[5:0] = 21 from

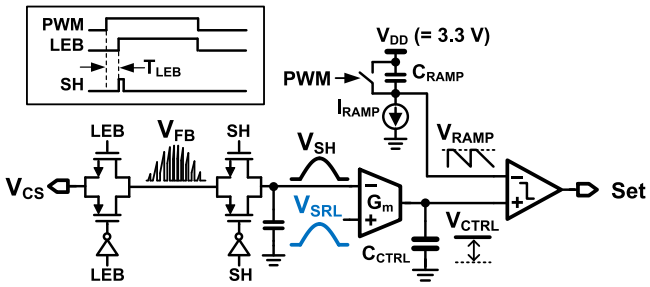

Fig. 16. Implementation of the AOTC in the RSA controller.

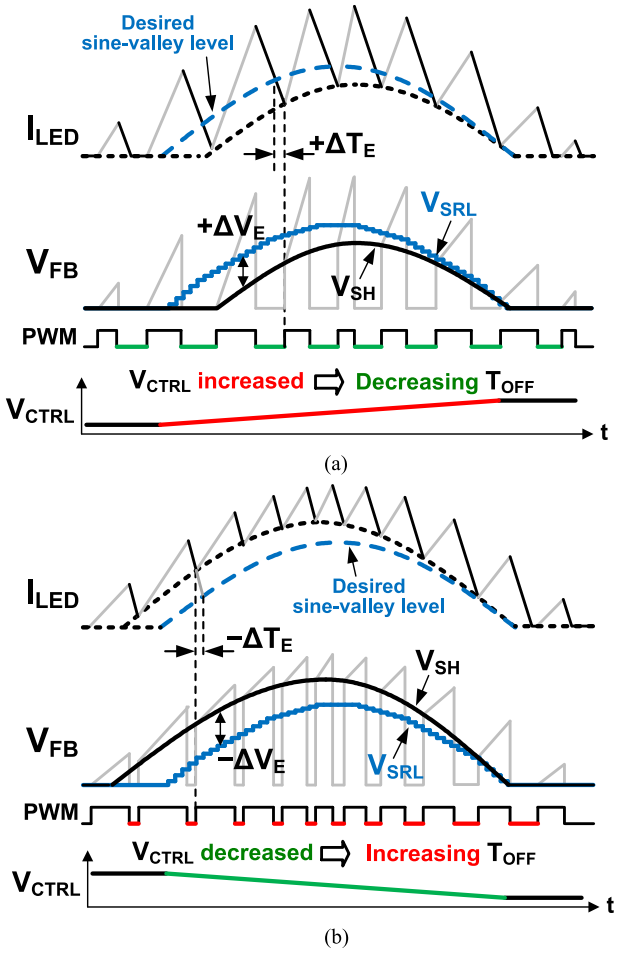

Fig. 17. Operations of the AOTC to adjust the off-time for the rectified sine-valley current regulation with (a) long off-time and (b) short off-time.

(18). Consequently, assuming the non-DIM mode, the overall SRB waveform is depicted in Fig. 14.

C. Phase Dimming Variation Filter (PDVF)

In the phase-cut dimming mode, the PDVF controls the dimming angle of the SRB waveform to eliminate phase dimming variations from the LED current. Fig. 15 shows how the PDVF generates a steady dimming angle Θ_{DIM} with the dimming hysteresis by utilizing N_PS[5:0]. At the beginning, the start-phase step A[5:0] and the end-phase step B[5:0] for phase-cut

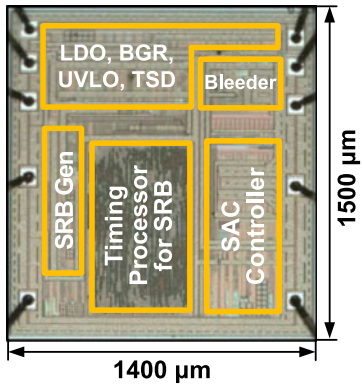

Fig. 18. Integrated chip micrograph.

TABLE I
DESIGN SPECIFICATION OF THE PROPOSED LED DRIVER

Parameter	Symbol	Condition
Technology		$0.35-\mu$m 3.3 V/ 18 V CMOS
Chip area		1400 μm × 1500 μm
AC input voltage	V_{IN}	$90-260\,\mathrm{V_{AC}}$
Number of LEDs	N_{LED}	$10-36$ @220 $\mathrm{V_{AC}}$
Operating supply voltage	V_{CC}	12 V
Avg. LED current	$I_{\mathrm{LED,AVG}}$	200 mA
Peak sine-average current	$I_{\mathrm{SAVG,PK}}$	400 mA
LED current ripple	ΔI_R	160 mA
Inductor	L	3.3 mH, $R_{\mathrm{DCR}}=4.4\,\Omega$
Current sensing resistor	R_{CS}	2.55 Ω
Avg. switching frequency	$f_{\mathrm{SW,AVG}}$	100 kHz @ 220 $\mathrm{V_{AC}}$
Power MOSFET	M_{N}	600 V, 1.9 A, $R_{\mathrm{ON}}=4.7\,\Omega$
1-LED forward voltage	$V_{F,\mathrm{LED}}$	3.1 V @ $I_{\mathrm{LED,AVG}}=200$ mA
$\mathrm{T_{OFF}}$ control capacitor	C_{CTRL}	220 nF
Output capacitor	C_{OUT}	0

dimming are initialized as 0 and 63, respectively. When ZCL_R (or ZCL_F) comes out of the dimming hysteresis due to a change in the dimming angle, the value of N_PS[5:0] is immediately stored to A[5:0] (or B[5:0]). As a result, Θ_{DIM} is set to logic "1" when A[5:0] < N_PS[5:0] and is reset to logic "0" when N_PS[5:0] < B[5:0]. For an example 45° dimming angle, LEDIM leads to A[5:0] = 47 and B[5:0] = 63, while TEDIM results in A[5:0] = 0 and B[5:0] = 16.

In addition, two dimming hysteresis signals, D_{H+} and D_{H-} are formed outside of the Θ_{DIM} by the hysteresis phase step DH[3:0]. Therefore, Θ_{DIM} is synchronized with the innermost phase edges of the phase dimming variations and fixed in the steady state as long as the variations are within the specific dimming hysteresis.

D. Adaptive Off-Time Control (AOTC)

Fig. 16 shows the implementation of the AOTC in the RSA controller. To sense and track the level of the LED valley current, the sample-and-hold circuit immediately captures V_{FB} when PWM is on. Then, the voltage error between V_{SRL} and V_{SH} is integrated into C_{CTRL} through G_{m}, generating V_{CTRL}. The set signal of PWM is generated when the down slope ramp voltage V_{RAMP} crosses V_{CTRL}. In this way, V_{CTRL} adaptively controls

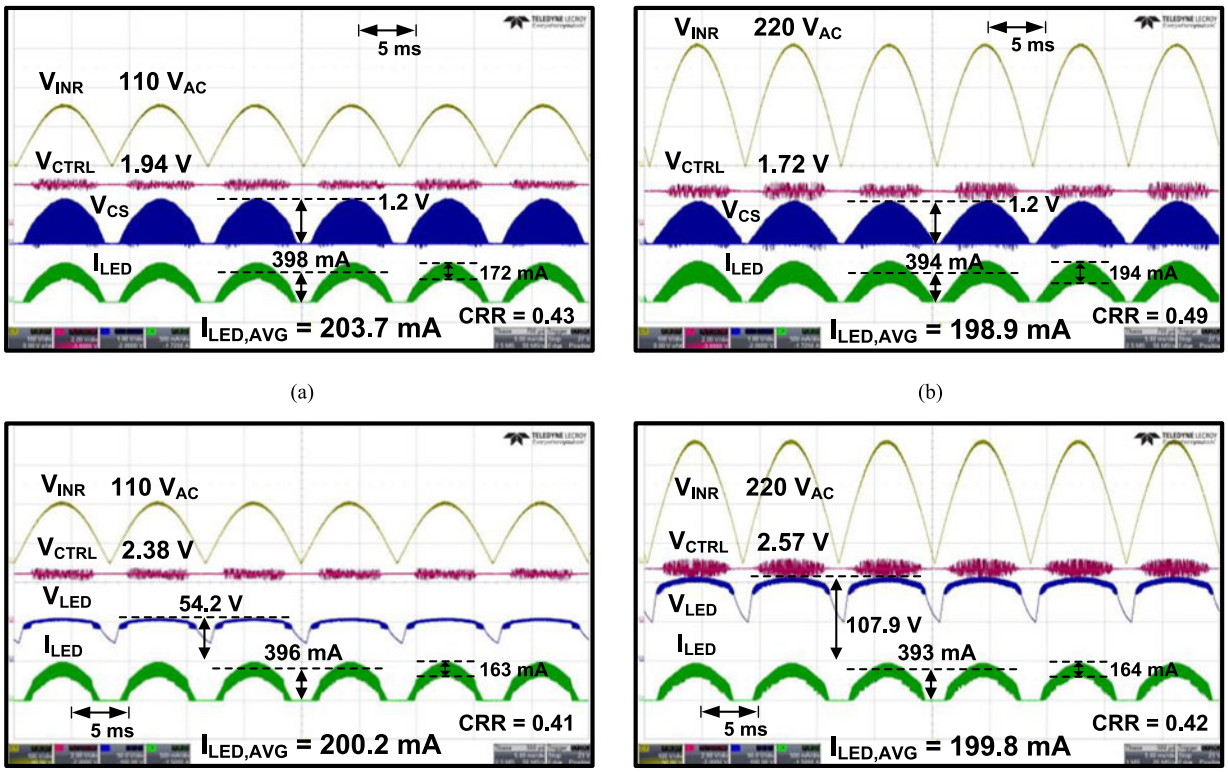

Fig. 19. Measured waveforms of the RSA current under (a) 110 V_{AC}, 12 LEDs, (b) 220 V_{AC}, 12 LEDs, (c) 110 V_{AC}, 18 LEDs, and (d) 220 V_{AC}, 36 LEDs.

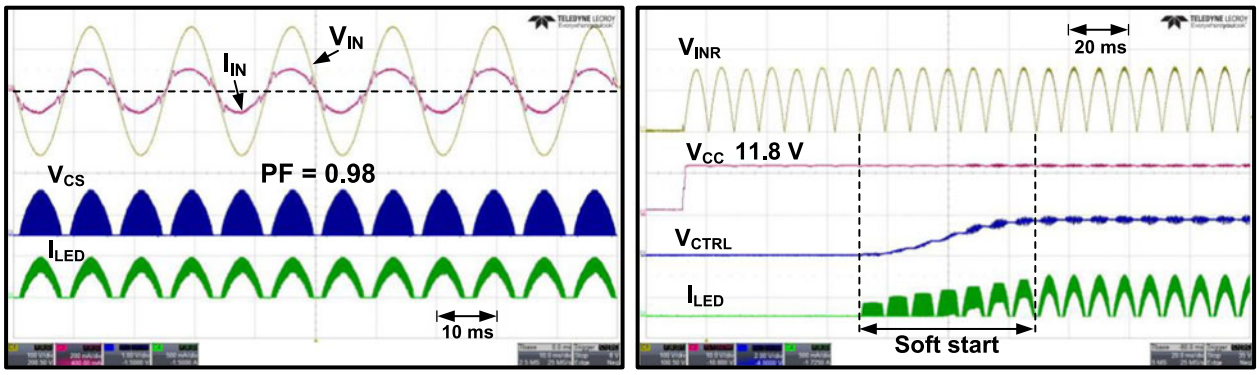

Fig. 20. Measured waveforms of (a) input voltage and input current at 110 V_{AC} and (b) start-up and soft start operations.

the off-time duration $T_{\rm OFF}$ for the rectified sine-valley current regulation, and $T_{\rm OFF}$ is given by

$$T_{\rm OFF} = \frac{C_{\rm RAMP}}{I_{\rm RAMP}} \cdot (V_{\rm DD} - V_{\rm CTRL}) \tag{19}$$

where $C_{\rm RAMP}$ and $I_{\rm RAMP}$ are the capacitor and current source of the ramp generator, respectively.

Fig. 17 illustrates the operations of the AOTC to adjust the off-time duration, $T_{\rm OFF}$. When $T_{\rm OFF}$ is longer than the desired value, its off-time error, $+\Delta T_E$ can be converted to the voltage error of $+\Delta V_E$ $(= V_{\rm SRL} - V_{\rm SH})$ as shown in Fig. 17(a). Thus, $T_{\rm OFF}$ will be shortened from (19) as $V_{\rm CTRL}$ is increased by $+\Delta V_E$. On the other hand, when $T_{\rm OFF}$ is too short, $V_{\rm CTRL}$ decreases due to $-\Delta V_E$ corresponding to $-\Delta T_E$ in Fig. 17(b). Therefore, $T_{\rm OFF}$ will increase until the desired off-time. As a result, the $V_{\rm SH}$ can be equal to $V_{\rm SRL}$, in the steady state, $\Delta V_E = \Delta T_E = 0$. Since this operation is achieved by a negative feedback loop, the AOTC can ensure the regulation of the rectified sine-valley current with high accuracy and reliability.

IV. Experimental Results

The proposed LED driver was fabricated with a 0.35-μm 3.3 V/18 V CMOS process, and the chip micrograph is shown

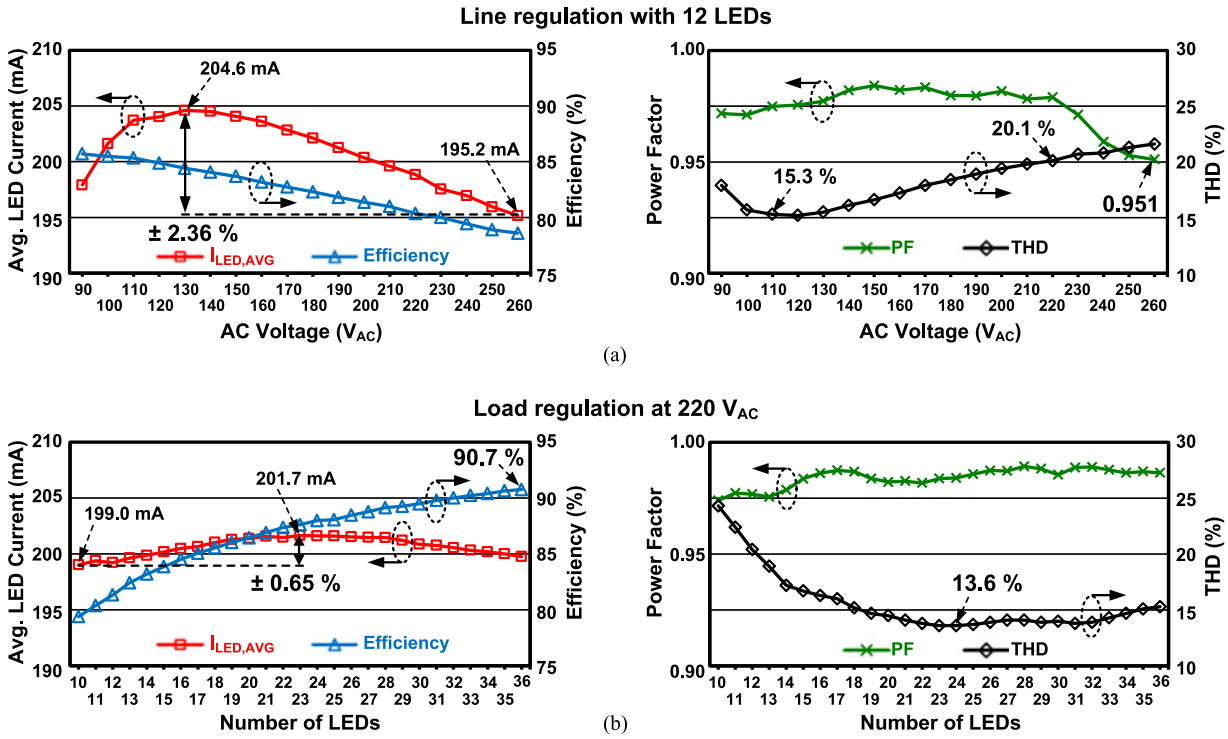

Fig. 21. Measured results of the RSA current control for the average LED current, efficiency, PF, and THD. (a) Line regulation with 12 LEDs. (b) Load regulation at 220 V_{AC}.

in Fig. 18. The chip includes not only the proposed controller but also the additional circuits for bias and protection, and the total chip area is 2.1 mm^2. The proposed driver can support a wide input range from 90 to 260 V_{AC} and drive various numbers of LEDs from 10 to 36. For sensing the LED current (I_{LED}), the sensing resistor R_{CS} was chosen to have 2.55 Ω. Also, a 3.3 mH inductor and a 600 V/1.9 A low-side power MOSFET are used as external components in the driver. In the experiment, an output capacitor for the LED load is not needed. The detailed design specifications of the proposed LED driver are listed in Table I.

Fig. 19 shows the measured waveforms of the RSA current under different ac input voltages and different numbers of output LEDs. The I_{LED} waveforms verify that the proposed driver performs current regulation to maintain the average LED current regardless of external conditions. In all cases, the peak value of the RSA current ($I_{SAVG,PK}$) and the average value of the LED current ($I_{LED,AVG}$) are close to 400 and 200 mA, respectively. Some variations of the current ripple level occur due to the propagation delay (from the transition of the PWM signal to the actual switching operation of M_N) and the leading-edge blanking time when the rising slope of the LED current is varied [12], [35]. In particular, as the current rising slope increases, the LED current ripple is larger than the desired value. However, the RSA LED current is not affected by the variation of the current ripple if the propagation delay and the leading-edge blanking time are similar. In Fig. 20(a), the measured input voltage and input current waveforms prove that the RSA current control can achieve a high PF. The sine-wave I_{LED} controlled in phase with the ac input voltage enables the input current to follow the input

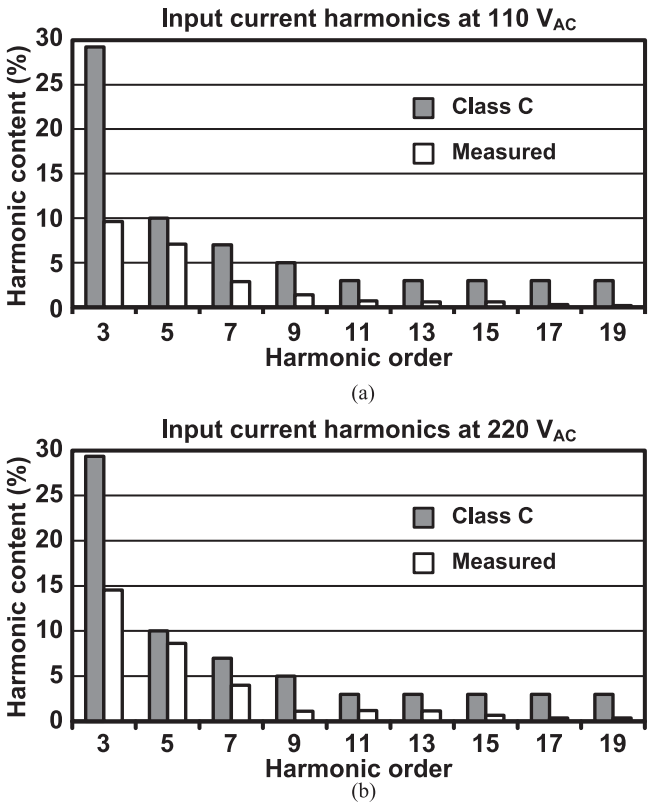

Fig. 22. Measured input current harmonic content compared with the IEC 61000-3-2 Class C standard. (a) 110 V_{AC}. (b) 220 V_{AC}.

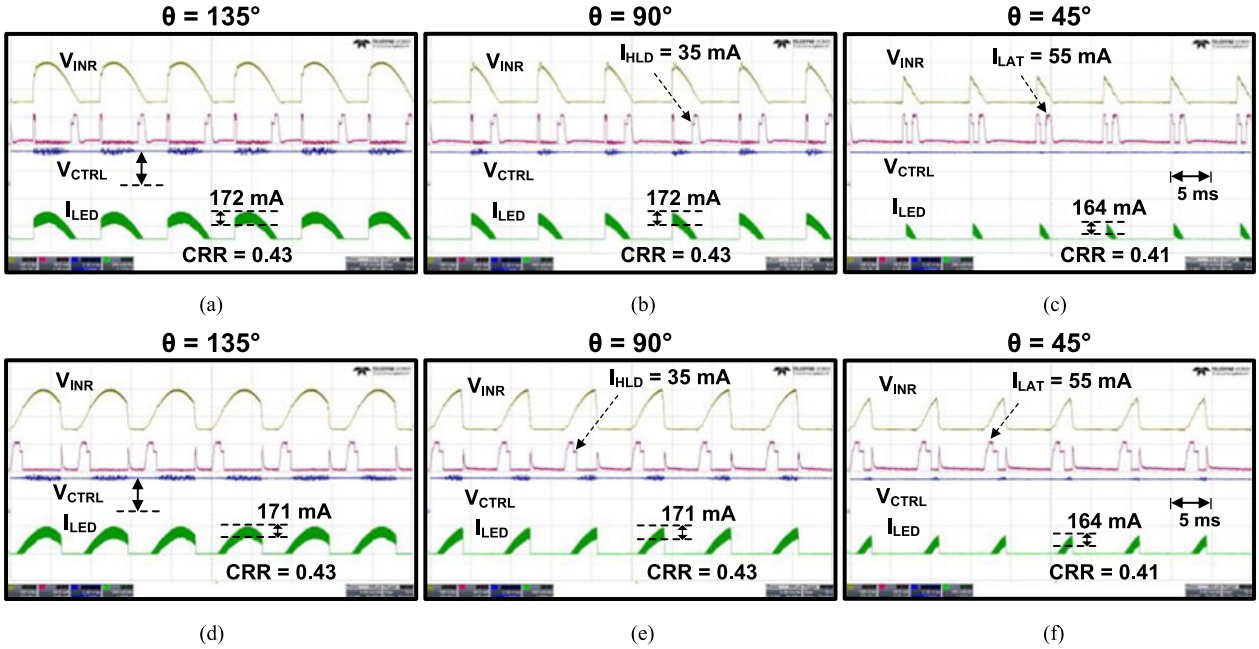

Fig. 23. Dimming LED current of the proposed phase-cut dimming control at different diming angles. (a) LEDIM. (b) TEDIM.

voltage waveform. Fig. 20(b) shows the measured waveforms of the start-up and soft start operations. When the ac source is powered ON, $V_{\rm CC}$ rapidly increases up to about 12 V, and then the soft start is activated during seven cycles of $V_{\rm INR}$. At the same time, $V_{\rm CTRL}$ also begins to be controlled. In the measurement, $C_{\rm VCC} = 10\,\mu$F and $C_{\rm CTRL} = 220$ nF are used for $V_{\rm CC}$ and $V_{\rm CTRL}$, respectively.

Fig. 21 shows the experimental results of the RSA current control for the line regulation (with 12 LEDs) and the load regulation (at 220 $\rm V_{AC}$). The RSA current control of the proposed LED driver can achieve the line regulation of $\pm 2.36\%$ over the ac input range from 90 to 260 $\rm V_{AC}$ and the outstanding load regulation of $\pm 0.65\%$ when the number of LEDs changes from 10 to 36. In the line regulations, the power efficiency tends to increase as the ac input voltage decreases owing to the larger duty ratio of the driver. Similarly, in the load regulation, the power efficiency increases with the number of output LEDs because the output power level increases proportionally to the LED voltage. The proposed LED driver can achieve the peak efficiency of 90.7% (with no bleeding current) at 220 $\rm V_{AC}$ and 36 LEDs, including the power consumption of the driver. The PF is above 0.95 under all conditions of the line and load regulations. The lowest total harmonic distortion (THD) is 13.6% at 220 $\rm V_{AC}$ and 24 LEDs. The input current harmonic content measured with 12 LEDs at 110 and 220 $\rm V_{AC}$ is shown in Fig. 22. It can be seen that the proposed driver meets the IEC 61000-3-2 Class C standard with a sufficient margin.

Fig. 23 shows the measured waveforms of the phase-cut dimming LED current for different dimming angles. The leading-edge and trailing-edge dimmers used in the experiment are DVCL-153P and NTELV-300 from Lutron, respectively. To stably operate the various phase-cut dimmers, the latching and holding current values are set to 50 and 35 mA respectively, using $R_{\rm LAT} = 220\,\Omega$ and $R_{\rm HLD} = 3.3\,\Omega$. Although the waveform of the phase-cut ac input voltage changes depending on the dimming type and angle, the proposed phase-cut dimming control ensures that the shape of the $I_{\rm LED}$ is the same as that of the dimming input voltage. The values of the CRR also remain fairly constant during the phase-cut dimming operation. Furthermore, the dynamic bleeder circuit can control the on-off timing of the holding current to minimize its power loss.

Fig. 24 illustrates the comparison of the dimming LED current with and without the PDVF to verify the effectiveness of the PDVF on the visible dimming flicker. In the measured waveforms, the peak level of the dimming $I_{\rm LED}$ with the PDVF is uniform, while the peak level of the dimming $I_{\rm LED}$ without the PDVF is uneven in each cycle. The difference of the dimming $I_{\rm LED}$ in each cycle causes the visible flicker, especially at low dimming angles. The analysis of the flicker frequency shown in Fig. 24(b) clearly demonstrates the visible dimming flicker of the $I_{\rm LED}$ without the PDVF at the AC line frequency of 60 Hz. In contrast, the visible flicker is completely eliminated in the $I_{\rm LED}$ with the PDVF. Even though the invisible flicker at twice the line frequency still exists because the output capacitor is not used, at frequencies above 70 Hz, flicker is not consciously perceived by the human eye [29].

The performance summary and comparisons of the buck driver using the proposed SRB-controlled average current technique with the state-of-the-art are listed in Table II. Compared with previous works, the proposed ac–dc buck LED driver can achieve outstanding current regulation performance and a higher PF over a wide range of ac input voltages and the number of LEDs. In addition, the proposed phase-cut dimmable driver enables control of the two types of dimmers, and it does not require

TABLE II
PERFORMANCE SUMMARY AND COMPARISONS

	[12]	[13]	[14]	[15]	**This Work**
Technology	0.35–μm CMOS	0.5–μm CMOS	0.35–μm CMOS	Discrete components	**0.35–μm CMOS**
Topology	DC–DC Buck	AC–DC Buck	AC–DC Buck	AC–DC Buck	**AC–DC Buck**
Input voltage	110–200 V	85–265 V_{AC}	100–120 V_{AC}	90–265 V_{AC}	**90–260 V_{AC}**
LED power	46.5*–77.5*W	2.5–7 W	7–22 W	12 W	**5–22 W**
Control scheme	Integrated current control	PCC	Burst mode control	Tapped-inductor PFC control	**SRB-controlled average current technique**
Line regulation (Input voltage)	$\pm$1.7% (110–200 V)	N.A	N.A	N.A	**$\pm$2.36% (90–260 V_{AC})**
Load regulation (No. of LEDs)	N.A	$\pm$15%* (5–15)	N.A	N.A	**$\pm$ 0.65% (10–36)**
Power factor	N.A	0.83*–0.98	0.78* – 0.96	0.957–0.994	**0.95–0.99**
Max. efficiency	98.16%	89%*	90.6%	88.7%	**90.7%**
Dimming	PWM	N.A	N.A	N.A	**Phase-cut dimmer (leading- & trailing-edge)**
Output capacitor	0.15 μF	1 μF	15 μF	1000 μF	**0**
Inductance	1 mH	5.5 mH	850 nH, 12 μH	3 mH	**2–5 mH**

* Estimated from measurement results.

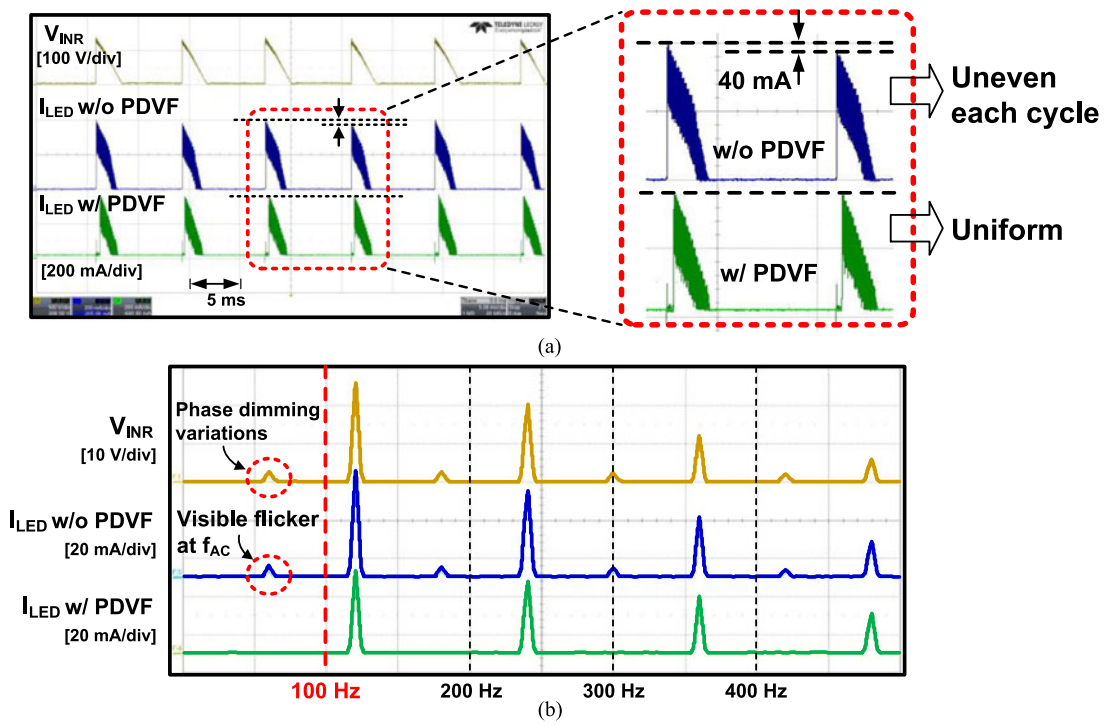

Fig. 24. PDVF effect on the visible dimming flicker. (a) Comparison of the phase-cut dimming LED current with and without the PDVF. (b) Analysis of flicker frequency.

an output capacitor to remove the visible dimming flicker, which was considerably difficult in previous works.

V. CONCLUSION

This paper has presented the SRB-controlled RSA current technique for a phase-cut dimmable ac–dc buck LED driver. For the proposed control scheme, the phase-cut dimmable SRB generator and RSA controller were implemented and verified experimentally. According to the results obtained for the operation of this technique, the RSA current control of the proposed LED driver can simultaneously achieve excellent line/load regulation and a high PF over a wide range of ac input voltages and output LED loads. In addition, the proposed dimmable driver including the phase-cut dimming control is not only compatible with different types of dimmers, but is also able to eliminate the visible dimming flicker at the ac line frequency without any output capacitor. The SRB-controlled LED driver can be widely used in ac-powered electrolytic capacitor-less LED lighting applications.

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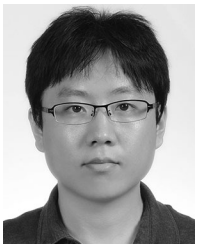

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