Seamless Fault-Tolerant Operation of a Modular Multilevel Converter With Switch Open-Circuit Fault Diagnosis in a Distributed Control Architecture

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***Abstract*—Modularity and high reliability from redundancy are the two attractive advantages of modular multilevel converters (MMCs). This paper elaborates a switch open-circuit fault diagnosis and a fault-tolerant operation scheme for MMCs with distributed control. The proposed fault diagnosis and fault-tolerant control method can significantly improve the reliability of the MMC while maintaining the modularity of its software implementation. By distributing fault diagnosis into submodules, its local controller is capable of identifying the switching devices in open-circuit fault without extra hardware circuitry. Based on the real-time measurements of submodule terminal voltage and arm current, single, or multiple faulty switches can be identified within 3.5 ms without triggering faulty alarms. Furthermore, a new fault-tolerant operation is proposed to maintain the output current, internal dynamics, and switching harmonics unchanged after the faulty submodule is bypassed. This is achieved by resetting the period and phase registers in the local controller according to the information of bypassed submodules. The control loops of the MMC are not influenced by the proposed fault diagnosis and fault-tolerant operation, making the operation transition seamless and reliable. Experimental results show that fault identification and system reconfiguration can be completed within 5 ms, and the MMC can seamlessly and smooth ride through the switch open-circuit faults without severe malfunction and catastrophic damages.**

***Index Terms*—Distributed control, fault diagnosis, fault-tolerant operation, modular multilevel converter.**

I. Introduction

MODULAR multilevel converter (MMC) is one of the promising topologies in recent years for medium or high-voltage industrial applications, such as high-voltage dc transmission [1], medium voltage variable speed drives [2], and static synchronous compensators [3]. The wide adoption of MMCs in the industry is mainly due to its modularity, flexible expandability, high reliability from redundancy, transformer-less configuration, common dc bus, etc. Although the considerable submodules in an MMC are regarded as potential failure points and may deteriorate the system reliability, the redundant submodules, as well as fault diagnosis and fault-tolerant techniques, actually increase the reliability of the MMC system [4].

Fault diagnosis is the precondition of fault-tolerant operation for MMCs. A sliding mode observer-based MMC fault detection and an assumption verification process based fault identification are proposed in [5], which locate the faulty switch within 50 ms with relatively high computational burdens. The Kalman filter is adopted to detect open-circuit faults and the faulty submodule is then located by comparing the capacitor voltages in the same arm in [6]. The method proposed in [6] can locate different faults occurring in a 50 ms interval. However, the period required to locate the submodules ranges from 85 ms to more than 250 ms in different scenarios. A state-observer-based fault detection and capacitor voltage comparison based fault locating are introduced in [7], where only single faulty submodule can be identified in 50 to 150 ms. The above-mentioned fault diagnosis methods employ complicated algorithms with relatively high computational loads to detect the fault based on the MMC states first, and then identify the faulty submodule according to the MMC internal dynamics, e.g., the circulating current or submodule capacitor voltages. These methods, either estimating the system states based on the overall MMC model or gathering the submodule capacitor voltages for fault locating, are suitable for a centralized control architecture. Generally, it also takes a long time to locate the fault in an MMC for aforementioned methods.

On the other hand, the faulty submodules identified are generally bypassed and the MMC is required to continuously operate without interruption or significant performance degradation under fault-tolerant operation schemes. Hot reserved redundant submodule schemes [4], [8] are preferred in fault-tolerant operation schemes for the sake of excellent transient performance and a higher submodule utilization ratio. An MMC control strategy under submodule fault conditions, which adjusts the capacitor voltage in the faulty arm based on energy balancing of arms with asymmetrical numbers of submodules is presented in [8]. In [9], two indexes, i.e., dynamic redundancy and submodule utilization ratio, and synthetical analysis of the MMC operation under fault conditions were proposed. An optimized fault-tolerant control strategy based on the nearest level modulation scheme is then introduced. An extensive control process for an MMC to ride through a single insulated-gate bipolar transistor

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(IGBT) open-circuit fault, including fault detection, locating, and system reconfiguration, is detailed in [7]. However, since the faulty IGBT can only be identified after around 50 ms, a fault-tolerant method has to be adopted to actively compensate the voltage disturbances caused by the faulty submodule before the fault is located.

This paper aims to elaborate a seamless switching device open-circuit fault diagnosis and fault-tolerant operation of MMCs for system reliability improvement. A fault diagnosis method is proposed with the following distinct features:

1) it is implemented in submodules and only requires arm current and locally measured voltage to diagnose the fault, which can maintain the modularity of the MMC;
2) it is suitable for MMCs with a large number of submodules and can be easily extended for applications with different number of submodules;
3) it can identify faulty switching devices within a short period before severe malfunction of the MMC or a secondary fault occurs;
4) it can simultaneously locate multiple switching device faults;
5) no extra hardware circuit or sensor is required.

Based on the fault diagnosis, the faulty submodule can be bypassed and an effective and easy-to-implement fault-tolerant operation scheme with hot reserved submodules is discussed in this paper. Even with asymmetrical submodule in operation, the output current, internal dynamics, and switching harmonics cancellation of the MMC can all remain the same as those in the normal operation. In order to generate a sufficient ac voltage, the capacitor voltages in the faulty arm might be adjusted according to the number of submodules bypassed in the corresponding arm. By properly adjusting the period and phase registers of the pulse width modulation (PWM) modules in the local controller, the fault-tolerant operation can be achieved without affecting the control loops of the MMC system. Experimental results show that the proposed fault diagnosis can identify faulty switches within 3.5 ms and this method is also immune to system noises and disturbances. The obtained experimental waveforms under fault-tolerant operation are in good agreement with the characteristics analysis of the MMC, implying the effectiveness of the proposed fault-tolerant operation. Moreover, it is proved that the fault identification and system reconfiguration for fault-tolerant operation can be accomplished within 5 ms after the occurrence of switch open-circuit faults in different scenarios. The MMC can operate seamlessly to ride through such faults without interruptions or catastrophic failures.

II. MMC Principles and Distributed Control Architecture

The basic structure and operation principles of an MMC have been extensively explained in the literature [10]–[12] and will not be discussed in detail in this paper. A single-phase MMC-based inverter system shown in Fig. 1 is adopted in this paper. There are $N + N_r$ submodules connected in series in the upper and lower arms, respectively. The first N submodules are normal ones required to generate the MMC output voltage. The extra N_r

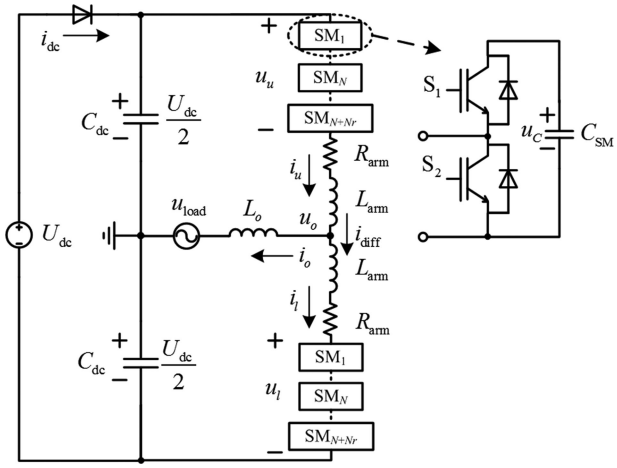

Fig. 1. Structure of a single-phase MMC-based inverter.

submodules operate as hot reserved redundant ones to increase the reliability of the overall MMC system [4]. Each arm is equipped with an arm inductor $L_{\rm arm}$. An equivalent resistor $R_{\rm arm}$ is employed in each arm to represent the losses on the semiconductors, equivalent series resistance in $C_{\rm SM}$ and $L_{\rm arm}$, etc. The output terminals of the MMC, which are located at the middle points of the two arms and the dc bus capacitors, are connected to the load represented by a voltage source $u_{\rm load}$ via an inductor L_o.

If the output voltage and current of the MMC are well regulated, they can be expressed as

$$\begin{cases} u_o = U_o \cos(\omega_o t) \\ i_o = I_o \cos(\omega_o t + \phi_o) \end{cases} \tag{1}$$

where U_o and I_o are the amplitudes of u_o and i_o, respectively, ω_o refers to the fundamental angular frequency, and ϕ_o stands for the phase displacement between the output voltage and current. The differential current in the phase leg is defined as

$$i_{\rm diff} = I_{\rm dc} + i_{\rm cir} \tag{2}$$

where $I_{\rm dc}$ is a dc current that maintains the power balance between the dc and ac sides of the MMC [2], [13], and $i_{\rm cir}$ is the circulating current ripple that is dominated by the second-order harmonic [11], [14]. The arm currents can be written as

$$\begin{cases} i_u = i_{\rm diff} + \frac{i_o}{2} \\ i_l = i_{\rm diff} - \frac{i_o}{2} \end{cases}. \tag{3}$$

Assuming the submodule capacitor voltages are well balanced, the normalized modulation index of the kth submodule in the upper and lower arms can be obtained as

$$\begin{cases} n_{uk} = \frac{1}{2} - \frac{{u_o}^*}{2} - {u_{\rm diff}}^* \\ n_{lk} = \frac{1}{2} + \frac{{u_o}^*}{2} - {u_{\rm diff}}^* \end{cases} \tag{4}$$

$$\begin{cases} {u_o}^* = \frac{2u_o}{U_{\rm dc}} \\ {u_{\rm diff}}^* = \frac{U_{\rm diff\_dc} + U_{\rm diff\_2}\cos(2\omega_o t + \phi_{\rm diff\_2})}{U_{\rm dc}} \end{cases} \tag{5}$$

where $U_{\rm diff\_dc}$ is a dc voltage to induce $I_{\rm dc}$, and $U_{\rm diff\_2}\cos(2\omega_o t + \phi_{\rm diff\_2})$ is the voltage utilized to suppress

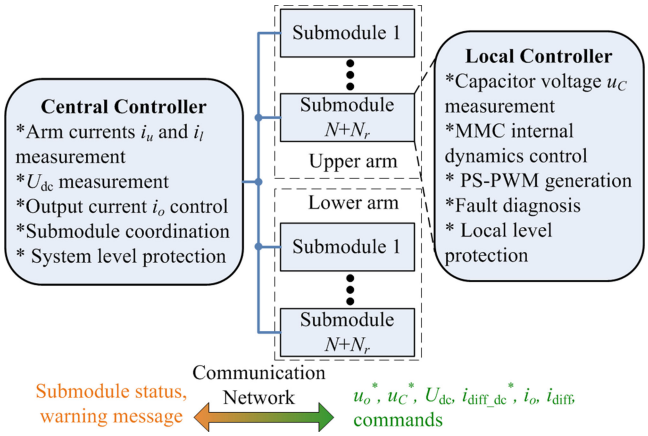

Fig. 2. Distributed control structure for MMCs.

the second-order harmonics in the differential current [15]. According to the analysis in [2], the capacitor voltage of the kth submodule in the upper and lower arms can be written as

$$\begin{cases} u_{Cuk} = U_C + U_{C\_1}\sin(\omega_o t + \phi_{C\_1}) + U_{C\_2}\sin(2\omega_o t + \phi_o) \\ u_{Clk} = U_C - U_{C\_1}\sin(\omega_o t + \phi_{C\_1}) + U_{C\_2}\sin(2\omega_o t + \phi_o) \end{cases} \tag{6}$$

where U_C denotes the average voltage across the submodule capacitor, $U_{C\_1}\sin(\omega_o t + \phi_{C\_2})$ and $U_{C\_2}\sin(2\omega_o t + \phi_o)$ represent the voltage ripples with fundamental and second-order frequencies, respectively.

The structure of the distributed control architecture for the MMC is illustrated in Fig. 2, where the control tasks are assigned to different controllers, i.e., a central controller and local controllers located in submodules [16]. The central controller mainly coordinates and manages the overall operation of the MMC. The output current control is implemented in the central controller with measured arm currents within each control cycle. The reference of the submodule capacitor voltage $u_C{}^*$ can be calculated by the central controller according to the dc bus voltage and operation requirements of the MMC. The local controller deals with the internal dynamics, fault diagnosis, PWM generation, and immediate protections of the submodule. It measures the capacitor voltage of the corresponding submodule for voltage control and regulates the inner differential current of the MMC. The internal dynamics regulation and fault diagnosis have to be achieved based on the arm currents and local information, e.g., submodule terminal voltage, to keep the modularity of software implementation in the local controller. The phase-shifted PWM (PS-PWM) scheme [17], [18] is adopted in the distributed control architecture. A PS triangular carrier is generated in each local controller. The phase displacements of triangular carriers are calculated based on the number of submodules in each arm and assigned to the local controllers when the MMC is initialized after powering up.

Necessary information is exchanged between the central and local controllers through a communication network. One message containing $u_o{}^*$, $i_{\mathrm{diff\_dc}}{}^*$, i_o, and i_{diff}, which conveys adequate information for the real-time control in local controllers, can be broadcasted by the central controller through the communication network in each control cycle. The communication protocol is selected mainly based on the data rate of the communication network and the number of messages transmitted per second. In the MMC prototype with a short transmission distance, the controller area network (CAN) protocol having a 1-Mbps data rate with a maximum bus length of 40 m can be adopted to transmit 6000 messages containing aforementioned four signals per second for executing the distributed control in real time. In those cases where more information, higher transmission rate, or longer transmission distance is required, the high-speed CAN with flexible data-rate protocol (2-Mbps data rate) or even the ethernet for control automation technology (EtherCAT) protocol (100-Mbps data rate) can be used in the communication network. Each submodule is assigned a sole sequence number (SN) so that it can communicate with the central controller individually as well. If any fault is detected by the local controller, the necessary protective actions can be executed locally and a warning message with the fault code is immediately sent out to inform the central controller for further decision making. In order to further improve the response of the fault-tolerant operation, the submodule that detects an open-circuit fault triggers an external interrupt to inform the central controller the fault condition. The central controller is able to identify the faulty submodule according to the interrupt sources. This information can also be sent through the communication network in an MMC with a larger number of submodules, with a slightly slower response.

III. Proposed Switch Open-Circuit Fault Diagnosis in Local Controllers

There are two types of switching device faults, i.e., short-circuit fault and open-circuit fault, that should be considered in practical applications. Since the short-circuit fault detection and protection are normally integrated into commercial device drivers [5], [7], only the open-circuit fault of switching devices is discussed in this paper. Unlike most existing switch open-circuit fault diagnosis methods where fault detection and fault locating are independently implemented and require a relatively long execution period [5]–[7], this paper develops a real-time measurement based fault diagnosis method that is implemented in the local controller and can identify the faults in one step within a few milliseconds.

A. Submodule Characteristics With Switch Open-Circuit Faults

The submodule characteristics with switch open-circuit faults are investigated in this section. The current paths of the submodule with open-circuit fault at different devices are illustrated in Fig. 3. It can be seen in Fig. 3(a) that, when S_1 is open circuit, the current paths are the same as those in the normal condition if $i_{\mathrm{arm}} > 0$, and the submodule is bypassed through the body diode of S_2 if $i_{\mathrm{arm}} < 0$ regardless of the gating signals for the switching devices. Such current paths indicate that the submodule capacitor C_{SM} could not be discharged, which eventually leads to capacitor overvoltage. On the other hand, if S_2 is in open-circuit fault, the submodule operates normally when

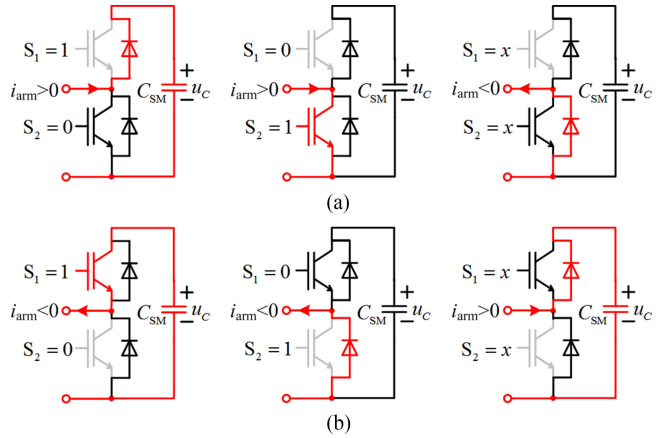

Fig. 3. Current paths of the submodule with: (a) S_1 open-circuit fault; (b) S_2 open-circuit fault.

TABLE I
SUBMODULE TERMINAL VOLTAGE

	$i_{\rm arm} > 0$		$i_{\rm arm} < 0$	
	$S_1 = 1$ and $S_2 = 0$	$S_1 = 0$ and $S_2 = 1$	$S_1 = 1$ and $S_2 = 0$	$S_1 = 0$ and $S_2 = 1$
Normal	u_C	0	u_C	0
S_1 fault	u_C	0	0	0
S_2 fault	u_C	u_C	u_C	0

$i_{\rm arm} < 0$, and the capacitor is always inserted into the main circuit and continuously charged when $i_{\rm arm} > 0$. In this case, the capacitor voltage will increase as well because it absorbs much more power than that of normal submodules. In general, the submodule with switch open-circuit faults is subject to capacitor overvoltage problems, which might lead to waveform distortions and malfunction of the MMC system. Therefore, the switch open-circuit faults should be detected and located as soon as possible so that the submodule bypassing and necessary fault-tolerant operation can be seamlessly activated before catastrophic failures occur in the MMC.

The submodule output voltage, which is the voltage across the two terminals of each submodule, can be determined by the gating signals and the direction of the arm current in all conditions. As summarized in Table I, the device fault can be detected and located based on the combination of current direction, gating signals, and the submodule terminal voltage $u_{\rm SM}$. Specifically, $u_{\rm SM} = 0$ when $i_{\rm arm} < 0$ and $S_1 = 1$ and $S_2 = 0$ indicate that S_1 is open circuit, and $u_{\rm SM} = u_C$ when $i_{\rm arm} > 0$ and $S_1 = 0$ and $S_2 = 1$ implies that an open-circuit fault occurs at S_2. Therefore, the submodule terminal voltage is utilized in the switch open-circuit fault diagnosis in this paper.

B. Proposed Open-Circuit Fault Diagnosis

The submodule voltage has to be measured in order to utilize its characteristics to detect the switch open-circuit fault. Normally, adding extra voltage transducers and hardware circuitry into the MMC is undesirable from a cost-effective point of view. It should be noted that there is already one voltage sensor embedded in each submodule for capacitor voltage control and balancing purposes. Therefore, the measuring points of the existing voltage sensors are reconfigured so that the submodule terminal voltage can be monitored. As can be seen in Fig. 4, one of the measurement points is moved to the middle point of the two switching devices to monitor the submodule terminal voltage.

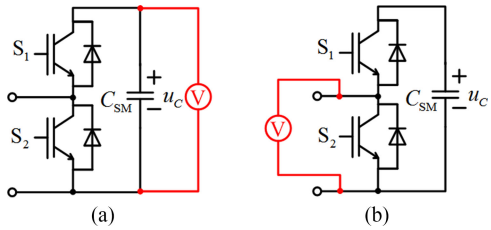

Fig. 4. Measurement points of the voltage sensor: (a) conventional; (b) proposed.

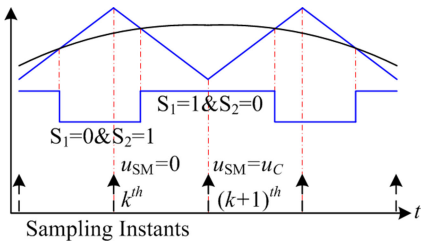

Fig. 5. Voltage sampling instant associating with the triangular carrier.

The voltage measurement instant are associated with the triangular carrier as shown in Fig. 5, where the terminal voltage $u_{\rm SM}$ is measured at the peaks and valleys of the triangular carrier. According to Fig. 5 and Table I, in normal operations, $u_{\rm SM}$ is equal to zero when the carrier is at peak values (for example, the kth sampling instant) and $u_{\rm SM} = u_C$ when the carrier reaches zero (the $(k+1)$th sampling instant). Therefore, $u_{\rm SM} = 0$ and $u_{\rm SM} = u_C$ are alternatively obtained at sampling instants triggered by the ePWM module in the local controller. The capacitor voltages are conditionally accessible during the MMC start-up precharging and the temporary shutdown cases as long as the capacitor is charged through the body diode of the switch S_1.

The implementation of the switch open-circuit fault diagnosis combined with the capacitor voltage measurement in a local controller is illustrated by the flowchart shown in Fig. 6. Two objectives, i.e., capacitor voltage feedback for control loops and open-circuit fault diagnosis, have to be simultaneously achieved. In the normal operation, the measured voltage at the carrier valleys are directly deemed as the submodule capacitor voltage and utilized in capacitor voltage control and balancing, as long as the corresponding submodule is not overmodulated. On the other hand, switch open-circuit faults can be identified by the combination of sampling instants, submodule terminal voltage, and arm current direction. If $u_{\rm SM} > u_{\rm SM\_thr1} = 0.7u_C{}^*$ is obtained at the peak points of the carrier for $i_{\rm arm} > 0$, an open-circuit fault occurs at S_2; if $u_{\rm SM} < u_{\rm SM\_thr2} = 0.3u_C{}^*$ is obtained at the valley points of the carrier for $i_{\rm arm} < 0, S_1$ is open circuit.

It should be noted that the terminal voltage sampled at carrier valley being less than $u_{\rm SM\_thr2}$ might be caused either by

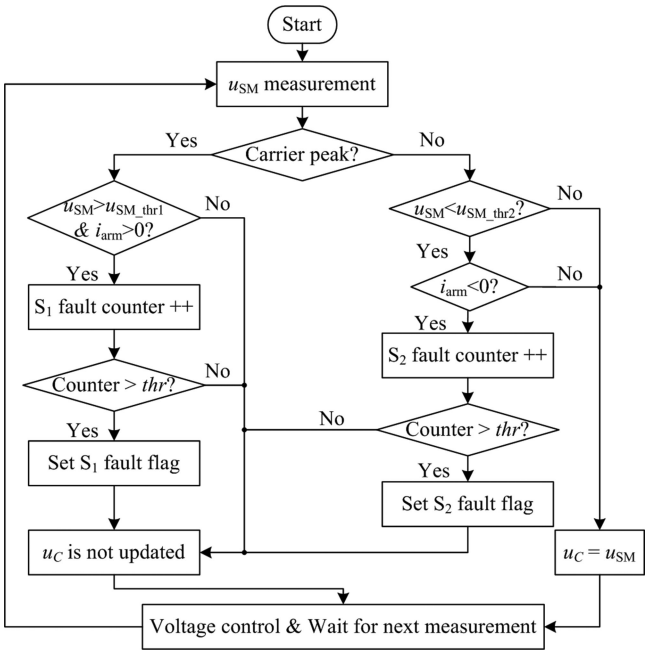

Fig. 6. Flowchart of the fault diagnosis in the local controller.

the low-capacitor voltage or S_2 open-circuit fault. In this case, arm current direction is required in order to determine if the measured terminal voltage can be used as the capacitor voltage. $i_{\rm arm} > 0$ implies that the capacitor voltage is actually quite low so that $u_C = u_{\rm SM}$ is utilized in capacitor voltage control, while u_C is not updated if $i_{\rm arm} < 0$. This mechanism prevents that, when there is an open-circuit fault at S_2, the incorrect voltage is utilized in the closed-voltage control loops and consequently leads to rapid divergence or severe oscillation of submodule capacitor voltages. The fault counters and threshold (thr), as shown in Fig. 6, are adopted to prevent false alarm introduced by measurement noises or disturbances. The fault flags are set only if the values of the counters are higher than the threshold, and the counters are cleared if the values are lower than the threshold for one fundamental period. Therefore, a trade-off is made between the speed and accuracy of fault identification.

Since the proposed fault detection method is directly based on real-time measurements, it is possible to identify the faulty switches within a short time, e.g., a few sampling intervals. Moreover, as the device fault detection is implemented in the local controller with the information of only current direction, capacitor voltage, and the sampling instant of the corresponding submodule, it can be easily extended to MMCs with a large number of submodules and is able to simultaneously identify multiple device open-circuit faults. The identified faulty switch information could be also helpful for future fault analysis, system maintenance, and components replacement.

IV. Proposed Fault-Tolerant Operation Scheme

After identifying the open-circuit fault, the local controller immediately bypasses the corresponding submodule with the faulty switch and sends a warning message to the central controller to indicate the bypassed submodule. The central controller adjusts the capacitor voltage references for remaining submodules according to the operation condition of the MMC and broadcasts the information regarding the bypassed submodule to other submodules in the same arm within one or two control cycles. The remaining submodules then operate in a fault-tolerant mode after receiving that information. The interval between the fault occurrence and the fault-tolerant operation is short enough so that the MMC works seamlessly during the operation mode transition. The control loops in the central and local controllers are scarcely affected by the fault-tolerant operation.

A. Normal Operation

The distributed control system in the normal operation of the MMC is depicted in Fig. 7 to clearly show the signals required by different controllers. The output current i_o regulation, the $i_{\rm diff\_dc}{}^*$ calculation for active power balancing and capacitor voltage reference generation are implemented in the central controller. A proportional-resonant (PR) controller is adopted to regulate the output current. The output of the PR controller is used as the reference of the MMC output voltage $u_o{}^*$. A dc current $i_{\rm diff\_dc}{}^* = U_o I_o \cos(\phi_o)/(2U_{\rm dc})$ is calculated for the power balance between the dc and ac sides of the MMC. The reference of the submodule capacitor voltage $u_C{}^*$ can be obtained according to the dc bus voltage and operation requirements of the MMC. Practically, the rated amplitude of the output voltage in the normal operation can be designed as $0.5U_{\rm dc}N/(N+N_r)$. It is reasonable if a relatively large number of submodules are adopted in the MMC and $N >> N_r$. Therefore, defining $u_C{}^* = U_{\rm dc}/(N+N_r)$ for all $N+N_r$ submodules in each arm, the N normal submodules are capable of generating the required output voltage with reduced voltage stress on the submodule capacitors. The rated working voltage of the submodule capacitor can be selected as $U_{\rm dc}/N$ while its voltage limitation is $(1+\alpha)U_{\rm dc}/N$, where α in per unit is the voltage margin reserved. Note that $u_C{}^*$ is not necessarily sent to local controllers in each control cycle since, ideally, it is unchanged in the normal operation of the MMC. Only the four signals $u_o{}^*, i_{\rm diff\_dc}{}^*, i_{o,}$ and $i_{\rm diff}$ have to be transmitted to the local controller for the real-time controls in each control cycle.

As can be seen in the local controller part in Fig. 7, the internal dynamics of the MMC, i.e., differential current and capacitor voltage, are locally controlled in individual submodule without the awareness of capacitor voltages in other submodules. The detailed control loops in the *k*th local controller are shown in Fig. 8. The reference of the inner differential current $i_{\rm diff}{}^*$ is obtained from capacitor voltage control in the local controller and active power balancing in the central controller $(i_{\rm diff\_dc}{}^*)$. Two resonant (R) controllers coping with the signal at the fundamental and second-order frequencies are paralleled to a proportional (P) controller to regulate $i_{\rm diff}$. The capacitor average voltage control loop, whose reference $u_C{}^*$ is given by the central controller, is illustrated in Fig. 8, where the equilibrium voltage is $U_{\rm dc}/(N+N_r)$ and a feedforward path is designed to regulate the average voltage by adjusting the equivalent number of submodules inserted into the phase leg. In addition, a

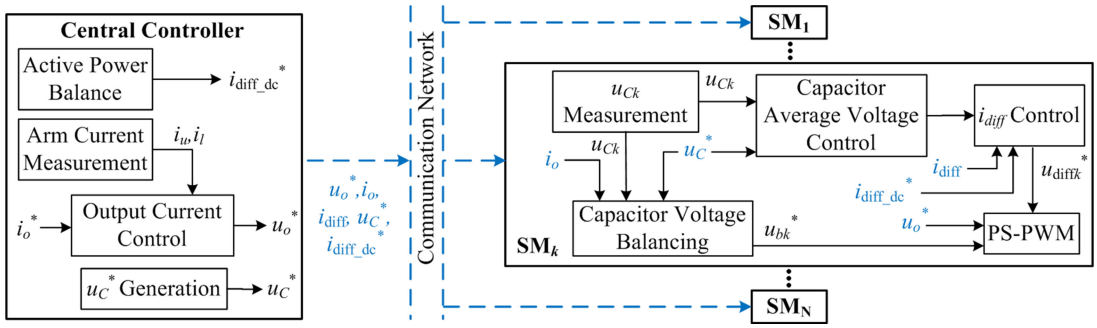

Fig. 7. Block diagram of the signals for the distributed control.

proportional controller is employed to fine-tune the capacitor average voltage in the submodule. An ac component with fundamental frequency $(u_{bk}{}^*)$ is intentionally added to the output voltage reference to generate a small amount of controllable active power, in order to balance the submodule capacitor voltages.

B. MMC Operates With Submodule Bypassed

After identifying the switch open-circuit fault, the corresponding submodule is bypassed and the MMC has to operate with reduced and asymmetrical numbers of submodules in arms. Noting that the output reference calculated by the central controller for all submodules is identical as $u_o{}^*$, a distorted output voltage will be inevitably introduced since the numbers of the submodules in the upper and lower arms are different due to the failure. Assuming N_f submodules are bypassed in the upper arm and denoting the well-balanced capacitor voltages in the two arms as u_{Cu} and u_{Cl}, respectively, the inserted voltages of the two arms can be expressed as

$$\begin{cases} u_{u\_f} = u_{Cu} n_u (N + N_r - N_f) \\ u_l = u_{Cl} n_l (N + N_r) \end{cases}. \tag{7}$$

Ignoring the voltage ripples in (6), the capacitor voltages can be denoted as $u_{Cu} = u_{Cl} = U_C = U_{\rm dc}/(N + N_r)$. According to (1), (4), (5), and (7), the output voltage of the MMC under the fault condition can be written as

$$u_{o\_f} = \frac{u_l - u_{u\_f}}{2} \approx \left(1 - \frac{0.5N_f}{N + N_r}\right) u_o + \frac{0.25N_f}{N + N_r} U_{\rm dc} \tag{8}$$

where the terms containing $u_{\rm diff}{}^*$ are ignored since normally $u_{\rm diff}{}^* << u_o{}^*$. It is obvious in (8) that the fundamental component of the MMC output voltage is reduced by $0.5u_o N_f/(N + N_r)$ and a dc bias $0.25U_{\rm dc}N_f/(N + N_r)$ exists in the output voltage. The output current regulation in the central controller will try to force the output current to track its reference by adjusting the output voltage reference as $u_{o\_f}{}^*$. Letting $u_{o\_f} = u_o$, the voltage reference $u_{o\_f}{}^*$ under the fault condition can be obtained as

$$u_{o\_f}{}^* = -\frac{0.5N_f}{N + N_r - 0.5N_f} + \frac{N + N_r}{N + N_r - 0.5N_f} \frac{2U_o \cos(\omega_o t)}{U_{\rm dc}}. \tag{9}$$

Moreover, the voltage applied onto the arm inductors and resistors in the fault condition can be expressed as

$$\begin{aligned} u_{\rm diff\_f} &= U_{\rm DC} - u_l - u_{u\_f} \\ &= U_C \left[2(N + N_r) u_{\rm diff}{}^* + N_f \left(0.5 - 0.5u_{o\_f}{}^* - u_{\rm diff}{}^*\right)\right] \\ &= 2U_{\rm dc} u_{\rm diff}{}^* + \frac{0.5N_f U_{\rm dc}}{N + N_r - 0.5N_f} - \frac{N_f U_o \cos(\omega_o t)}{N + N_r - 0.5N_f} - \frac{N_f U_{\rm dc} u_{\rm diff}{}^*}{N + N_r}. \end{aligned} \tag{10}$$

The first term on the right-hand side of (10) is the differential voltage applied in normal conditions. The other three terms will introduce a dc bias and low-frequency components into the differential voltage and consequently result in undesirable capacitor voltage shifting [11] and low frequency circulating current ripples in the phase leg, which are disturbances for internal dynamics controls.

Moreover, the switching functions of the *i*th submodule in the upper and lower arms generated based on the PS-PWM can be

$$\begin{cases} s_{u\_i} = \frac{1}{2} - \frac{u_{o\_f}{}^*}{2} + \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{mk\pi}{2}\right) \times \cos\left[k\left(\omega_c t + \alpha + \beta + (i-1)\frac{2\pi}{N+N_r}\right) + n(\omega_o t + \pi)\right] \\ s_{l\_i} = \frac{1}{2} + \frac{u_{o\_f}{}^*}{2} + \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{mk\pi}{2}\right) \times \cos\left[k\left(\omega_c t + \alpha + (i-1)\frac{2\pi}{N+N_r}\right) + n\omega_o t\right] \end{cases} \tag{11}$$

$$\begin{cases} s_u = \frac{N+N_r-N_f}{2} - \frac{(N+N_r-N_f)u_{o\_f}{}^*}{2} + \sum_{i=1}^{N+N_r \,\&\, i \notin N_{\rm by}} \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] \\ \times J_n\left(\frac{mk\pi}{2}\right) \times \cos\left[k\left(\omega_c t + \alpha + \beta + (i-1)\frac{2\pi}{N+N_r}\right) + n(\omega_o t + \pi)\right] \\ s_l = \frac{N+N_r}{2} + \frac{(N+N_r)u_{o\_f}{}^*}{2} + \sum_{i=1}^{N+N_r} \sum_{k=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2}{k\pi} \sin\left[\frac{(k+n)\pi}{2}\right] \times J_n\left(\frac{mk\pi}{2}\right) \times \cos\left[k\left(\omega_c t + \alpha + (i-1)\frac{2\pi}{N+N_r}\right)\right. \\ \left. + n\omega_o t\right]. \end{cases} \tag{12}$$

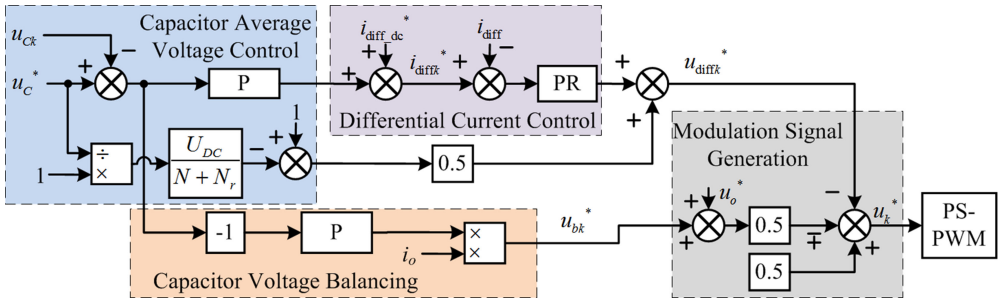

Fig. 8. Block diagram of the local controller.

expressed in Fourier series form [17]–[19] as in (11) shown at the bottom of the previous page, where $m = 2U_o/U_{\rm dc}$, k is the harmonic order of the carrier and n is the harmonic order of the reference. J_n refers to the Bessel function and ω_c is the angular frequency of the carrier. α is the phase displacement between the carrier waves and the modulating signal, and β indicates the angle displacement between the carrier waveforms in the upper and lower arms. Denoting the N_f bypassed submodules in the upper arm as $\mathrm{N_{by}} = \{N_{by\_1}, \ldots, N_{by\_Nf}\}$, the sums of the switching functions in the upper and lower arms can be expressed as in (12) shown at the bottom of the previous page. Noting that (13) shown at the bottom of the page, and (12) can be rewritten as in (14).

Although α and β are selected so that the low-order switching harmonics can be well canceled [17], [18] in normal operations, (14) suggests that harmonics and sidebands around carrier frequency ω_c can be found due to the asymmetrical switching actions in s_u after bypassing N_f submodules in the upper arm.

C. Proposed Fault-Tolerant Operation Scheme

In the fault-tolerant operation, the output and internal dynamics of the MMC should keep the same as those in the normal operation, with balanced capacitor average voltages in the same arm or phase leg [8]. The dc and fundamental components in the arm currents have to remain unchanged for the same input and output power of the MMC. Equation (7) suggests that the inserted voltage in the upper arm is reduced because N_f submodules are bypassed. Therefore, the output voltage of each submodule in the upper arm has to be increased to meet the requirement of the loads, which can be achieved by increasing the amplitude of the fundamental component in n_{uk} or increasing the average capacitor voltage in the faulty arm as long as the capacitors are in the safe operation area. On the other hand, the input dc power of submodules in the upper arm has to be accordingly adjusted as well to compensate their output active power, by introducing a dc bias into n_{uk}. The proposed fault-tolerant operation can be implemented in two scenarios, according to the number of faulty submodules.

1) Scenario I: $N_r \geq 2N_f$: The maximum symmetrical output voltage of the MMC under the fault condition can be expressed as

$$\min\left[\left(N+N_r-N_f\right)u_{Cu\_f}, \left(N+N_r\right)u_{Cl}\right] - \frac{U_{\rm dc}}{2} \geq \frac{N}{N+N_r}\frac{U_{\rm dc}}{2} \tag{15}$$

where u_{Cu_f} is the balanced submodule capacitor voltage in the upper arm with N_f submodules bypassed. It should be noted that $u_{Cl} = U_{\rm dc}/(N+N_r)$ always satisfies the inequality (15), therefore only the $(N+N_r-N_f)u_{Cu\_f}$ term is discussed. The minimum u_{Cu_f} required to generate the desired output voltage can be obtained as

$$u_{Cu\_f} = \left(\frac{N+0.5N_r}{N+N_r}\right)\frac{U_{\rm dc}}{(N+N_r-N_f)} \tag{16}$$

$$u_{Cu} - u_{Cu\_f} = \frac{0.5N_r - N_f}{(N+N_r-N_f)(N+N_r)}U_{\rm dc}. \tag{17}$$

$$\begin{cases} \sum_{i=1}^{N+N_r}\cos\left((i-1)\frac{2k\pi}{N+N_r}\right) = 0, \frac{k}{N+N_r} \notin \mathbb{N}^+ = \{1,2,\ldots\} \\ \sum_{i=1}^{N+N_r}\sum_{k/(N+N_r)\in\mathbb{N}^+}\cos\left[k\left(\omega_c t+\alpha+(i-1)\frac{2\pi}{N+N_r}\right)+n\omega_o t\right] = (N+N_r)\sum_{k/(N+N_r)\in\mathbb{N}^+}\cos\left[k\left(\omega_c t+\alpha\right)+n\omega_o t\right] \end{cases} \tag{13}$$

$$\begin{cases} s_u = \frac{N+N_r-N_f}{2} - \frac{(N+N_r-N_f)u^*_{o\_f}}{2} + \\ \sum_{k/(N+N_r)\in\mathbb{N}^+}\sum_{n=-\infty}^{\infty}\frac{2(N+N_r)}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right]\times J_n\left(\frac{mk\pi}{2}\right)\times\cos\left[k\left(\omega_c t+\alpha+\beta\right)+n\left(\omega_o t+\pi\right)\right] \\ -\sum_{i\in\mathbb{N}_{\rm by}}\sum_{k=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{2}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right]\times J_n\left(\frac{mk\pi}{2}\right)\times\cos\left[k\left(\omega_c t+\alpha+\beta+(i-1)\frac{2\pi}{N+N_r}\right)+n\left(\omega_o t+\pi\right)\right] \\ s_l = \frac{N+N_r}{2} + \frac{(N+N_r)u^*_{o\_f}}{2} + \sum_{k/(N+N_r)\in\mathbb{N}^+}\sum_{n=-\infty}^{\infty}\frac{2(N+N_r)}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right]\times J_n\left(\frac{mk\pi}{2}\right)\times\cos\left[k\left(\omega_c t+\alpha\right)+n\omega_o t\right] \end{cases} \tag{14}$$

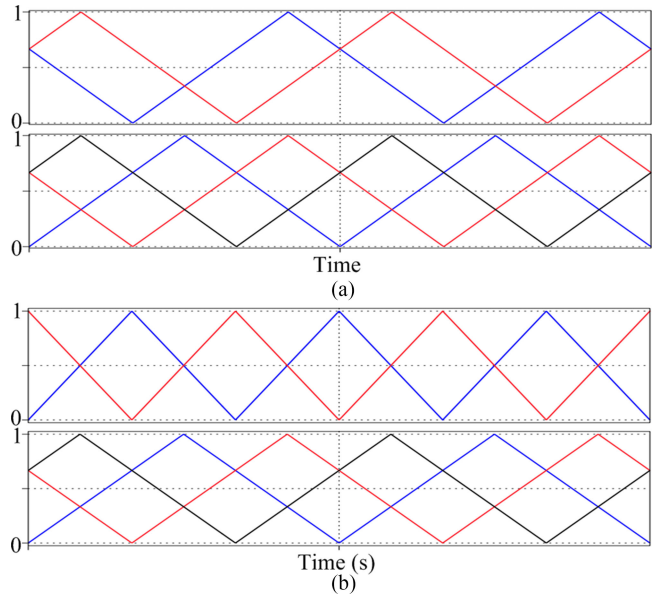

Fig. 9. Triangular carriers: (a) In normal PS-PWM scheme while one submodule is bypassed; (b) In modified PS-PWM scheme.

It can be seen in (17) that the capacitor average voltage in the normal operation ($u_{Cu} = U_{\rm dc}/(N+N_r)$) is sufficient to generate the required output voltage in the case of $N_r \geq 2N_f$. Therefore, in this scenario, the average capacitor voltage reference for all submodules remains unchanged. By rescaling the modulation signals for the submodules in the upper arm by $(N+N_r)/(N+N_r-N_f)$, both the output voltage and the dc bias for active power balancing are increased. Ideally, the voltage inserted into the upper arm is $u_u = u_{Cu} n_{uk} (N+N_r)$, which is the same with that in the normal operation. Consequently, the output and differential voltages remain uninfluenced even N_f submodules are bypassed in the upper arm.

Moreover, the harmonics and sidebands around the frequency ω_c in (14) significantly increase the current ripples in the upper arm, since the lowest frequency of the switching harmonics in the arm current is reduced from $(N+N_r)f_c$ to f_c. In order to achieve the same switching harmonics cancellation, the carrier frequency of the submodules in the upper arm is increased to $(N+N_r)/(N+N_r-N_f)f_c$ and the phase displacement between adjacent carriers is reset to $2\pi/(N+N_r-N_f)$ to obtain the symmetrically distributed carriers shown in Fig. 9. The modified PS-PWM scheme shown in Fig. 9(b) also guarantees the same control bandwidth for current control loops.

Applying the aforementioned modulation signal rescaling, triangular carrier frequency adjusting and phase angle modification, (14) can be expressed in (18) as shown at the bottom of this page, which reveals that the same low-frequency components and switching harmonic cancellation can be achieved as in the normal operation. Noting that the amplitude of the voltage ripples U_{C_1} and U_{C_2} in (6) are influenced by the modulation signals [2], the submodule capacitor voltage in the upper arm under the fault-tolerant operation can be expressed as

$$\begin{cases} u_{Cu\_f} = U_C + U_{C\_1\_f}\sin(\omega_o t + \phi_{C\_1\_f}) + U_{C\_2\_f} \\ \quad \sin(2\omega_o t + \phi_o) \\ U_{C\_1\_f} = \sqrt{\frac{\left(\frac{N+N_r}{N+N_r-N_f}\right)^4 m^4\cos^4\phi_o + 4}{m^4\cos^4\phi_o + 4}}\, U_{C\_1} \\ U_{C\_2\_f} = \frac{N+N_r}{N+N_r-N_f} U_{C\_2}. \end{cases} \tag{19}$$

The voltage applied on the arm inductors and resistors can be obtained as in (20) as shown at the bottom of the next page. Fundamental components, which are introduced by the asymmetrical voltage ripples across the capacitors in the upper and lower arms, can be found in (20) and eventually induce fundamental circulating current ripples in the phase leg. Such fundamental circulating current can be suppressed by the paralleled resonant controller coping with signals at the fundamental frequency in the differential current controller shown in Fig. 8.

The fault-tolerant operation scheme in this scenario can be easily implemented in the distributed control architecture. After receiving the warning message from a particular submodule N_p, the central controller informs the submodules in the same arm that the N_pth submodule is bypassed and these submodules should be in fault-tolerant operation. By setting ePWM period registers of remaining local controllers in the faulty arm to be $T_c(N+N_r-N_f)/(N+N_r)$, the frequency of the carrier is increased and the amplitude of the triangle is reduced. The modulation signals for the submodules in the corresponding arm are consequently rescaled. The phase registers of these ePWM modules are updated as well to ensure the phase displacement of $2\pi/(N+N_r-N_f)$ among triangular carriers. Since each submodule possesses a unique SN, the exact value assigned to the phase register can be decided based on the number of remaining submodules and its SN. To be specific, only the submodule having an SN behind the bypassed N_pth submodule need to reset its phase register according to its new sequence in the faulty arm. The overall process can be completed within a few control cycles.

2) Scenario II: $2N_f > N_r \geq N_f$*:* Since the right-hand side of (17) is less than zero in this scenario, the capacitor voltages in the faulty arm should be increased to generate the desired output voltage with reduced submodules. All the values assigned to the period and phase registers in the local controller are the same with those in Scenario I. The only difference is that the new capacitor voltage reference $u_{C\_f}{}^*$ is calculated according to the number of the remaining submodules in the faulty arm,

$$\begin{cases} \mathrm{s}_u = \frac{N+N_r}{2} - \frac{(N+N_r)u_o{}^*}{2} + \sum_{k/(N+N_r-N_f)\in\mathbb{N}^+}\sum_{n=-\infty}^{\infty}\frac{2(N+N_r-N_f)}{k\pi}\sin\left[\left(\frac{N+N_r}{N+N_r-N_f}k+n\right)\frac{\pi}{2}\right] \\ \times J_n\left(\frac{N+N_r}{N+N_r-N_f}\frac{mk\pi}{2}\right)\times\cos\left[\frac{N+N_r}{N+N_r-N_f}k\left(\omega_c t+\alpha+\beta\right)+n\left(\omega t+\pi\right)\right] \\ \mathrm{s}_l = \frac{N+N_r}{2} + \frac{(N+N_r)u_o{}^*}{2} + \sum_{k/(N+N_r)\in\mathbb{N}^+}\sum_{n=-\infty}^{\infty}\frac{2(N+N_r)}{k\pi}\sin\left[\frac{(k+n)\pi}{2}\right]\times J_n\left(\frac{mk\pi}{2}\right)\times\cos\left[k\left(\omega_c t+\alpha\right)+n\omega t\right] \end{cases} \tag{18}$$

TABLE II
PARAMETERS OF THE MMC SYSTEM

Parameters	Values
DC bus voltage: $U_{\rm dc}$	240 V
DC bus capacitance: $C_{\rm dc}$	4.4 mF
Output inductance: L_o	0.7 mH
Load resistance: R_l	16 Ω
Rated output frequency: f_o	50 Hz
No. of SM in each arm: N	3
Arm inductance: $L_{\rm arm}$	5 mH
Arm resistance: $R_{\rm arm}$	0.025 Ω
SM capacitance: $C_{\rm SM}$	940 uF
Carrier frequency: f_c	2 kHz

TABLE III
CONTROLLER PARAMETERS

Current Controllers	
Proportional gain for i_o : $K_{\rm P\_io}$	15
Resonant gain for i_o : $K_{\rm R\_io}$	400
Proportional gain for $i_{\rm diff}$: $K_{\rm P\_idiff}$	25
Resonant gain for $i_{\rm diff}$ (50 Hz) :$K_{\rm R1\_idiff}$	500
Resonant gain for $i_{\rm diff}$ (100 Hz) :$K_{\rm R2\_idiff}$	500
Voltage Controllers	
Proportional gain for voltage averaging: $K_{\rm P\_uC\_ave}$	0.07
Proportional gain for voltage balancing: $K_{\rm P\_uC\_bal}$	4

e.g., $u_{C\_f}{}^* = U_{\rm dc}/(N + N_r - N_f)$. In this scenario, the voltage ripples across the capacitors in the upper and lower arms are almost the same since the modulation signals for all submodules in that phase are nearly the same. Therefore, little fundamental circulating current is induced in the phase leg. The current ripples in the faulty arm caused by switching actions have the same frequencies as those in Scenario I.

V. EXPERIMENTAL RESULTS

The proposed fault diagnosis and fault-tolerant operation schemes for the MMC are implemented in a laboratory prototype and the experimental verifications are presented in the following subsections. The key parameters of the single-phase MMC system shown in Fig. 1 are listed in Table II. Three submodules are connected in series in each arm. The resistor R_l and inductance L_o are regarded as an inductive–resistive load for the MMC in this paper. The equivalent switching frequency of the MMC is $6f_c = 12$ kHz [10], [17], [18]. The sampling frequency in the central controller is designed to be $f_s = 6$ kHz, and the control system is synchronized with it, having a period of $T_s = 1/f_s$. On the other hand, the sampling frequency for capacitor voltage measurement in the local controller is $f_c = 2$ kHz. The period for the voltage control cycle is $T_c = 1/f_c$. Therefore, there will be a $1.5T_s$ and $1.5T_c$ digital control delays [20]–[22] in the current and capacitor voltage control loops. The different digital control delays have to be taken into account while designing the controller parameters [13]. The controller parameters for the MMC system can be found in Table III.

A. MMC Performance in the Normal Operation

The performance of the MMC in the normal operation is illustrated in the following experiments. The capacitor voltage references for all submodules were set to be 80 V ($U_{\rm dc}/(N + N_r)$) and the amplitude of the output voltage was 96 V (output current is 6 A). Fig. 10 shows the voltage and current waveforms of the MMC in steady-state operation, where a seven-level output

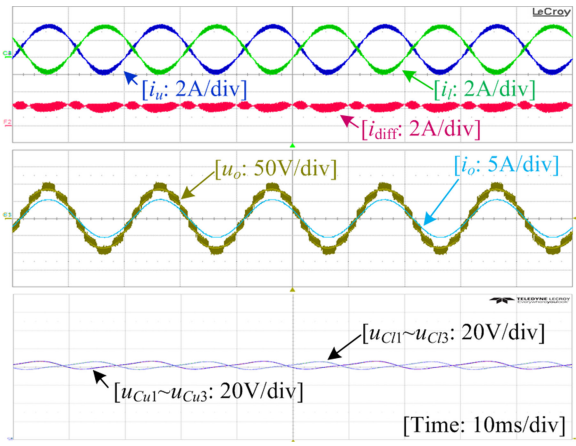

Fig. 10. Voltage and current waveforms of the MMC in the steady-state operation.

voltage and a sinusoidal output current tracking its reference accurately can be observed. The second-order harmonics in $i_{\rm diff}$ is effectively suppressed with the help of the resonant controller, leaving a dc component in $i_{\rm diff}$ with negligible ripples. Moreover, the submodule capacitor voltages are well balanced around their setting point 80 V. The dynamic response of the MMC during large current reference step changes was evaluated in the experiments, in which the output current was initially set to be 3 A and then stepped to 6 A at $t1$. The voltage and current waveforms of the MMC with the distributed control are depicted in Fig. 11, where the MMC system is stable and the transients are smooth during large operation point step changes.

The waveforms of the MMC in the steady state and during step changes imply that the voltage measurement point modification and measured data processing proposed in this paper will not introduce any influence into the control loops. All the MMC control objectives, such as output and internal dynamics regulation, are achieved without performance deterioration. Moreover, the proposed voltage measurement and fault diagnosis are immune to the noises and disturbances in the steady state

$$\begin{aligned} u_{\rm diff} &= U_{\rm dc} - u_{u\_f} - u_l = U_{\rm dc} - (N + N_r)\left\{u_{Cu\_f}\left[0.5 - 0.5m\cos(\omega_o t)\right] + u_{Cl}\left[0.5 + 0.5m\cos(\omega_o t)\right]\right\} \\ &= \tfrac{(N+N_r)}{2}\left[U_{C\_1}\sin(\omega_o t + \phi_{C\_1}) - U_{C\_1\_f}\sin(\omega_o t + \phi_{C\_1\_f}) + \tfrac{0.5mN_f U_{C\_2}}{N+N_r-N_f}\sin(\omega_o t + \phi_o) + \text{other terms}\right] \end{aligned} \tag{20}$$

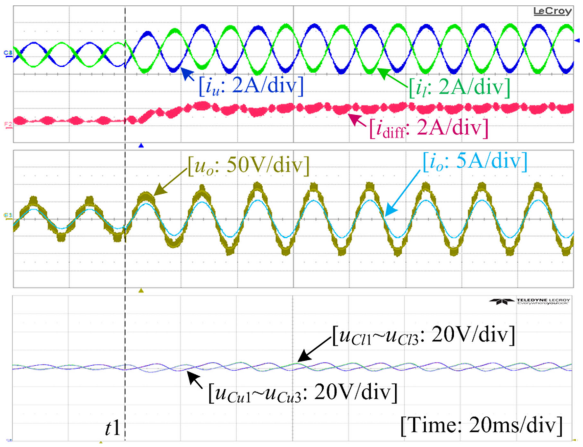

Fig. 11. Voltage and current waveforms of the MMC during current reference step changes.

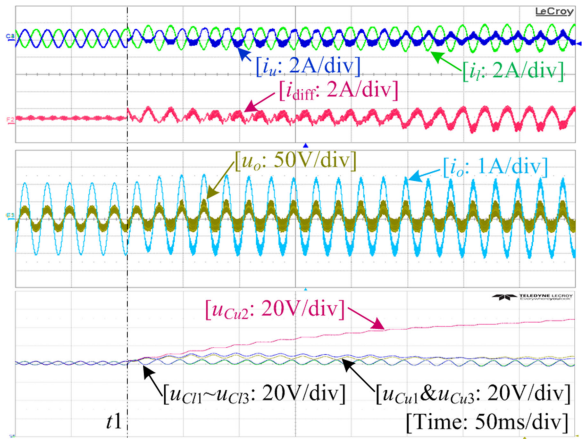

Fig. 12. Voltage and current waveforms of the MMC with S_1 open-circuit fault in SM_{u2}.

and during large step changes since no false alarm was triggered in the normal operation of the MMC.

B. MMC Performance With Switch Open-Circuit Faults

In the following sets of experiments, the MMC performance in fault-tolerant operation with one and multiple switch open-circuit faults was investigated and evaluated. The open circuit fault of the switch was generated by applying a low-level gating signal to the corresponding device. The open-circuit faults at different switches were identified by submodules themselves. After identifying the fault, the local controller bypassed the faulty submodule by assigning a high-level gating signal to the lower switch in that submodule. The central controller coordinated the operation of remaining submodules as soon as it had received the fault information.

1) Single Switch Open Circuit: In this set of experiments, single switch open-circuit fault in the second submodule in the upper arm (SM_{u2}) was generated.

a) Fault-tolerant operation Scenario I: In this scenario, $N = 1, N_r = 2$, and $N_f = 1$ were selected and the maximum output voltage of the MMC was 40 V according to the discussion in Section IV-A. The output current was regulated as 2.3 A so that the amplitude of the output voltage was 37 V. The average capacitor voltage of the submodules in the entire phase leg remained unchanged as 80 V.

The voltage and current waveforms of the MMC when the switch S_1 in SM_{u2} was forced to open are presented in Fig. 12, where no fault diagnosis and fault-tolerant operation was applied. It can be seen that the arm currents and differential current are highly distorted. An obvious fundamental component can be observed in the differential current, and high switching current ripples can be found in the arm current as well. The capacitor voltage of SM_{u2} increases to a quite high value and might result in capacitor failure due to overvoltage. Once the switch open-circuit fault occurs, the MMC system without fault diagnosis and fault-tolerant operation has to shut down to avoid secondary failure.

Fig. 13 illustrates the waveforms of the MMC with S_1 open-circuit fault in SM_{u2} while the proposed fault diagnosis and

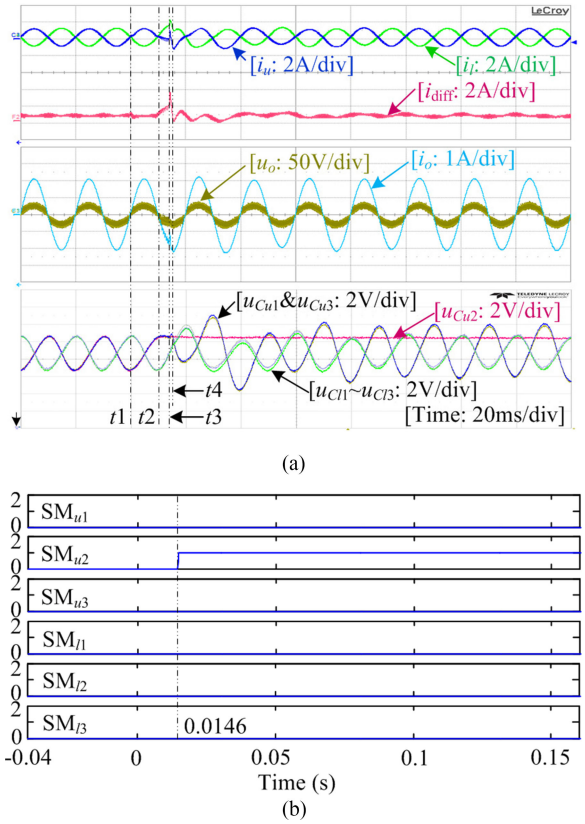

Fig. 13. Waveforms in fault-tolerant operation Scenario I with S_1 open-circuit fault in SM_{u2}: (a) current and voltage waveforms; (b) fault detection results for the six submodules.

fault-tolerant operation were applied. The open-circuit fault detection results of all submodules are presented in Fig. 13(b), where the curves indicate the status of the devices in each submodule. The S_1 open-circuit fault is detected if the status is 1 and the S_2 open-circuit fault is identified if the status is 2. After S_1 being forced to open at $t1 = 0$ s, the MMC operated normally with slightly distorted current in the upper arm since the arm current was positive and flew as normal through the body diode of S_1, until the upper arm current crossed zero at $t2 = 11.8$ ms. The fault diagnosis started to execute from $t2$

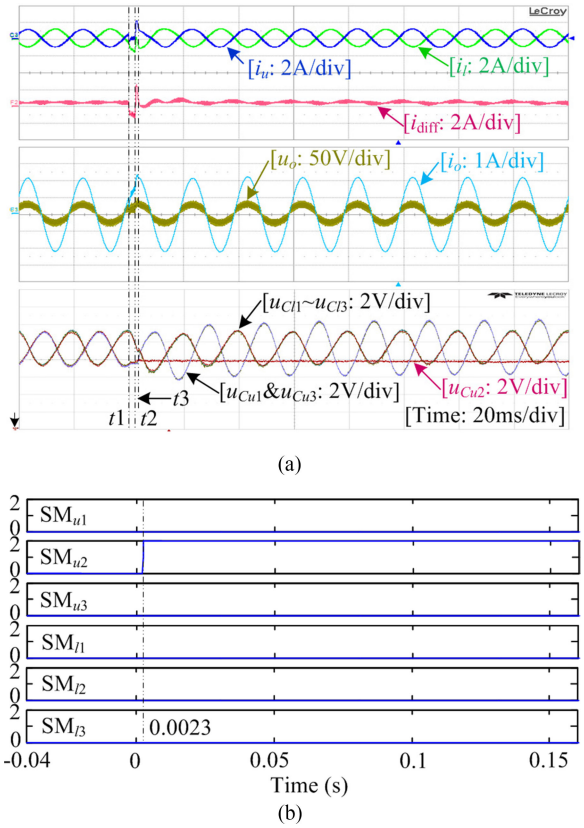

Fig. 14. Waveforms in fault-tolerant operation Scenario I with S_2 open-circuit fault in SM_{u2}: (a) current and voltage waveforms; (b) fault detection results for the six submodules.

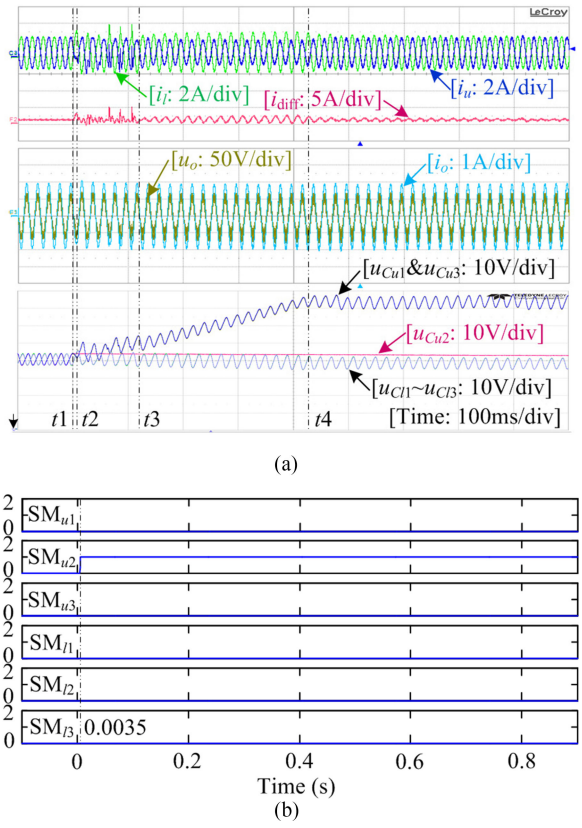

Fig. 15. Waveforms in fault-tolerant operation Scenario II with S_1 open-circuit fault in SM_{u2}: (a) current and voltage waveforms; (b) fault detection results for the six submodules.

and the S_1 open-circuit fault in SM_{u2} was correctly identified at $t3 = 14.6$ ms, 2.8 ms later after $t2$, as shown in Fig. 13(b). After $t3$, u_{Cu2} was a straight line since SM_{u2} was immediately bypassed. The central and local controllers exchanged the necessary fault and operation information, and then the period and phase registers for the PWM generation for submodules in the upper arm were accordingly reset, at $t4 = 15.3$ ms. At $t4$, the process of fault diagnosis and system reconfiguration had completed within 3.5 ms and the MMC operated under the proposed fault-tolerant operation scheme. It is clear in Fig. 13(a) that the output voltage and current were almost the same before and after the open-circuit fault occurred. The current ripple and high-frequency harmonics in the arm currents were scarcely affected by bypassing the faulty submodule, which means that the same equivalent switching frequency and switching harmonics cancellation are achieved for both the normal and fault-tolerant operations. The capacitor voltages remained around 80 V, and higher voltage ripples across the capacitors in the upper arm could be evidently observed. The fundamental component of the differential current, which was introduced by the asymmetrical capacitor voltage ripples, was negligible owing to the paralleled resonant controller for $i_{\rm diff}$ regulation.

The waveforms of the MMC with S_2 open-circuit fault in SM_{u2} are shown in Fig. 14, where the switch open-circuit fault occurred at $t1 = 0$ s, the fault was correctly identified at $t2 = 2.3$ ms and the fault-tolerant operation started at $t3 = 3.6$ ms. Other waveforms of the MMC are similar with those in Fig. 13, which confirms the effectiveness of the proposed fault diagnosis and fault-tolerant operation in Scenario I when there is a single device open-circuit fault in the MMC.

b) Fault-tolerant operation Scenario II: In this scenario, $N = 2, N_r = 1$, and $N_f = 1$ were selected and the maximum output voltage of the MMC was 80 V according to the discussion in Section IV-A. The output current of the MMC was regulated as 4 A so that the amplitude of the MMC output voltage was 64 V. The average capacitor voltage of the submodules in the entire phase leg was initially set as 80 V, and the capacitor voltage references for the submodules in the upper arm increased to 115 V after the faulty submodule in that arm had been bypassed.

The waveforms of the MMC in fault-tolerant operation Scenario II when S_1 open-circuit fault in SM_{u2} occurred at $t1 = 0$ s are depicted in Fig. 15. The open-circuit fault was identified at 3.5 ms and the fault-tolerant operation took effect at $t2 = 4.8$ ms. After that, the capacitor voltage reference for the submodules in the upper arm started to increase to 115 V with a slope of 100 V/s to clearly show the process. u_{Cu1} and u_{Cu3} tried to follow their references as shown in Fig. 15(a). It is obvious that the arm currents, differential current, and capacitor voltages in the upper arm were distorted until $t3 = 126.5$ ms when the capacitor voltages were higher than 92 V so that the output voltage 64 V can be generated as normal according to (15). A fundamental frequency component, which contributes

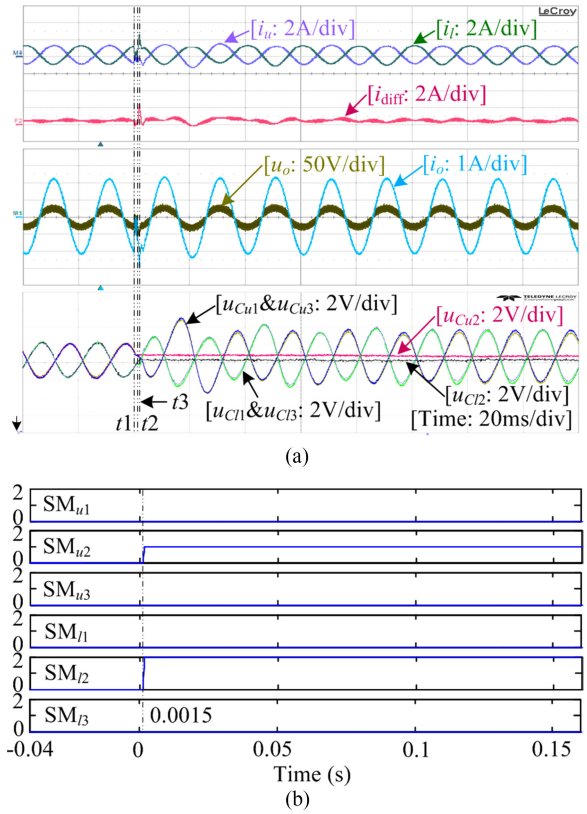

Fig. 16. Waveforms of the MMC with S_1 open-circuit fault in SM_{u2} and S_2 open-circuit fault in SM_{l2}: (a) current and voltage waveforms; (b) fault detection results for the six submodules.

to increasing the capacitor voltages in the upper arm [11], can be found in the differential current from $t3$ to $t4 = 428.8$ ms. Consequently, the capacitors of remaining submodules in the upper arm were charged to 115 V. After $t4$, the MMC operated at a steady state in the fault-tolerant operation Scenario II. The capacitor voltage ripples in the two arms were almost the same, which coincides with the analysis in Section IV-C.

2) Multiple Switch Open Circuit: In this set of experiments, the performance of the fault diagnosis and fault-tolerant operation was investigated while multiple switch open-circuit faults simultaneously occurred. The output current of the MMC was regulated as 2.3 A and the capacitor voltages were maintained as 80 V. Fig. 16 demonstrates the waveforms of the MMC when simultaneous open-circuit faults occurred at S_1 in SM_{u2} and S_2 in SM_{l2}. The faults were given to these two switches simultaneously at $t1 = 0$ s and were identified around $t2 = 1.5$ ms. All the remaining submodules in the upper and lower arms were reconfigured at $t3 = 2.6$ ms, and the MMC then operated under the fault-tolerant operation Scenario I. The waveforms of the MMC were scarcely affected even two submodules were bypassed, except for the higher voltage ripples across the capacitors of remaining submodules in both arms.

VI. Conclusion

This paper has presented a seamless fault-tolerant operation scheme for MMCs with distributed control and hot reserved redundant submodules in order to improve the system reliability. The proposed fault diagnosis is fully implemented in the local controllers of submodules, which can greatly improve the modularity of MMCs without adding additional hardware circuit or sensors. Single and multiple faults can be detected and identified accurately within 3.5 ms, and the diagnosis method is also immune to the noises and disturbances in the system. In order to achieve the same system output, internal dynamics and switching harmonics cancellation as in the normal operation, the period and phase registers of the PWM modules and the capacitor voltages in fault-tolerant operation are properly adjusted according to the information of bypassed submodules. The control loops of the MMC are barely influenced by the fault-tolerant operation. The entire process of fault diagnosis and system reconfiguration for fault-tolerant operation can be completed in about 5 ms after the occurrence of switch open-circuit faults, making the operation transition seamless and reliable. The effectiveness of the proposed fault diagnosis and fault-tolerant operation is confirmed in different scenarios on a laboratory prototype. Seamless operation of the MMC system riding through switch open-circuit faults before the occurrence of severe malfunctions or catastrophic damages is achieved, and good agreement is attained between theoretical analysis and experimental results.

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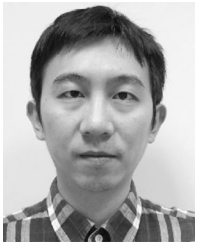

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