Improvement of Power-Conversion Efficiency of AC–DC Boost Converter Using 1:1 Transformer

Seok-Hyeong Ham, Hyung-Jin Choe, Hyeon-Seok Lee, and Bongkoo Kang, *Member, IEEE*

***Abstract*—This paper proposes a circuit structure that can improve the power-conversion efficiency η_e of an AC–DC boost converter. The circuit uses a 1:1 transformer and a voltage boost circuit composed of an inductor, a capacitor, and a diode. The transformer forces the converter to operate in continuous conduction mode for input current, and thereby reduces input ripple. The voltage boost circuit enables the switch to operate in critical conduction mode, so the power loss due to turn-ON of switch and reverse recovery of diode is minimized. The proposed converter has high η_e over a wide range of AC input voltage $V_{\rm ac}$: $\eta_e = 92.9\%$ at $V_{\rm ac} = 85$ V and $\eta_e = 97.4\%$ at $V_{\rm ac} = 265$ V, when the converter was operated at DC output voltage of 400 V and output power of 500 W. The temperature of the switch stabilized at ∼84 °C for $V_{\rm ac} = 85$ V, at ∼70 °C for $V_{\rm ac} = 110$ V, and at ∼42 °C for $V_{\rm ac} = 220$ V, whereas that in other AC–DC converters either failed or stabilized at much higher levels. The proposed converter is well suited to systems that require an input voltage range of 85–265 V in root-mean-square value.**

***Index Terms*—AC–DC power conversion, stress, switched mode power supplies, transformers.**

I. Introduction

THE AC–DC boost converter is simple in structure and can improve the power factor (PF) by shaping the input current waveform [1], [2]. The conventional AC–DC boost converter [see Fig. 1(a)] can be operated in continuous conduction mode (CCM) or critical conduction mode (CrM). The input current $i_{\rm in}$ does not fall to zero during CCM operation, but does fall to zero during CrM operation. The inductor L_b for CCM operation has high inductance to reduce the slope of $i_{\rm in}$. The ripple and peak of $i_{\rm in}$ obtained by CCM operation are smaller than those obtained by CrM operation at the same average value of $i_{\rm in}$ [3]. However, CCM operation produces a power loss from hard switching and reverse recovery of diode D_O [4], [5].

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S.-H. Ham, H.-S. Lee, and B. Kang are with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang 37673, South Korea (e-mail: ham1234@postech.ac.kr; hsasdf@postech.ac.kr; bkkang@postech.ac.kr).

H.-J. Choe is with the LG Display Co. Ltd., Paju 10845, South Korea (e-mail: hjchoe82@lgdisplay.com).

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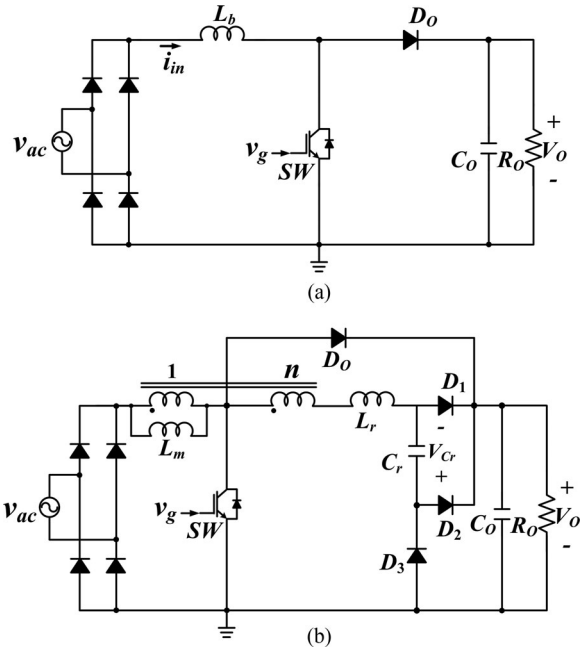

Fig. 1. Structures of (a) conventional AC–DC boost converter and (b) converter of [6].

Several passive snubbers [6]–[10] have been proposed to overcome the problem of CCM operation. The passive snubber in [6] [see Fig. 1(b)] reduces the reverse recovery current of diode D_1, but requires five additional components: a capacitor, three diodes, and a 1:n coupled inductor. The passive snubber in [7] requires a three-winding coupled inductor, two capacitors, and five diodes; one winding of the coupled inductor acts as the boost inductor, so this converter does not require any additional core. The turn-ON snubber enables a soft turning on of switch and reduces the reverse recovery current of output diode. The turn-OFF snubber reduces the voltage stress of switch. The passive snubber in [8] requires a coupled inductor, a resistor, three capacitors, and three diodes. This snubber enables a zero voltage turn ON of switch, while allowing the converter operation in CCM. Also, it solves the problem of the reverse recovery current using the coupled inductor by sending the energy stored in the boost inductor to the output. The snubber in [9] requires two capacitors, three inductors, and four diodes. It reduces the reverse recovery current using a resonant inductor, and provides soft-switching conditions without increasing voltage and current stresses of the switch. The snubber in [10] requires two capacitors, two inductors, and four diodes. It provides zero current turn

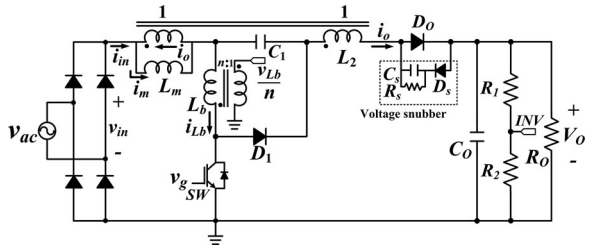

Fig. 2. Structure of the proposed AC–DC boost converter.

ON and zero voltage turn OFF conditions of the switch without increasing voltage stress. The boost diode is turned OFF at zero voltage switching condition, so the reverse recovery current is minimized.

For CrM operation, a current sensor detects the time point at which $i_{\rm in} = 0$, then this signal is used to turn-ON switch SW. Therefore, $i_{\rm in}$ of the converter in CrM reaches 0 at the end of each switching period, and in this way reduces turn-ON switching loss [11]–[13]. One drawback of CrM operation is that the peak of $i_{\rm in}$ is twice the average input, so $i_{\rm in}$ ripple and the size of the input filter increase [14]–[16].

This paper proposes a circuit structure of AC–DC boost converter that operates in CCM for the input current and in CrM for the inductor current i_{Lb}. The proposed circuit increases the power conversion efficiency η_e by reducing both turn-ON switching loss and reverse recovery current of diode. Also, it reduces input current ripple and current stress on the switch. The circuit structure and principle of operation are given in Section II, design considerations are given in Section III, experimental results are given in Section IV, and a conclusion is given in Section V.

II. Circuit Structure and Principle of Operation

A. Circuit Structure

The proposed circuit (see Fig. 2) consists of a boost capacitor C_1, a 1:1 transformer, and a diode D_1, in addition to the components L_b, D_O, C_O, and SW, which are required for the conventional AC–DC boost converter. The transformer is represented with a magnetizing inductance L_m and an ideal 1:1 transformer. The transformer between input and output decreases the slope of $i_{\rm in}$ when *SW* is turned OFF; this prevents $i_{\rm in}$ from reaching 0 A while allowing inductor current i_{Lb} to reach 0 A, and reduces the input current ripple. L_m and L_b control the turn-ON slope of switch current i_{sw} that reduces the turn-ON switching loss and the current stress of SW. C_1 is located between two windings of transformer, creates a freewheeling path for i_{Lb} when *SW* is turned OFF, and acts as a charge pump capacitor to increase the voltage gain. C_1 is charged when SW is turned OFF, and it is discharged when SW is turned ON. D_1 provides a current path for i_{Lb} when SW is turned OFF. The capacitances of C_O and C_1 are high enough that C_O and C_1 can be represented as two DC-voltage sources during one switching period T_s. A pickup coil was wound on L_b to detect the zero-crossing point of i_{Lb}. A voltage snubber composed of C_s, R_s, and D_s prevents the voltage ringing due to a resonance in the current path formed by $L_b - L_m - SW$ and the junction capacitance of D_O; this snubber is not discussed in Section II-B, because D_O was assumed to be ideal.

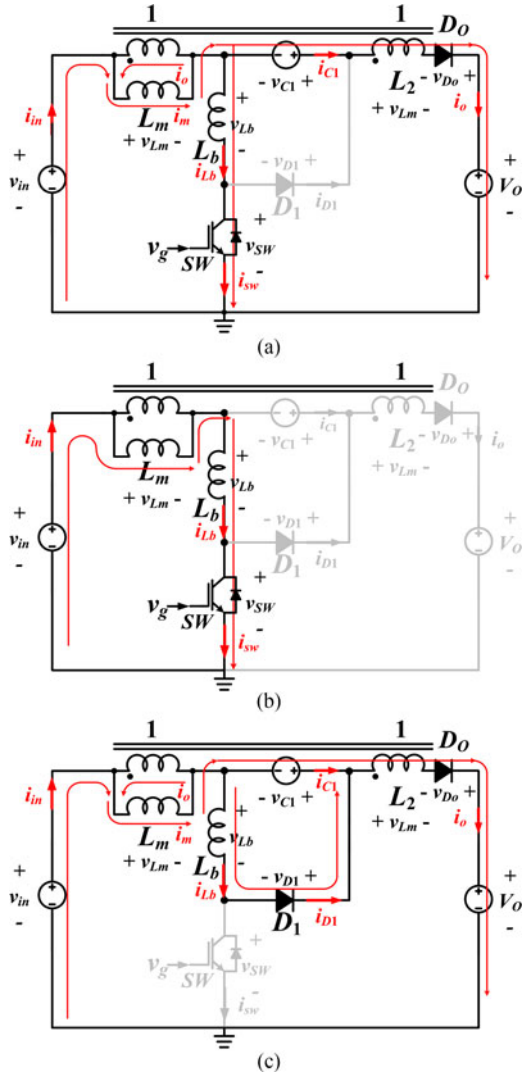

Fig. 3. Modes of operation. (a) *Mode* 1 $(t_0 < t < t_1)$. (b) *Mode* 2 $(t_1 < t < t_2)$. (c) *Mode* 3 $(t_2 < t < t_3)$.

B. Principle of Operation

The proposed converter controls the output DC voltage V_O using a pulse width modulation (PWM) at a variable switching frequency $f_s = 1/T_s$. The switch ON time DT_s of the converter is fixed for a given sinusoidal input voltage $v_{\rm in}(t) = V_{\rm in}\sin(120\pi t)$. This forces the peak of $i_{\rm in}$ to follow $v_{\rm in}$ because the slope of $i_{\rm in}$ is proportional to $v_{\rm in}$, so a high PF is achieved. The zero-crossing point of i_{Lb} determines T_s, so CrM operation of i_{Lb} is guaranteed. The voltage conversion ratio $V_O/V_{\rm in}$ is controlled by adjusting D, where $V_{\rm in}$ is the peak input voltage.

This converter has three sequential modes of operation, as shown by the equivalent circuits (see Fig. 3) and waveforms (see Fig. 4). Before the start of each switching period, SW is at OFF state, $i_{SW}(t_0) = i_{Lb}(t_0) = 0$ A, and $i_{\rm in}(t_0) = i_o(t_0)$. The first operation [*Mode* 1, Fig. 3(a)] starts at $t = t_0$ by turning ON SW. During this operation, D_O stays ON and D_1 stays OFF.

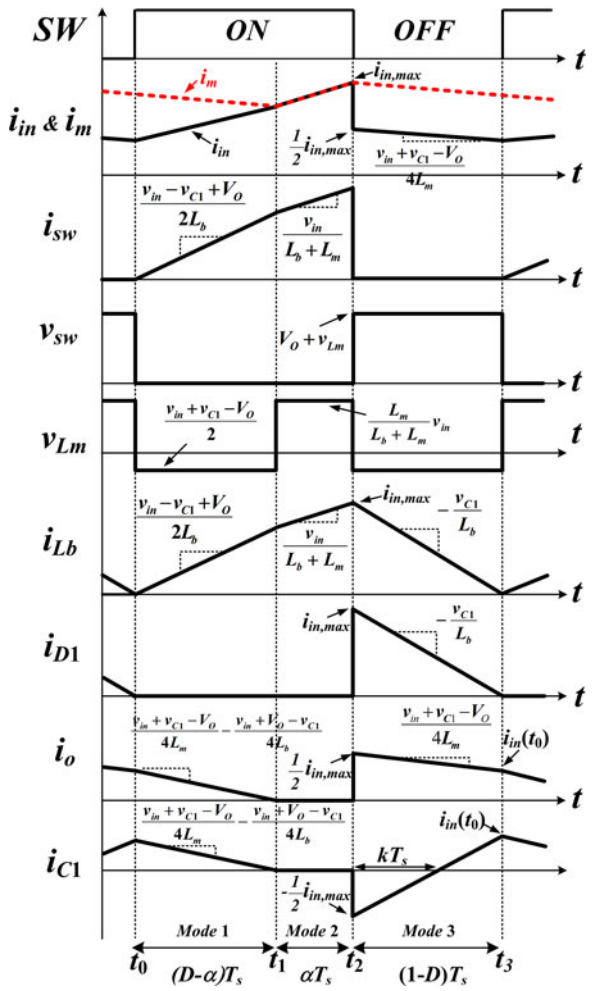

Fig. 4. Theoretical voltage and current waveforms of the proposed AC–DC boost converter.

Because $v_{Lm} = (v_{\rm in} + v_{C1} - V_O)/2$ and $v_{Lb} = (v_{\rm in} + V_O - v_{C1})/2$, i_{Lb} and i_m are given by

$$i_{Lb}(t) = i_{SW}(t) = \frac{v_{\rm in} + V_O - v_{C1}}{2L_b}(t - t_0)$$

$$i_m(t) = \frac{v_{\rm in} + v_{C1} - V_O}{2L_m}(t - t_0) + i_m(t_0) \quad (1)$$

i_o and $i_{\rm in}$ are obtained using $i_m(t) = i_{\rm in}(t) + i_o(t)$ and $i_{\rm in}(t) = i_{Lb}(t) + i_o(t)$ as

$$i_o(t) = \frac{v_{\rm in} + v_{C1} - V_O}{4L_m}(t - t_0) + \frac{i_m(t_0)}{2} - \frac{v_{\rm in} + V_O - v_{C1}}{4L_b}(t - t_0)$$

$$i_{\rm in}(t) = \frac{v_{\rm in} + v_{C1} - V_O}{4L_m}(t - t_0) + \frac{i_m(t_0)}{2} + \frac{v_{\rm in} + V_O - v_{C1}}{4L_b}(t - t_0).$$

Mode 1 ends when i_o decreases to 0 A.

The second operation [*Mode* 2, Fig. 3(b)] starts at $t = t_1$ when D_O turns OFF. During *Mode* 2, SW stays ON and D_1 stays OFF. $i_{\rm in}$ can flow only through SW because D_O is OFF, so

$$i_{\rm in}(t) = i_m(t) = i_{Lb}(t) = \frac{v_{\rm in}}{L_m + L_b}(t - t_1) + i_{Lb}(t_1). \quad (2)$$

Mode 2 ends when *SW* is turned OFF.

The last operation [*Mode* 3, Fig. 3(c)] starts at $t = t_2$ when *SW* is turned OFF. D_1 and D_O turn ON during this mode. Because $v_{Lm} = (v_{\rm in} + v_{C1} - V_O)/2$, i_m is given by

$$i_m(t) = \frac{v_{\rm in} + v_{C1} - V_O}{2L_m}(t - t_2) + i_m(t_2).$$

$i_{\rm in}$ is obtained using $i_{\rm in}(t) = i_o(t)$ and $i_m(t) = i_{\rm in}(t) + i_o(t)$ as

$$i_{\rm in}(t) = \frac{v_{\rm in} + v_{C1} - V_O}{4L_m}(t - t_2) + \frac{1}{2}i_m(t_2). \quad (3)$$

The converter operates in CCM for $i_{\rm in}$ because the transformer decreases the slope of $i_{\rm in}(t)$. A freewheeling current path is formed by L_b, D_1, and C_1, so $v_{Lb} = -v_{C1}$, and i_{Lb} is given by

$$i_{Lb}(t) = i_{D1}(t) = -\frac{v_{C1}}{L_b}(t - t_2) + i_{Lb}(t_2). \quad (4)$$

Because SW is turned on at $i_{Lb} = 0$ A, the boost inductor L_b is operated in CrM, so the power loss caused by turn-ON of *SW* and from the reverse recovery of D_1 is reduced. Because $i_m(t_2) = i_{Lb}(t_2)$ and $i_{\rm in}(t) = i_o(t)$ during this mode, i_{C1} is obtained using (3) and (4) as

$$i_{C1}(t) = i_O(t) - i_{Lb}(t) = \frac{v_{\rm in} + v_{C1} - V_O}{4L_m}(t - t_2) - \frac{1}{2}i_{Lb}(t_2) + \frac{v_{C1}}{L_b}(t - t_2). \quad (5)$$

i_{C1} flows in the direction to charge C_1 when $i_{C1}(t) < 0$ for $t_2 < t < t_2 + kT_s$, and it flows in the direction to discharge C_1 when $i_{C1}(t) > 0$ for the other periods. The value of *k* is obtained using (5), $i_{C1}(t_2 + kT_s) = 0$, and $i_{Lb}(t_2) = v_{C1}(1 - D)T_s/L_b$ as

$$k = \frac{v_{C1}}{2L_b}(1 - D)\left(\frac{v_{\rm in} + v_{C1} - V_O}{4L_m} + \frac{v_{C1}}{L_b}\right)^{-1}. \quad (6)$$

Mode 3 ends when SW is turned ON for the next switching period.

C. Voltage Conversion Ratio

The voltage-second balance law of L_b and L_m at the peak of input voltage ($v_{\rm in}(t) = V_{\rm in}$) results in the following equations:

$$\frac{V_{\rm in} + V_O - v_{C1}}{2}(D - \alpha) + V_{\rm in}\frac{L_b}{L_m + L_b}\alpha - v_{C1}(1 - D) = 0 \quad (7)$$

$$\frac{V_{\rm in} + v_{C1} - V_O}{2}(1 - \alpha) + V_{\rm in}\frac{L_m}{L_m + L_b}\alpha = 0 \quad (8)$$

where D is the ON switching duty and αT_s is the duration of *Mode* 2. Solving (7) and (8) for v_{C1} yields

$$v_{C1} = \frac{V_{\rm in}(1+D) - V_O(1-D)}{1-D}. \quad (9)$$

Inserting (9) into (7) yields the voltage conversion ratio

$$\frac{V_O}{V_{\rm in}} = \frac{1}{1-D} + \frac{L_m}{L_m + L_b}\frac{\alpha}{1-\alpha}. \quad (10)$$

The ampere-second balance law of C_1 results in the following equation:

$$\frac{V_{\rm in} + v_{C1} - V_O}{4L_m}(1-k-\alpha) + \frac{v_{C1}}{2L_b}(1-2k-\alpha) = 0 \quad (11)$$

where kT_s is the duration at which $i_{C1} \le 0$ A during *Mode* 3 (see Fig. 4). Inserting k in (6) into (11) yields

$$\alpha = \frac{L_b(V_{\rm in} + v_{C1} - V_O) + 2L_m v_{C1} D}{L_b(V_{\rm in} + v_{C1} - V_O) + 2L_m v_{C1}}. \quad (12)$$

Combining (9), (10), and (12) yields the voltage conversion ratio

$$\frac{V_O}{V_{\rm in}} = \frac{L_b(3+D) + 2L_m(1+D) - \sqrt{{L_b}^2(1+D)^2 + 4L_m L_b D}}{2(L_m + L_b)(1-D)} \quad (13)$$

which can be simplified to

$$\frac{V_O}{V_{\rm in}} \approx \frac{5 + 3D - \sqrt{(1+D)^2 + 4D}}{4(1-D)} \quad (14)$$

when $L_b \approx L_m$.

III. Design Considerations

A. Boost Inductor L_b

The proposed converter is designed to operate at $85 \le V_{\rm ac} \le 265$ V, $V_O = 400$ V, $100 \le P_O \le 500$ W. Because f_s decreases as input line voltage increases or power increases, the minimum switching frequency $f_{s,\min}$ appears at $v_{\rm in}(t) = V_{\rm in}$ and $P_O = 500$ W. The switching power loss can be reduced by decreasing f_s, but an audible noise is generated when f_s decreases too much. Considering this, the lowest switching frequency $f_{s,\min}$ was chosen as 50 kHz.

The condition that the average of output current $< i_o(t) >$ for one switching period T_s equal to the average current $< i_{D1}(t) >$ is used to determine L_b. From (4), $i_{D1}(t) = -v_{C1}(t - t_2)/L_b + i_{Lb}(t_2)$ during *Mode* 3, and $i_{D1}(t) = 0$ during the other modes. The following equation is obtained using $i_{D1}(T_s) = 0$, $< i_{D1}(t) >= (1-D)T_S i_{Lb}(t_2)/2 =< i_o(t) >$, $T_S - t_2 = (1-D)T_S$, and $i_{Lb}(t_2) = i_{SW}(t_2) = v_{C1}(1-D)T_s/L_b$:

$$i_{SW}(t_2) = i_{Lb}(t_2) = \frac{2 < i_o(t) >}{(1-D)} = \frac{v_{C1}}{L_b}(1-D)T_S \quad (15)$$

$f_{s,\min}$ is calculated as

$$f_{s,\min} = \frac{(1-D)(V_{\rm in}(1+D) - V_o(1-D))}{2 i_{o,\rm peak} L_b} \quad (16)$$

using (9) and (15), and defining $i_{o,\rm peak}$ as the $< i_o(t) >$ at the peak of input sinusoidal voltage. The lowest value of $f_{s,\min}$ for $V_O = 400$ V occurs at $V_{\rm in} = 85\sqrt{2}$ V and $P_O = 500$ W, at which $D \approx 0.651$ from (14). Because $P_O = 2V_O i_{o,\rm peak}/\pi$, L_b should satisfy the following condition:

$$L_b \le \frac{(1-D)(V_{\rm in}(1+D) - V_o(1-D))}{\pi P_o f_{s,\min}} V_o = 104\,\mu\text{H}$$

to have $f_{s,\min} \ge 50$ kHz.

The low limit of L_b is determined using the following condition for a soft turning-ON of SW

$$\frac{V_{\rm in} - v_{C1} + V_O}{2L_b} << \frac{I_{sw,\max}}{t_{\rm rise}} \quad (17)$$

where $I_{sw,\max}$ is the highest SW current and $t_{\rm rise}$ is the fastest SW turn-ON time; $L_b \ge 16\,\mu$H for $I_{sw,\max} = 28$ A and $t_{\rm rise} = 260$ ns. Because the switching turn-ON loss increases as L_b decreases, $L_b = 81\,\mu$H has been chosen to secure operation margin and to prevent hard switching in the proposed converter.

B. Magnetizing Inductance L_m

After determining $L_b = 81\,\mu$H, the range of L_m was determined using the condition $0.05 \le D \le 0.66$ for $85\sqrt{2} \le V_{\rm in} \le 265\sqrt{2}$ V and $V_O = 400$ V; when $D > 0.66$, the time to decrease i_{Lb} to zero becomes insufficient; the converter was designed to operate at $(1-D) \ge 1/3$.

Solving (13) for D yields where $A \equiv {V_O}^2(L_b + L_m)$ and $B \equiv {V_{\rm in}}^2(L_b + 2L_m)$. The D for $85\sqrt{2} \le V_{\rm in} \le 265\sqrt{2}$ V, $V_O = 400$ V, and $L_b = 80\,\mu$H has been calculated using (18), as shown at the bottom of this page, while varying L_m. Then, it has been found that $L_m \ge 60\,\mu$H is required to have $0.05 \le D \le 0.66$. At the peak of sinusoid, the switch voltage is given by

$$v_{SW} = V_O + v_{Lm} = \frac{1}{2}(V_{\rm in} + V_O + v_{C1}) = \frac{V_{\rm in}}{1-D}. \quad (19)$$

This equation results in $v_{SW} \approx 352$ V for $V_{\rm in} = 85\sqrt{2}$ V, $V_O = 400$ V, $L_b = 80\,\mu$H, and $L_m = 60\,\mu$H ($D = 0.659$), which is ~50 V lower than that of the conventional boost converter.

$$D = \frac{2A - B - 2L_b V_{\rm in} V_O + V_{\rm in}\sqrt{L_b({V_{\rm in}}^2(L_b - 4L_m) + 4A - 4L_b V_{\rm in} V_O)}}{2(V_{\rm in} + V_O)(L_b V_O + L_m(V_{\rm in} + V_O))} \quad (18)$$

The voltage stress of the output diode is

$$v_{Do} = V_O + v_{Lm} - v_{C1} - v_{Lb} = 2V_O + v_{\text{in}}\left(\frac{L_m - L_b}{L_m + L_b} - \frac{1+D}{1-D}\right). \quad (20)$$

Inserting (18) into (20) gives v_{Do} as a function of V_{in}, V_O, L_b, and L_m, which is used to obtain the maximum value of L_m. V_{Do} is highest when V_{ac} is highest, so V_{Do} has been calculated at the peak of $V_{\text{ac}} = 265\,\text{V}$; $L_m < 300\,\mu\text{H}$ is required to have $v_{Do} \le 600$ V when $v_{\text{in}} = 265\sqrt{2}\,\text{V}$, $V_O = 400\,\text{V}$, $D \approx 0.06$, and $L_b = 80\,\mu\text{H}$. So $L_m = 93\,\mu\text{H}$ has been chosen for the proposed converter.

C. Capacitor C_1

The value of C_1 is determined from the condition that $\Delta v_{C1} << v_{C1}$ because V_{C1} should be almost constant for one switching period T_s, where Δv_{C1} is the voltage ripple of C_1. During *Mode* 3, C_1 charges through L_b and D_1; this results in a voltage ripple Δv_{C1} of C_1; $\Delta v_{C1} \approx < i_o(t) > T_s/2C_1$ because the current through C_1 increases linearly from $- < i_o(t) > /(1-D)$A at $t \approx DT_S$ to 0 A at $t \approx T_S$. Therefore

$$C_1 >> \frac{i_{o,\text{peak}}}{2f_{s,\text{min}}v_{C1}}. \quad (21)$$

For $85 \le V_{\text{ac}} \le 265\,\text{V}$, $f_{s,\text{min}} = 50\,\text{kHz}$, $100 \le P_O \le 500\,\text{W}$, and $V_O = 400\,\text{V}$, $C_1 = 1\,\mu\text{F}$ was determined using (9), (14), and (21).

D. Switch and Diodes

Solving (14) for D yields

$$D = \frac{4{V_O}^2 - 2V_O V_{\text{in}} - 3{V_{\text{in}}}^2 + V_{\text{in}}\sqrt{8{V_O}^2 - 4V_O V_{\text{in}} - 3{V_{\text{in}}}^2}}{2(V_{\text{in}} + V_O)(V_{\text{in}} + 2V_O)}. \quad (22)$$

Inserting (22) into (19) and (15) yields

$$v_{SW} = \frac{V_{\text{in}}}{(1-D)} = \frac{2(V_{\text{in}} + V_O)(V_{\text{in}} + 2V_O)}{5V_{\text{in}} + 8V_O - \sqrt{8{V_O}^2 - 4V_{\text{in}}V_O - 3{V_{\text{in}}}^2}} \quad (23)$$

and

$$i_{SW}(t_2) = \frac{2i_{o,\text{peak}}}{1-D} = \frac{4i_{o,\text{peak}}(V_{\text{in}} + V_O)(V_{\text{in}} + 2V_O)}{V_{\text{in}}(5V_{\text{in}} + 8V_O - \sqrt{8{V_O}^2 - 4V_{\text{in}}V_O - 3{V_{\text{in}}}^2})}. \quad (24)$$

The highest voltage of D_1 occurs when both SW and D_O are turned ON, while D_1 is turned OFF. So the voltage stress of D_1 is $V_O + v_{Lm} = (v_{\text{in}} + V_O + v_{C1})/2$, i.e., it equals v_{SW}. Also, the current stress of D_1 equals $i_{SW}(t_2)$ because $i_{D1}(t_2) = i_{SW}(t_2)$, and the current stress of D_{O} is $i_{SW}(t_2)/2$ because $i_{Do}(t_2) = i_{SW}(t_2)/2$. Inserting the D in (22) into (20) yields

$$v_{Do} = \frac{(V_{\text{in}} + 2V_O)(V_{\text{in}} + 4V_O - \sqrt{8{V_O}^2 - 4V_{\text{in}}V_O - 3{V_{\text{in}}}^2})}{5V_{\text{in}} + 8V_O - \sqrt{8{V_O}^2 - 4V_{\text{in}}V_O - 3{V_{\text{in}}}^2}}. \quad (25)$$

The current peaks are highest when V_{ac} is lowest, so the current stress of the switch was calculated as $i_{SW}(t_2) \approx 11.2$ A, using (24) at $V_{\text{ac}} = 85\,\text{V}$, $P_O = 500\,\text{W}$, $V_O = 400\,\text{V}$, and $i_{o,\text{peak}} \approx 1.96$ A, which resulted in $i_{D1} \approx 11.2\,\text{A}$ and $i_{Do} \approx 5.6\,\text{A}$. The voltage peaks are highest when V_{ac} is highest, so the voltage stress of the switch was calculated as $v_{SW} \approx 398.5\,\text{V}$ using (23) at $V_{\text{ac}} = 265\,\text{V}$, $P_O = 500\,\text{W}$, and $V_O = 400\,\text{V}$, which resulted in $v_{D1} \approx 398.5\,\text{V}$. The voltage stress of D_o was calculated as $v_{Do} \approx 419.3\,\text{V}$ using (25) at same operating conditions. The proposed converter used a MOSFET (FDA28N50, Fairchild Semiconductor) and two diodes (30ETH06, Vishay); the MOSFET has the maximum ratings of $i_{SW} = 28\,\text{A}$ and $v_{SW} = 500\,\text{V}$, and the diode has the maximum ratings of $i_{Do} = 30\,\text{A}$ and $v_{Do} = 600\,\text{V}$. So these devices can endure the calculated voltage and current stresses.

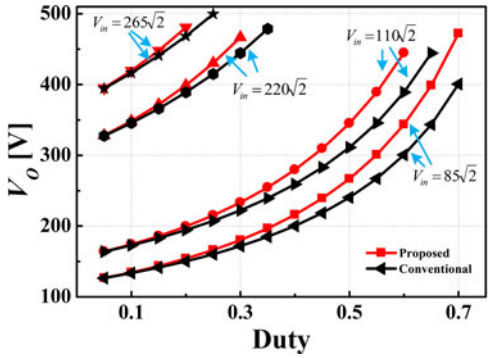

Fig. 5. V_O versus D for the conventional and proposed converters; $85\sqrt{2} \le V_{\text{in}} \le 265\sqrt{2}\,\text{V}$, $0.05 \le D \le 0.7$.

V_O versus D (see Fig. 5) for $L_b = 80\,\mu\text{H}$, $L_m = 93\,\mu\text{H}$, $85\sqrt{2} \le V_{\text{in}} \le 265\sqrt{2}\,\text{V}$, and $0.05 \le D \le 0.7$ was calculated using (13), but it was calculated using $V_O = V_{\text{in}}/(1-D)$ for the conventional boost converter. To have $V_O = 400\,\text{V}$ for the given range of V_{in}, $0.06 \le D \le 0.65$ was required for the proposed converter, while $0.06 \le D \le 0.7$ was required for the conventional boost converter. At given V_{in} and D, the proposed converter had higher V_O than the conventional boost converter.

IV. Experimental Results

The proposed AC–DC converter (see Fig. 6) was designed to operate at $85 \le V_{\text{ac}} \le 265\,\text{V}$, $V_O = 400\,\text{V}$, $100 \le P_O \le 500\,\text{W}$. The values of circuit components were determined using (16)–(22). Three other AC–DC converters were also built and tested to compare with the proposed converter; they include the conventional CrM, CCM boost converter, and converter of [6], which were designed (see Table I) to operate at the same input and output conditions. All converters were built using the same MOSFETs and diodes to ensure fair comparison. The experimental circuits were implemented using FDA28N50 (28 A, 500 V) nMOSFETs from Fairchild Semiconductor Co.,

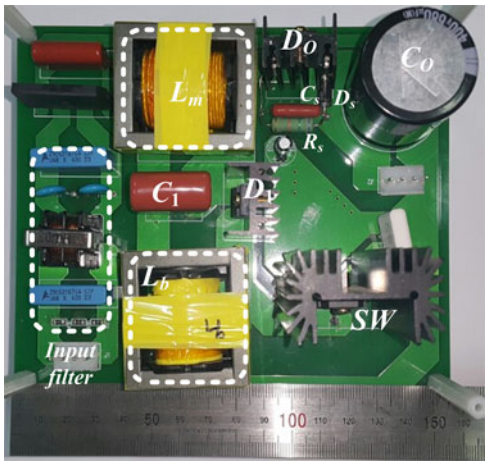

Fig. 6. Photograph of the proposed AC–DC boost converter.

TABLE I
VALUES OF COMPONENTS OF THE EXPERIMENTAL CONVERTERS

Components	Proposed Converter	Conventional Boost Converter (CrM)	Conventional Boost Converter (CCM)	Converter of [6]
L_b	81 μH	81 μH	230 μH	–
L_m	93 μH	–	–	230 μH
L_r	–	–	–	12 μH
Turn ratio	1 : 1	–	–	1 : 0.1
SW	FDA28N50	FDA28N50	FDA28N50	FDA28N50
D_o	30ETH06	30ETH06	30ETH06	30ETH06
D_1	30ETH06	–	–	30ETH06
D_2	–	–	–	30ETH06
D_3	–	–	–	30ETH06
C_1	1 μF	–	–	220 nF
C_o	680 μF	680 μF	680 μF	680 μF
Driver chip	FAN7930B	FAN7930B	L4981AD	L4981AD
f_s	Variable	Variable	85 kHz	85 kHz

Sunnyvale, CA, USA, for SWs, 30ETH06 (30 A, 600 V) diodes from Vishay Inc., Malvern, PA, USA, FAN7930B CrM PFC controller from Fairchild Semiconductor Co., and L4981AD CCM PFC controller from STMicroelectronics Inc., Geneva, Switzerland. To prevent the voltage ringing observed in *Mode* 2 due to a resonance in the current path formed by $L_b - L_m - SW$ and the junction capacitance of D_O, a voltage snubber in Fig. 2 was implemented using $R_s = 100\,\text{k}\Omega$, $C_\text{s} = 68$ nF, and the STTH3L06 diode from STMicroelectronics Inc.

The FAN7930B CrM PFC controller (see Fig. 7) uses a voltage-mode PWM control. Inputs for this controller are $\text{zero} - \text{crossing} - \text{detector}\,(ZCD)$, INV, and V_ref, and output is the PWM signal V_g. The ZCD signal, which is proportional to i_{Lb}, was generated by integrating the voltage v_{Lb}/n of pickup coil, and it was amplified using the clamp circuit to produce V_{ZCD}. Then, V_{ZCD} was compared with 1.5 V to detect the zero-cross point of i_{Lb}. When the state of v_g changes from low to high, the switch turns ON and the voltage sawtooth starts. The INV signal was generated using a voltage divider consisted of R_1 and R_2 in the converter (see Fig. 2); INV is an attenuated

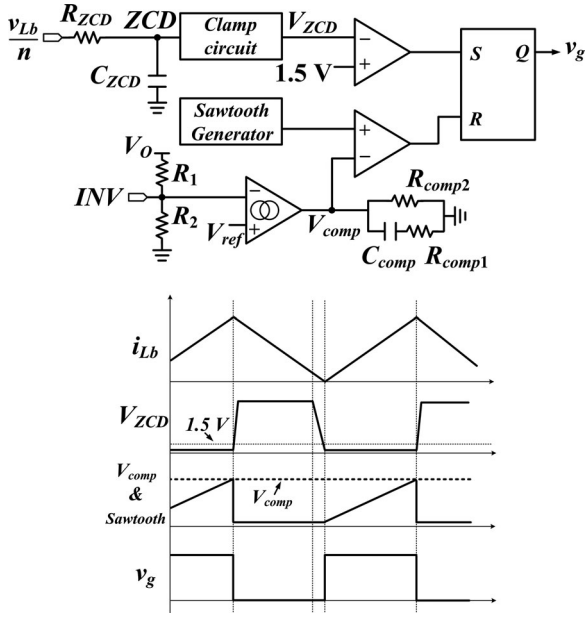

Fig. 7. Block diagram and waveforms for FAN7930B CrM PFC controller.

signal of V_O. The difference $V_\text{ref} - INV$ was amplified, and the amplified signal V_comp was compared with the voltage sawtooth to generate the reset pulse R. R resets the Flip–Flop and the sawtooth generator. INV decreases when the output voltage decreases, so V_comp increases. The switching duty D increases as V_comp increases, that increases i_{Lb}, I_o, and V_o. So the switch turns OFF when the state of v_g changes from high to low. This voltage-mode PWM does not use any input information, so the power loss for sensing input information is saved.

The voltage and current waveforms of *SW* [see Fig. 8(a)–(d)] were measured at $V_\text{ac} = 85$ V and $P_O = 500$ W. The proposed converter used a pickup coil wound on L_b to detect the zero-crossing point of i_{Lb}, and the zero-current signal was used as a turn ON signal of SW, so the SW turned ON under zero-current condition [see Fig. 8(a)]. The CrM boost converter had zero current turn-ON, but it had higher current peak than the proposed converter [see Fig. 8(b)]. The CCM boost converter was subjected to hard switching and the reverse recovery of its D_O produced a current spike in the switch current [see Fig. 8(c)]. The converter of [6] had no current spike from the reverse recovery of D_O because it used a passive snubber [see Fig. 8(d)].

The voltage and current waveforms of C_1 [see Fig. 9(a)], D_1 [see Fig. 9(b)], and D_O [see Fig. 9(c)] were also measured at $V_\text{ac} = 85$ V and $P_O = 500$ W. As expected, v_{C1} was constant for one switching period, and i_{C1} and i_o followed the theoretical waveforms, but v_{Do} had voltage ringing due to a resonance in the current path formed by $L_b - L_m - SW$ and the junction capacitance of D_O.

The input voltage and current waveforms of the proposed converter [see Fig. 10(a)] and the CrM boost converter [see Fig. 10(b)] were measured at $V_\text{ac} = 85$ V and $P_O = 500$ W. The proposed converter had an input ripple current Δi_in of 9.7 A because it was operated in CCM using the 1:1 transformer,

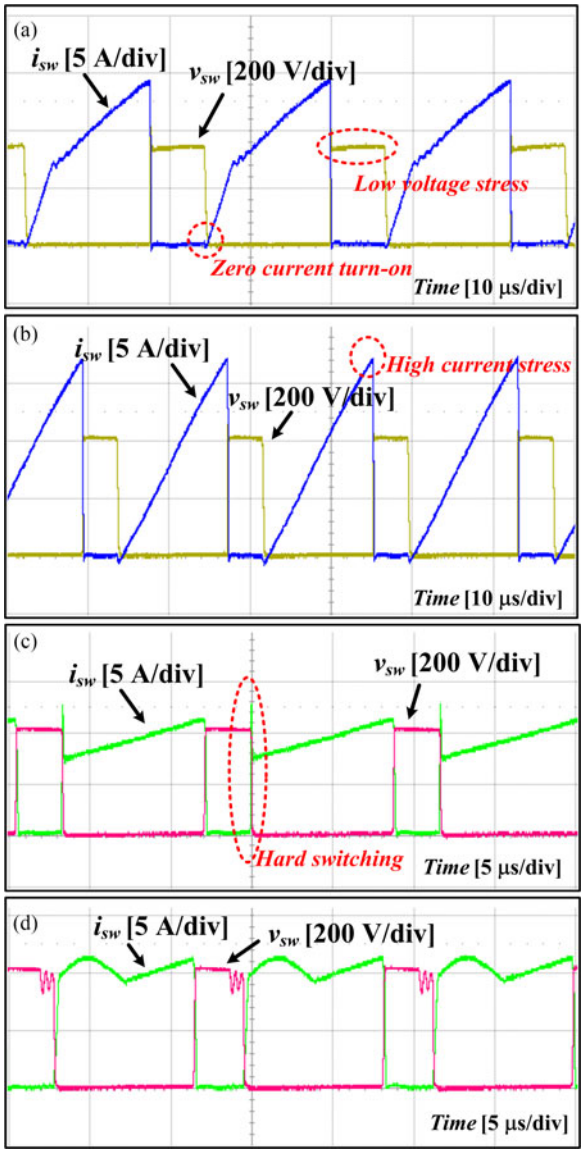

Fig. 8. Voltage and current waveforms of switch measured at $V_{\rm ac} = 85\,{\rm V}$, $V_O = 400\,{\rm V}$, and $P_O = 500\,{\rm W}$. (a) Proposed AC–DC boost converter. (b) Conventional AC–DC CrM boost converter. (c) Conventional AC–DC CCM boost converter. (d) Converter of [6].

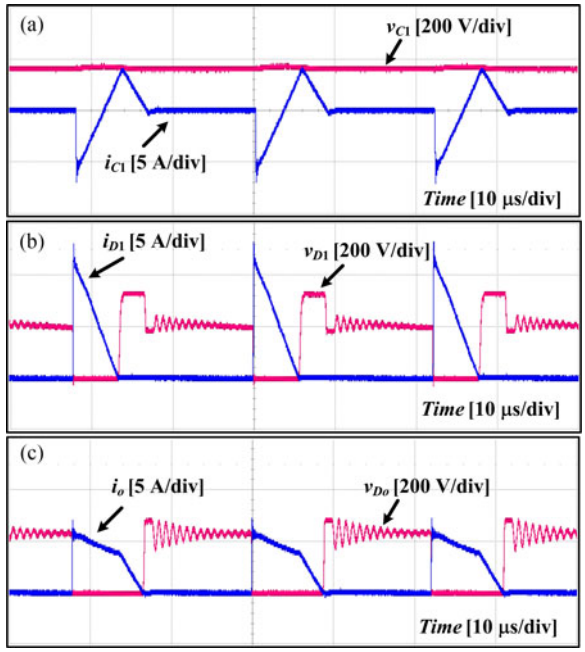

Fig. 9. Voltage and current waveforms of capacitor and diodes of the proposed converter measured at $V_{\rm ac} = 85\,{\rm V}$, $V_O = 400\,{\rm V}$, and $P_O = 500\,{\rm W}$. (a) C_1. (b) D_1. (c) D_O.

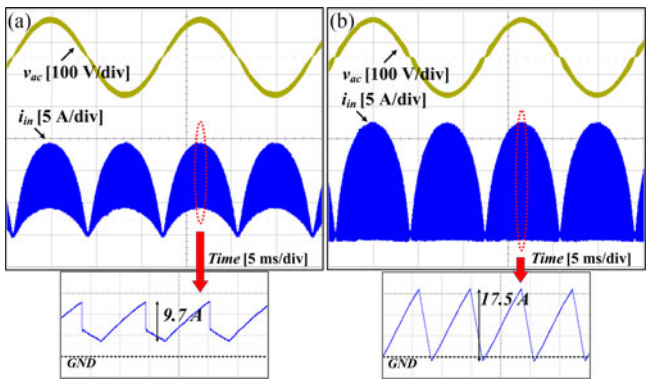

Fig. 10. Input voltage and current waveforms measured at $V_{\rm ac} = 85\,{\rm V}$, $V_O = 400\,{\rm V}$, $P_O = 500\,{\rm W}$. (a) Proposed AC–DC boost converter. (b) Conventional AC–DC CrM boost converter.

whereas the CrM boost converter had $\Delta i_{\rm in} = 17.5\,{\rm A}$ because the input current becomes zero at the end of each switching period.

Curves of η_e on $V_{\rm ac}$ [see Fig. 11(a)] were measured at $85 \le V_{\rm ac} \le 265\,{\rm V}$, $V_O = 400\,{\rm V}$, $P_O = 500\,{\rm W}$. For all converters, η_e increased as $V_{\rm ac}$ increased; η_e at $V_{\rm ac} = 85\,{\rm V}$ (265 V) was 92.9% (97.4%) for the proposed converter, 83.5% (97.6%) for the CrM converter, 85.4% (96.4%) for the CCM converter, and 89.5% (95.0%) for the converter of [6]. The curves of η_e on P_O measured at $V_{\rm ac} = 85\,{\rm V}$, $V_O = 400\,{\rm V}$, $100 \le P_O \le 500\,{\rm W}$ [see Fig. 11(b)] show that η_e at $V_{\rm ac} = 85\,{\rm V}$ increased to 94.28% (proposed), 95.18% (CrM), 90.94% (CCM), and 90.53% (converter of [6]) at $P_O = 100\,{\rm W}$. These results show the followings: η_e of all converters decreased as either $V_{\rm ac}$ decreased or P_O increased; the proposed converter had the highest η_e over wide input voltage and output power ranges, and η_e at $P_O = 500\,{\rm W}$ and $V_{\rm ac} < 130\,{\rm V}$ of the converter of [6] was higher than those of CrM and CCM boost converters.

Using a digital temperature recorder (GL-220, GRAPHTEC), the temperature T of SW [see Fig. 12] was measured for 50 min while operating the converters at $85 \le V_{\rm ac} \le 220\,{\rm V}$, $V_O = 400\,{\rm V}$ and $P_O = 500\,{\rm W}$. The CCM converter failed for $V_{\rm ac} = 85\,{\rm V}$ and 110 V after $<$ 17 min of operation, the converter of [6] failed also for $V_{\rm ac} = 85\,{\rm V}$ after $<$ 15 min, the CrM converter stabilized at 150 °C for $V_{\rm ac} = 85\,{\rm V}$, but the proposed converter stabilized at 84 °C for $V_{\rm ac} = 85\,{\rm V}$, at 70 °C for $V_{\rm ac} = 110\,{\rm V}$, and at 42 °C for $V_{\rm ac} = 220\,{\rm V}$. These data show that the proposed converter has better thermal stability than the others.

The PF and total harmonic distortion (THD) of the proposed converter (see Fig. 13) were measured at $85 \le V_{\rm ac}$ 265 V, $V_O = 400\,{\rm V}$, and $100 \le P_O \le$ 500 W. This measurement

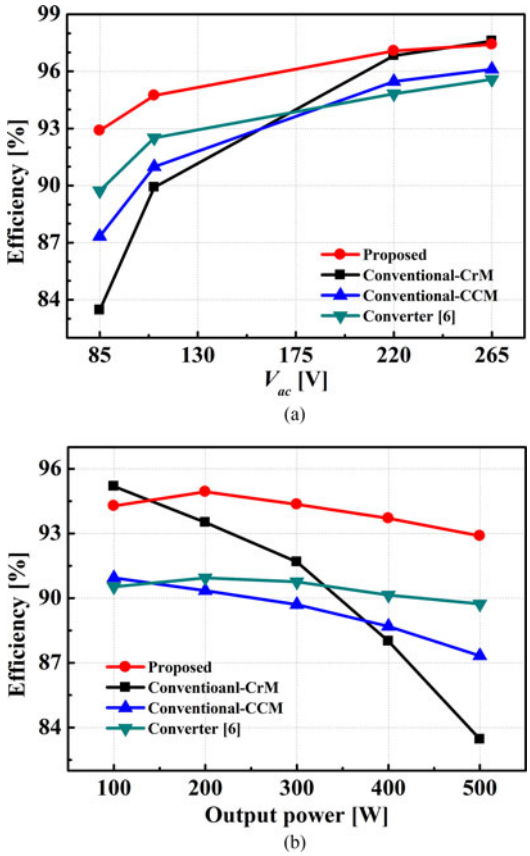

Fig. 11. (a) η_e versus $V_{\rm ac}$ measured at $85 \leq V_{\rm ac} \leq 265$ V, $V_O = 400$ V, $P_O = 500$ W. (b) η_e versus P_O measured at $V_{\rm ac} = 85$ V, $V_O = 400$ V, $100 \leq P_O \leq 500$ W.

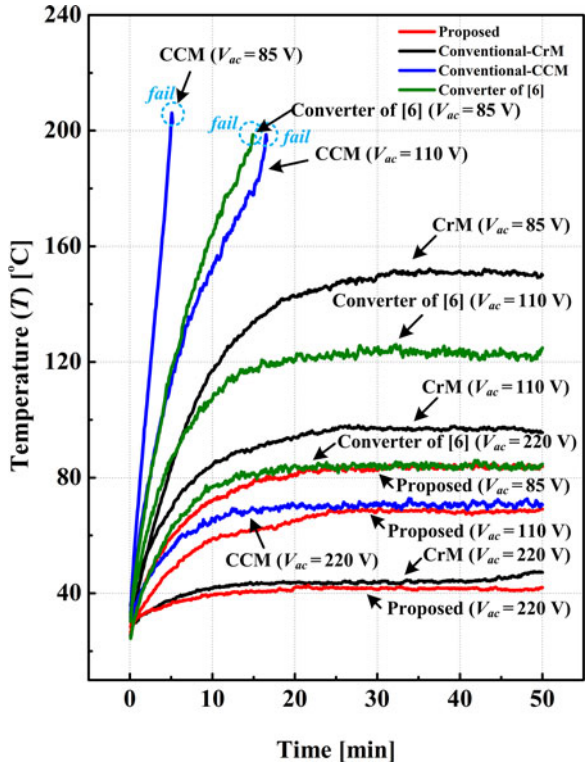

Fig. 12. Temperature of switch versus operation time for the experimental converters: measured at $85 \leq V_{\rm ac} \leq 220$ V, $V_O = 400$ V, $P_O = 500$ W.

shows that PF decreased and THD increased either as $V_{\rm ac}$ increased or as P_o decreased, i.e., as either input or output current decreased. So one may infer that PF and THD degradations of the proposed converter are associated with the input/output current levels. The cause of having the above observations can be understood from the characteristics of FAN7930B CrM PFC controller, which was adopted as the controller for the proposed converter. This controller uses a voltage mode PWM control to stabilize the output voltage, and uses a ZCD signal to achieve CrM operation. The maximum switching frequency $f_{\rm s,max}$ is limited to ∼300 kHz. At a given P_O, i_{Lb} decreases as $V_{\rm ac}$ increases, so the switching frequency $f_{s,\rm min}$ at the peak of sinusoidal input voltage increases. (At a given $V_{\rm ac}$, i_{Lb} decreases as P_O decreases, so $f_{s,\rm min}$ increases also.) So the range of f_s variation to construct 60Hz sinusoidal input current decreased as either input or output current decreased, that caused the observed PF and THD degradations.

Although the proposed converter had some difficulty to achieve good THD when the input/output current is too low, PF ≥ 0.9 and THD $\leq$ 30% for the operating conditions as wide as 85 V $\leq V_{\rm ac} \leq$ 265 V and 100 W $\leq P_O \leq$ 500 W are good enough for many industrial applications.

The current and voltage stress of the proposed, CrM, CCM, and converter of [6] were measured at $V_{\rm ac} = 85$ V, $V_O = 400$ V, and $P_O = 500$ W (see Table II). Without parasitic effects, the

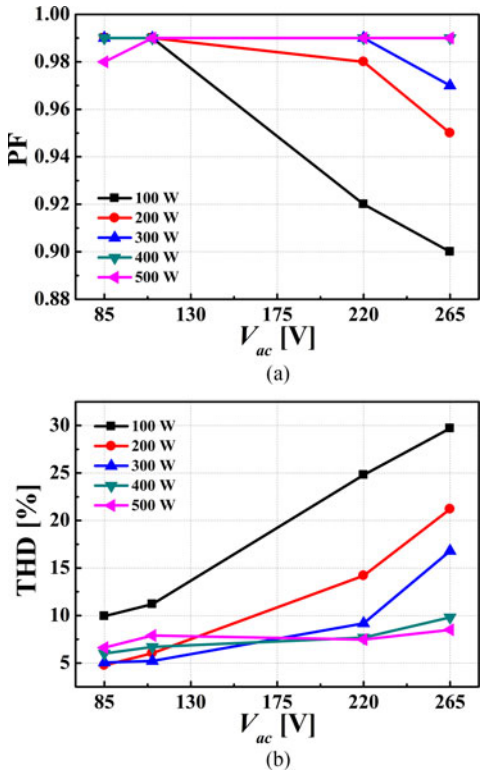

Fig. 13. (a) PF versus $V_{\rm ac}$ and (b) THD versus $V_{\rm ac}$: measured at $85 \leq V_{\rm ac} \leq 265$ V, $V_O = 400$ V, and $100 \leq P_O \leq 500$ W.

TABLE II
VOLTAGE AND CURRENT STRESSES OF SWITCH AND DIODES IN THE EXPERIMENTAL CONVERTERS

	Component	Proposed Converter	Conventional Boost Converter (CrM)	Conventional Boost Converter (CCM)	Converter of [6]
Peak voltage stress [V]	SW	385	422	425	425
	D_o	291	413	419	419
	D_1	337	–	–	475
	D_2	–	–	–	444
	D_3	–	–	–	425
Peak current stress [A]	SW	13.1	16.4	13.1	11.4
	D_o	7.3	16.4	11.7	9.5
	D_1	13.1	–	–	7.3
	D_2	–	–	–	6.6
	D_3	–	–	–	3.3

highest voltages of SW and diodes are given as the following: 1) in the conventional CrM and CCM converter [see Fig. 1(a)], $v_{SW} = V_O$ because D_O is turned ON when SW is turned OFF, and $v_{Do} = V_O$ because SW is turned ON when D_O is turned OFF; 2) in the converter of [6] [see Fig. 1(b)], $v_{SW} = V_O$ because D_O is turned ON when SW is turned OFF, and $v_{D1} = V_O + V_{Cr}$ because D_3 is turned ON, and D_O and D_2 are turned OFF when D_1 is turned OFF; 3) in the proposed converter (see Fig. 2), $v_{SW} = V_O + v_{Lm}$ because D_1 and D_O are turned ON when SW is turned OFF, and $v_{D1} = V_O + v_{Lm}$ because SW and D_O are turned ON when D_1 is turned OFF. $v_{Lm} < 0\,\mathrm{V}$ when D_O is turned ON, so the proposed converter had the lowest voltage stresses of SW and diodes. The current stress of SW decreased as the value of inductance increased, so the current stress of SW was highest in the CrM converter, and lowest in the converter of [6]. The current stress of SW was lower in the proposed converter than in the CrM converter because L_b and L_m were connected in series at the turn-ON of SW. L_b in the CCM converter was the same as that in the converter of [6], but the CCM converter had higher current stress of SW than the converter of [6] because of the reverse recovery current of diode in the CCM converter.

V. CONCLUSION

This paper proposes an AC–DC converter that can operate over a wide range of input voltage. The proposed converter reduces the ripple of input current by using a 1:1 transformer, and decreases the switching loss by operating the switch in a CrM. Experimental results at $85 \le V_{\mathrm{ac}} \le 265\,\mathrm{V}$, $V_O = 400\,\mathrm{V}$, and $100 \le P_O \le 500\,\mathrm{W}$ show that the proposed converter had higher power conversion efficiency than the other previous AC–DC converters. Also, the voltage stresses of SW and diodes were lower than in other converters. The temperature of switch at $V_O = 400\,\mathrm{V}$ and $P_O = 500\,\mathrm{W}$ stabilized at ∼84 °C for $V_{\mathrm{ac}} = 85\,\mathrm{V}$, at ∼70 °C for $V_{\mathrm{ac}} = 110\,\mathrm{V}$, and at ∼42 °C for $V_{\mathrm{ac}} = 220\,\mathrm{V}$, while that in other AC–DC converters either stabilized at much higher temperature or increased to the fail temperature of 200 °C. These results show that the proposed converter is well suited for a system that requires an input voltage range of 85 ∼265 V in root-mean-square value.

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Seok-Hyeong Ham received the B.S. degree in electrical engineering from Pusan National University, Busan, South Korea, in 2013, and the M.S. degree in electrical engineering from Pohang University of Science and Technology, Pohang, South Korea, in 2015, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include the LED driving circuit, power-factor-correction circuits, and microinverters.

Hyung-Jin Choe received the B.S. degree in electrical engineering from Chungnam National University, Daejeon, South Korea, in 2009, and the M.S. and Ph.D. degrees in electrical engineering from Pohang University of Science and Technology, Pohang, South Korea, in 2011 and 2014, respectively.

He is currently an Engineer with LG Display Co., Ltd. LCD Industrial Complex, Paju, South Korea. His research interests include the power-factor-correction circuits, new converter topologies, and soft-switching techniques in AC-DC and DC-DC converters.

Hyeon-Seok Lee received the B.S. degree in electrical engineering from Chungnam National University, Daejeon, South Korea, in 2013, and the M.S. degree in electrical engineering from Pohang University of Science and Technology, Pohang, South Korea, in 2015, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include the LED driving circuit, soft-switching techniques in DC–DC converter, and microinverter.

Bongkoo Kang (S'83–M'86) received the Ph.D. degree in electrical engineering from the University of California Berkeley, Berkeley, CA, USA, in 1986.

Following his graduation, he joined the Electronics and Telecommunication Research Laboratory, Daejeon, South Korea, where he worked on developing semiconductor processing equipment. Since 1989, he has been a Professor with the Department of Electrical Engineering, Pohang University of Science and Technology, Pohang, South Korea. His current research interests include the design of drive circuits for display devices and the modeling, and characterization of semiconductor devices.