General Impedance Representation of Passive Devices Based on Measurement

Tung Ngoc Nguyen, *Student Member, IEEE*, Handy Fortin Blanchette, *Member, IEEE*, and Ruxi Wang, *Senior Member, IEEE*

***Abstract*—Noise propagation from power stages of power converters to their low-voltage control boards depends on multiple complex paths, generally created by parasitic capacitors across isolation barriers. These barriers can be easily crossed by the high frequencies (up to 100 MHz [5]) generated by new semiconductor technologies such as SiC and GaN resulting in compromised signal integrity on the control side. A common approach to overcome this problem is by using filter. However, due to the presence of several complex propagation paths, DM and CM modes are not properly defined at board level, causing difficulties to predict filter's performance. To cope with this issue, the node-to-node impedance function (NIF) is proposed to identify the impedance of all possible propagation paths in the filter. In the considered frequency range (>30 MHz), NIF parameters identification precision is altered by the impedance of shorting paths used in measurement procedure. In this paper, an optimization procedure based on Newton–Raphson algorithm is proposed to remove these errors. This improved version of NIF is named General Impedance Representation (GIR). Thanks to its generality, the GIR can also applicable for all kinds of passive devices. Experimental results are presented to confirm the effectiveness of GIR.**

***Index Terms*—Electromagnetic interference (EMI), equivalent circuit, filters, impedance measurement, modeling, noise.**

I. Introduction

THE incoming of SiC and GaN technologies in power conversion bring several benefits such improved power density and higher efficiency. However, high switching frequency (hundreds of kilohertz to megahertz) combined with short rise and fall times of SiC and GaN devices produce higher electromagnetic interference (EMI) than standard Si-based converters in the conducted EMI frequency range (10–30 MHz) [1]–[4]. Moreover, the voltage and current spectra through switching devices in SiC-based converters are 20–30 dBμV and 20–30 dBμA higher than those in the Si-based ones in frequency range from 20 to 100 MHz, respectively [5]. These augmented spectral contents at high frequency will be translated into significant increase of EMI at the converter input [6]. In addition to increasing the noise on the power leads, these high-frequency currents will travel more easily across the multiple insulation barriers inside the converter, as shown in the simplified example of Fig. 1. In this example, one observes parasitic capacitors in parallel with the insulation of the gate driver dc/dc converter (C_1 and C_2) as well as the parasitic capacitor ($C_{\rm CM}$) between the low power rails of the converter and the heatsink. These capacitors create unexpected propagation paths for the noise generated by the power stage to the surrounding circuits and more precisely the low-voltage power rails. These low-voltage power rails are used to supply semiconductors dedicated to control such as DSP and analog circuits. These circuits are very sensitive to the quality of their supply and malfunctions can arise if voltage spikes are present in the rails, decreasing the converter reliability [7]. Therefore, the noise level propagated from the power stage to the low power rails must be under control. Of course, a natural approach to force this control is integrating filters between these two parts of the converter.

A difficult question arises at this point. The basis of this questioning is illustrated on Fig. 1(a). The propagation path $i_{\rm dm}$ is considered as the differential mode (DM) noise from the filter point of view, without considering the effect of the metallic parts (case, heatsink) of the converter. However, noise propagates in multiples other paths as shown by propagation paths $i_{\rm cm}$, and i_1 in Fig. 1(b) with the presence of the parasitic capacitance between the heatsink and low power rails ($C_{\rm CM}$), and switching devices (C_D). This simplified example shows that the formal DM and common mode (CM) definitions are difficult to interpret from the filter point of view. In fact, noise can travel from any pin of the filter to any other one.

The proposed approach to cope with this ambiguous current distribution is the node-to-node impedance function (NIF) black-box-model modeling, as shown in Fig. 2 [8], [9]. This modeling approach does not assume DM or CM noise but provides propagation path impedance between each pin of the filter. Also, NIF provides a good insight of filter weakness and performance in the frequency domain. Finally, NIF modeling is general and it can be effectively used for all passive devices, such as common chokes, on-board transformers, planar structures, etc. Consequently, the main contribution of this paper is to extend the validity of NIF models in a large frequency bandwidth (from 100 kHz to 200 MHz). As explained in Section II, extending NIF in this frequency range will introduce shorting impedance issues for parameters identification, solved by the contribution in this paper. The resulting improved impedance representation

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T. N. Nguyen and H. F. Blanchette are with the Le Groupe de Recherche en Électronique de Puissance et Commande Industrielle, École de Technologie Supérieure, Montréal, QC H3C1K3, Canada (e-mail: nngoctungbk@gmail.com; handy.fortin-blanchette@etsmtl.ca).

R. Wang is with the GE Global Research Center, Schenectady, NY 12309 USA (e-mail: ruxiwang@ge.com).

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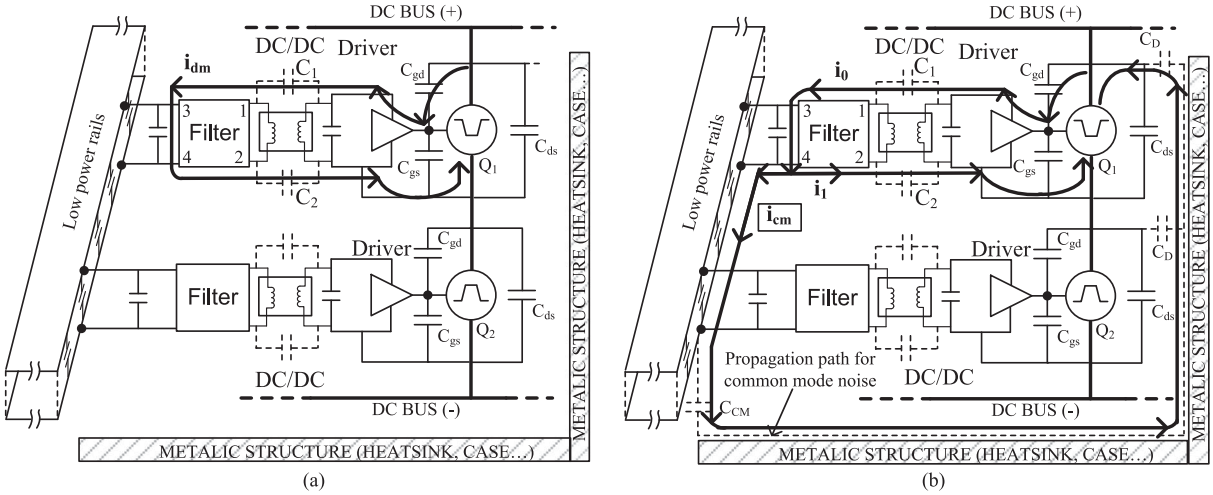

Fig. 1. Basic noise paths in a power converter. (a) Only differential mode current. (b) Including common mode current.

is called General Impedance Representation (GIR). Since it has been shown that offline impedance of the passive parts of the power converter are useful to precisely predict EMI of a power converter [2], [10], [11], this contribution will help to improve EMI filter characteristics for the next generation of power transistors such as SiC and GaN.

The paper is organized as follow. In Section II, a review of NIF and passive modeling is presented. In Section III, the measurement procedure to build GIR model is presented. It is followed by the analysis of the impact of the shorting path impedance on the connecting impedance computation in Section IV. In Section V, an optimization procedure based on Newton–Raphson is presented with the required assumptions to ensure the accuracy and convergence of the algorithm. Finally, Section VI provides the experimental results of a commercial *LC* filter followed by the conclusion in Section VII.

II. Passive Components Modeling and Impedance Extraction

In the literature, passive components have been modeled by using computational and measurement-based methods. Computational methods are employed for designing devices such as FEM [12] and PEEC [13] based on device geometry and materials. These methods have great advantages but they are not able to handle commercial *black-box* devices, where all components are integrated and covered in a case. Measurement-based methods are the answer to this issue. For these methods, a set of impedance measurement is performed to determine all the elements of a given theoretical model such as transformers [14]–[15] and common—choke [16]–[24]. Advanced common choke models taken into account the complex permeability [22] and core saturation under bias conditions [23] have been recently developed. An online impedance measurement method of the common choke based on the performance of the common mode current was introduced in [24]. However, the limit frequency range of 25 kHz is not sufficient enough for modeling in the EMI frequency. Scattering parameter measurements are used to extract the model of planar *LC* filter [25]. Although the results are good, this approach still needs a predefined model

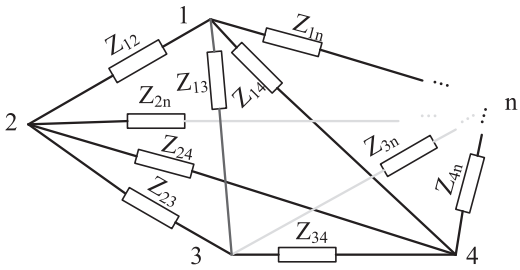

Fig. 2. Equivalent circuit of *an n*-pin passive device.

that is not available easily for many parts. The NIF models are developed in [8], [9], [26]–[29] to cope with the unknown predefined model devices. In this modeling approach, each pin pair is linked together by a connecting impedance, as shown in Fig. 2. The connecting impedance is computed from the data obtained by measurements. Due to the fact of frequency-based measurement, all frequency-dependent parameters (such as permeability and skin effect) are embedded in the measured data.

A. Impedance Extraction

Although measurement-based methods are attractive due to their generality, impedance extraction is an important topic by itself. A survey of this topic is presented hereafter. There are two impedance measurement methods that can be employed: direct or indirect measurement. The direct measurement method is employed in [26] using Vector Network Analyzer (VNA) with an auxiliary connection board, including current sensor and jumpers-to-ground, to measure the admittance matrix of a power transformer. The errors caused by measurement cables are eliminated by taking its transmission line model into computation [27]. The other direct methods are introduced in [28] and [29] for the cables. In [28], the connecting impedance matrix is converted from the *S*-parameters measured on the short circuit and matching load configurations. It is not applicable for general devices with unknown matching load of pins. In [29], the guarding technique of Impedance Analyzer (IA) is exploited to measure the connecting impedance. In this technique, two measured pins are connected to the High and Low terminals

whereas the nonmeasured pins are shorted to the *guard terminal* while neglecting the impedance of connecting paths. The indirect measurement method using IA was introduced in [8]. In this approach, the pins of the devices are divided into two groups, pins in each group are shorted together. The impedance is measured between two groups to write a linear equation for the connecting impedance variables. This procedure is repeated until enough equations are completed. The impedance matrix is then obtained by a simple matrix inversion. The two measured-based methods in [8] and [29] are applicable for unknown matching load devices, but they are limited on the computing approaches of connecting impedance. These computing methods are based on the assumption of zero shorting path impedance, which is not always valid. This assumption is valid for specific applications where impedance of target devices, i.e., transformer and cables, are more inductive and less capacitive than that of the shorting paths. However, it is no longer valid for several passive devices such as small common mode chokes, EMI filters, on-board transformers, or other devices with capacitive ports. There is a variety of connecting impedance which can interact with that of the shorting paths in EMI frequency leading to modeling errors, and hence wrong power converter EMI propagation model.

As pointed before, the main contribution in this paper is to improve connecting impedance accuracy by removing the errors caused by the shorting path impedance. This paper also contributes on the measurement approach by introducing the measurements of voltage transfer gain (VTG) and *open impedance* for accurately extracting the connecting impedance and verification purposes. It is important to emphasize that even though the measurements are taken offline in this paper, it does not mean that the proposed GIR is only effective for offline impedance. Also, shorting impedance problems need to be overcome, whether the device is under bias or not.

III. GIR Approach

In this section, the analytical equations and measurement procedure of GIR based on NIF model [8] are summarized to introduce the connecting impedance and the method of taking measurements.

A passive device can be represented by a general impedance matrix, as shown in Fig. 2. In details, each pin is connected to each of the others by a connecting impedance. For instance, for a n-pins device, pin 1 is connected to pins $2, 3, \ldots, n$ by impedance $Z_{12}, Z_{13}, \ldots, Z_{1n}$, respectively. In this definition:

1) $Z_{ij} = Z_{ji}$ for all i, j.
2) There are $C_n^2 = n(n-1)/2$ connecting impedances.

The Kirchoff's current law equation at all pins is

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \end{bmatrix} = \begin{bmatrix} \sum\limits_{i\neq 1}^{n} Y_{i1} & -Y_{12} & \cdots & -Y_{1n} \\ -Y_{12} & \sum\limits_{i\neq 2}^{n} Y_{i2} & \cdots & -Y_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ -Y_{1n} & -Y_{2n} & \cdots & \sum\limits_{i\neq n}^{n-1} Y_{in} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} \quad (1)$$

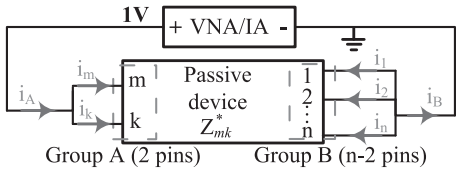

Fig. 3. Group—impedance measurement by VNA.

where $Y_{ij} = 1/Z_{ij}$ is the connecting admittance.

Equation (1) shows the fact that all Y_{ij} can be calculated with given v and i. However, they cannot be measured simultaneously by a two-port VNA/IA. Thus, n pins of devices are grouped into two groups namely Group A and B. Assuming that pins in each group are shorted together with zero impedance shorting paths, all of them share the same voltage level; then, the n-pin device can be considered as a 2-pin device whose impedance seen from A and B, hereafter called *group-impedance*, can be measured by 2-port VNA/IA. Fig. 3 shows an example of grouping and impedance measurement methods of a n-pin device, where Group A contains pins numbered *m* and *k*, group B contains the remaining pins.

Considering VNA/IA as a normalized 1V voltage source without losing generality, the basic circuit elements are

$$v_m = v_k = 1; \quad v_{i,i\notin\{m,k\}} = 0 \quad (2)$$

$$Y^*_{mk} = 1/Z^*_{mk} = i_m + i_k \quad (3)$$

where Z^*_{mk} and Y^*_{mk} is the measured impedance and admittance seen from A and B, respectively.

Substituting (2) and (3) into (1) yields

$$Y^*_{mk} = \sum_{i\notin\{m,k\}}^{n} (Y_{im} + Y_{ik}) \quad (4)$$

(4) is an equation used to solve Y_{ij} once Y^*_{mk} is measured. For a n-pin device, there are C_n^2 variables which require C_n^2 independent equations to solve. Thus, the procedure of selecting *m* and *k* is repeated until C_n^2 equations are completed. Note that the number of pins in each group can vary from 1 to $(n-1)$, and the independence of the selected set of equations must be satisfied. The connecting admittance matrix is computed as

$$\mathbb{Y}_n = \mathbb{C}_n^{-1}\mathbb{Y}_n^* \quad (5)$$

where $\mathbb{C}_n$ is the connecting matrix; $\mathbb{Y}_n^*$ and $\mathbb{Y}_n$ are admittance matrices that are measured and calculated, respectively.

IV. Nonzero Impedance Shorting Paths Analysis

In this section, the connecting impedance identification procedure of a 3-pin device is investigated with the shorting path impedance. There are three impedance measurements taken following the procedure introduced in Fig. 4. By including the shorting path impedance ΔZ, corresponding to an admittance ΔY, the equivalent circuits are shown in Fig. 5. The measured

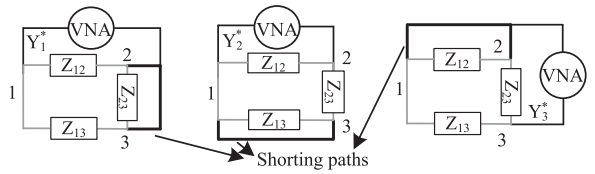

Fig. 4. Impedance measurement procedure for 3-pins device with perfect shorting impedance paths.

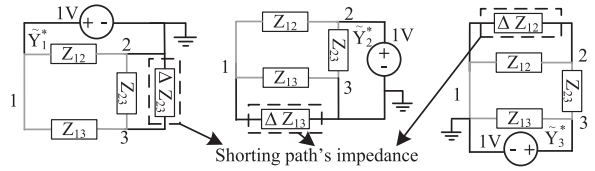

Fig. 5. Impedance measurement procedure for 3-pins device with imperfect shorting impedance paths.

admittance is computed as follows:

$$\tilde{Y}_1^* = \underbrace{Y_{12}+Y_{13}}_{Y_1^*} - \underbrace{\frac{Y_{13}^2}{\Delta Y_{23}+Y_{13}+Y_{23}}}_{e_1^*}$$

$$\tilde{Y}_2^* = \underbrace{Y_{23}+Y_{12}}_{Y_2^*} - \underbrace{\frac{Y_{12}^2}{\Delta Y_{13}+Y_{12}+Y_{13}}}_{e_2^*}$$

$$\tilde{Y}_3^* = \underbrace{Y_{13}+Y_{23}}_{Y_3^*} - \underbrace{\frac{Y_{23}^2}{\Delta Y_{12}+Y_{23}+Y_{12}}}_{e_3^*} \quad (6)$$

where Y_i^* is the measured impedance assuming the zero impedance of shorting path, as inferred from (4), e_i^* is the error of the ith measurement compared to ideal case, and Y_{ij} is the accurate connecting impedance.

The difference of the connecting admittance between the ideal and practical cases, $\tilde{Y}_{ij}$, is

$$\begin{aligned}\tilde{Y}_{12}-Y_{12} &= 0.5(-e_1^*-e_2^*+e_3^*)\\ \tilde{Y}_{13}-Y_{13} &= 0.5(-e_1^*+e_2^*-e_3^*)\\ \tilde{Y}_{23}-Y_{23} &= 0.5(e_1^*-e_2^*-e_3^*).\end{aligned} \quad (7)$$

This difference depends on the impedance level ratio between ΔY and Y_{ij}. In fact, the shorting path is inductive and its impedance value depends on material and geometry.

In case of high inductive and small capacitive device such as transformers [8] or cables [29], the shorting path impedance may be small compared to the connecting impedance at considered frequencies, i.e., $\Delta Y \gg Y_{ij} \longrightarrow e_i^* \approx 0$. Hence, the measured error can be neglected; the impedance matrix is achieved correctly without taking care of the shorting path impedance.

Conversely, the error derived from (6) can become significant in this three following cases:

1) If parallel connecting impedance is capacitive at specific frequency range and comparable with that of shorting path impedance, as shown in Fig. 6(a), e.g., $\Delta Y_{23} \approx -Y_{23} \gg Y_{12}, Y_{13}$, then $e_1^* \approx Y_{13}$, the error can be comparable to connecting admittance. The example for this case is the integrated EMI filter or power supply.
2) In worst case, at any specific frequency range, if $\Delta Y_{23} \approx -(Y_{13}+Y_{23}) \longrightarrow e_1^* \gg Y_{13}^2$, as shown in Fig. 6(b), the error can be much greater than square of connecting admittance.
3) If the shorting path is poor, i.e., long and thin conductor, its inductance can be in the same order of magnitude to the smallest connecting impedance, as shown in Fig. 6(c), e.g., $\Delta Y_{23} \approx Y_{13} \gg Y_{12}, Y_{23} \longrightarrow e_1^* \approx Y_{13}/2$, the error can be a half of connecting admittance. An example of this case is the high-power transformer with large distance between ports.

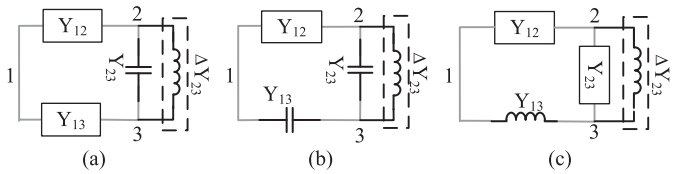

Fig. 6. Specific cases in which significant errors are created. (a) $\Delta Y_{23} \approx -Y_{23}$. (b) $\Delta Y_{23} \approx -(Y_{23}+Y_{13})$. (c) $\Delta Y_{23} \approx Y_{13}$.

In the general case of passive devices with unknown model, no cases can be ignored. For larger pin amount devices, the interaction between shorting paths and connecting impedance becomes more complicated resulting in unknown measured errors, further degrades the computational precision.

V. Proposed Newton–Raphson Method

As pointed in Section IV, the precision of NIF model is degraded by the impedance of shorting paths used in measurements. The error level is unknown since it depends on the ratios between the impedances of shorting paths and the unknown connecting impedance of devices. Therefore, this issue cannot be completely solved by only improving the layout of the shorting paths, which usually reduces its inductance. Instead, we propose to improve the accuracy of the connecting impedance, which is obtained by the NIF model (5) using curve fitting method. To avoid the impact of the impedance of shorting path used in measurements, the fitting curves are chosen as follows.

1) The *open admittance* which is measured by VNA at two pins, whereas the remaining pins are untouched. Thus, no shorting path appears in measurements.
2) The VTG between pin pairs of the devices. A common ground plane is used in measurements, but its influence to the measured data is removed by the *S*-parameter calibration procedure, as presented in Appendix A. In addition, fitting VTG curves helps to direct the connecting impedance to all correct VTGs between pin pairs of the devices, which is mandatory for computing noise propagation in the power converter via VTGs.

Solving the system of nonlinear equations is not obvious without information of the system roots. Thus, we propose to employ the newton raphson (NR) iterative method as the fit-

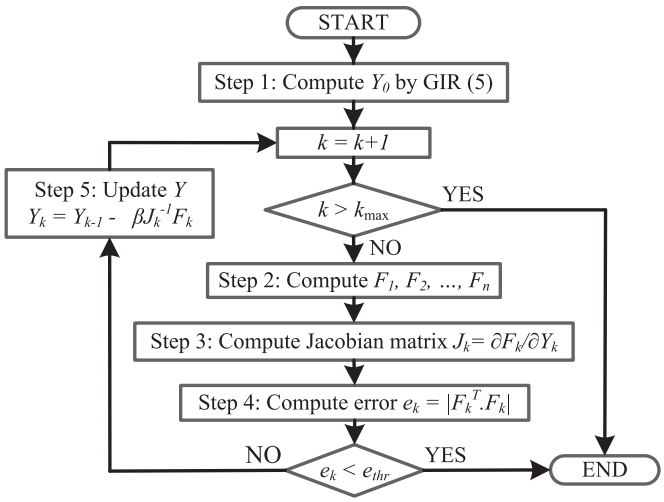

Fig. 7. Newton–Raphson method for GIR at each frequency.

ting algorithm due to its ability of solving nonlinear equations for complex variables. The NR method's accuracy and convergence depend on the distance between the *initial guess* and the system roots [31]. Therefore, the connecting impedances obtained by (5) are used as the *initial guess* since the gap between them and the system roots is significant only in some specific frequency ranges as discussed in Section IV and small at the remaining frequency ranges. Instead of these data, an arbitrary *initial guess* can force the NR to diverge or converge to the wrong roots. The summary of proposed NR approach is shown in Fig. 7. The details of each step are presented in the following sections.

A. Step 1: Variables Definition

The connecting admittance Y is used as the variables for NR iterations. It is initiated by the result obtained in (5)

$$Y^0 = [Y_{12}^0, Y_{13}^0, \ldots, Y_{(n-1)n}^0]^T = \mathbb{Y}_n. \tag{8}$$

B. Step 2: Write NR Functions

The form of NR iteration equations is

$$\begin{cases} F_1(Y_{12}, Y_{13}, \ldots, Y_{(n-1)n}) = 0 \\ F_2(Y_{12}, Y_{13}, \ldots, Y_{(n-1)n}) = 0 \\ \ldots \quad \ldots \quad \ldots \\ F_{C_n^2}(Y_{12}, Y_{13}, \ldots, Y_{(n-1)n}) = 0. \end{cases} \tag{9}$$

Each equation of F_i is formed by equalizing the measured result and their corresponding analytical equations. Two selections of F_i are discussed below with their measurement methods and equation derivations.

1) Open Admittance: An example of *open admittance* between pin 1 and pin 2, $Y_{12}^{*\text{op}}$, of a 4-pin device is shown in Fig. 8(a). Its corresponding closed form equation is derived by considering the VNA as a voltage source. For the sake of generality, this voltage source is excited in both ways: $V_{12} = 1V$ and $V_{21} = 1V$, as depicted in Fig. 8(b) and (c), respectively. The computed *open admittance* is the average of these two sources

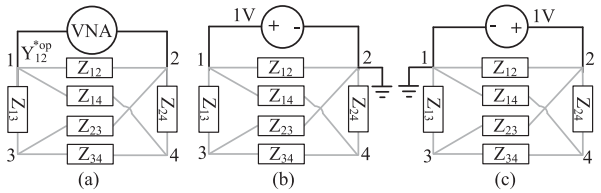

Fig. 8. Open admittance between pins 1–2. (a) Measurement. (b) Computing - $V_1 = 1, V_2 = 0$. (c) Computing - $V_1 = 0, V_2 = 1$.

$$Y_{12}^{\text{op}} = 0.5 \times \left\{ \sum_{i \neq 1}^{n} Y_{1i} - \begin{bmatrix} Y_{13} & Y_{14} \end{bmatrix} A_{12}^{-1} \begin{bmatrix} Y_{13} \\ Y_{14} \end{bmatrix} + \sum_{i \neq 2}^{n} Y_{2i} - \begin{bmatrix} Y_{23} & Y_{24} \end{bmatrix} A_{12}^{-1} \begin{bmatrix} Y_{23} \\ Y_{24} \end{bmatrix} \right\} \tag{10}$$

where A_{12} is defined as the *identified matrix* of pin pair 1–2

$$A_{12} = \begin{bmatrix} \sum_{i \neq 3}^{n} Y_{i3} & -Y_{34} \\ -Y_{34} & \sum_{i \neq 4}^{n} Y_{i4} \end{bmatrix}. \tag{11}$$

In case that the pin number of device increases, i.e., $n - pin$, (10) is unchanged. Only A_{12} is extended to be a $(n-2) \times (n-2)$ matrix. This task is straightforward.

The *open admittance* equation at pins 1–2 for NR is

$$F_i = Y_{12}^{\text{op}} - Y_{12}^{*\text{op}} = 0. \tag{12}$$

In fact, the NR for a set of all equations of *open admittance* may approach to the wrong root at some specific frequency ranges due to the subtracting operator in (10) and the fact that only connecting admittance appears in the equation. During the iterative process, all connecting admittances, Y_{ij}, may reduce to very small amplitudes, resulting in very small amplitudes of both terms

$$\left\{ \sum_{i \neq 1}^{n} Y_{1i} + \sum_{i \neq 2}^{n} Y_{2i} \right\}$$

and

$$\left\{ \begin{bmatrix} Y_{13} & Y_{14} \end{bmatrix} A_{12}^{-1} \begin{bmatrix} Y_{13} \\ Y_{14} \end{bmatrix} + \begin{bmatrix} Y_{23} & Y_{24} \end{bmatrix} A_{12}^{-1} \begin{bmatrix} Y_{23} \\ Y_{24} \end{bmatrix} \right\},$$

while effectively approaching the correct Y_{12}^{op}. As a result, even though the *open admittance* is fit, all the connecting admittances converge to the wrong roots whose amplitudes are very small and presents wrong VTG between pin pairs of devices. This issue is avoided by adding the VTG curve with different form of equation to the system, as presented in the next section.

2) VTGs Between Pin Pairs: An example of VTG V_{12}^{42}, where V_{42} is computed/measured considering the excitation source $V_{12} = 1V$, is presented for a 4-pin device. The experimental VTG V_{12}^{*42} is obtained indirectly by measuring

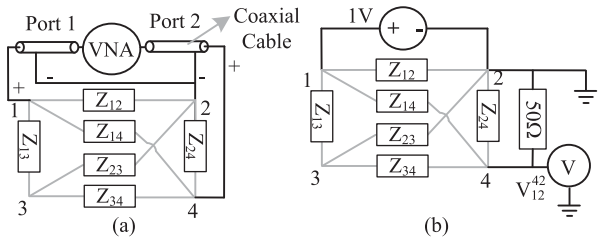

Fig. 9. VTG. (a) Measurement by S-ports. (b) Computational model.

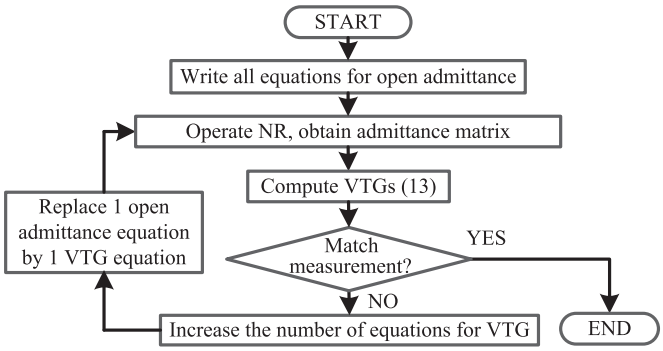

Fig. 10. Proposed NR with the combined set of equations.

S-parameters employing coaxial cables, as shown in Fig. 9(a). The data conversion is introduced in [30]. The analytical equation to compute V_{12}^{42} is derived from the equivalent circuit shown in Fig. 9(b) as follows:

$$\begin{bmatrix} \cdots \\ V_{12}^{42} \end{bmatrix} = \begin{bmatrix} \sum_{i\neq 3}^{n} Y_{i3} & -Y_{34} \\ -Y_{34} & \sum_{i\neq 4}^{n} Y_{i4} + \dfrac{1}{50} \end{bmatrix}^{-1} \begin{bmatrix} Y_{13} \\ Y_{14} \end{bmatrix} \tag{13}$$

where 50 Ω is the internal resistor of port 2 of the VNA.

Finally, VTG equation for the NR method is written as

$$F_i = V_{12}^{42} - V_{12}^{*42} = 0. \tag{14}$$

In fact, the VTG below -80 dB is not used NR equation due to the possible errors created by the precision limit of the VNA.

3) Combined Equations: One proposes to use the NR method with the set of equations combined of *open admittance* and VTGs by the procedure described in Fig. 10.

In which, the GIR is started by the original NIF, and the *open admittance* is used as verification purpose. If the error is not acceptable (condition of Match measurement is not satisfied), an equation of VTG is added to improve the computational precision. Otherwise, if the error is very small, the procedure is done, the connecting impedance computed by the original NIF is used as the final result. This is the case of cable and transformer, where errors are negligible as presented in the previous publications [26]–[29].

C. Step 3: Jacobian Matrix Computing

The Jacobian matrix J is the derivative function of F as

$$J = \frac{\partial F}{\partial Y} = \begin{bmatrix} \dfrac{\partial F_1}{Y_{12}} & \dfrac{\partial F_1}{Y_{13}} & \cdots & \dfrac{\partial F_1}{Y_{(n-1)n}} \\ \dfrac{\partial F_2}{Y_{12}} & \dfrac{\partial F_2}{Y_{13}} & \cdots & \dfrac{\partial F_2}{Y_{(n-1)n}} \\ \vdots & \vdots & \ddots & \vdots \\ \dfrac{\partial F_{C_n^2}}{Y_{12}} & \dfrac{\partial F_{C_n^2}}{Y_{13}} & \cdots & \dfrac{\partial F_{C_n^2}}{Y_{(n-1)n}} \end{bmatrix}. \tag{15}$$

It must be calculated at each iteration, and usually takes the longest computing time due to the multiple derivative operations. To improve the computation speed, the closed-form function of each element of J is derived offline from the closed form of $F(9)$ by symbolic mathematical packages. Then, J is evaluated at each iteration by placing the real value of variables into its closed-form functions.

D. Step 4: Error Computing

The error at each iteration of NR method is evaluated by

$$e = \|F\|^2 = \sum_{i=1}^{n} |F_i|^2. \tag{16}$$

The iteration process ends as soon as the error reaches a given threshold, $e < e_{\text{thr}}$, where e_{thr} is chosen based on the measurement device precision. For typical devices, whose precision of impedance and VTG is 1 mΩ and -80 dB, respectively, e_{thr} can be chosen at 10^{-8}.

E. Step 5: Connecting Admittance Update

The connecting admittance is computed by the generalized Newton's formula (17) [31]–[32]. The o-r factor β is used to control the convergence rate, and hence, must be adjusted carefully to ensure the convergence of the NR method

$$Y_k = Y_{k-1} - \beta J_k^{-1} F_k. \tag{17}$$

F. Overrelaxation Factor Computing Strategy

Generally, the NR convergence rate is low with too small β but it may diverge with too high β. The selection of β prior to computation is difficult since it depends on the complicated functions of variables, which may vary differently iteration by iteration. To cope with this problem, one proposes an o-r factor computing method to calculate the proper β at each iteration. More precisely, one employs a logic of β control based on the error ratio, which is divided by the errors of current and previous iterations, as shown in Fig. 11. This strategy is used between Step 4 and Step 5 of the NR approach.

VI. Experimental Results

In this section, the experimental model of an *LC* filter, formed by the commercial common choke WE-SL2 250 μH (L_1) and a 0.1 μF capacitor (C_1), is extracted by using GIR. The experimental results present the errors caused by the shorting

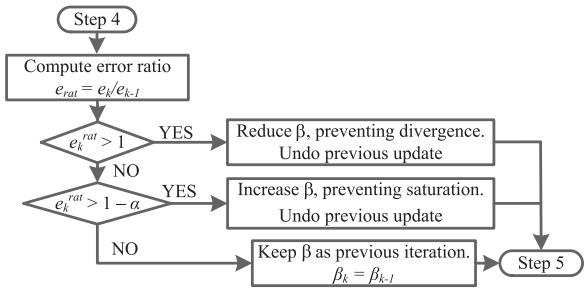

Fig. 11. Overrelaxation factor computing algorithm.

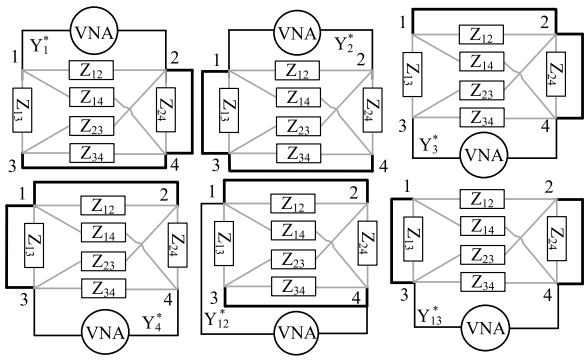

Fig. 12. Impedance measurement procedure for 4-pin device.

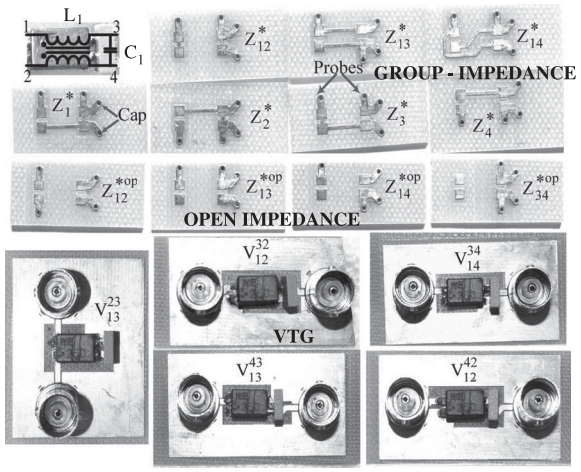

Fig. 13. Measured prototypes of the *LC* filter.

path impedance regarding to case 1 and case 3 (as discussed in Section IV), and the effectiveness of the proposed GIR to cancel these errors. To remove the impacts of extra components used in measurements, i.e., cables and measured jig's geometry, the measurements are performed in two separate frequency ranges, i.e., 100 kHz–30 MHz and 30–200 MHz, with proper calibrations. Considering the *LC* filter as a 4-pin device, the *initial guess* of the connecting impedance is computed by the impedance measurements taken following the procedure presented in Fig. 12.

The measured jigs used to extract the impedance and VTG are shown in Fig. 13. All measurements are performed using a Agilent E5061B VNA. They are presented in Figs. 14 and 15. The following nomenclatures are used on these pictures:

1) the term "measured" indicates the data extracted by the VNA;
2) the term "w/o-NR" indicates the data computed from the connecting impedance obtained in (5) without NR (also means the results with the original NIF);
3) the term "w-NR" indicates the data computed from the connecting impedance resulted in the NR method (also means the results with GIR).

A. Experimental Results at Conducted EMI Frequencies

The experimental results of the *LC* filter in frequency range 100 kHz–30 MHz is shown in Fig. 14. Fig. 14(a) shows six measured group–impedance described in Fig. 3. One observes the small impedance of Z_3^*, Z_4^*, Z_{13}^*, and Z_{14}^* in frequency range 3–7 MHz. They are used in (5) to compute the connecting impedances, i.e., Z_{ij} w/o-NR, also used as the *initial guess* of NR, as introduced in Section V-A.

The impact of the shorting path impedance is shown in Fig. 14(b) by the differences between computation w/o-NR and measurements of V_{12}^{32}, V_{12}^{42}, $Z_{12}^{\rm op}$, and $Z_{34}^{\rm op}$ in frequency range 3–7 MHz. These differences are caused by the interaction between the small impedance of C_1 and the impedance of shorting paths as given in Fig. 6(b), and analyzed in Section IV. Similar disturbances are observed in the performances of VTGs V_{14}^{34}, V_{24}^{34}, and V_{13}^{23}, as shown in Fig. 14(d).

To eliminate these errors, the proposed NR method is employed. As the symmetry of L_1, i.e., $Z_{13} = Z_{24}$ and $Z_{14} = Z_{23}$, instead of six equations for the general case, only four equations are needed to solve the four connecting impedance variables. The equations of V_{12}^{32}, V_{12}^{42}, $Z_{12}^{\rm op}$, and $Z_{34}^{\rm op}$ are written as described in Section V-B. Thanks to the proposed NR method, V_{12}^{32}, V_{12}^{42}, $Z_{12}^{\rm op}$, and $Z_{34}^{\rm op}$ fit well with measurements, as observed in Fig. 14(b).

The curves of connecting impedance obtained by GIR with and without NR method are shown in Fig. 14(c). One observes the significant improvements of the connecting impedance Z_{13} and Z_{14} in frequency range 3–7 MHz. The same improvement is observed on Z_{34} in frequency range 3–30 MHz whereas Z_{12} remains unchanged. The small changes of all connecting impedance below 1 MHz are to fit the VTG V_{12}^{42}. They correspond well to the disturbances as aforementioned.

The VTGs V_{14}^{34}, V_{24}^{34}, and V_{13}^{23}, not used to be fit by NR, are plotted in Fig. 14(d). As observed, the VTGs obtained by NR overlap their measurements well including small gains of V_{14}^{34} and V_{24}^{34} as well as nearly unity gain of V_{13}^{23}. The small error appearing on V_{24}^{34} at frequency of 2 MHz is resulted from the small errors in measurements at the corner frequency of $Z_{12}^{*\rm op}$, V_{12}^{*32}, and V_{12}^{*42}.

B. Experimental Results at Radiated EMI Frequencies

This section presents the experimental results of the *LC* filter in frequency range 30–200 MHz, as shown in Fig. 15, to point out the effectiveness of NR to correct the errors caused as case 3 introduced in Section IV. Fig. 15(a) shows the measured

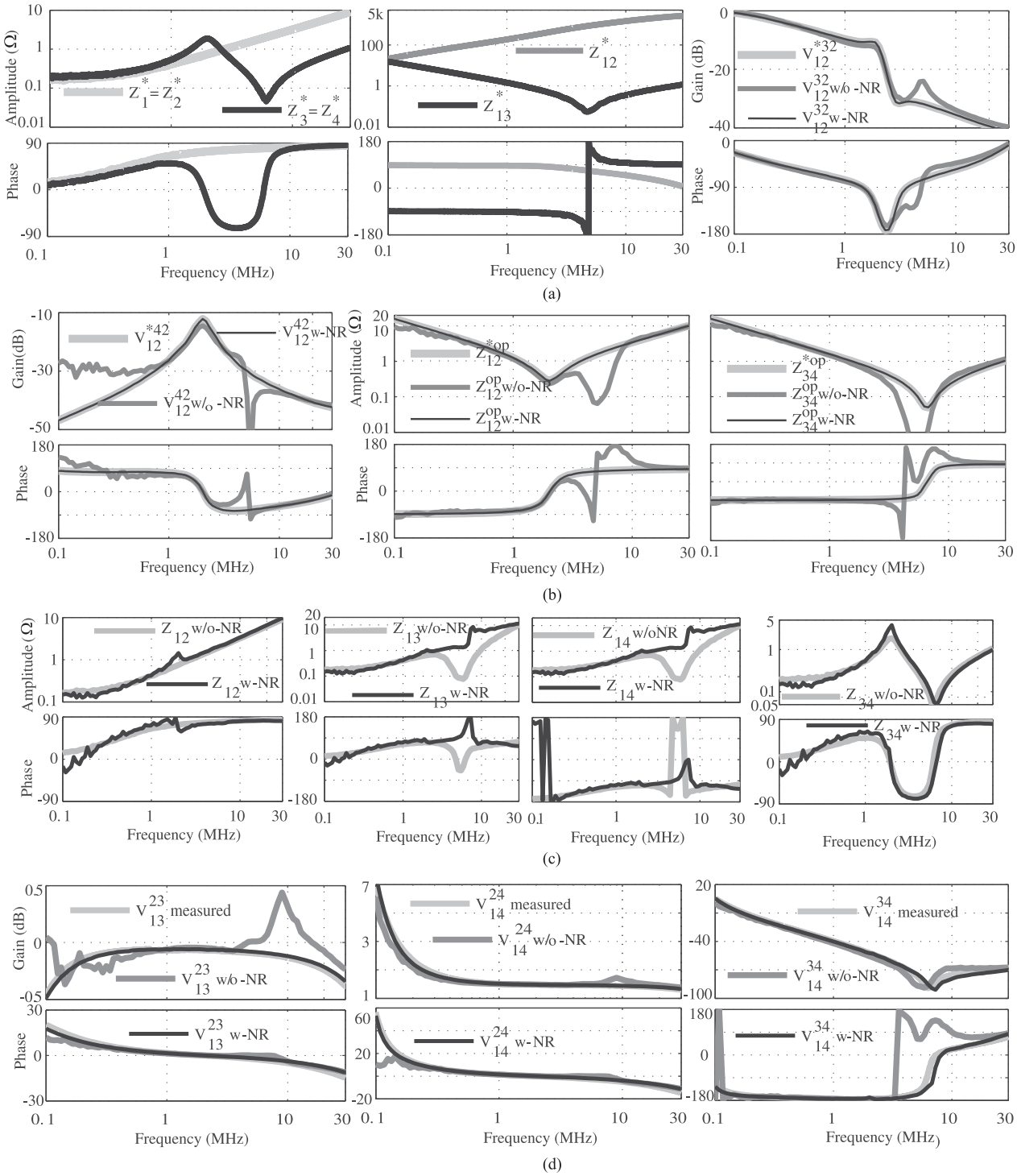

Fig. 14. Experimental results for LC filter at low frequency. (a) Measured group—impedance. (b1) Transfer function fitting V_{12}^{32}. (b2) Transfer function fitting V_{12}^{42}. (b3) Open impedance fitting $Z_{12}^{\rm op}$. (b4) Open impedance fitting $V_{34}^{\rm op}$. (c1) Connecting impedance Z_{12}. (c2) Connecting impedance $Z_{13} = Z_{24}$. (c3) Connecting impedance $Z_{14} = Z_{23}$. (c4) Connecting impedance Z_{34}. (d) Transfer function tests.

group-impedance. It is observed that the inductive behaviors of $Z_1^* = Z_2^*$ and $Z_3^* = Z_4^*$ decreases with frequency. The *initial guess* of NR is computed from these data as mentioned in Section VI-A.

The effect of the shorting path impedance is shown in Fig. 15(b) by the gaps between measurement and computation of V_{12}^{32}, V_{12}^{42}, $Z_{12}^{\rm op}$, and $Z_{34}^{\rm op}$. The differences between measurements and computations are small with the biggest errors of 4 dB of V_{12}^{32}, shown in Fig. 15(b1). One also observes that the error magnitude increases with frequency for all data. This error increasing is caused by the impedance of the shorting path (printed circuit board (PCB) trace which is mostly inductive)

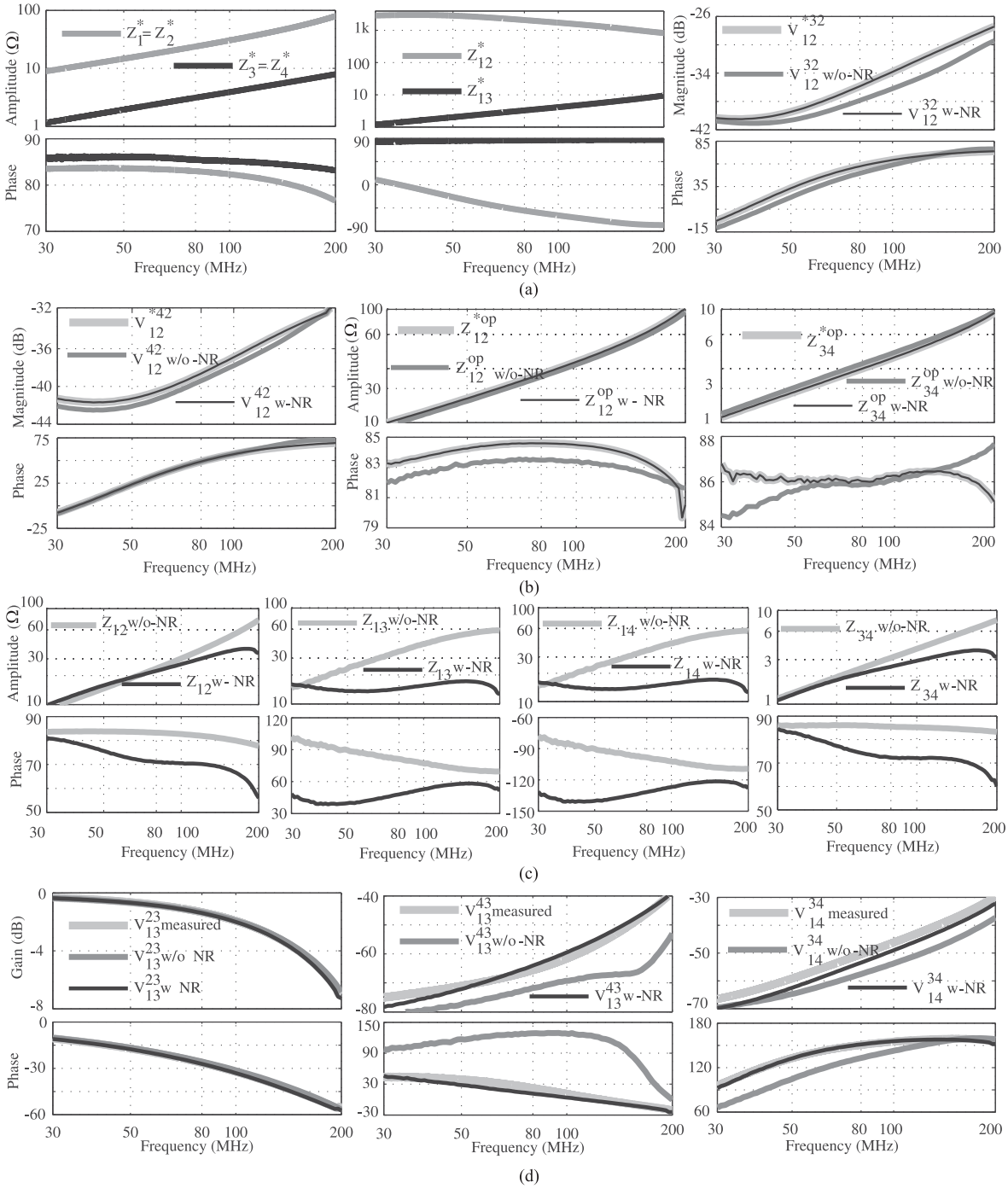

Fig. 15. Experimental results for *LC* filter at high frequency. (a) Measured group–impedance. (b1) Transfer function fitting V_{12}^{32}. (b2) Transfer function fitting V_{12}^{42}. (b3) Open impedance fitting Z_{12}^{op}. (b4) Open impedance fitting V_{34}^{op}. (c1) Connecting impedance Z_{12}. (c2) Connecting impedance $Z_{13} = Z_{24}$. (c3) Connecting impedance $Z_{14} = Z_{23}$. (c4) Connecting impedance Z_{34}. (d) Transfer function tests.

increases faster than connecting impedance (whose inductance usually reduces with frequency), leading to higher error at high frequency. This is the error case 3 discussed in Section IV. This trend is confirmed with the disturbances of V_{13}^{43} and V_{34}^{14}, as shown in Fig. 15(d).

In order to remove these errors, the proposed NR approach is used to fit the computations with measurements of V_{12}^{32}, V_{12}^{42}, Z_{12}^{op}, and Z_{34}^{op}. It results in the connecting impedance shown in Fig. 15(c). One observes the significant improvements of the connecting impedance, i.e., Z_{12} and Z_{34} in frequency of 80–200 MHz; Z_{13} and Z_{14} in frequency of 30–200 MHz, thanks to the proposed NR method. It shows that the inductance of common choke decreases with frequency, which is a typical behavior. The accuracy of the proposed method is validated by the performances of VTGs V_{13}^{23}, V_{13}^{43}, and V_{34}^{14}, depicted in Fig. 15(d). As seen, the VTGs computed from the connecting

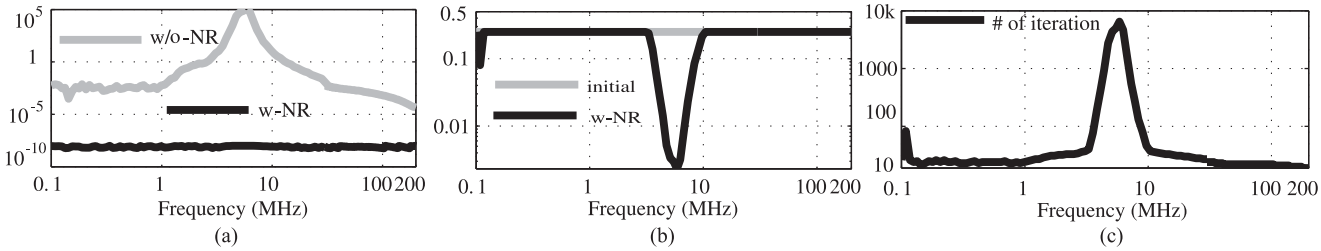

Fig. 16. Newton–Raphson characteristics. (a) Error. (b) Over relaxation factor. (c) Number of iteration.

impedance obtained by NR match their measurements very well. It is a very good improvement considering the errors of 20 dB (V_{13}^{43}) and 10 dB (V_{34}^{14}) achieved with the original connecting impedance computed by the original NIF.

The characteristics of NR method are illustrated in Fig. 16 including error, o-r factor and number of iterations. As seen, the o-r factor is 0.4 and only few iterations are needed in frequency below 1 MHz and above 30 MHz since the *initial guess* is very closed to the root, shown by small errors in those frequency ranges. In addition, the lowest o-r factor and highest number of iterations correspond to the highest initial error in the frequency of 3–30 MHz. For instance, the o-r factor is decreased to prevent NR from diverging making the convergence rate slower than that in the remaining frequency ranges. It confirms the effectiveness of the computing approach proposed in Section V-F. In addition, Fig. 16(a) also shows that the proposed GIR is dedicated to correct both small errors, usually present with cables and transformers using NIF, and significant errors, where NIF is not accurate to implement.

VII. Conclusion

In this paper, an effective GIR is proposed for modeling the passive device used in power converter based on the measurements of impedance and Scattering parameters. It is developed from the original NIF with the improvement of correcting computational errors created by the shorting path impedance used in the measurement procedure. This paper also introduces the new measured data, i.e., VTG and *open impedance*, and the complete identification procedure required to ensure the model accuracy. In addition, the computing approach for overrelaxation method is proposed to guarantee the NR convergence with different input data. As a result, the proposed GIR is precise whether the effect on the shorting path impedance is negligible (as NIF), or significant (as the considered components in this paper). Thanks to GIR, all passive devices without specific models can be accurately modeled and integrated into the power converter EMI model to predict the noise spectrum of the next generation of SiCFET and GaN - based converter.

Appendix

A. S-Port Calibration Procedure

To remove the effect of cable impedance, the S-port calibrations, i.e., open, short, load, and through, must be performed at the end of the cables, as depicted in Fig. 17.

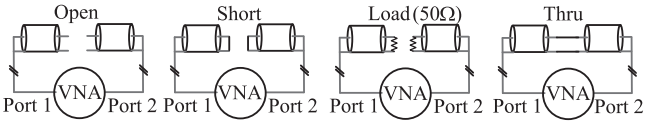

Fig. 17. Calibration procedure of a 2-port VNA.

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Tung Ngoc Nguyen (S'14) was born in Phu Yen province, Vietnam. He received the B.S. degree in electrical engineering from Hochiminh City University of Technology, Ho Chi Minh, Vietnam, in 2010. He is currently working toward the Ph.D. degree in electrical engineering at the École de Technologie Supérieure, Montreal, QC, Canada, where he researches on EMI for power converter.

From 2016 to 2017, he was with Current, powered by GE, Lachine, QC, Canada, where he worked on LED driver. Since 2017, he has been with Idénergie, Montréal, QC, Canada, where he is doing research and development of a smart—grid interactive photovoltaic system. His research interests include power converter modeling, EMI prediction/attenuation, and grid-tied SiC/GaN based power converter.

Handy Fortin Blanchette (S'07–M'10) received the B.Eng., M.Eng., and Ph.D. degrees in electrical engineering from the École de Technologie Supérieure (ÉTS), Montréal, QC, Canada, in 2001, 2003, and 2010, respectively.

From 1994 to 1997, he was engaged in industrial automation. From 1998 to 2000, he was with the Bombardier Transport-ETS Research Laboratory, Montréal, QC, Canada, where he worked on a high-power traction system. From 2001 to 2003, he was involved in the development of an electrical drive library for the Simulink (MATLAB) environment. From 2007 to 2010, he was with OPAL-RT Technologies, where he led CPU-based and FPGA-based power electronics real-time simulation projects. From 2010 to 2011, he was a Visiting Scholar in the Center for Power Electronic and System, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, where he was involved in the packaging of high-temperature converters for aircraft applications. He is currently a Professor of electrical engineering at ÉTS. His current research interests include EMI prediction, circuit modeling, and high density power converters packaging.

Ruxi Wang (S'09–M'12–SM'16) received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, and the Ph.D. degree in high power density and high temperature converter design for transportation application from the Center for Power Electronics Systems (CPES), Virginia Tech, Blacksburg, VA, USA, in 2004, 2007, and 2012, respectively.

In 2012, he joined the Global Research Center of General Electric Company, Niskayuna, NY, USA, as a Lead Electrical Engineer. He has published more than 40 papers in refereed journals and international conference proceedings and more than 20 awarded or pending patents. His research interests include high-power-density converter design in transportation application, healthcare electronics, electromagnetic interference technology, more electrical aircraft system, advanced components, and packaging technology.

Dr. Wang received the William M. Portnoy Award for the Best Paper published in the IEEE Energy Conversion Congress and Exposition (ECCE) in 2012. From 2013 to 2016, he was the General Chair for 2011 CPES Annual Conference and the Technical Program Chairs, the Session Chairs, and the Topic Chairs for ECCE. Since 2015, he has been an Associate Editor of the IEEE TRANSACTION ON INDUSTRIAL APPLICATIONS and also was the Vice Chair of the Power Electronics Devices and Components Committee in IEEE Industry Applications Society.