Delay and Decoupling Analysis of a Digital Active EMI Filter Used in Arc Welding Inverter

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***Abstract*—Arc welding inverter supply with switch and digital control is widely used, due to the advantages of high controllability, small size, and high efficiency. With the constant increasing of switching frequency and decreasing of arc welding machine size, the conducted electromagnetic interference (EMI) becomes serious, especially for common mode (CM)-conducted EMI. Meanwhile, as the development of digital processing technique, digital active EMI filter (DAEF) technology, which uses digital control and embedded mode, has become a hot research topic. However, the conventional DAEF fails to consider time delay effect. Its model cannot accurately describe DAEF filtering behavior. Moreover, decoupling circuit lacks scientific design method. To cope with these, this paper proposes a precise DAEF model which considers both the time delay of digital processing portion and the parasitic parameters of passive components. Moreover, based on impedance matching principle, a detailed and scientific design method of decoupling circuit is put forward. Meanwhile, the arc welding inverter system with embedded DAEF is designed, modeled, and compensated. Finally, experiment results show that the proposed precise model can predict the system filtering performance accurately. And the proposed design method of decoupling circuit is very effective to suppress the CM-conducted EMI. The embedded DAEF can improve system stability and dynamic performance.**

***Index Terms*—Common mode (CM) conducted electromagnetic interference (EMI), decoupling, delay model, digital active embedded, EMI filter, EMI.**

I. Introduction

THE arc welding machine with switching power conversion and digital control is a hot research pot in current arc welding technology field [1]. It is now developing toward the direction of digitalization and intelligentization. This brings forward higher demands for arc welding inverter supply, such as stable control capability [2], [3], flexible dynamic response ability [1]–[4], good electromagnetic interference (EMI) performance [5]–[7], etc. With the constant increase of switching frequency and decrease of arc welding machine size, EMI issue has inevitably become a serious problem [8], [9], especially for common mode (CM)-conducted EMI. CM-conducted EMI not only pollutes public power grid, but also influences the operation of surrounding electronic devices. What is more, the stability and reliability of arc welding inverter itself can also be affected.

In the face of those serious EMI problems, the task of EMI minimization method becomes more and more overwhelming. To suppress conducted EMI, the most generally used method is to set EMI filters. Traditional EMI filters can be divided into: passive EMI filter (PEF), active EMI filter (AEF), and hybrid active EMI filter (HAEF).

PEFs are widely used for their simplicity and reliability [10]–[18]. However, they suffer from such disadvantages as bulky, heavy, unacceptable component loss, and poor high-frequency performance. These make them difficult to satisfy the critical design requirements of power electronics equipment. AEFs make use of closed-loop control by EMI sensing, reverse amplification, and injection with high flexibility [19]–[25]. They overcome the drawbacks of size and loss relative to PEFs. But due to the limitations of gain bandwidth, AEFs are not good at suppressing high-frequency noise and high amplitude current noise. On considering the features of PEFs and AEFs, HAEF is introduced to make a full use of both passive filtering components and active amplifying circuit [26]–[31]. However, gain bandwidth problem still exists. It is difficult to obtain better suppression results in a wide frequency range. Moreover, the additional voltage supply of amplifier is still an application bottle neck to be considered. Nevertheless, these contributions are very important to power electronics and EMI research. It is widely believed that this line of research has not yet reached its majority.

As well known, with the improvement of digital processing technique, such as high speed and high precision field-programmable gate array (FPGA), analog-digital converter (ADC), and digital-analog converter (DAC), the dream of using digital active EMI filter (DAEF) technique to reduce conducted EMI has come to true. The concept of DAEF was first proposed in 2012 by Queen's University, as stated in [32]. It is an AEF using digital signal processing technique. Since the signal is no longer traditional analog one, the reconstruction procedure can be more accurate with various digital control methods. More importantly, it opens up a new idea which uses digital active controller to suppress the conducted EMI.

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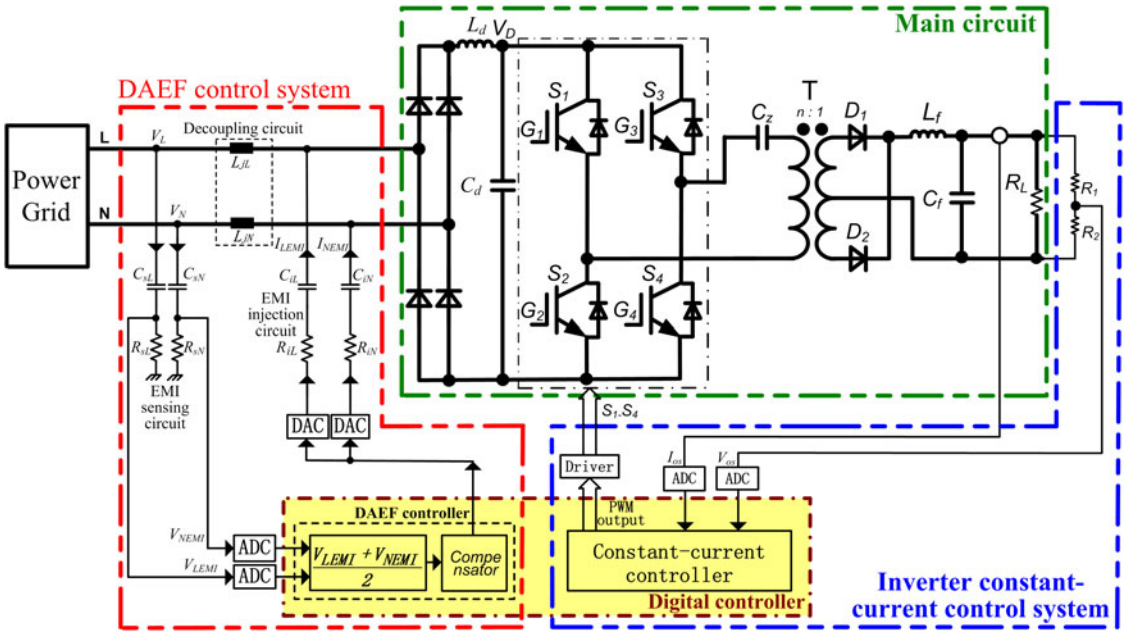

Fig. 1. Proposed DAEF control system embedded in arc welding inverter.

In the past few years, the effectiveness of DAEF had been verified in photovoltaic grid-connected inverters [33], electric vehicle converters [34], and other switching power converters [35]. A scheme, which can selectively suppress the CM and DM EMI in accordance with the actual situation of CM EMI and DM EMI, is reported in [36] and [37]. DAEF forms a digital closed-loop control system through sensing EMI, ADC sampling, digital compensation computing, DAC output, and injection EMI cancelling. However, there are still some problems existing in these DAEF technologies. First, traditional model neglects the influence of time delay (digital processing portion) on EMI filtering performance. It cannot accurately describe the behavior of DAEF filters. Second, the decoupling mechanism between sensing point and injection point is not clear. Therefore, the decoupling circuit lacks scientific design method.

On considering the above-mentioned problems, a precise digital active EMI filtering model to reduce CM-conducted EMI of arc welding inverters is proposed in this paper. The main contributions of the digital active filtering method are listed as follows.

1) An embedded DAEF precise model is proposed. The model considers both time delay of digital processing portions and parasitic parameters of passive components. And the time delay impact on EMI filtering performance is analyzed in detail.
2) Based on impedance matching principle, decoupling mechanism between sensing and injection point is proposed. And a detailed and scientific design method of decoupling circuit is put forward.
3) A digital control system of arc welding inverter embedded a DAEF controller is designed. And the control system stability and dynamic performance of the arc welding inverter is analyzed.

The proposed DAEF controller has some advantages as follows.

1) The proposed embedded DAEF precise model can accurately describe the DAEF filtering behavior, due to simultaneously considering parasitic parameters and delay effect.
2) There is only a single-turn inductor in the main power circuit of the proposed decoupling circuit. And there is no other component in series with the power circuit of arc welding inverters. Therefore, the size and loss of the arc welding inverter embedded DAEF can be reduced a lot.
3) The proposed DAEF controller not only can selectively suppress the CM EMI and DM EMI, but also can effectively prevent interconversion between CM and DM interference.
4) Since the DAEF is embedded in the inverter, the control system performance of arc welding inverter is improved in high frequency.

This paper is organized as follows. Section II presents the embedded DAEF precise model with time delay and the parasitic parameters. Then arc welding inverter control system model with embedded DAEF is derived. Section III analyzes delay effect of the embedded DAEF controller. Section IV proposes a scientific design method for DAEF decoupling circuit. Section V designs a compensator of the arc welding inverter with embedded DAEF. Experimental results are presented and discussed in Section VI. And then, some main conclusions are given in Section VII.

II. Proposed DAEF Control System Embedded in Arc Welding Inverter

The DAEF control system embedded in arc welding inverter is shown in Fig. 1. The controller of DAEF is embedded in the

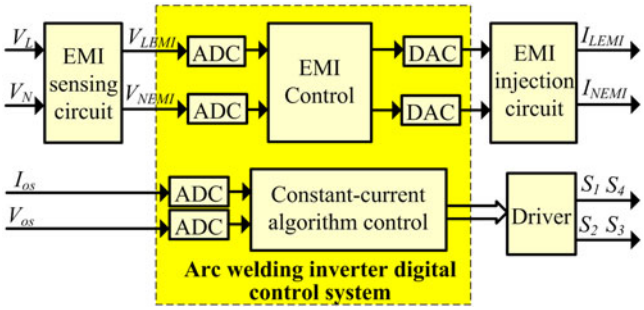

Fig. 2. Control signal flow direction diagram of arc welding inverter control system with DAEF.

digital controller system of arc welding inverter. DAEF is set in the front of arc welding inverter to suppress the conducted EMI.

A. DAEF Topology and Principle

As shown in Fig. 1, the circuit topology of proposed embedded DAEF includes six classes: EMI sensing circuit, EMI injection circuit, ADC sampling circuit, DAC output circuit, digital controller, and decoupling circuit between the injection point and sensing point. For *L* line and *N* line of power supply, the suppressing principles of conducted EMI are same. EMI sensing circuit, which consists of a resistor and a capacitor, actually is an *RC* high-pass filter and senses the conducted EMI signal generated by arc welding inverters. And EMI injection circuit actually is a low-pass filter and it injects the EMI signal reconstructed by digital controller to cancel EMI noise source. ADC sampling circuit transfers the sensed EMI signal to digital signal for DAEF controller. DAC output circuit transfers the reconstructed digital EMI signal to analog EMI signal. ADC and DAC generally need high sample rate to improve data conversion accuracy in high-frequency band. DAEF controller is embedded in the digital controller of arc welding inverter. It can not only save total cost of power converters, but also easily implement coordinating and flexible control strategy of DAEF. DAEF controller usually uses FPGA as a control unit, which programs with hardware description language and has parallel processing ability, so it can improve system rapidity and filtering performance. The decoupling circuit reduces the high-frequency coupling between sensing point and injection point to improve filtering performance.

The signal flow direction of embedded DAEF control system is shown in Fig. 2. EMI sensing circuit picks up conducted EMI signal V_{LEMI} and V_{NEMI} from *L* and *N* power line for ADC sampling circuit. ADC sampling circuit acquires sensed conducted EMI signals V_{LEMI} and V_{NEMI}, and transfers them to digital signals for DAEF controller. DAEF controller reconstructs sensed digital EMI signals to generate EMI injection signals for canceling EMI source at a certain control algorithm by programming. And controller outputs them to DAC output circuits. DAC output circuit transfers reconstructed EMI signal to a 0–20 mA EMI signal I_{LEMI} (I_{NEMI}) which can cancel 120 dBμV EMI noise source. The I_{LEMI} (I_{NEMI}) cancels the EMI signal on *L* (*N*) power line generated by arc welding inverters as EMI noise source through EMI injection circuit.

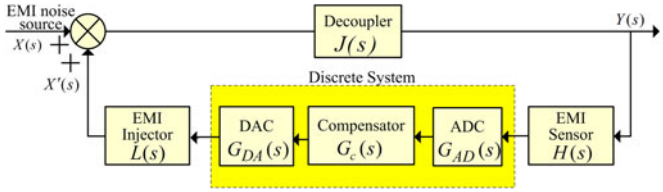

Fig. 3. Control block diagram of embedded DAEF control system.

B. Proposed Embedded DAEF Precise Model

The feedback system diagram of embedded DAEF is illustrated in Fig. 3. $X(s)$ is EMI noise generated by arc welding inverters, and is picked up from *L* (*N*) power line. $X'(s)$, which is based on sensed EMI noise $Y(s)$, is the injection EMI noise sent by DAC to cancel noise source $X(s)$. $Y(s)$ is EMI noise canceled by $X'(s)$ to $X(s)$ through decoupling, and it flows to power grid by conducting mode along *L* (*N*) power line. It is the ideal aim to make the $Y(s)$ equal to zero.

So, the closed-loop system transfer function of DAEF can be written as

$$G_{\mathrm{DAEF}}(s) = \frac{J(s)}{1 - H(s)G_{\mathrm{AD}}(s)G_C(s)G_{\mathrm{DA}}(s)L(s)J(s)}. \quad (1)$$

The filtering performance of embedded DAEF is badly affected by the time delay of digital processing portion and the parasitic parameters of passive components, especially in the high-frequency band. Only considering these two factors can the precise model of embedded DAEF accurately describe the filtering behavior of DAEF. So, for ADC sampling circuit, DAC output circuit and digital controller, their delay characteristic should be considered; for the model of EMI sensing circuit, EMI injection circuit and decoupling circuit, their high-frequency parasitic parameters should be considered. In this section, taking the embedded DAEF system on *L* power line, the precise model of embedded DAEF is built.

Digital processing portion of DAEF includes ADC sampling circuit, DAC output circuit, and digital controller. Every circuit has its delay time. The time $t_{\mathrm{AD}d}$ is delay time of ADC sampling circuit. And it is a nonlinear function about sampling voltage V_s. It can be described as

$$t_{\mathrm{AD}d} = \frac{K_{\mathrm{AD}}V_s}{(V_s - V_{\mathrm{th}})^{\alpha}} \quad (2)$$

where K_{AD} is a constant that depends on the device or process parameters and the capacitive loading of the gate. The value of α (1.5–2) also depends on process technology. V_{th} is threshold voltage. And V_s is sampling signal voltage [38], [39]. For DAEF control system on *L* power line, $V_s = V_{LEMI}$. So, considering delay time $t_{\mathrm{AD}d}$, the transfer function $G_{\mathrm{AD}}(s)$ of ADC sampling circuit of DAEF can be expressed as

$$G_{\mathrm{AD}}(s) = \frac{1}{T_{\mathrm{sp}}}(1 + e^{-\mathrm{st}_{\mathrm{AD}d}}) = \frac{1}{T_{\mathrm{sp}}}\left(1 + e^{-s\frac{K_{\mathrm{AD}}V_{LEMI}}{\left(V_{LEMI}-V_{\mathrm{th}}\right)^{\alpha}}}\right) \quad (3)$$

where T_{sp} is sampling period.

Generally, DAC is a zero-order holder. When considering the delay time and nonlinear portion of DAC output circuit, the transfer function $G_{\mathrm{DA}}(s)$ of DAC can be expressed as

$$G_{\mathrm{DA}}(s) = \frac{D_{\mathrm{zoh}}(s)B(s)}{s} \tag{4}$$

where $D_{\mathrm{zoh}}(s)$ is the transfer function of zero-order holder [34], [35], $B(s)$ represents the delay time and nonlinear portion, and can be described as

$$B(s) = \frac{e^{-st_{\mathrm{DA}d}}}{1+\tau_{\mathrm{DA}}s} \tag{5}$$

where $t_{\mathrm{DA}d}$ is DAC delay time and τ_{DA} is a constant about nonlinear portion [40]. Therefore, by replacing $B(s)$ in (4) by (5), the transfer function $G_{\mathrm{DA}}(s)$ of DAC with delay time and nonlinear characteristic can be expressed as

$$G_{\mathrm{DA}}(s) = \frac{D_{\mathrm{zoh}}(s)e^{-st_{\mathrm{DA}d}}}{s(1+\tau_{\mathrm{DA}}s)}. \tag{6}$$

Digital controller of DAEF compensates EMI signal at a certain control algorithm by programming. The compensator usually is designed based on the system index requirement. In this paper, an inverted proportional compensator is selected. Furthermore, the run time τ_{con} of program cannot be ignored. So, the transfer function $G_C(s)$ of DAEF digital controller with delay time can be described as

$$G_C(s) = -Ke^{-s\tau_{\mathrm{con}}} \tag{7}$$

where K is a proportional coefficient, and τ_{con} is delay time introduced by digital controller program [41].

EMI sensing circuit actually is an *RC* high-pass filter, and its high-frequency equivalent model of *L* power line is shown in Fig. 4(a), where $R_{C_{\mathrm{sL}}}$ and $L_{C_{\mathrm{sL}}}$, respectively, are equivalent series resistance (ESR) and equivalent series inductance (ESL) of the capacitor C_{sL}, and where $L_{R_{\mathrm{sL}}}$ and $C_{R_{\mathrm{sL}}}$, respectively, are ESL and equivalent parallel capacitance (EPC) of the resistor R_{sL}. So, the transfer function $H(s)$ of EMI sensing circuit with parasitic parameters can be expressed as (8) shown at the bottom of this page, where $\omega_{\mathrm{sen}} = 2\pi f_{\mathrm{sen}} = \frac{1}{R_{\mathrm{sL}}C_{\mathrm{sL}}}$ is the corner frequency of high-pass filter. According to the standard CISPR11 [45], f_{sen} should be 150 kHz to pick up EMI noise signal above 150 kHz.

EMI injection circuit is an *RC* low-pass filter. Its high-frequency equivalent circuit model of *L* power line is shown in Fig. 4(b), where $R_{C_{iL}}$ and $L_{C_{iL}}$, respectively, are ESR and ESL of the capacitor C_{iL}, and where $L_{R_{iL}}$ and $C_{R_{iL}}$, respectively, are ESL and EPC of the capacitor R_{iL}. The capacitor C_{iL} of EMI injection circuit mainly prevents the 50 Hz current and its harmonic current on *L* (*N*) power line from destroying DAC sampling circuit. Because the value of capacitor C_{iL} is in nF level, it shows high impedance of MΩ level for the 50 Hz current as well as its harmonic current. So, the transfer function $L(s)$ of EMI injection circuit with parasitic parameters can be expressed as (9) shown at the bottom of this page, where $\omega_{\mathrm{inj}} = 2\pi f_{\mathrm{inj}} = \frac{1}{R_{iL}C_{iL}}$ is the corner frequency of low-pass filter. According to the standard CISPR11 [45], f_{inj} should be 30 MHz to inject EMI noise below 30 MHz.

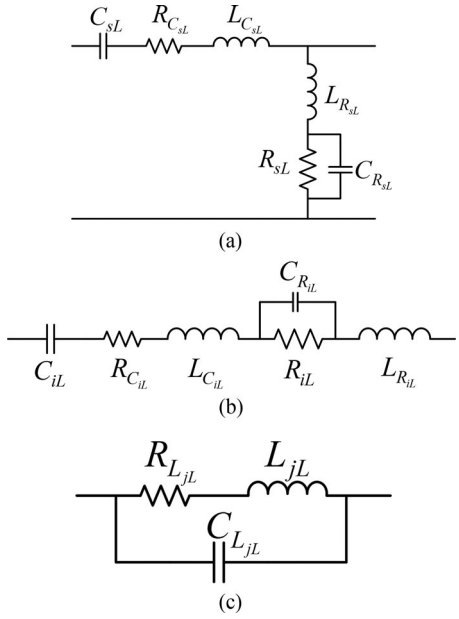

Fig. 4. High-frequency equivalent circuit model: (a) sensing circuit, (b) injection circuit, and (c) decoupling circuit.

The decoupling circuit is located between the injection point and sensing point, and single-turn inductor is used to be as decoupling component. Its high-frequency equivalent circuit model on *L* power line is shown in Fig. 4(c), where $R_{L_{jL}}$ and $C_{L_{jL}}$, respectively, are ESR and EPC of the inductor L_{jL}. The inductor L_{jL} mainly reduces the coupling between EMI sensing point and injection point. The transfer function $J(s)$ of decoupling circuit with parasitic parameters can be expressed as

$$J(s) = \frac{L_{jL}s + R_{L_{jL}}}{C_{L_{jL}}L_{jL}s^2 + R_{L_{jL}}C_{L_{jL}}s + 1}. \tag{10}$$

Therefore, by replacing $G_{\mathrm{AD}}(s), G_{\mathrm{DA}}(s), G_C(s), H(s), L(s)$, and $J(s)$ in (1) by (3), (6), (7), (8), (9), and (10), respectively, the transfer function $G_{\mathrm{DAEF}}(s)$ of embedded DAEF precise model

$$H(s) = \frac{L_{R_{\mathrm{sL}}}C_{R_{\mathrm{sL}}}s^3 + \frac{L_{R_{\mathrm{sL}}}}{R_{\mathrm{sL}}}s^2 + s}{(L_{C_{\mathrm{sL}}}C_{R_{\mathrm{sL}}} + L_{R_{\mathrm{sL}}}C_{R_{\mathrm{sL}}})s^3 + \left(R_{C_{\mathrm{sL}}}C_{R_{\mathrm{sL}}} + \frac{L_{C_{\mathrm{sL}}}+L_{R_{SL}}}{R_{\mathrm{sL}}}\right)s^2 + \left(\frac{C_{R_{\mathrm{sL}}}}{C_{\mathrm{sL}}} + \frac{R_{C_{\mathrm{sL}}}}{R_{\mathrm{sL}}} + 1\right)s + \omega_{\mathrm{sen}}} \tag{8}$$

$$L(s) = \frac{L_{C_{iL}}C_{R_{iL}}s^3 + \left(R_{C_{iL}}C_{R_{iL}} + \frac{L_{C_{iL}}}{R_{iL}}\right)s^2 + \left(\frac{C_{R_{iL}}}{C_{iL}} + \frac{R_{C_{iL}}}{R_{iL}}\right)s + \omega_{\mathrm{inj}}}{(L_{R_{iL}}C_{R_{iL}} + L_{C_{iL}}C_{R_{iL}})s^3 + \left(R_{C_{iL}}C_{R_{iL}} + \frac{L_{C_{iL}}}{R_{iL}} + \frac{L_{R_{iL}}}{R_{iL}}\right)s^2 + \left(\frac{C_{R_{iL}}}{C_{iL}} + \frac{R_{C_{iL}}}{R_{iL}} + 1\right)s + \omega_{\mathrm{inj}}} \tag{9}$$

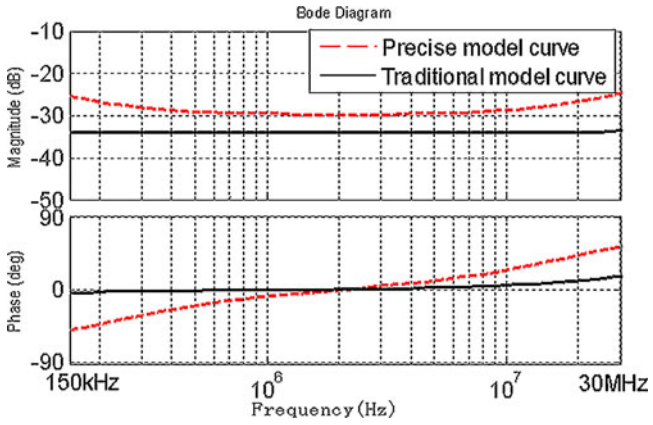

Fig. 5. Frequency-response curves of the closed-loop transfer function of DAEF precise model and traditional model.

with time delay, parasitic and nonlinear characteristics can be obtained.

The frequency-response curves of the closed-loop transfer function of DAEF precise model and traditional model without parasitic and delay characteristics are shown in Fig. 5, where $\omega_{\rm sen} = 2\pi f_{\rm sen} = 1/R_{\rm sL}C_{\rm sL} = 2\pi \times 150 \times 10^3$, the corner frequency of $L(s): \omega_{\rm inj} = 2\pi f_{\rm inj} = 1/R_{iL}C_{iL} = 2\pi \times 30 \times 10^6$. The L_{jL} of $J(s)$ is 0.63 μH. $K = 1$, $\tau_{\rm con} = 0.3$ ns, the sampling rate of ADC and DAC are all 1G SPS, the maximum of $T_{\rm sp}$ is 1 ns. $t_{{\rm DA}d} = 0.8$ ns, $t_{{\rm AD}d} = 1$ ns, $\tau_{\rm DA} = 0.2$ ns. The horizontal axis represents the frequency range (150 kHz to 30 MHz), and the vertical axis represents amplitude and phase of the closed-loop transfer function of the embedded DAEF. The whole curves show the changing of the amplitude and phase of the closed-loop transfer function of embedded DAEF with frequency. Meanwhile, these curves also reflect attenuation performance of the DAEF to EMI noise. For example, at the frequency point of 2 MHz, DAEF with precise model can reduce the EMI noise to 30 dB, but will not change the phase of the EMI noise. In Fig. 5, the traditional model curve shown by the black solid lines is based on the principle and equation presented in [35]. On the whole, Fig. 5 shows that the attenuation performance of DAEF precise model is lower than traditional model. This attenuation performance only reaches –30 dB in the middle-frequency band, and is far weaker in low-frequency and high-frequency band.

C. Data Conversion Resolution Design of DAEF

The attenuation performance of embedded DAEF control system is also directly affected by data conversion resolution of ADC and DAC. If the data conversion bits are not enough, although the EMI noise source fluctuates in unallowed range, the EMI injection signal output by DAC has no any change, and cannot cancel this unallowed fluctuation. It can reduce the attenuation precision of DAEF. So, in order to ensure that the minimum resolution of ADC sampling is better than the requested error of filtered EMI noise, the minimum bits of ADC sampling can be described as

$$k_{\min} = \mathrm{INT}\left[\log_2 \frac{V_{ad\_\max}}{\Delta V_{\rm EMI} \times H}\right] \tag{11}$$

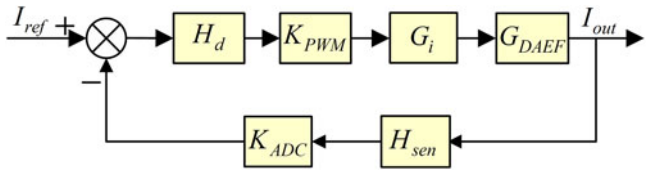

Fig. 6. Control system diagram of arc welding inverter with embedded DAEF.

where $V_{ad\_\max}$ is the allowed maximum input voltage of ADC; $\Delta V_{\rm EMI}$ is the requested error of filtered EMI noise; H is the sensing gain of filtered EMI noise, it actually is the ratio of reference voltage $V_{\rm ref}$ to the emission standard limits $V_{\rm sd}$ of conducted disturbance.

Based on the standard CISPR11 [45], the emission standard limits $V_{\rm sd}$ of conducted disturbance is selected as 46 dBμV. In order to ensure the reliable attenuation performance of DAEF system, one thousandth of $V_{\rm sd}$ is selected as $\Delta V_{\rm EMI}$, so, $\Delta V_{\rm EMI} = 0.001 \times 46$ dBμV $= 0.2$ μV. Thus, the value of the minimum bits of ADC sampling is computed by

$$k_{\min} = \mathrm{INT}\left[\log_2 \frac{V_{ad\_\max}}{\Delta V_{\rm EMI} \times H}\right] = 11 \tag{12}$$

where $V_{ad\_\max}$ is 3 V; $H = V_{\rm ref}/V_{\rm sd} = 2/46$ dBμV $= 10\,000$. So, in this paper, the bits of ADC and DAC should be selected 12.

D. Arc Welding Inverter System With Embedded DAEF

As shown in Fig. 1, the arc welding inverter system with embedded DAEF includes three major parts: main circuit for power conversion, DAEF control system for suppressing conducted EMI, and constant-current control system for ensuring welding performance. The signal flow direction of output constant-current control system is shown in Fig. 2. The output current signal $I_{\rm os}$ is sensed by hall sensor, and output voltage signal $V_{\rm os}$ is obtained by resistance divider. The controller samples $I_{\rm os}$ and $V_{\rm os}$ to make pulse width modulation (PWM) signal to control dc/dc full-bridge converter by constant-current algorithm. So, the control system diagram of the arc welding inverter with embedded DAEF is shown in Fig. 6.

In Fig. 6, $G_{\rm DAEF}(s)$ is the transfer function of embedded DAEF with time delay, parasitic and nonlinear characteristics described in Section B. $G_i(s)$ is the transfer function of dc/dc converter with full-bridge inverter and full-wave rectification using current-controlled mode, and it can be derived as

$$G_i(s) = \frac{V_D}{n} \frac{1}{C_f L_f R_L s^2 + L_f s + R_L} \tag{13}$$

where V_D is the front-end rectifier voltage, n is transformer ratio. C_f and L_f, respectively, are the filtering capacitor and filtering inductor of rear-end rectifier. R_L is the equivalent resistance of load.

$H_d(s)$ is transfer function of time delay in arc welding inverter control system. It can be expressed as

$$H_d(s) = e^{-\tau_d s} \tag{14}$$

where τ_d is delay time constant of the arc welding inverter control system.

$K_{\mathrm{ADC}}(s)$ is transfer function of ADC of arc welding inverter. And its transfer function can be expressed as

$$K_{\mathrm{ADC}}(s) = \frac{2^m}{V_{\mathrm{ref\_ADC}}} \times e^{-\tau_{\mathrm{ADC}} s} \tag{15}$$

where $V_{\mathrm{ref\_ADC}}$ is reference voltage of A/D converter of current sampling, m is the bit of A/D converter, and τ_{ADC} is delay time constant of the A/D converter.

K_{PWM} is the gain of PWM control. And it can be expressed as

$$K_{\mathrm{PWM}} = \frac{2^p}{T_{\mathrm{sw}}} \tag{16}$$

where T_{sw} is switching period of the switching tube, and p is the bit of counter register.

$H_{\mathrm{sen}}(s)$ is the transfer function of current sensor, and consists of sensor gain K_{sen} and a first-order *RC* filter. It can be expressed as

$$H_{\mathrm{sen}}(s) = \frac{K_{\mathrm{sen}}}{1 + \tau_{\mathrm{RC}} s} \tag{17}$$

where sensor gain K_{sen} can be determined by turns ratio and second site resistance, and τ_{RC} is time constant of *RC* filter.

So, the open-loop transfer function of discrete control model of arc welding inverter power supply system with DAEF can be expressed as

$$T_{\mathrm{uncom\_op\_}i} = H_d \cdot K_{\mathrm{PWM}} \cdot G_i \cdot G_{\mathrm{DAEF}} \cdot H_{\mathrm{sen}} \cdot K_{\mathrm{ADC}}. \tag{18}$$

III. Delay Effect Analysis of Embedded DAEF Controller

For further analyzing delay time effect on filtering performance, using MATLAB software, with different delay time, DAEF system frequency-response curves can be obtained by simulation. DAEF compensator selects inverse proportional controller of –100. The total delay time of DAEF is set in accordance with different type ADC and DAC with 12 bits resolution. The case of 0 ns represents the ideal case in which the ADC and DAC have no delay time.

In condition with different delay time, the frequency-response curves of the closed-loop transfer function of DAEF system can be shown in Fig. 7(a). In this simulation, the corner frequency of the transfer function $H(s)$ of EMI sensing circuit: $\omega_{\mathrm{sen}} = 2\pi f_{\mathrm{sen}} = 1/R_{\mathrm{sL}}C_{\mathrm{sL}} = 2\pi \times 150 \times 10^3$, the corner frequency of $L(s)$: $\omega_{\mathrm{inj}} = 2\pi f_{\mathrm{inj}} = 1/R_{iL}C_{iL} = 2\pi \times 30 \times 10^6$. The L_{jL} of $J(s)$ is 0.5 μH. $K = 200$, the sampling rate of ADC and DAC are all 1G SPS, the maximum of T_{sp} is 1 ns, $\tau_{\mathrm{DA}} = 0.2$ ns. The set delay time is a total value of t_{ADd}, t_{DAd}, and τ_{con}, and is 0, 0.5, 1.5, 2.5, 3.5, and 4 ns, respectively. The magnified detail chart is shown in Fig. 7(b).

As can be observed in Fig. 7, with the delay time increasing, the magnitude of DAEF frequency-response curves rises from −46 to −39 dB. So the attenuation ability of DAEF gradually decreases. There is no effect on phase in middle and low frequency. When delay time is less than 4 ns, in the frequency range of 150 kHz–30 MHz, DAEF system is stable. But when

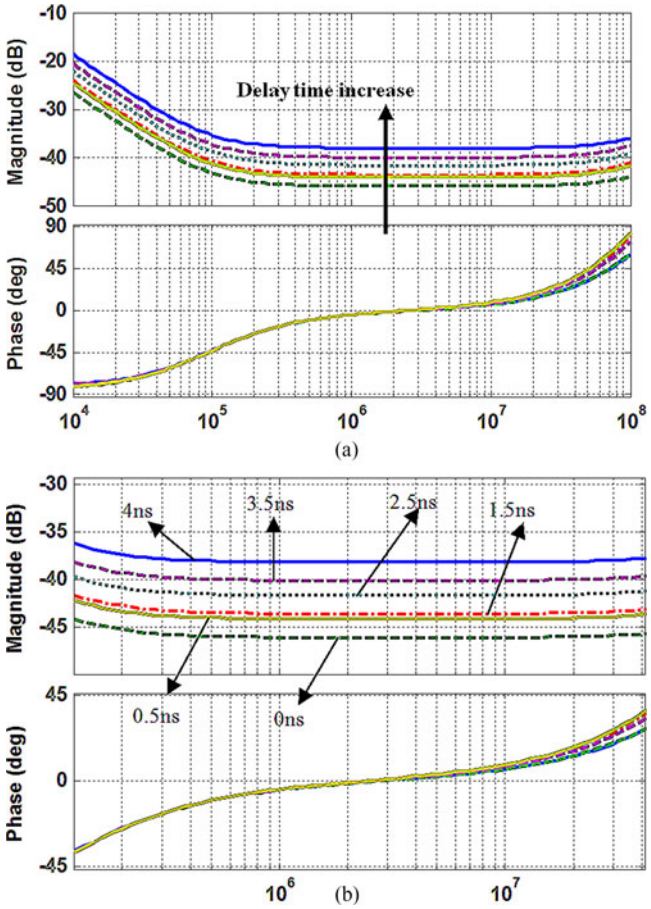

Fig. 7. Frequency-response curves of the closed-loop transfer function of DAEF with different delay time: (a) tendency chart and (b) detail chart.

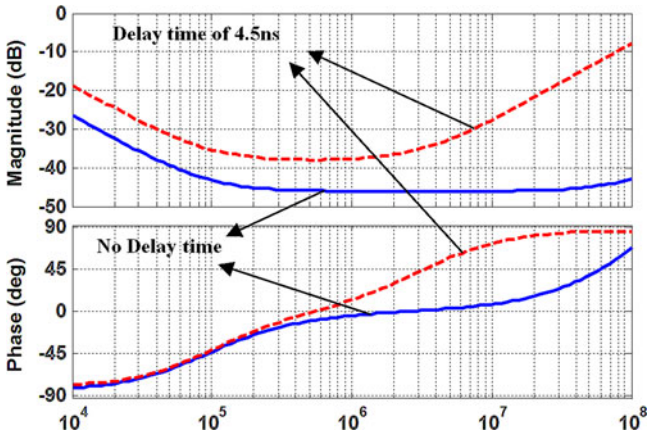

Fig. 8. Frequency-response curves of the closed-loop transfer function of DAEF with 0 and 4.5 ns delay time.

delay time is set to 4.5 ns, the attenuation ability of DAEF obviously declines, especially in middle- and high-frequency band, as shown in Fig. 8. In Fig. 8, the solid lines represent the ideal case without delay time; red-dotted lines represent the case with 4.5 ns delay time. So, with the delay time increasing, the filtering performance of DAEF gradually weakens. When delay time reaches at a certain value, the DAEF system tends to be unstable.

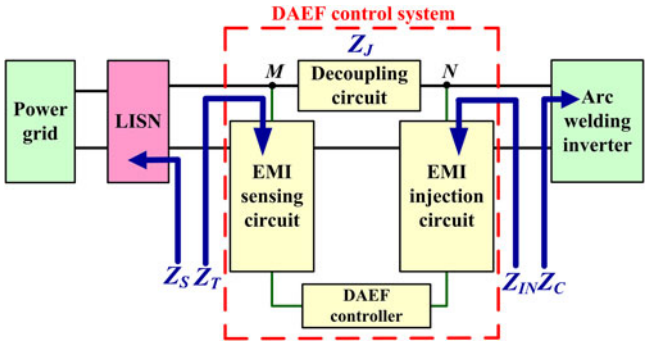

Fig. 9. Equivalent impedance diagram around decoupling circuit.

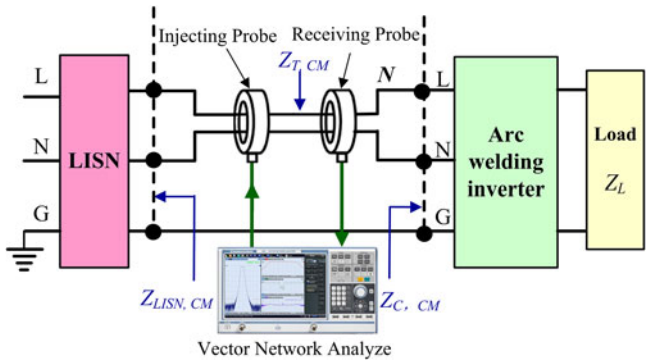

Fig. 10. Input impedance measurement setup circuit of arc welding inverter [42].

For the simulation and analysis of delay effect of DAEF, it not only helps to analyze system stability and attenuation ability of DAEF, but also helps to find the maximum total delay time. And then, the simulation also helps to allocate the delay time of every single processing stage in DAEF system.

For reducing or controlling the delay time in DAEF system, up to now, the most straightforward method is to raise the sampling rate of ADC and DAC. Moreover, another effective method is to increase the crystal oscillation frequency of the digital controller. As far as possible, DAEF uses FPGA controller, which programs with hardware description language and has parallel processing ability. Therefore, it can also increase system processing speed and decrease the delay time. In general, these methods are all based on the choice of hardware devices. It will inevitably increase the cost of DAEF to a great extent.

For compensating the delays of DAEF system in digital control way, a strategy can be considered. It is based on the periodicity of conducted EMI emission of arc welding inverter. On the one hand, at the time scale of sampling period, sampling and cancellation of EMI noise are implemented. On the other hand, at the time scale of switching period of power converters, the closed-loop compensation of conducted EMI is implemented. Thus, it will be implemented in different time scales. This strategy may be an effective measure to solve the bottleneck that the delays of DAEF affect the DAEF filtering effect.

IV. Design and Analysis of Decoupling Circuit

In order not to weaken the DAEF advantage in decreasing size and loss, the inductor of decoupling circuit cannot cascade to main power circuit of inverters. So, the single-turn inductor is the best choice as a decoupling inductor. The design of decoupling inductor is based on decoupling mechanism analysis. Hence, design of impedance, design of core formula, and determination of core size are three key issues.

A. Decoupling Mechanism Analysis

The decoupling mechanism analysis is based on impedance matching principle. The equivalent impedances around decoupling circuit all need to be analyzed and obtained. The equivalent impedance diagram around decoupling circuit in the arc welding inverter system with DAEF is shown in Fig. 9.

As seen in Fig. 9, Z_J is the equivalent impedance of decoupling circuit; Z_S is the equivalent impedance viewed from sensing point M to power grid to ground. Because of the existence of LISN, Z_S is approximately equal to 50 Ω. Z_T is the equivalent impedance viewed from sensing point M to EMI sensing circuit of DAEF to ground. In the high-frequency range, Z_T is approximately equal to the impedance of resistance R_{sL} (R_{sN}). $Z_{\rm IN}$ is the equivalent impedance viewed from injection point N to EMI injection circuit of DAEF to ground. In the high-frequency range, $Z_{\rm IN}$ is approximately equal to the impedance of resistance R_{iL} (R_{iN}). Z_C is the equivalent impedance viewed from injection point N to arc welding inverter.

According to the principle of impedance matching, the equivalent impedance Z_J of decoupling circuit should present high impedance for arc welding inverter and EMI injection circuit in the whole frequency range. So Z_J should satisfy (19). Similarly, the equivalent impedance Z_S should present high impedance for decoupling circuit and EMI sensing circuit in the whole frequency range. So Z_J should also satisfy (20)

$$Z_J >> Z_C//Z_{\rm IN} = \frac{Z_C \cdot Z_{\rm IN}}{Z_C + Z_{\rm IN}} \tag{19}$$

$$Z_S >> Z_J//Z_T = \frac{Z_J \cdot Z_T}{Z_J + Z_T}. \tag{20}$$

The impedance range expression (21) of Z_J can be derived from (19) and (20)

$$\frac{Z_C \cdot Z_{\rm IN}}{Z_C + Z_{\rm IN}} << Z_J << \frac{Z_S \cdot Z_T}{Z_T - Z_S}. \tag{21}$$

B. Impedance Design of Decoupling Inductor

A simple circuit model about measurement of input impedance curve of arc welding inverter has been built, as shown in Fig. 10 [42]. It uses the two-probe approach. The two-probe approach to measure input impedance of arc welding inverter, consists of an injecting current probe, a receiving current probe, and a vector network analyzer [42]–[44]. Port 1 of the vector network analyzer generates an ac signal into the circuit through the injecting probe, and the resulting signal current in the circuit is measure at port 2 of the vector network analyzer through the receiving probe.

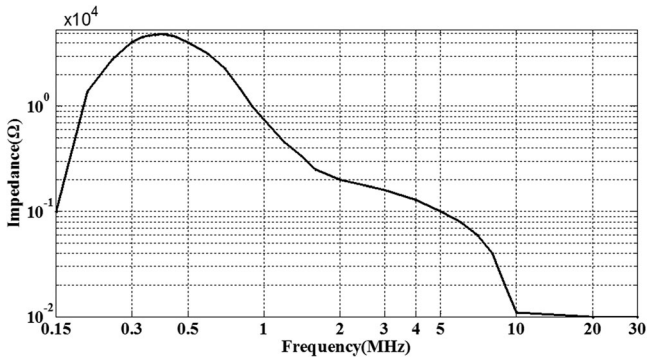

Fig. 11. Input impedance z_c curve of arc welding inverter.

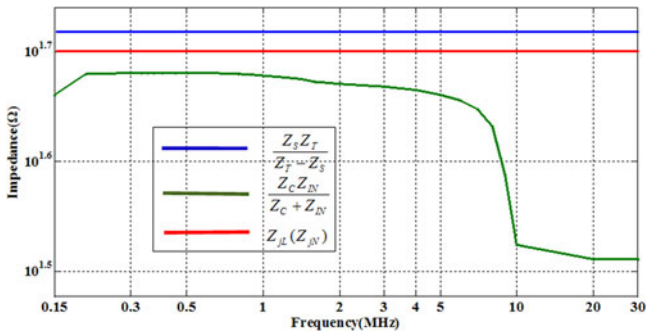

Fig. 12. Impedance curve range and resulting inductor's curve of decoupling inductor.

So, the impedance Z_C curve of arc welding inverter as interference source can be obtained. The Z_C curve views from the input port to load of arc welding inverter, as shown in Fig. 11.

The impedance Z_C of arc welding inverter is shown in Fig. 11, $Z_{\rm IN}$ is approximately equal to the impedance of resistance R_{iL} (R_{iN}). So the impedance curve of $\frac{Z_C \cdot Z_{\rm IN}}{Z_C + Z_{\rm IN}}$ can be obtained, and is shown in Fig. 12. Z_S is approximately equal to 50 Ω, and Z_T is approximately equal to the impedance of resistance $R_{\rm sL}$ (R_{sN}). So the impedance curve of $\frac{Z_S \cdot Z_T}{Z_T - Z_S}$ can be obtained, and is also shown in Fig. 12.

As seen in Fig. 12, and also according to (21), the impedance curve range of decoupling inductor should be in between the $\frac{Z_S \cdot Z_T}{Z_T - Z_S}$ curve and $\frac{Z_C \cdot Z_{IN}}{Z_C + Z_{IN}}$ curve. Based on the impedance curve range of decoupling inductor shown in Fig. 12, it can be determined that the impedance curve of decoupling inductor is set to 50 Ω in the whole frequency range, as shown by red line, i.e., $Z_{jL}(Z_{jN}) = 50\ \Omega$.

C. Core Formula Design of Decoupling Inductor

Due to better performance of Ni-Zn ferrite for suppressing EMI in the high-frequency range, so, in this paper, the Ni-Zn ferrite is selected as the core material of decoupling inductor. The Ni-Zn ferrite core can be operated at the frequency range of 100 kHz–140 MHz, based on the formula of NiO and ZnO.

There is a direct relationship between the formula ratio of Fe_2O_3: NiO: ZnO and the operating upper cutoff frequency of Ni-Zn ferrite core, as well as relative permeability μ_r. The common relationship list between formula ratios of Fe_2O_3: NiO: ZnO and upper cutoff frequency is shown in Table I.

TABLE I
RELATIONSHIP BETWEEN NI-ZN FERRITE FORMULA AND RELATIVE PERMEABILITY, CUTOFF FREQUENCY

Fe_2O_3 : NiO : ZnO	μ_r	Cutoff frequency/MHz
50.3:17.5:33.2	320	10
50.2:24.9:24.9	150	30
50.8:31.7:16.5	85	75
51.6:39.0:9.4	44	140

In the standard CISPR11 [45], the frequency range of conducted EMI test standard is 150 kHz–30 MHz, so the Ni-Zn ferrite core formula with upper cutoff frequency 30 MHz should be selected, i.e., the core formula with Fe_2O_3: NiO: ZnO = 50.2:24.9:24.9 is determined. Referring to Table I, the relative permeability μ_r of determined Ni-Zn ferrite core is set to 150.

D. Core Size Determination of Decoupling Inductor

The relationship between decoupling inductance value $L_{jL}(L_{jN})$ and its size parameters such as cross-sectional area A_C, and core length h can be described as

$$L_{jL}(L_{jN}) = \frac{\mu A_C}{h} \tag{22}$$

where μ is the permeability of decoupling inductance core. Because $\mu_r = 150$, $\mu = \mu_r \cdot \mu_0 = 150 \times 4\pi \times 10^{-7} = 1.88 \times 10^{-4}$.

The cross-sectional area A_C of decoupling inductor can be expressed as

$$A_C = \frac{h}{2} \times (D - d). \tag{23}$$

By substituting (23) into (22), $L_{jL}(L_{jN})$ can be derived as

$$L_{jL}(L_{jN}) = \frac{\mu}{2}(D - d). \tag{24}$$

According to the standard IEC 62317-12 [46], the ratio of outside diameter and inside diameter of ring cores is $D/d = 1.67$, and The ratio of length and inside diameter of ring cores is $h/d = 0.67$.

On the other hand, $L_{jL}(L_{jN})$ also can be expressed as

$$L_{jL}(L_{jN}) = \frac{Z_{jL}(Z_{jN})}{2\pi f_{\rm cen}} \tag{25}$$

where $Z_{jL}(Z_{jN})$ is the equivalent impedance of decoupling inductor on *L* line (*N* line), is set to 50 Ω in the whole frequency range in Section C, as shown in Fig. 12; $f_{\rm cen}$ is the center frequency of filtering frequency range, and it takes 1 5 MHz.

According to (24) and (25), the core size parameters can be obtained: $D = 14.04$ mm, $h = 5.63$ mm, and $d = 8.41$ mm.

V. COMPENSATOR DESIGN

A. Control System Performance Analysis

As described in Section II, the open-loop transfer function of digital control model of arc welding inverter power supply system with DAEF can be expressed as (18). So, the

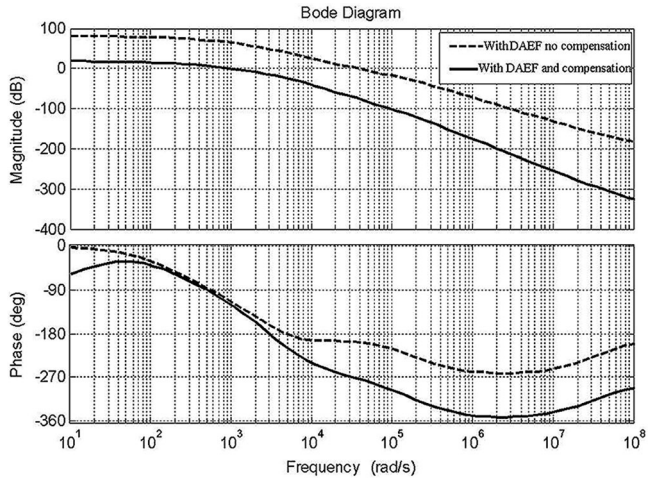

Fig. 13. Open-loop bode plots of arc welding inverter system with DAEF.

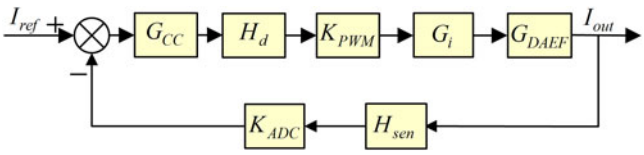

Fig. 14. Control system diagram of arc welding inverter with compensation controller.

open-loop bode plot of arc welding inverter under the uncompensated condition can be shown in Fig. 13 by dotted lines.

As can be observed in Fig. 13, magnitude margin of the uncompensated system is –41.1 dB, phase margin is -16°, and the system is unstable, therefore a compensation controller needs to be designed for arc welding inverter system.

B. Compensator Design

This paper adopts a double-pole double-zero compensating network to compensate arc welding inverter system, and its transfer function can be expressed as

$$G_{\mathrm{CC}}(s) = \frac{K_p(T_{\mathrm{z1}}s+1)(T_{z2}s+1)}{s(T_{p1}s+1)(T_{p2}s+1)} \tag{26}$$

where K_p is direct voltage gain. The double-pole double-zero compensating network can produce two zero points $-1/T_{z1}$ and $-1/T_{z2}$ in the left half of S plane, and can produce two pole points $-1/T_{p1}$ and $-1/T_{p2}$.

The control diagram of arc welding power source control system after compensation is shown in Fig. 14.

So, the open-loop transfer function of arc welding inverter power supply system with compensator can be expressed as

$$T_{\mathrm{com\_op\_}i} = G_{\mathrm{CC}} \cdot H_d \cdot K_{\mathrm{PWM}} \cdot G_i \cdot G_{\mathrm{DAEF}} \cdot H_{\mathrm{sen}} \cdot K_{\mathrm{ADC}}. \tag{27}$$

The open-loop bode plot of the arc welding power system with compensator can be shown in Fig. 13 by the solid lines. As can be seen in Fig. 13, after compensation, magnitude margin of the system is 20.5 dB, phase margin is 64°, and the system is stable. Comparing with the bode plot of uncompensated system in Fig. 13, stability of the compensated system has been increased.

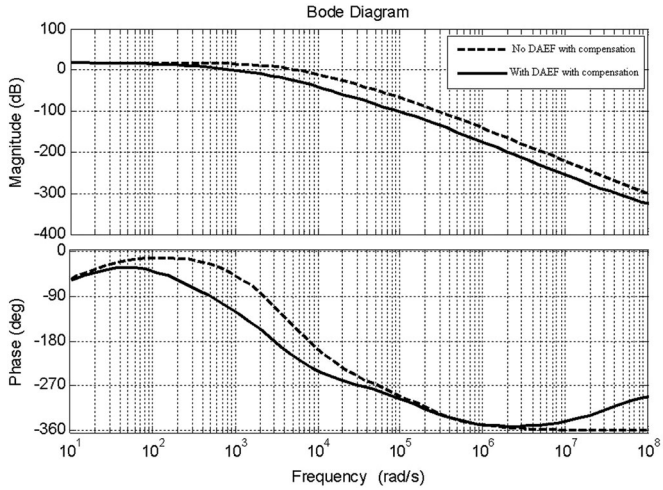

Fig. 15. Open-loop bode plots of arc welding inverter with and without DAEF.

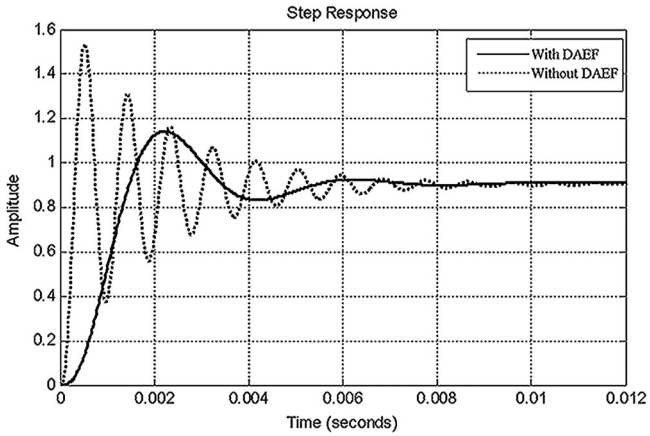

Fig. 16. Close-loop step response curves of arc welding inverter without DAEF and with DAEF.

Its magnitude margin has an improvement of 61.6 dB, and its phase margin has an improvement of 80°.

C. Control Performance Simulation Verify

DAEF control system not only controls the conducted EMI, but also affects the performance of power control system of arc welding inverters. The open-loop bode plots of arc welding power system without DAEF and with DAEF are shown in Fig. 15 by the dotted lines and the solid lines, respectively.

As can be seen in Fig. 15, the magnitude margin of the compensated arc welding system without DAEF is 7.3 dB, and its phase margin is 20°; the magnitude margin of the compensated arc welding system with DAEF is 20.5 dB, and its phase margin is 64°. So, comparing with the bode plot without DAEF in Fig. 15, stability of the system with DAEF has been increased. Its magnitude margin has an improvement of 13.2 dB, and its phase margin has an improvement of 44°. It shows that DAEF improves the arc welding system performance.

The closed-loop step response curves of the arc welding power system without DAEF and with DAEF are shown in Fig. 16 by the dotted lines and the solid lines, respectively.

TABLE II
PARAMETERS OF THE FABRICATED DAEF PROTOTYPE

Circuit	Symbol	Model and Parameters	Manufacturer
Sampling	ADC	ADS4229, 12bits, 250MSPS, 2 channels	Texas Instruments
	DAC	DAC5662A, 12bits, 275MSPS, 2 channels	Texas Instruments
Sensing	R_{sL}/C_{sL}	880 Ω/0.1 μF	ROHM
	R_{sN}/C_{sN}	880 Ω/0.1 μF	ROHM
Rejection	R_{iL}/C_{iL}	48 Ω/1 nF	ROHM
	R_{iN}/C_{iN}	48 Ω/1 nF	ROHM
Decoupling	L_{jL}/L_{jN}	0.63 μH	TDK

As can be seen in Fig. 16, the overshoot of arc welding inverter system without DAEF is 53.7%, while its overshoot with DAEF decreases to 14%. Comparing with arc welding inverter system without DAEF, its rising time with DAEF becomes longer, but its settling time with DAEF can be reduced slightly. This shows that dynamic performances of the system with DAEF have been improved as a whole.

From the above, it can be seen that adding DAEF control system in arc welding power supply system not only improves system stability, but also improves the dynamic performances.

VI. EXPERIMENTAL RESULTS

A. Experimental Platform Setup

In order to verify the accuracy of the proposed DAEF precise model and rationality of decoupling method, a 4 kW high-frequency arc welding inverter prototype has been fabricated with the following specifications:

1) input voltage: $U_{\text{in}} = 220$ V;
2) output power: $P_{\text{out}} = 4$ kW;
3) output voltage: $V_{\text{out}} = 20$ V;
4) output current: $I_{\text{out}} = 200$ A;
5) switching frequency: $f_{\text{sw}} = 20$ kHz.

The control system algorithm is implemented using the FPGA controller. The EMI control of DAEF and the constant-current control of arc welding inverter share the FPGA controller. Because the filtered EMI frequency reaches up to 30 MHz, a high-speed and high-precision ADC and DAC are needed to sample and convert the EMI signal. Meanwhile, the resistors and capacitors in DAEF are expected to be noninductance or smaller parasitic resistor and noninductance or smaller parasitic capacitor. The components are used to implement the DAEF control system are given in Table II.

The complete system test platform according to the standard CISPR 16-1-1 [47], CISPR 16-1-2 [48], and CISPR 16-2-1 [49], is depicted in Fig. 17. In this test platform, the LISN is R&S ENV216 to pick up the EMI signal from *L* line and *N* line; the EMI receiver is R&S ESL3. The standard CISPR11 [45] describes the applicable limits for measurement.

B. Filtering Effect Test

CM-conducted EMI voltage in arc welding inverter system is the average of the conducted EMI voltage on *L* line and *N* line. The first test was performed without any EMI filters in the arc welding inverter system. The resulting CM spectrum is shown by green curve in Fig. 18, in which the red straight line indicates CM-conducted EMI emission limits line in the standard CISPR11 [45], and there are quasi-peak limits line and average limits line. From Fig. 18, without EMI filter, an average peak of 48 dBμV can be seen, with the highest peak of 79 dBμV at around 0.98 MHz.

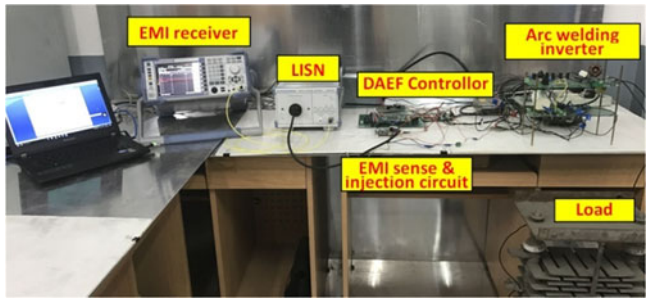

Fig. 17. Arrangement and apparatus of conducted EMI test platform.

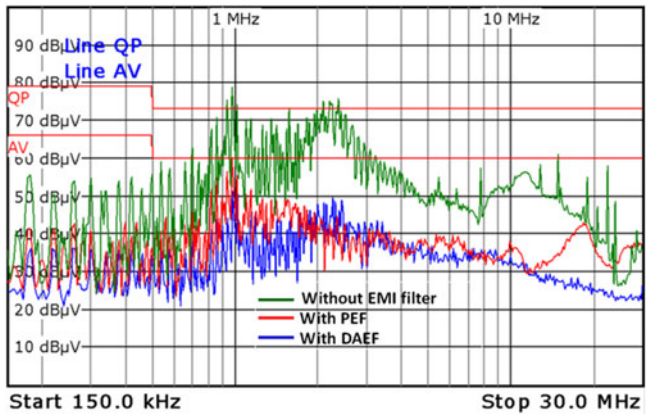

Fig. 18. CM-conducted EMI spectrum of arc welding inverter without EMI filter, with PEF, and with DAEF.

The second round of testing was conducted with PEF installed in the arc welding inverter system. The result is reflected by red curve in Fig. 18. So, with PEF, an average peak of 37 dBμV across the spectrum (150 kHz to 30 MHz) can be observed, with the highest peak of 59 dBμV at 0.98 MHz.

The last test was done with the proposed DAEF embedded in the arc welding inverter system. In this test, the decoupling circuit is designed using the proposed method described in Section IV. The resulting CM EMI spectrum is depicted by blue curve in Fig. 18. So, with PEF, an average peak of 33 dBμV across the spectrum (150 kHz to 30 MHz) is obtained with the highest peak of 51 dBμV at 0.99 MHz.

Fig. 18 shows that the CM-conducted EMI spectrum significantly exceeds the both standard limits of CISPR11 [45] when without any EMI filter. From Fig. 18, it can be seen that the PEF and DAEF both can greatly decrease the CM-conducted EMI spectrum generated by the arc welding inverter below the standard limits. And it can be obtained that the EMI filtering performance of DAEF is equal to or better than the one of traditional PEF, across the frequency range of 150 kHz to 30 MHz.

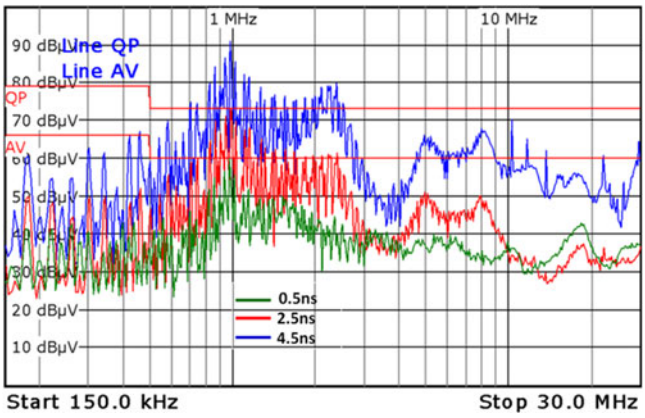

Fig. 19. CM-conducted EMI spectrum with 0.5 ns delay, 2.5 ns delay, and 4.5 ns delay.

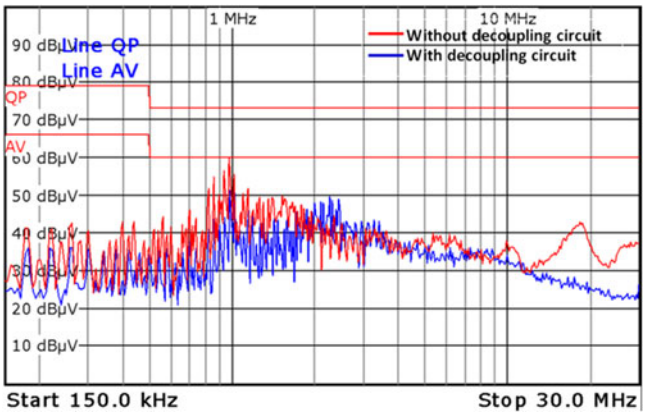

Fig. 20. CM-conducted EMI spectrum of arc welding inverter without decoupling circuit and with decoupling circuit.

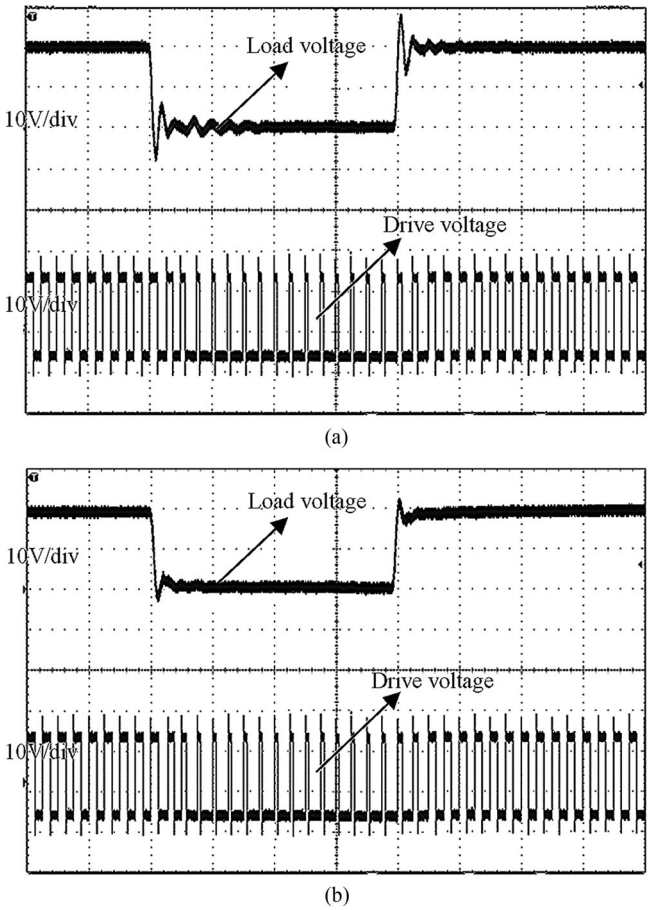

Fig. 21. Transient response curves of arc welding inverter system: (a) without DAEF and (b) with DAEF.

C. Delay Characteristics Test

For further verifying delay time effect on EMI filtering performance, the delay time is introduced in the proposed digital DAEF controller. The CM-conducted EMI spectrum with DAEF of 0.5 ns delay, 2.5 ns delay, and 4.5 ns delay is shown in Fig. 19.

As can be observed in Fig. 19, with the delay time increasing, the filtering performance weakens. When the delay time reaches to 2.5 ns, the CM-conducted EMI spectrum exceeds the standard average limits of CISPR11 [45], especially in middle-frequency band (0.8–1.5 MHz). When the delay time reaches to 4.5 ns, the CM-conducted EMI spectrum not only significantly exceeds the both standard limits of CISPR11 [45] across the frequency range of 150 kHz to 30 MHz, but also exceeds the EMI spectrum described by green curve in Fig. 18 without any EMI filter in individual frequency band, which shows the DAEF system has tended to be unstable.

D. Decoupling Method Test

For verifying the effect of decoupling circuit in DAEF on EMI filtering performance, one test was performed with DAEF, but without decoupling circuit. The resulting CM-conducted EMI spectrum is shown by red curve in Fig. 20. From the red curve, an average peak of 38 dBμV can be seen, with the highest peak of 59 dBμV at around 0.98 MHz. Another was performed with DAEF and with decoupling circuit. The resulting CM-conducted EMI spectrum is shown by blue curve in Fig. 20. By comparing red curve without decoupling circuit with blue curve with decoupling circuit, it can be obtained that decoupling circuit can improve the DAEF filtering performance.

E. System Dynamic Performance Test

The dynamic performance of the arc welding inverter system can be revealed by the step response on the load. Fig. 21(a) and (b) shows the system transient responses to a step load change without DAEF and with DAEF, respectively. The load changes first from 75% to 50%, then from 50% to 75%.

As can be seen in Fig. 21, when with DAEF, the dynamic performance of the arc welding inverter system can be improved, the overshoot of the system decreases from 46% to 14%, and the settling time is also reduced.

VII. Conclusion

In this paper, an improved digital active filtering method has been demonstrated as being a valid EMI suppression technique for arc welding inverters. Meanwhile, this paper builds an embedded DAEF precise model, which considers both

the time delay of digital processing portion and the parasitic parameters of passive components. Based on impedance matching principle, decoupling mechanism between sensing point and injection point has been explored. And a detailed and scientific design method of decoupling circuit has been put forward. The designed decoupling circuit is implemented by a single-turn inductor which does not cascade in power circuit. Moreover, a digital control system of arc welding inverters embedded a DAEF controller and its compensator both have been designed. And the control system stability and dynamic performance of arc welding inverter has been analyzed. Finally, experimental results show that the proposed embedded DAEF precise model can describe DAEF filtering behavior accurately. And the proposed design method of decoupling circuit can effectively improve filtering performance of DAEF. Both simulation and experimental results show that the embedded DAEF can improve system stability and dynamic performance.

The proposed improved digital active filtering method not only can selectively suppress the CM EMI and DM EMI, but also can effectively prevent interconversion between CM and DM interference. Compared with the traditional PEFs, the proposed DAEF has equal or better filtering performance. But more importantly, because the proposed design method of decoupling circuit has no component in series with the power circuit, the size and loss of DAEF can be reduced a lot.

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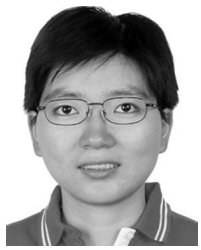

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