Critical Conduction Mode Boost PFC Converter With Fixed Switching Frequency Control

Kai Yao, *Member, IEEE*, Yi Wang, Jian Guo, and Kaili Chen

***Abstract*—Critical conduction mode (CRM) boost power factor (PF) correction converter features zero-current turn-on for the switch and no reverse recovery in diode, which is suitable for low-to-medium power applications. However, the switching frequency varies in a line cycle, and the wide variation range of the switching frequency is different under different input voltage and load conditions. This makes the conducted electromagnetic interference (EMI) spectra appearing great differences and complicates the design of EMI filter. In this paper, based on the expression of the switching frequency for traditional CRM control strategy, a variable on-time control strategy is proposed, and the implementation circuit is designed to realize a fixed switching frequency in a half-line cycle. The proposed strategy also achieves a lower output voltage ripple and a lower peak current for the power components. In spite of the PF decrease, the input current harmonic values are much lower than the IEC 61000-3-2 Class D limits. A 120 W prototype has been fabricated and tested in the laboratory and the experimental results are presented to verify the effectiveness of the proposed method.**

***Index Terms*—Critical conduction mode (CCM), fixed switching frequency control, power factor correction (PFC).**

I. Introduction

POWER factor correction (PFC) converters have been widely used in ac–dc power conversions to achieve a high power factor (PF) and a low total harmonic distortion (THD) [1]–[5]. A review of active PFC circuits found out that the boost converter is widely employed in commercial power supplies because of its continues input current, low cost and its high performance in terms of efficiency, power factor, and simplicity [6]–[10]. Depending on the inductor current to be continuous or not, there are three basic operating modes: continuous conduction mode (CCM), critical conduction mode (CRM), and discontinuous conduction mode (DCM) [11]–[15]. For high-power applications, a CCM boost PFC converter can achieve a theoretical unity PF and a low inductor current ripple, and the switch operates in hard-switching mode and the diode suffers reverse recovery [16]–[21]. For low-power applications, a boost PFC converter usually operates in DCM with zero-current switching (ZCS), no reverse recovery in diode, fixed switching frequency and simple control [22], [23]. However, the PF is not high, especially under a high input voltage, and the variable-duty-cycle control can increase the PF effectively [24], [25]. A CRM boost PFC converter has the advantages of switching zero-current turn-on, no reverse recovery in diode, relatively simple control circuit, and theoretical unity PF, and the converter is widely used in low- and medium-power conversion applications [26]–[35].

For a digital-controlled CRM boost PFC converter, the work in [26] proposes a family of predictive methods which include leading-edge, trailing-edge and triangular digital pulse width modulations. For the proposed control methods, the switching period retaining ZCS is predicted and the turn-on period is determined by the voltage controller, and there is no need for zero-current detection and high-frequency A/D converter. A technique of perturbation on-time and adaptive control of the minimum off time are put forward in [27] to improve the PF and efficiency. The research in [28] proposes an optimized total harmonic distortion improvement (THDI) technique with the line voltage recovery (LVR) over a wide line voltage range. The LVR detects the input line root-mean-square (RMS) voltage to generate the digital equivalent code for optimizing the THD by tuning the on-time value under different line voltages. In addition, the LVR and the THDI provide a feedforward path to reduce the ripple of the feedback voltage for further improving the THD.

With interleaved technology, the output power can be extended without sacrificing the advantages of a single converter, and also, the input and output current ripple as well as electromagnetic interference (EMI) filter can be reduced [29]–[31]. In [29], four open-loop interleaving methods for CRM boost PFC converters with a master–slave relationship are thoroughly analyzed. It is shown that the only open-loop method that results in stable operation is the synchronization of the slave converter to the turn-on instant of the master converter, where each converter operates with current-mode control. The effects of mismatched inductances, phase-shift error, switching-frequency limit, and valley switching on the input current ripple and input current distortion are also discussed in detail. The research conducted in [30] presents a novel open-loop synchronized-off voltage-mode master-made-modulated control scheme for a two-phase interleaved CRM boost PFC converter. An on-time tuning scheme of

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the slave converter is presented to stabilize the interleaved converter without using a phase-locked loop, or multiplier and current sensors. It can be implemented not only by an analog circuit, but also an alternative approach, which is calculated by a digital processor such as DSP. The work in [31] presents a two-phase interleaved CRM boost PFC converter with a variation-tolerant phase shifter (VTPS), which ensures accurate 180° phase shift between the two interleaved converters. A feedback loop similar to a phase-locked loop controls the amount of the phase shifting of the VTPS. The proposed VTPS has better immunity of process, supply, and temperature variations than the conventional phase shifter.

A totem-pole CRM boost bridgeless PFC rectifier with simple zero-current detection and full-range zero-voltage switching (ZVS) is proposed in [32]. Comparing with the boundary dual boost bridgeless rectifier, the required number of power components is reduced by one third and two current transducers can be eliminated. A new driver topology is introduced in [33] for the high-side switch in a synchronous CRM boost PFC converter to obtain full ZVS without additional control circuit to adjust the timing of the switches. The line current distortion is reduced through the use of on-time extension technique. The research in [34] presents the analysis and modeling of a single-phase multicell CRM PFC rectifier and discusses the implications on the design of an extremely thin converter with a targeted thickness of 1 mm. A single-stage CRM boost PFC converter for light-emitting diode (LED) applications using silicon carbide (SiC) is reported in [35].

In a CRM boost PFC converter, the switching frequency varies in a line cycle and the variation range is very large, especially under a high input voltage. The huge increase of the switching frequency results in greater turn-off loss of the switch. Furthermore, unlike the fixed switching frequency operation manner of a boost PFC converter in CCM or DCM, where the EMI noises just exist at the switching frequency and the multiples of switching frequency, and their maximum values normally happen under the low line and full load, the conducted EMI of a CRM boost PFC converter distributes in a wide frequency range, and finding the worst spectrum by repetitive measurements or interactive calculations under different input voltage and load conditions are time consuming [36]–[40]. Interestingly, there is a technique called frequency dithering which varies the switching frequency in a certain range, e.g., HR1200 from MPS. This can spread the noise energy over this range and reduce the peak values in the noise spectrum [41]–[50]. However, this method is normally applied for the converter with a fixed frequency control. Whether the variable switching frequency in a CRM PFC converter is beneficial in the same way could be a subject of a separate research. Many control ICs for the CRM PFC converter cannot achieve a very high switching frequency. For instances, L6561 and UCC28060 limit the switching frequency around the zero crossing point of the input voltage. Further, NCP1601A and NCP1601B can realize a mixed function of fixed switching frequency DCM and variable frequency CRM. However, the switching frequency is still variable during other parts of $[0, \pi]$, though the maximum value is limited around 0 and π of a line cycle.

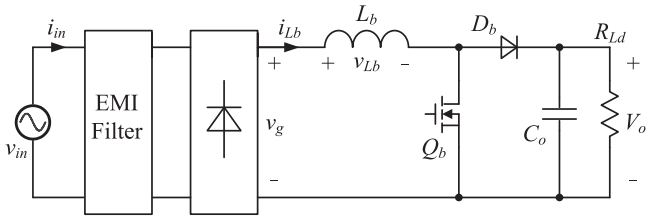

Fig. 1. Main circuit of a boost PFC converter.

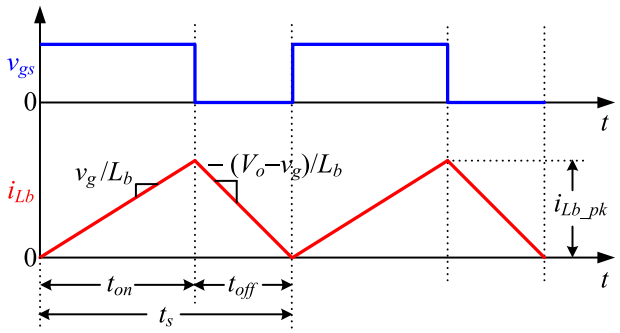

Fig. 2. Inductor current waveform in switching cycles.

Variable on-time (VOT) has been presented to improve the input current harmonics and PF of the CRM buck [51] and flyback PFC converter [52]. The objective of this paper is to propose a control scheme of fixed switching frequency during a line cycle for a CRM boost PFC converter. Section II analyzes the input current and the switching frequency of the converter in detail. In Section III, the variation law of the on time to achieve the fixed switching frequency is derived and the implementation control circuit is presented. In Section IV, the comparison between the proposed method and the traditional control is made in terms of the PF, input current harmonics, the peak and RMS current of the power components, and the output voltage ripple. A 120 W prototype has been built and tested, and the experimental results are presented in Section V.

II. Operating Principle of a CRM Boost PFC Converter

Fig. 1 shows the main circuit of a boost PFC converter. When the converter operates in CRM, the inductor current waveform in switching cycles is shown in Fig. 2. For traditional variable switching frequency control and the proposed fixed switching frequency control, the inductor current waveforms during a half-line cycle are plotted in Fig. 3(a) and (b), respectively.

The input voltage, the peak inductor current, and the average inductor current, as well as the input current, in a switching cycle are

$$v_{\rm in} = V_m \sin \omega t \tag{1}$$

$$i_{Lb\_\rm pk} = \frac{v_g}{L_b} t_{\rm on} = \frac{V_m \left|\sin \omega t\right|}{L_b} t_{\rm on} \tag{2}$$

$$v_{\rm in} = V_m \sin \omega t \tag{3}$$

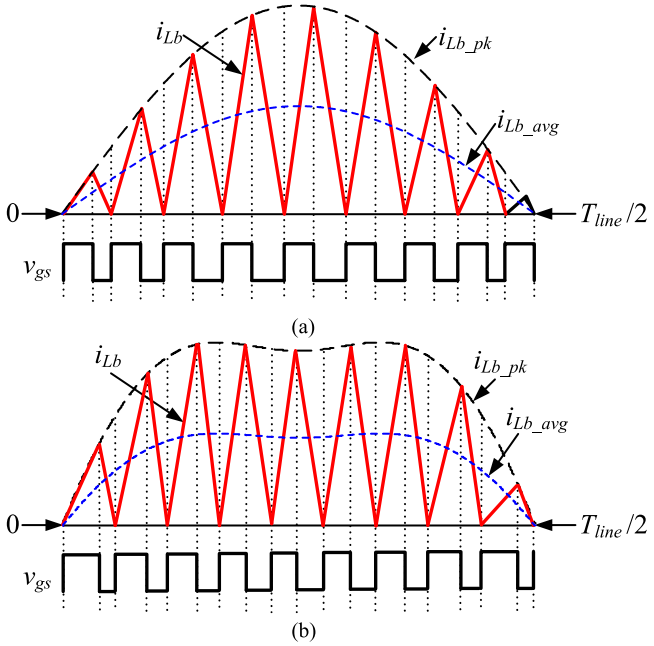

Fig. 3. Inductor current waveform in a half-line cycle: (a) COT control and (b) VOT control.

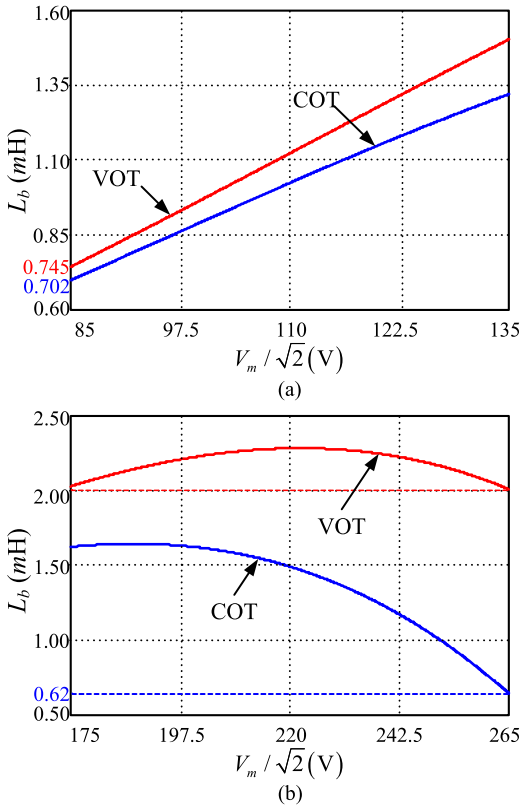

Fig. 4. Critical inductance over the input voltage range: (a) under 85–135 VAC and (b) under 175–265 VAC.

where V_m and ω are the amplitude and angular frequency of the input voltage, respectively, $t_{\rm on}$ is the on time of the switch, and L_b is the boost inductance.

Traditionally, $t_{\rm on}$ is constant in a half-line cycle, which is called constant on-time (COT) control. Assuming lossless operation yields the on-time

$$t_{\rm on} = \frac{4L_bP_o}{V_m^2}. \tag{4}$$

It can be clearly seen from (3) and (4) that the average input current waveform is sinusoidal and the PF is unity.

The switching frequency is formulated as

$$f_s = \frac{V_o - V_m\,|\sin\omega t|}{V_o}\cdot\frac{1}{t_{\rm on}} = \frac{V_m^2\,(V_o - V_m\,|\sin\omega t|)}{4L_bP_oV_o} \tag{5}$$

where V_o is the output voltage.

Equation (5) demonstrates that the switching frequency is variable in a half-line cycle. The minimum switching frequency occurs at the center of the half-line voltage period, while the maximum one emerges at the edges of the half-line voltage period, respectively, i.e.,

$$f_{s\_\max} = f_{s\_0} = \frac{V_m^2}{4L_bP_o} \tag{6a}$$

$$f_{s\_\min} = f_{s\_\pi/2} = \frac{V_m^2}{4L_bP_o}\left(1 - \frac{V_m}{V_o}\right). \tag{6b}$$

Selecting a minimum switching frequency, we can get the inductance from [6(b)]

$$L_b = \frac{V_m^2}{4f_{s\_\min}P_o}\left(1 - \frac{V_m}{V_o}\right). \tag{7}$$

Fig. 4 is plotted according to (7) and the specifications of the converter in Section VI, where 702 and 640 μH are obtained for COT under the input voltage of 85–135 VAC and 175–265 VAC, respectively. The switching frequency curves under the input voltages of 85, 110, 135, and 175 VAC, 220 VAC, 265 VAC in a half-line cycle at full load and 20% load are plotted in Fig. 5. At full load, the minimum and maximum switching frequency are about 30 and 43 kHz, 44 and 72 kHz, 57 and 108 kHz, 79 and 208 kHz, 73 and 328 kHz, and 30 and 476 kHz, under 85, 110, 135, 175, 220, and 265 VAC, respectively. At 20% load, the curves are the same while the values are five times of that at full load. Fig. 5 indicates that the switching frequency of the converter with COT has a big variation range.

III. Fixed Switching Frequency Control

A. Derivation of the VOT

It can be observed from (5) that if the on-time of the switch varies as (8), then the switching frequency during a half-line cycle is constant

$$t_{\rm on} = T_s\left(1 - \frac{V_m}{V_o}\,|\sin\omega t|\right) \tag{8}$$

where T_s is an undetermined coefficient which will be calculated afterward.

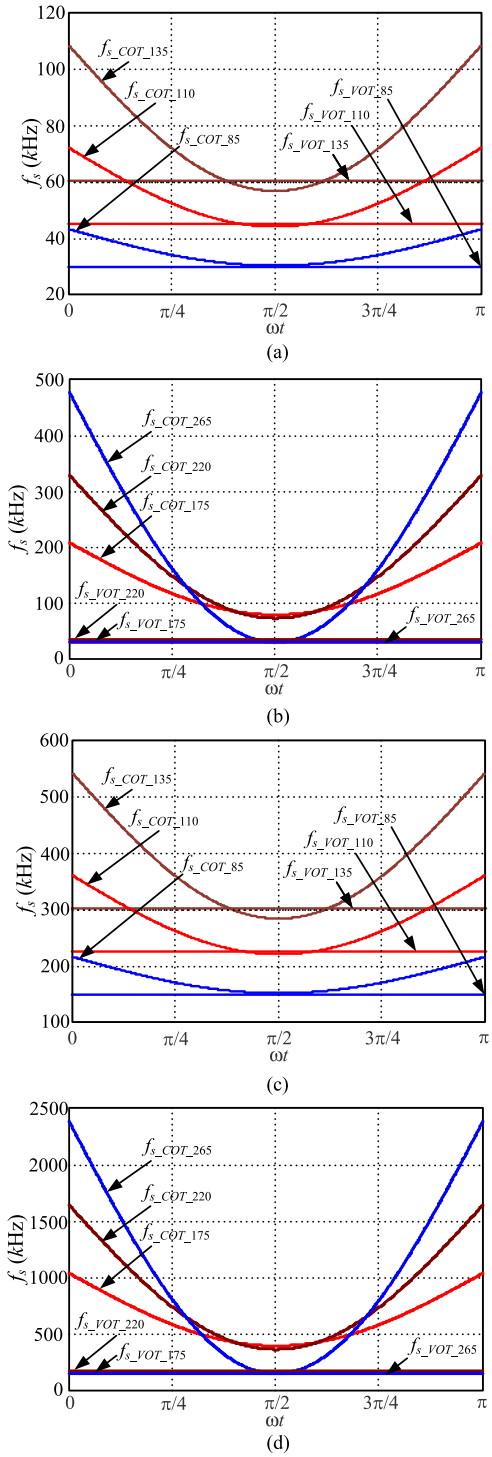

Fig. 5. Switching frequency over the input voltage range: (a) under 85–135 VAC and full load, (b) under 175–265 VAC and full load, (c) under 85–135 VAC and 20% load, and (d) under 175–265 VAC and 20% load.

Based on the power balance between the input and output, (9) can be obtained from (1), (3), and (8)

$$f_s = \frac{1}{T_s} = \frac{V_m^2\left[1/2 - (4V_m/3\pi V_o)\right]}{2P_o L_b}. \quad (9)$$

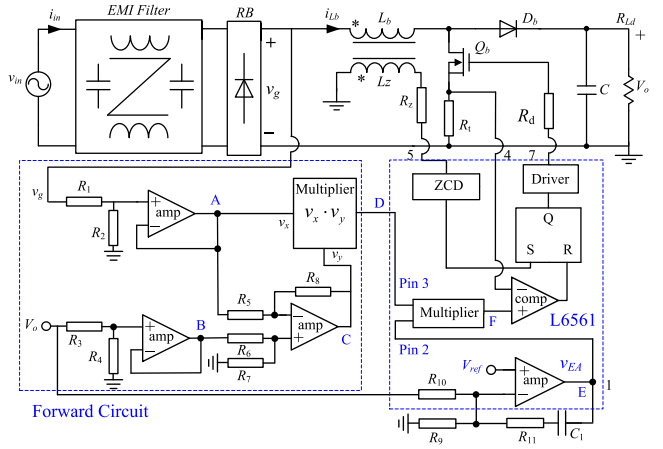

Fig. 6. Control circuit for CRM boost PFC converter with fixed switching frequency.

Substituting [9] into [8] yields

$$t_{\rm on} = \frac{2P_o L_b}{V_m^2\left[1/2 - (4V_m/3\pi V_o)\right]}\left(1 - \frac{V_m}{V_o}|\sin\omega t|\right). \quad (10)$$

The inductance of the converter with VOT can be easily obtained from (9) as

$$L_b = \frac{V_m^2\left[1/2 - (4V_m/3\pi V_o)\right]}{2P_o f_{s\_\min}}. \quad (11)$$

The curve of (11) is depicted in Fig. 4, where 745 and 2010 μH are obtained for VOT under the input voltage of 85–135 VAC and 175–265 VAC, respectively. The switching frequency of the converter with VOT under various input voltage and load conditions is drawn in Fig. 5. At full load, the switching frequency with VOT under the input voltages of 85, 110, 135, 175, 220, and 265 VAC are nearly 30, 45, 60, 30, 34, and 30 kHz, respectively. We can find that the switching frequency with VOT still changes with the input voltage; however, the variation range is greatly reduced, compared to that with COT. In addition, considering the fact that the converter usually operates under a nominal voltage, the influence of the input voltage change on the frequency is relatively small.

Under 110 VAC, the switching frequency with VOT is 45 and 225 kHz at 100% and 20% load, respectively. Under 220 VAC, the corresponding value is 34 and 170 kHz, respectively. However, the situation with COT is that when the load is changed between 100% and 20%, the minimum and maximum switching frequency is 44 and 360 kHz, 73 and 1640 kHz under 110 and 220 VAC, respectively. Therefore, though VOT cannot realize a constant switching frequency under the condition of a changing load, the variation range is significantly reduced, compared to that with COT.

B. Derivation of the VOT

The control circuit for VOT is illustrated in Fig. 6. Thae rectified input voltage is sensed by a voltage divider composed of R_1 and R_2, and $v_A = rV_m|\sin\omega t|$, where r is the voltage sensor gain. The output voltage is detected by R_3 and R_4, and $R_3/R_4 = R_1/R_2$, then $v_B = rV_o$. R_5, R_6, R_7, R_8,

and the amplifier construct the subtraction circuit. When $R_5 = R_6 = R_7 = R_8$, the output of the subtractor will be $v_C = r(V_o - V_m|\sin\omega t|)$. Multiplying v_A with v_C yields the product $v_D = r^2 V_m|\sin\omega t|\,(V_o - V_m|\sin\omega t|)$. The output voltage is regulated by an error amplifier, and the sensed output voltage across a voltage divider composed of R_9 and R_{10} is compared with the reference voltage $V_{\rm ref}$. Given the condition that $V_{\rm ref}$ is 2.5 V and the output voltage sensor gain is set as 2.5/400, i.e., $R_{10} = 159R_9$. R_{11} and C_1 form the compensation network, and $v_{\rm EA}$ and v_D are sent to the multiplier 2, then $v_F = v_{\rm EA}\, r^2 V_m|\sin\omega t|\,(V_o - V_m|\sin\omega t|)$. v_F and the sensed voltage of the switch peak current are connected to the comparator. The output of the comparator determines the turn-off and the ZCD signal controls the turn-on of the switch, respectively. Therefore, the on-time of the switch varies as expressed in (10).

IV. Performance Comparison

A. PF and Input Current Harmonics

Substituting (8) and (9) into (3), we can obtain

$$i_{\rm in} = \frac{P_o \sin\omega t\left(1 - \frac{V_m}{V_o}|\sin\omega t|\right)}{V_m\,[1/2 - (4V_m/3\pi V_o)]}. \tag{12}$$

Combining (1) with (12) yields the power factor with VOT

$$PF = \frac{P_{\rm in}}{\frac{1}{\sqrt{2}}V_m I_{\rm in\_rms}} = \frac{\frac{1}{\pi}\int_0^\pi v_{\rm in} i_{\rm in}\, d(\omega t)}{\frac{1}{\sqrt{2}}V_m\sqrt{\frac{1}{\pi}\int_0^\pi i_{\rm in}^2\, d(\omega t)}}$$

$$= \frac{\sqrt{\frac{2}{\pi}}\int_0^\pi \sin^2\omega t\left(1 - \frac{V_m}{V_o}|\sin\omega t|\right) d(\omega t)}{\sqrt{\int_0^\pi \left[\sin\omega t\left(1 - \frac{V_m}{V_o}|\sin\omega t|\right)\right]^2 d(\omega t)}}. \tag{13}$$

Fig. 7 depicts the curve, where the PF is 0.998, 0.995, 0.991, 0.976, 0.931, and 0.786 under 85, 110, 135, 175, 220, and 265 VAC, respectively, which are lower than unity. That is to say, the fixed switching frequency is achieved at the cost of PF, especially under a high input voltage. It should be noted here that the PF is only dependent on V_m/V_o. If V_o is 380 or 390 V instead of 400 V, the PF will be slightly lower than that in Fig. 7.

We apply the Fourier decomposition to (12) and the input current harmonics are acquired as follows:

$$I_n = \frac{1}{\pi}\int_0^{2\pi} \frac{P_o \sin\omega t\left(1 - \frac{V_m}{V_o}|\sin\omega t|\right)}{V_m\,[1/2 - (4V_m/3\pi V_o)]}\sin n\omega t d\omega t$$

$$= \begin{cases} \frac{2P_o}{V_m}\,(n=1) \\ \frac{8P_o}{(n^3-4n^2)\left(\pi V_o - \frac{4}{3}V_m\right)}\,(n=3,5,7\cdots). \end{cases} \tag{14}$$

The normalized amplitudes of the third, fifth, and seventh harmonics to the base of the fundamental component are formulated in [15(a)] and illustrated in Fig. 8, which reveals that the input current of the converter with VOT control mainly contains the third harmonic with an initial phase of 0. The ratio of the RMS values of the input current harmonics to the power is expressed in [15(b)] and exhibited in Fig. 9. According to IEC 61000-3-2

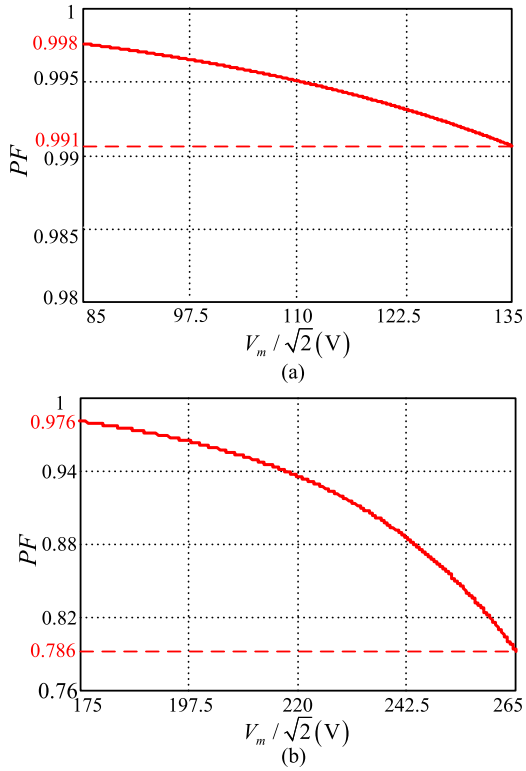

Fig. 7. PF of the converter with VOT: (a) under 85–135 VAC and (b) under 175–265 VAC.

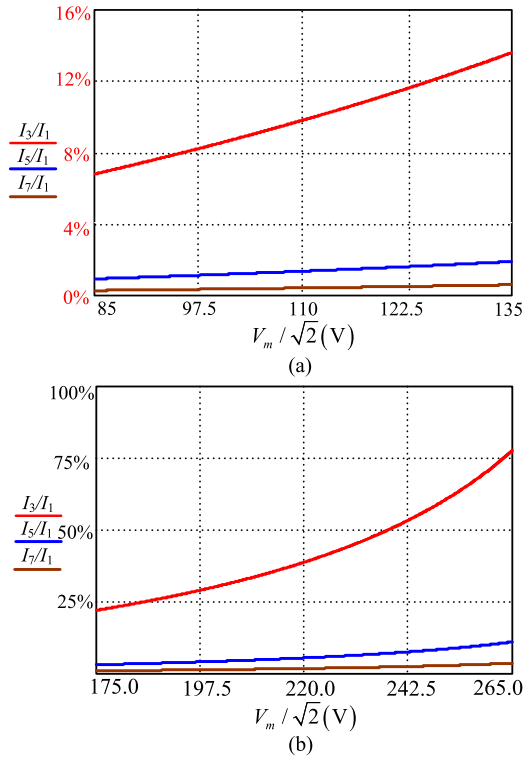

Fig. 8. Normalized amplitudes of the harmonics: (a) under 85–135 VAC and (b) under 175–265 VAC.

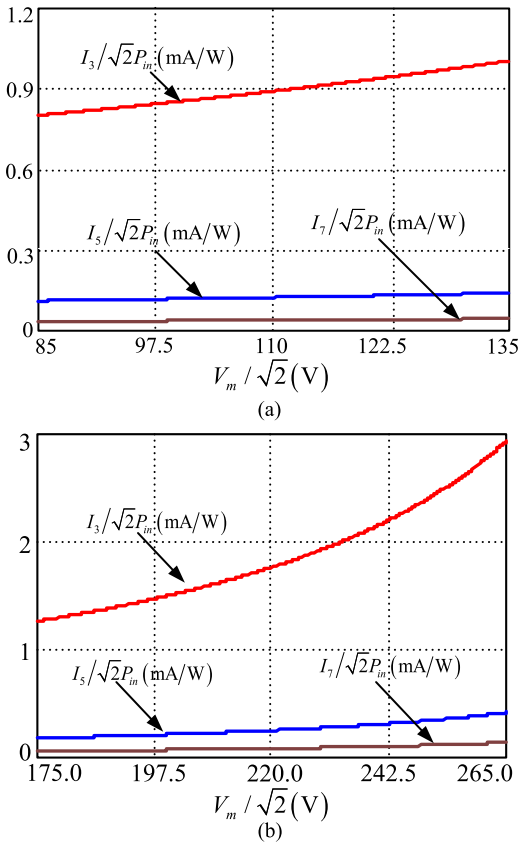

Fig. 9. Per watt content of the third, fifth, and seventh harmonics: (a) under 85–135 VAC and (b) under 175–265 VAC.

Class D, per watt contents of the third, fifth, and seventh harmonics should be less than 3.4, 1.9, and 1.0 mA/W, respectively. Obviously, the harmonics satisfy the standard requirements

$$\frac{I_n}{I_1} = \frac{1}{(n^3-4n^2)\left(\frac{\pi V_o}{4V_m}-\frac{1}{3}\right)}\ (n=3,5,7\cdots) \tag{15a}$$

$$\frac{I_n}{\sqrt{2}P_o} = \frac{\sqrt{2}}{(n^3-4n^2)\left(\frac{\pi V_o}{4}-\frac{V_m}{3}\right)}\ (n=3,5,7\cdots). \tag{15b}$$

B. Peak and RMS Current of the Inductor, Switch, and Diode

Using (2), (4), (8), and (9), we can get the inductor peak currents of the converter with COT and VOT, respectively, as

$$i_{Lb1\_\mathrm{pk}} = \frac{4P_o}{V_m}|\sin\omega t| \tag{16a}$$

$$i_{Lb2\_\mathrm{pk}} = \frac{2P_o\sin\omega t}{V_m\left[1/2-(4V_m/3\pi V_o)\right]}\left(1-\frac{V_m}{V_o}|\sin\omega t|\right). \tag{16b}$$

The peak current curves are shown in Fig. 10, which demonstrates that VOT achieves a lower value around $\pi/2$ and a higher value around 0 and π, compared to that with COT.

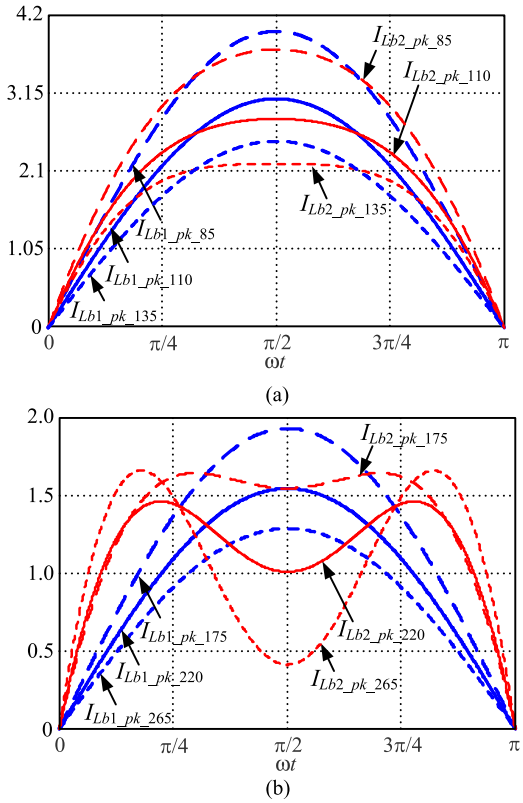

Fig. 10. Waveforms of the inductor peak current: (a) under 85–135 VAC and (b) under 175–265 VAC.

In a half-line cycle, the current's RMS value of the inductor, the switch and the diode are presented as follows:

$$I_{Lb1\_\mathrm{rms}} = \frac{2\sqrt{2}}{\sqrt{3}}\frac{P_o}{V_m} \tag{17a}$$

$$I_{Lb2\_\mathrm{rms}} = \frac{2P_o\sqrt{\int_0^\pi\left[\sin\omega t\left(1-\frac{V_m}{V_o}|\sin\omega t|\right)\right]^2 d\omega t}}{\sqrt{3}\pi V_m\left[1/2-(4V_m/3\pi V_o)\right]} = \frac{2P_o\sqrt{1/2-(8V_m/3\pi V_o)+3{V_m}^2/8{V_o}^2}}{\sqrt{3}V_m\left[1/2-(4V_m/3\pi V_o)\right]} \tag{17b}$$

$$I_{Qb1\_\mathrm{rms}} = \sqrt{\frac{16P_o^2}{3\pi V_m^2}\int_0^\pi(\sin\omega t)^2\left(1-\frac{V_m\sin\omega t}{V_o}\right)d\omega t} \tag{17c}$$

$$I_{Qb2\_\mathrm{rms}} = \sqrt{\frac{4P_o^2\int_0^\pi(\sin\omega t)^2\left(1-\frac{V_m|\sin\omega t|}{V_o}\right)^3 d\omega t}{3\pi V_m^2\left[1/2-(4V_m/3\pi V_o)\right]^2}} \tag{17d}$$

$$I_{Db1\_\mathrm{rms}} = \sqrt{\frac{16P_o^2}{3\pi V_o V_m}\int_0^\pi(\sin\omega t)^3 d\omega t} = \frac{8P_o}{3\sqrt{\pi V_o V_m}} \tag{17e}$$

$$I_{Db2\_\mathrm{rms}} = \sqrt{\frac{4P_o^2\int_0^\pi(\sin\omega t)^3\left(1-\frac{V_m|\sin\omega t|}{V_o}\right)^2 d\omega t}{3\pi V_o V_m\left[1/2-(4V_m/3\pi V_o)\right]^2}}. \tag{17f}$$

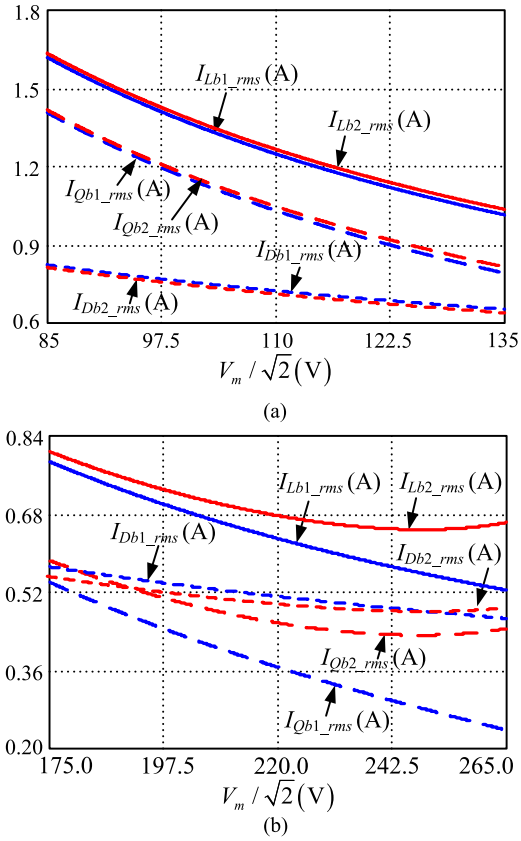

Fig. 11. RMS value of the current: (a) under 85–135 VAC and (b) under 175–265 VAC.

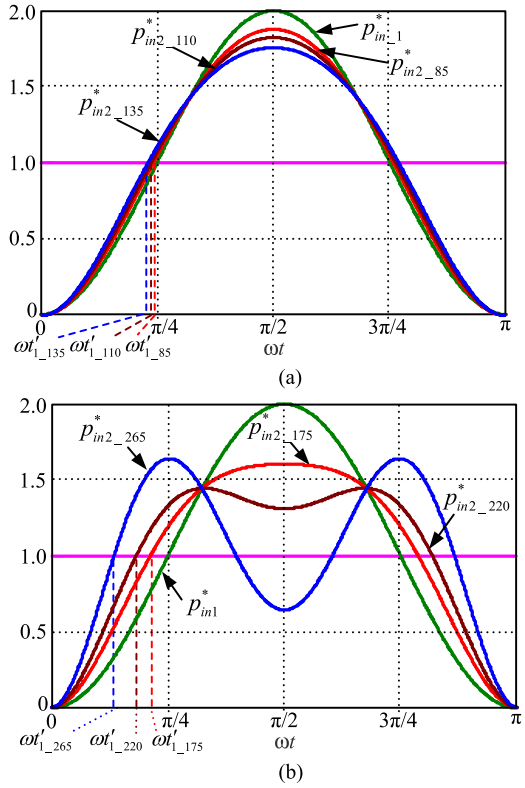

Fig. 12. Normalized instantaneous input power: (a) under 85–135 VAC and (b) under 175–265 VAC.

Based on (17), Fig. 11 is plotted, which indicates that VOT obtains nearly the same RMS value as that with COT, especially under a low input voltage.

The turns number N_b, the section area of the winding S, the air-gap δ, and the filling factor K_u of the inductor are calculated, respectively, as

$$N_b = \frac{L_b I_{Lb\_\mathrm{pk}\_\max}}{\Delta B A_e} \tag{18a}$$

$$S = \frac{I_{Lb\_\mathrm{rms}\_\max}}{J} \tag{18b}$$

$$\delta = \frac{\mu_0 N_b^2 A_e}{L_b} \tag{18c}$$

$$K_\mu = \frac{N_b S}{A_w} \tag{18d}$$

where $I_{Lb\_\mathrm{pk}\_\max}$ and $I_{Lb\_\mathrm{rms}\_\max}$ are the maximum peak and RMS value of the inductor current, respectively, ΔB is the flux density, A_e and A_w are the effective area and window area of the magnetic core, respectively, J is the current density, and μ_0 is the permeability.

Substitution of [18(a)] into [18(c)] leads to

$$\delta = \frac{\mu_0 L_b I^2_{Lb\_\mathrm{pk}\_\max}}{\Delta B^2 A_e}. \tag{19a}$$

Substituting [18(a)] and [18(b)] into [18(d)] yields

$$K_\mu = \frac{L_b I_{Lb\_\mathrm{pk}\_\max} I_{Lb\_\mathrm{rms}\_\max}}{\Delta B A_w A_e J}. \tag{19b}$$

Combining $L_{b1} = 702\ \mu$H, $I_{Lb1\_\mathrm{pk}\_\max} = 4.1$ A, $I_{Lb1\_\mathrm{rms}\_\max} = 1.63$ A and $L_{b2} = 745\ \mu$H, $I_{Lb2\_\mathrm{pk}\_\max} = 3.8$ A, $I_{Lb2\_\mathrm{rms}\_\max} = 0.89$ A with (19), δ and K_u with both of the control schemes can be calculated, respectively. The results show that K_u and δ with VOT are nearly the same as that with COT, which means that the inductor's core and size can remain basically the same, for despite increment in the inductance, the peak value of the inductor current is reduced.

C. Output Voltage Ripple

From (1), (3), (4), and (12), the normalized instantaneous input power with COT and VOT can be derived, respectively, as

$$p^*_{\mathrm{in}1} = \frac{v_{\mathrm{in}} i_{\mathrm{in}}}{P_o} = 2\sin^2 \omega t \tag{20a}$$

$$p^*_{\mathrm{in}2} = \frac{v_{\mathrm{in}} i_{\mathrm{in}}}{P_o} = \frac{\sin^2 \omega t}{1/2 - (4V_m/3\pi V_o)} \left(1 - \frac{V_m}{V_o} |\sin \omega t|\right). \tag{20b}$$

Fig. 12 can be plotted according to (18). When $p^*_{\mathrm{in}} > 1$, the output capacitor C_o is charged, and when $p^*_{\mathrm{in}} > 1$, C_o is discharged. t_1 and t'_1 are the time instants when $p^*_{\mathrm{in}\_1}$ and $p^*_{\mathrm{in}\_2}$ crosses 1 for the first time in a half-line cycle, respectively.

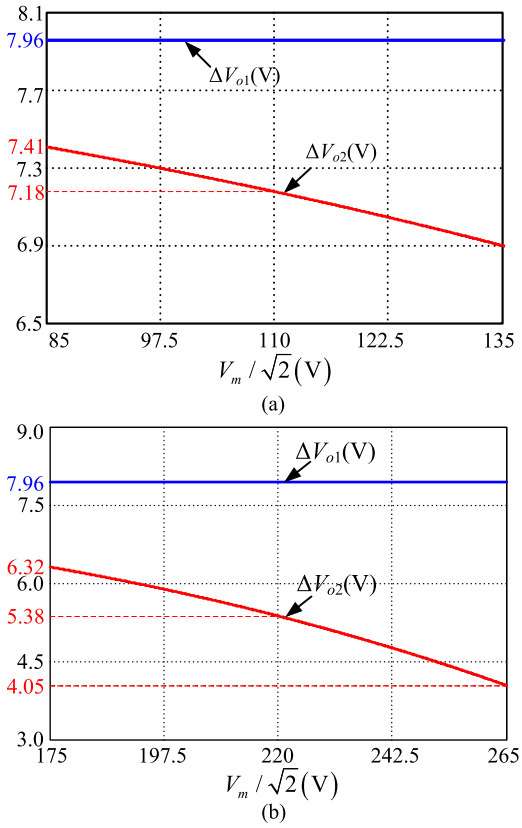

Fig. 13. Output voltage ripple: (a) under 85–135 VAC and (b) under 175–265 VAC.

By solving the equation of $p_{\text{in}}^* = 1$, we can obtain

$$\omega t_1 = \pi/4 \tag{21a}$$

$$\omega t_1' = \arcsin\left\{\left[1 + 2\sin\left(\frac{\pi}{6} - \frac{\theta}{3}\right)\right] \Big/ \left(\frac{3V_m}{V_o}\right)\right\} \tag{21b}$$

where $\theta = \arccos[\frac{27V_m^2}{V_o^2}(\frac{1}{4} - \frac{2V_m}{3\pi V_o}) - 1]$.

The output voltage ripple with COT and VOT can be calculated, respectively, as

$$\Delta V_{o1} = \left[2P_o \int_0^{\omega t_1} \left(1 - p_{\text{in}1}^*\right) d\omega t\right] \Big/ \left(\omega C_o V_o\right) \tag{22a}$$

$$\Delta V_{o2} = \left[2P_o \int_0^{\omega t'_1} \left(1 - p_{\text{in}2}^*\right) d\omega t\right] \Big/ \left(\omega C_o V_o\right). \tag{22b}$$

Fig. 13 is plotted according to (18)–(20) and the specifications of the converter. As seen, COT obtains a stable voltage ripple of 7.96 V, and VOT brings about a slightly lower value, which are 7.41, 7.18, 6.90, 6.32, 5.38, and 4.05 V under 85, 110, 135, 175, 220, and 265 VAC, respectively. In other words, if the maximum output voltage ripple is kept the same, the storage capacitance can be reduced, especially under a high input voltage. This may be in favor of the power density improvement, for electrolytic capacitors usually take up a considerable size and volume, especially in low-power applications.

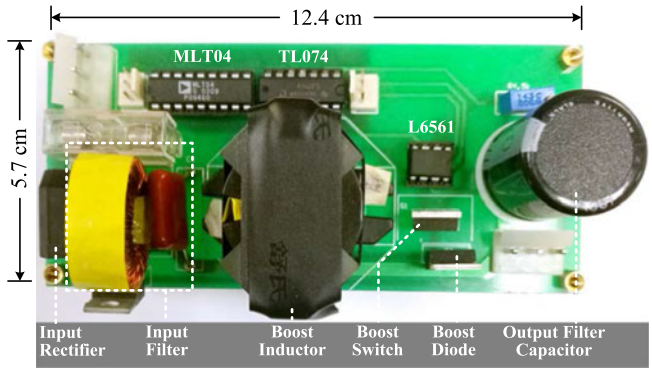

Fig. 14. Prototype photograph.

TABLE I
SPECIFICATIONS OF THE PROTOTYPE

Input voltage	Output voltage	Output current	Output power	Minimum switching frequency
$v_{\text{in}1}$ = 85-135 VAC/ 50 Hz $v_{\text{in}2}$ = 176-264 VAC/ 50 Hz	$V_o = 400$ VDC	0.3 A	$P_o = 120$ W	30 kHz

TABLE II
POWER COMPONENTS OF THE PROTOTYPE

Input rectifier bridge RB GBU406	Power switch Q_b FQPF5N60C	Boost diode D_b MUR460	Control IC L6561
Boost inductor low v_{in}: 702 μH (COT), 745 μH (VOT) High v_{in}: 640 μH (COT), 2010 μH (VOT)	Input filter inductor L_f = 850 μH	Input filter capacitor $C_f = 0.47$ μF	Output filter capacitor $C_o = 120$ μF

V. EXPERIMENTAL VERIFICATION

In order to verify the effectiveness of the theoretical analysis, a prototype has been built and tested in the lab, as shown in Fig. 14, where the power stage takes up a large part of the size. We should confess that it is unsophisticated. As can be seen from Fig. 6, only one additional multiplier is needed; however, MLT04 is adopted in the prototype, which contains four multipliers. In addition, three additional amplifiers are drawn in Fig. 6, and two of them are used only as a voltage follower, which are not necessarily required, for the input impedance of MLT04 is very high. Therefore, some of the increments in the components and size of the prototype shown in Fig. 14 are not necessary. Actually, if the proposed control is implemented in a digital way and well designed, the multiplier and some other additional components can be saved, for software can handle most of the issues. In consequence, the impact on the power density can be lowered. Moreover, if the on-chip technology and craft is adopted, the influence will be further reduced. The specifications and power components are listed in Tables I and II.

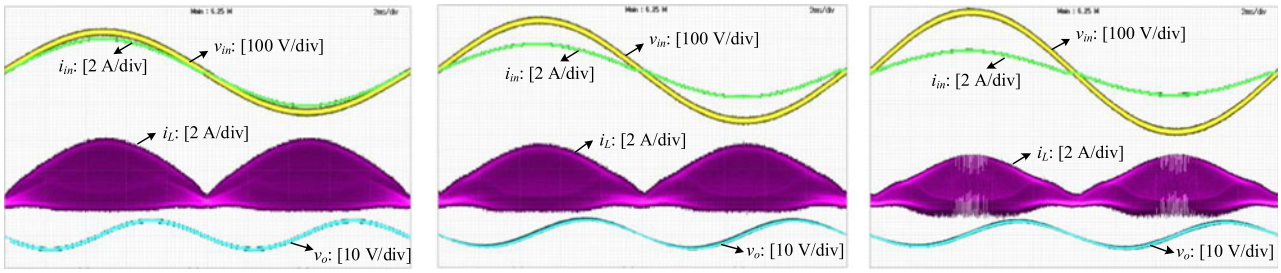

Fig. 15. Experimental waveforms with COT: (a) under 85 VAC, (b) under 110 VAC, and (c) under 135 VAC.

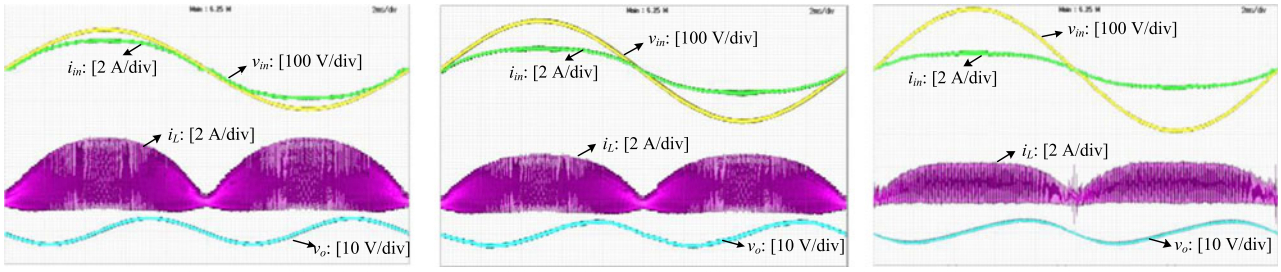

Fig. 16. Experimental waveforms with VOT: (a) under 85 VAC, (b) under 110 VAC, and (c) under 135 VAC.

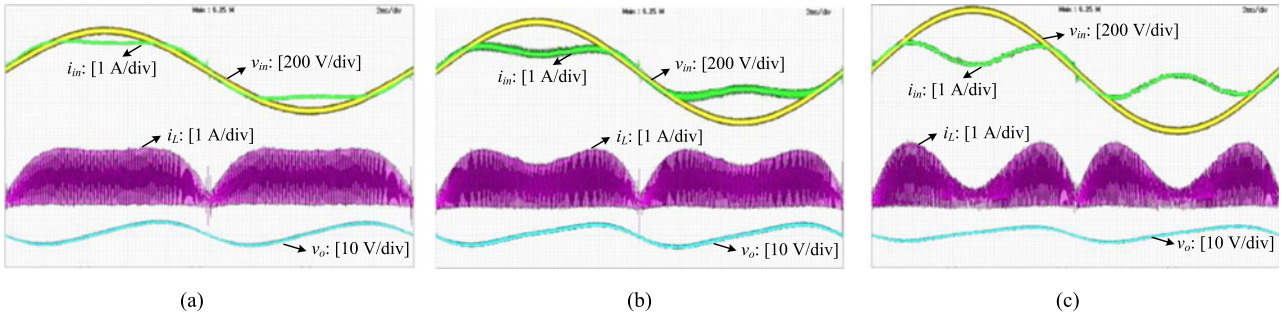

Fig. 17. Experimental waveforms with VOT: (a) under 175 VAC, (b) under 220 VAC, and (c) under 265 VAC.

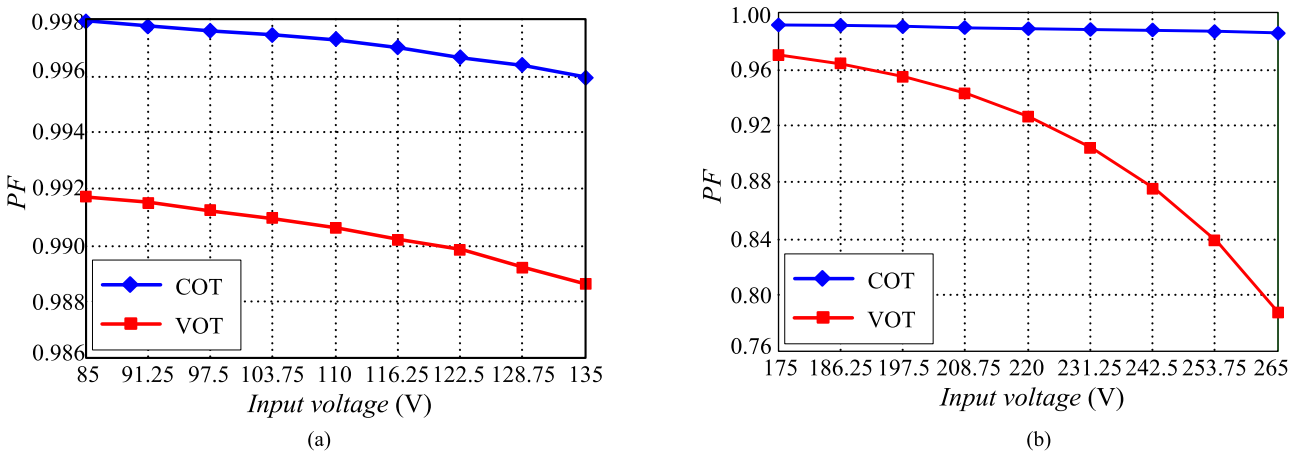

Fig. 18. Measured PF: (a) under 85–135 VAC and (b) under 175–265 VAC.

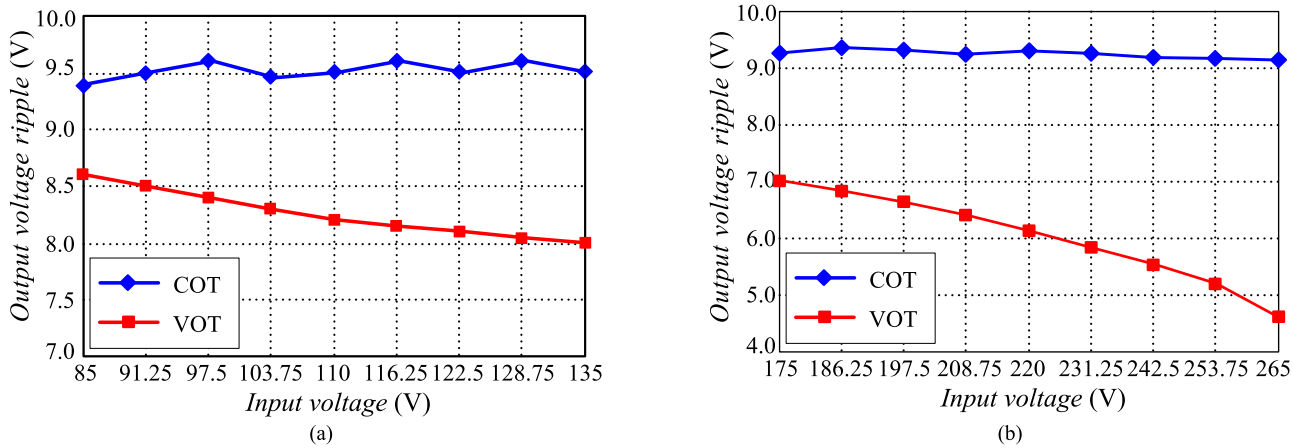

Fig. 19. Measured output voltage ripple: (a) under 85–135 VAC and (b) under 175–265 VAC.

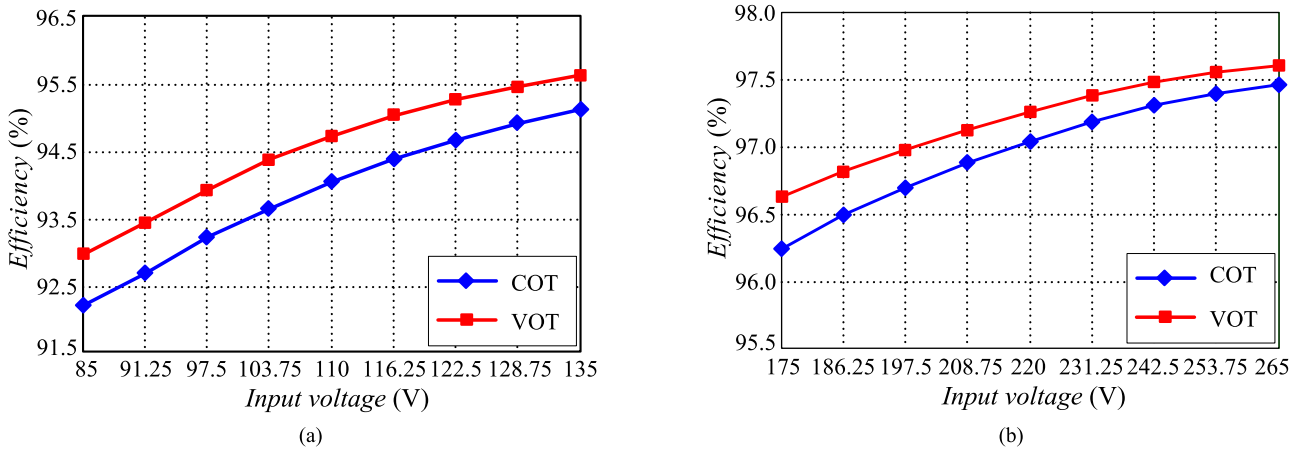

Fig. 20. Measured efficiency: (a) under 85–135 VAC and (b) under 175–265 VAC.

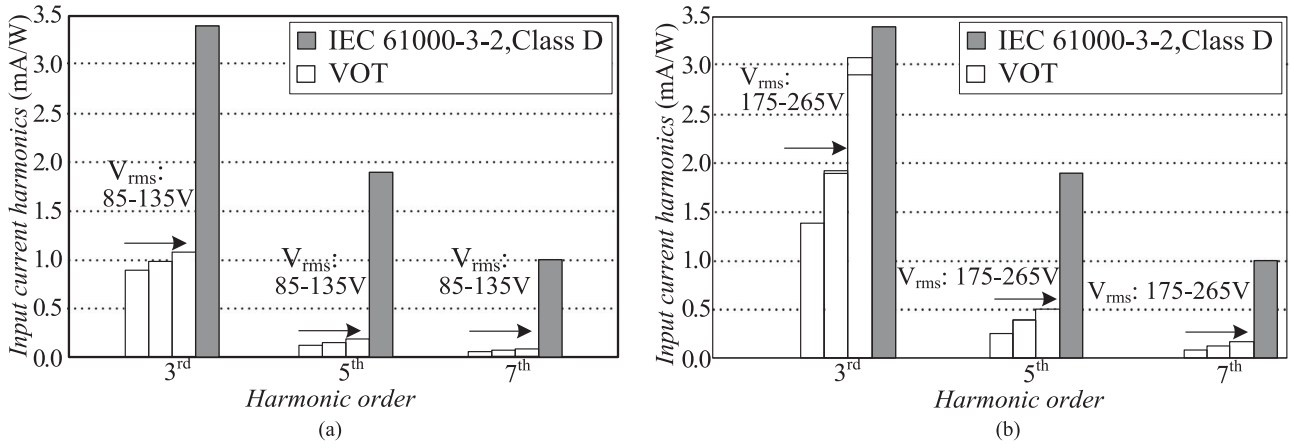

Fig. 21. Measured input current harmonics: (a) under 85–135 VAC and (b) under 175–265 VAC.

Figs. 15–17 show the experimental waveforms of the input voltage, input current, boost inductor current and output voltage ripple with COT and VOT under the input voltage of 85, 110, 135, 175, 220, and 265 VAC, respectively. It can be seen that the waveforms of the input current and inductor's peak current are sinusoidal with COT control. With VOT control, there are some distortions in the currents, especially under a high input voltage.

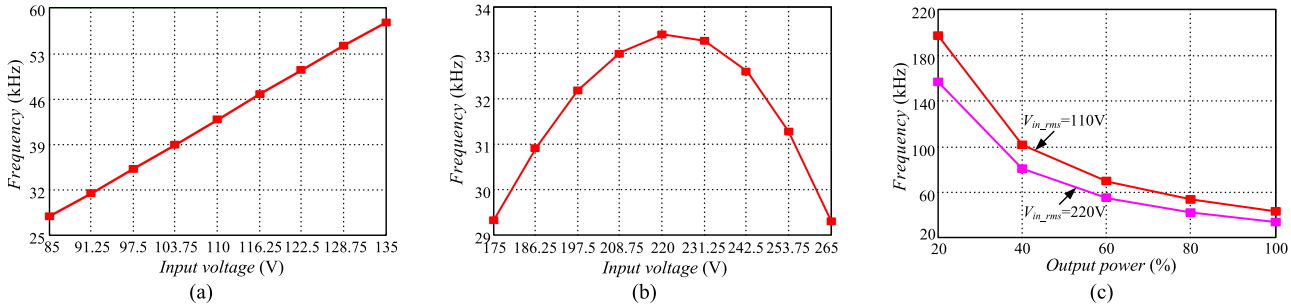

Fig. 22. Tested switching frequency: (a) under 85–135 VAC and full load, (b) under 175–265 VAC and full load, and (c) over the load.

The measured input PF is depicted in Fig. 18, from which it can be noticed that VOT obtains a lower PF than that with COT, especially under a high input voltage.

As can be seen from Fig. 19, with the increase of the input voltage, the output voltage ripple with VOT decreases, which is reduced compared to that with COT.

Fig. 20 illustrates the measured efficiency. It can be seen that the efficiency of the converter with VOT is higher than that with COT. The reason is as follows. From Fig. 11, it can be seen that the rms value of the currents with VOT are nearly the same as that with COT, which means that the conduction losses have little difference. Furthermore, Fig. 10 demonstrates that the peak value of the inductor current, i.e., the peak value of the switch current, increases around 0 and π, and decreases around $\pi/2$, and the most important of all, the switching frequency is greatly reduced, as shown in Fig. 5. Therefore, the switching turn-off loss is reduced.

Fig. 21 shows the recorded data of the third, fifth, and seventh input current harmonics. Obviously, VOT results in higher values of harmonics than that with COT. However, they still meet the IEC 61000-3-2 Class D limit.

Fig. 22 presents the measured switching frequency versus the input voltage and output power, which are slightly lower than the theoretical value in Fig. 5, for the efficiency of 100% cannot be achieved in the real experiment.

The experimental results agree well with that of the theoretical analysis.

VI. Conclusion

This paper proposes a fixed switching frequency control for a CRM boost PFC converter, which has potential significance in the EMI filter design. The VOT is derived and the implementation circuit is proposed, where a feedforward scheme is added to the existing basis of the control. With the proposed method, the input PF is lowered and the input current harmonics still well meet the IEC61000-3-2 Class D. Meanwhile, the output voltage ripple is reduced and the efficiency is improved. A 120-W prototype has been built and tested and the experimental results verify the theoretical analysis. The proposed control scheme is suitable for low-power applications in the countries where the nominal line voltage is around 110 or 120 VAC, for a fixed switching frequency can be achieved during a line cycle which is in favor of the EMI filter design, and the PF is around 0.99. Under the input voltage of 175–265 or 85–265 VAC, LED lighting may be an application field, for "ENERGY STAR" stipulates that the input PF of LED power supply should be not less than 0.9 and 0.7 for household and commercial occasions, respectively.

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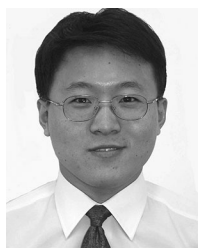

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