Approximate Discrete-Time Modeling of DC–DC Converters With Consideration of the Effects of Pulse Width Modulation

Xin Li, Xinbo Ruan, *Fellow, IEEE*, Qian Jin, *Student Member, IEEE*, Mengke Sha, and Chi K. Tse, *Fellow, IEEE*

***Abstract*—For dc–dc converters with pulsating output current, such as boost and buck–boost converters, the use of leading-edge or trailing-edge pulse width modulation (PWM) can result in distinctly different behavior. This phenomenon is not readily captured by the usual averaged model but can be predicted with a discrete-time model. However, the discrete-time model, which tracks the dynamics of state variables over a switching period, is usually more complex and less convenient to apply for the design of the feedback control. Based on the low-pass characteristics of dc–dc converters, an approximate discrete-time model is proposed in this paper, and upon transforming to the *s*-domain, the model results in transfer functions that can be conveniently used for deriving practical closed-loop parameters. With the proposed model, the loop gain, the input and output impedances are derived and analyzed. The effects of applying different types of PWM on the stability of a single dc–dc converter and a system of cascaded dc–dc converters are discussed. Finally, prototypes of a buck converter, a boost converter, and a cascaded system of buck and boost converters are constructed to verify the effectiveness of the approximate discrete-time model.**

***Index Terms*—Averaged model, discrete-time model, leading edge, pulse width modulation (PWM), stability, trailing edge.**

I. Introduction

PULSE width modulation (PWM) has been widely used in dc–dc converters. According to the form of the triangular carrier used, the implementation of PWM can be leading-edge modulation and trailing-edge modulation, as shown in Fig. 1. For the leading-edge modulation, the switch is turned OFF at the beginning of each switching period, and the turn-on time instant is controlled via a feedback arrangement. For the trailing-edge modulation, the switch is turned ON at the beginning of each switching period, and the turn-off time instant is controlled. In practice, most available PWM controllers are designed with the trailing-edge modulation. However, the leading-edge modulation is found to have advantages in some applications, e.g., in the nonlinear carrier controlled power factor correction [1], [2]. Besides, in a cascaded converter system, the leading-edge modulation is often used together with trailing-edge modulation to reduce the amount of the ripple current in the output capacitor and improve the efficiency [3], [4]. When digital control is applied, both leading-edge and trailing-edge modulation methods can be implemented through software programming [5], [6].

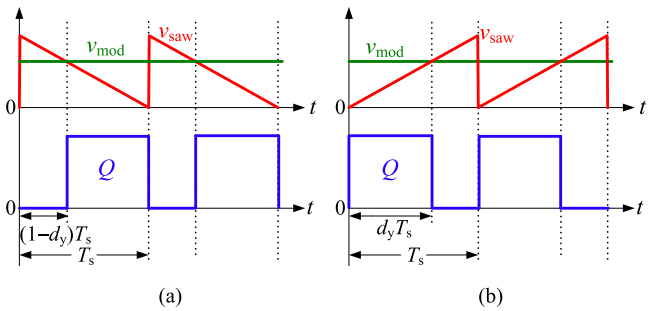

Fig. 1. Illustration of PWM showing sawtooth carrier and control signal (upper), and resulting pulse-width modulated signal (lower). (a) Leading-edge modulation. (b) Trailing-edge modulation.

It is well known that PWM dc–dc converters exhibit strong nonlinearity, and modeling the converters are nontrivial. The averaging technique has been applied for modeling the PWM dc–dc converters [7] by taking the averaged values of the circuit variables over a switching period resulting in a continuous-time model that can be linearized to produce a linear small-signal model. A few variants of the averaging technique have been proposed and widely adopted, such as the state-space averaged model [8], equivalent three-terminal switching model [9], [10], current injection equivalent circuit approach [11], and canonical circuit model [12]. The average models are simple, but the accuracy of the resulting linearized models is usually limited below one-fifth of the switching frequency. Besides, the averaged model disregards the switching sequence of the PWM modulation, and thus cannot capture the differences between leading-edge and trailing-edge modulation.

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X. Li, X. Ruan, Q. Jin, and M. Sha are with the Center for More-Electric-Aircraft Power System, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 211106, China (e-mail: lixin_1989@nuaa.edu.cn; ruanxb@nuaa.edu.cn; qian_jin@nuaa.edu.cn; shamengke@nuaa.edu.cn).

C. K. Tse is with the Department of Electronic and Information Engineering, the Hong Kong Polytechnic University, Hong Kong, China (e-mail: michael.tse@polyu.edu.hk).

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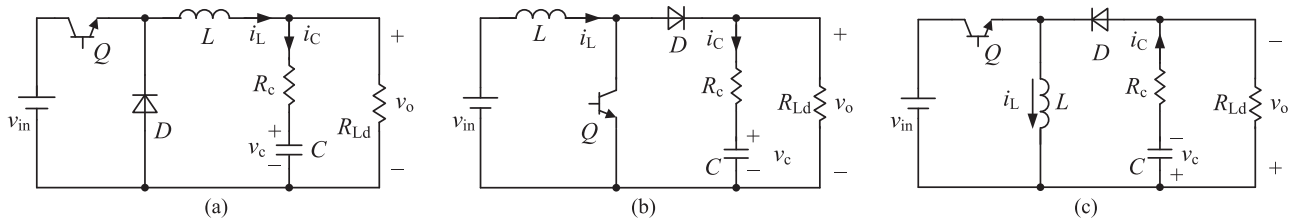

Fig. 2. Three basic dc–dc converters. (a) Buck converter. (b) Boost converter. (c) Buck–boost converter.

To capture the effects of specific PWM, the discrete-average model can be used [13], in which the expression of the output voltage is extended from the output voltage before the intersection [14], [15]. To be specific, for the leading-edge modulation, the expression of the output voltage is extended from the turn-off interval, whereas for the trailing-edge modulation, the expression of the output voltage is extended from the turn-on interval. Thus, the discrete-average model is capable of reflecting the distinction between different modulations. However, the discrete-average model is still based on the averaging technique. In fact, the PWM modulator has the characteristics of nature-sampling systems [16], the small-signal perturbation of the duty-cycle is an impulse sequence happening at the intersection instant [5]. This is the primary cause of the difference between the leading-edge and trailing-edge modulations. Moreover, the impulse sequence contains sideband components with the amplitudes being identical to that at the perturbation frequency [17].

Thus, the sideband components would also influence the small-signal model, and this influence is neglected by the averaging technique. Consequently, the discrete-average model predicts a higher phase margin of the loop gain, which brings stability issues for the dc–dc converters [17]. As a result, the discrete-average model is not accurate for deriving the transfer function from duty cycle to output voltage, $G_{\rm vd}$.

In the discrete-time model, the key variables are analyzed by sampling them at a fixed point of every switching cycle, which contributes to very high accuracy. However, it should be noted that the choice of the sampling point affects the resulting form of the discrete-time model and the information it captures. In conventional discrete-time models [18], [19], uniform sampling is often used, i.e., the sampling instant is the beginning of each switching cycle. However, for natural sampling, the sampling instants are the instants when the modulation (control) signal intersects with the sawtooth carrier. To better describe the characteristics of PWM dc–dc converters, sampling methods consistent with natural sampling should be used [16], [20]. However, this sampling choice would make the derivation of control-to-output transfer function, $G_{\rm vd}$, and the associated parameter expressions very complex and inconvenient to apply for closed-loop control design. To alleviate this problem, we consider in this paper the discrete-time model with the sampling instants fixed at the intersections of the control signal and the carrier, and propose an approximate discrete-time model based on the inherent low-pass characteristic of dc–dc converters. The approximate discrete-time model can readily capture the effects of different modulation methods on the dynamic behavior of PWM dc–dc converters.

This paper is organized as follows. In Section II, the discrete-time model with sampling points fixed at the intersecting instants of the control signal and the carrier for both leading-edge and trailing-edge modulation is analyzed. Then, an approximate discrete-time model is derived in Section III. Using the approximate discrete-time model, the effects of modulation on dc–dc converters and systems of cascaded converters are analyzed in Sections IV and V. To verify the effectiveness of the proposed model, three prototypes, namely a buck converter, a boost converter, and a cascaded system of buck and boost converters, are experimentally studied in Section VI. Finally, Section VII concludes this paper.

II. Discrete-Time Model Consistent With Natural Sampling

A. State-Space Description of Three Basic Converters

Fig. 2 shows the three basic dc–dc converters, namely buck, boost, and buck–boost converters, where $i_{\rm L}$ and $v_{\rm c}$ are the inductor current and output capacitor voltage forming the two state variables, $R_{\rm c}$ is the equivalent series resistor (ESR) of the output capacitor C, and other components and variables are as labeled in the diagram.

The standard form of state equation and output equation for the three converters can be obtained as [8]

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_j\mathbf{x}(t) + \mathbf{B}_j v_{\rm in}(t) \tag{1a}$$

$$v_o(t) = \mathbf{C}_j\mathbf{x}(t) \tag{1b}$$

where $j = 1$ for on-time interval, and $j = 2$ for off-time interval.

The state vector $\mathbf{x}(t)$ is $[\sqrt{L}i_L(t), \sqrt{C}v_c(t)]^T$. The expressions of the system matrices are listed in Table I, where $k = R_{\rm c}/(R_{\rm c} + R_{\rm Ld})$. Note that (1) is piecewise linear in time.

As seen from Table I, for the buck converter, $\mathbf{C}_1 = \mathbf{C}_2$, which indicates that the output voltage is continuous. In contrast, for the boost and buck–boost converters, $\mathbf{C}_1 \neq \mathbf{C}_2$, which means that the output voltage is discontinuous.

B. Discrete-Time Model With Sampling Instants Fixed at the Intersection Instant

By stacking the solutions of the linear equations in (1) for all subintervals over one switching period, a difference equation expressing values of the state variables at $t = (n+1)\,T_{\rm s} + T_{\rm sp}$

TABLE I
SYSTEM MATRICES OF BASIC DC–DC CONVERTERS WITH SUBSCRIPT 1 FOR ON-TIME AND 2 FOR OFF-TIME

Converters	$\mathbf{A}_1$	$\mathbf{A}_2$	$\mathbf{B}_1$	$\mathbf{B}_2$	$\mathbf{C}_1$	$\mathbf{C}_2$
Buck	$k\begin{bmatrix} -\frac{R_c}{L} & -\frac{1}{\sqrt{LC}} \\ \frac{1}{\sqrt{LC}} & -\frac{1}{R_{\rm Ld}C} \end{bmatrix}$	$k\begin{bmatrix} -\frac{R_c}{L} & -\frac{1}{\sqrt{LC}} \\ \frac{1}{\sqrt{LC}} & -\frac{1}{R_{\rm Ld}C} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{\sqrt{L}} \\ 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	$k\begin{bmatrix} \frac{R_c}{\sqrt{L}} & \frac{1}{\sqrt{C}} \end{bmatrix}$	$k\begin{bmatrix} \frac{R_c}{\sqrt{L}} & \frac{1}{\sqrt{C}} \end{bmatrix}$
Boost	$k\begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_{\rm Ld}C} \end{bmatrix}$	$k\begin{bmatrix} -\frac{R_c}{L} & -\frac{1}{\sqrt{LC}} \\ \frac{1}{\sqrt{LC}} & -\frac{1}{R_{\rm Ld}C} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{\sqrt{L}} \\ 0 \end{bmatrix}$	$\begin{bmatrix} \frac{1}{\sqrt{L}} \\ 0 \end{bmatrix}$	$k\begin{bmatrix} 0 & \frac{1}{\sqrt{C}} \end{bmatrix}$	$k\begin{bmatrix} \frac{R_c}{\sqrt{L}} & \frac{1}{\sqrt{C}} \end{bmatrix}$
Buck–Boost	$k\begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{R_{\rm Ld}C} \end{bmatrix}$	$k\begin{bmatrix} -\frac{R_c}{L} & -\frac{1}{\sqrt{LC}} \\ \frac{1}{\sqrt{LC}} & -\frac{1}{R_{\rm Ld}C} \end{bmatrix}$	$\begin{bmatrix} \frac{1}{\sqrt{L}} \\ 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \end{bmatrix}$	$k\begin{bmatrix} 0 & \frac{1}{\sqrt{C}} \end{bmatrix}$	$k\begin{bmatrix} \frac{R_c}{\sqrt{L}} & \frac{1}{\sqrt{C}} \end{bmatrix}$

TABLE II
SYSTEM MATRICES OF DISCRETE-TIME MODEL

Matrices	Modulations	Generic expressions
$\mathbf{\Phi}$	Leading edge	$e^{\mathbf{A}_2(1-D_y)T_s}e^{\mathbf{A}_1 D_y T_s}$
	Trailing edge	$e^{\mathbf{A}_1 D_y T_s}e^{\mathbf{A}_2(1-D_y)T_s}$
$\mathbf{\Gamma_d}$	Leading edge	$\mathbf{\Phi}[(\mathbf{A}_1-\mathbf{A}_2)\mathbf{X}[(1-D_y)T_s]+(\mathbf{B}_1-\mathbf{B}_2)V_{\rm in}]T_s$
	Trailing edge	$\mathbf{\Phi}[(\mathbf{A}_1-\mathbf{A}_2)\mathbf{X}(D_y T_s)+(\mathbf{B}_1-\mathbf{B}_2)V_{\rm in}]T_s$

in terms of those at $t = nT_s + T_{\rm sp}$, where $T_{\rm sp}$ is the time from the start of the period to the sampling instant, can be obtained as

$$\begin{cases} \mathbf{x}\left[(n+1)T_s + T_{\rm sp}\right] = e^{\mathbf{A}_2 T_{\rm sp}} e^{\mathbf{A}_1 (T_s - T_{\rm sp})}\mathbf{x}(nT_s + T_{\rm sp}) \\ + e^{\mathbf{A}_2 T_{\rm sp}} \displaystyle\int_0^{T_s - T_{\rm sp}} e^{\mathbf{A}_1 \tau}\mathbf{B}_1 v_{\rm in} d\tau + \int_0^{T_{\rm sp}} e^{\mathbf{A}_2 \tau}\mathbf{B}_2 v_{\rm in} d\tau \\ v_{\rm o\_dis}\left(nT_s + T_{\rm sp}\right) = \mathbf{C}_2\mathbf{x}\left(nT_s + T_{\rm sp}\right) \end{cases} \tag{2a}$$

for leading-edge modulation, and

$$\begin{cases} \mathbf{x}\left[(n+1)T_s + T_{\rm sp}\right] = e^{\mathbf{A}_1 T_{\rm sp}} e^{\mathbf{A}_2 (T_s - T_{\rm sp})}\mathbf{x}(nT_s + T_{\rm sp}) \\ + e^{\mathbf{A}_1 T_{\rm sp}} \displaystyle\int_0^{T_s - T_{\rm sp}} e^{\mathbf{A}_2 \tau}\mathbf{B}_2 v_{\rm in} d\tau + \int_0^{T_{\rm sp}} e^{\mathbf{A}_1 \tau}\mathbf{B}_1 v_{\rm in} d\tau \\ v_{\rm o\_dis}\left(nT_s + T_{\rm sp}\right) = \mathbf{C}_1\mathbf{x}\left(nT_s + T_{\rm sp}\right) \end{cases} \tag{2b}$$

for trailing-edge modulation. In our model, the sampling time $T_{\rm sp}$ is the instant when the modulation signal intersects with the carrier waveform. For the leading-edge modulation, $T_{\rm sp} = (1 - d_{\rm yn})T_{\rm s}$, whereas for the trailing-edge modulation, $T_{\rm sp} = d_{\rm yn}T_{\rm s}$. Thus, the output voltages of leading-edge and trailing-edge modulation at $T_{\rm sp}$ are $\mathbf{C}_2\mathbf{x}[nT_{\rm s} + (1 - d_{\rm yn})T_{\rm s}]$ and $\mathbf{C}_1\mathbf{x}(nT_{\rm s} + d_{\rm yn}T_{\rm s})$, respectively.

By imposing small-signal duty-cycle perturbation on (2), and then eliminating the quiescent values and ignoring the high order ac terms, the duty-cycle-to-output-voltage transfer function of the discrete-time model, $G_{\rm vd\_dis}(z)$, using z-transformation can be obtained as

$$G_{\rm vd\_dis}(z) = \mathbf{C}_{\rm mod}(z\mathbf{I} - \mathbf{\Phi})^{-1}\mathbf{\Gamma_d} \tag{3}$$

where $\mathbf{\Phi}$ and $\mathbf{\Gamma_d}$ are the system matrices of the discrete-time model, as shown in Table II. For the leading-edge modulation, $\mathbf{C}_{\rm mod} = \mathbf{C}_2$, and for the trailing-edge modulation, $\mathbf{C}_{\rm mod} = \mathbf{C}_1$. Since $\mathbf{C}_1 = \mathbf{C}_2$ for the buck converter, the expression of $G_{\rm vd\_dis}(z)$ of the buck converter using either modulation is the same.

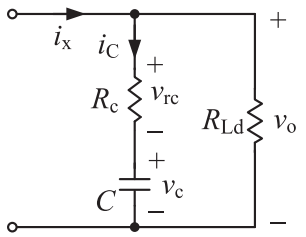

Fig. 3. Schematic diagram of the output terminals of the converters.

C. Analysis of the Basic Converters

The output terminals of the buck, boost, and buck–boost converters are shown in Fig. 3, where $i_{\rm x}$ denotes the sum of the output capacitor current and the load current, and the output capacitor current $i_{\rm C}$ is the ac component of $i_{\rm x}$.

For the buck converter, $i_{\rm x}$ is the inductor current $i_{\rm L}$, which is continuous. Therefore, both $i_{\rm C}$ and output voltage $v_{\rm o}$ are continuous. As a result, the relationship between $i_{\rm C}$ and $v_{\rm o}$ remains the same regardless of the type of modulation. Thus, the duty-cycle-to-output-voltage transfer function $G_{\rm vd\_dis}(z)$ for the buck converter is unaffected by the use of leading-edge or trailing-edge modulation.

For the boost and buck–boost converters, $i_{\rm x}$ is the diode current $i_{\rm D}$, which is discontinuous. Thus, $i_{\rm C}$ and $v_{\rm o}$ exhibit a step change at the turn-on and turn-off instants. According to the discrete-time model, the output voltages for the leading-edge and trailing-edge modulated converters are $\mathbf{C}_2\mathbf{x}(T_{\rm sp}) = kv_{\rm c}(T_{\rm sp}) + kR_{\rm c}i_{\rm L}(T_{\rm sp})$ and $\mathbf{C}_1\mathbf{x}(T_{\rm sp}) = kv_{\rm c}(T_{\rm sp})$, respectively. Since $i_{\rm L}(t)$ leads $v_{\rm c}(t)$ in phase, the output voltage in the leading-edge modulated boost or buck–boost converter has a leading phase angle under the same duty-cycle perturbation. Thus, the duty-cycle-to-output-voltage transfer function of the leading-edge modulated boost or buck–boost converter $G_{\rm vd\_dis\_lead}(z)$ shows a leading phase angle to that of the trailing-edge modulated converter $G_{\rm vd\_dis\_trail}(z)$.

III. APPROXIMATE DISCRETE-TIME MODEL OF DC–DC CONVERTERS

The discrete-time model can accurately capture the natural sampling characteristics of dc–dc converters. However, the

difference equation given in (3) is too complex to provide useful intuition or insights into the effects of the different types of PWM on the characteristics of dc–dc converters for the purpose of closed-loop control design. In this section, an approximate discrete-time model is proposed, taking into consideration the inherent low-pass characteristics of dc–dc converters. Since the dimension of $\mathbf{\Phi}$ is two, (3) can be rewritten as [21]

$$G_{\mathrm{vd\_dis}}(z) = \mathbf{C}_{\mathrm{mod}} \frac{z\mathbf{I} - \mathrm{adj}(\mathbf{\Phi})}{\det(z\mathbf{I} - \mathbf{\Phi})} \mathbf{\Gamma_d} \tag{4}$$

where $\mathrm{adj}(.)$ and $\det(.)$ represent the adjoint and determinant of a matrix, respectively.

Taking the trailing-edge modulated boost converter as an example, the derivation of the approximate $G_{\mathrm{vd\_dis}}(z)$ is given below. Normally, in order to maintain a small switching ripple in the output voltage, the circuit parameters should be chosen such that the following conditions are satisfied:

$$R_{\mathrm{Ld}}C >> T_s, L/R_c >> T_s, LC >> T_s^2. \tag{5}$$

For the boost converter, $e^{\mathbf{A_1}D_yT_s}$ is calculated as

$$e^{\mathbf{A_1}D_yT_s} = \begin{bmatrix} 1 & 0 \\ 0 & e^{-D_yT_s/(R_{\mathrm{Ld}}C)} \end{bmatrix}. \tag{6}$$

Using Taylor series and keeping the first-order term on (6), we have

$$e^{-D_yT_s/(R_{\mathrm{Ld}}C)} \approx 1 - D_yT_s/(R_{\mathrm{Ld}}C). \tag{7}$$

Substitution of (7) into (6) leads to

$$e^{\mathbf{A_1}D_yT_s} \approx \begin{bmatrix} 1 & 0 \\ 0 & 1 - D_yT_s/(R_{\mathrm{Ld}}C) \end{bmatrix}. \tag{8}$$

Similarly, $e^{\mathbf{A_2}(1-D_y)T_s}$ can be approximated to

$$e^{\mathbf{A_2}(1-D_y)T_s} \approx \begin{bmatrix} 1 - \frac{R_c}{L}(1-D_y)T_s & -\frac{1-D_y}{\sqrt{LC}}T_s \\ \frac{1-D_y}{\sqrt{LC}}T_s & 1 - \frac{1-D_y}{R_{\mathrm{Ld}}C}T_s \end{bmatrix}. \tag{9}$$

Substituting (8) and (9) into the expression of $\mathbf{\Phi}$ shown in Table II, we have

$$\begin{aligned} \mathbf{\Phi} &= e^{\mathbf{A_1}D_yT_s}e^{\mathbf{A_2}(1-D_y)T_s} \\ &\approx \begin{bmatrix} 1 - \frac{R_c}{L}(1-D_y)T_s & -\frac{1-D_y}{\sqrt{LC}}T_s \\ \left(1 - \frac{D_yT_s}{R_{\mathrm{Ld}}C}\right)\frac{1-D_y}{\sqrt{LC}}T_s & \left(1 - \frac{D_yT_s}{R_{\mathrm{Ld}}C}\right)\left(1 - \frac{1-D_y}{R_{\mathrm{Ld}}C}T_s\right) \end{bmatrix} \\ &\approx \begin{bmatrix} 1 - \frac{R_c}{L}(1-D_y)T_s & -\frac{1-D_y}{\sqrt{LC}}T_s \\ \frac{1-D_y}{\sqrt{LC}}T_s & 1 - \frac{T_s}{R_{\mathrm{Ld}}C} \end{bmatrix}. \end{aligned} \tag{10}$$

The inductor current $I_{\mathrm{L}}(t)$ arrives at its peak value at $D_{\mathrm{y}}T_{\mathrm{s}}$, and it is expressed as

$$I_L(D_yT_s) = \frac{V_{\mathrm{in}}}{(1-D_y)^2R_{\mathrm{Ld}}} + \frac{V_{\mathrm{in}}}{2L}D_yT_s. \tag{11}$$

Since the ripple voltage amplitude of the output capacitor is much smaller than its dc value, the value of $V_{\mathrm{C}}(t)$ at $D_{\mathrm{y}}T_{\mathrm{s}}$ can be replaced with the dc value, i.e.,

$$V_C(D_yT_s) = V_{\mathrm{in}}/(1-D_y). \tag{12}$$

With the results of (11) and (12), $\mathbf{X}(D_{\mathrm{y}}T_{\mathrm{s}})$ can be approximated as

$$\mathbf{X}(D_yT_s) \approx \begin{bmatrix} \sqrt{L}\left(\frac{V_{\mathrm{in}}}{(1-D_y)^2R_{\mathrm{Ld}}} + \frac{V_{\mathrm{in}}}{2L}D_yT_s\right) \\ \sqrt{C}\frac{V_{\mathrm{in}}}{1-D_y} \end{bmatrix}. \tag{13}$$

According to (10) and (13), an approximate expression of $\mathbf{\Gamma_d}$ can be written as (14), shown at the bottom of this page.

Furthermore, substitution of (10) and (14) into (4) yields an approximate expression of the duty-cycle-to-output-voltage transfer function of the trailing-edge modulated boost converter, $G_{\mathrm{vd\_dis\_bst\_trail}}(z)$, which is given by (15), shown at the bottom of this page.

Noted that (15) is expressed in the z-domain. For convenience of application in control design, it is desirable to express (15) in the s-domain. Using Padé transformation, for the operating frequency range below half of the switching frequency f_s, the following approximate transformation between the z-domain and the s-domain can be applied:

$$z \approx \frac{1 + 0.5sT_s + \left(\frac{sT_s}{\pi}\right)^2}{1 - 0.5sT_s + \left(\frac{sT_s}{\pi}\right)^2}. \tag{16}$$

$$\mathbf{\Gamma_d} = V_{\mathrm{in}}T_s \begin{bmatrix} \frac{\sqrt{L}}{(1-D_y)^2R_{\mathrm{Ld}}}\left[\frac{R_c}{L} - \left(\frac{R_c}{L}\right)^2(1-D_y)T_s + \frac{(1-D_y)T_s}{LC}\right] + \frac{1}{(1-D_y)\sqrt{L}}\left(1 - \frac{R_c}{L}(1-D_y)T_s\right) \\ \frac{1}{(1-D_y)^2\sqrt{C}R_{\mathrm{Ld}}}\left[-1 + \frac{R_c}{L}(1-D_y)T_s + \frac{T_s}{R_{\mathrm{Ld}}C}\right] + \frac{T_s}{L\sqrt{C}} \end{bmatrix} \tag{14}$$

$$G_{\mathrm{vd\_dis\_bst\_trail}}(z) \approx \frac{V_{\mathrm{in}}T_s\left[\left(T_s - \frac{L}{(1-D_y)^2R_{\mathrm{Ld}}}\right)(z-1) + T_s\right]}{LC(z-1)^2 + \left[R_cC(1-D_y)T_s + \frac{L}{R_{\mathrm{Ld}}}T_s\right](z-1) + [(1-D_y)T_s]^2} \tag{15}$$

Putting (16) in (15), and upon simplification, we get an approximate duty-cycle-to-output-voltage transfer function for the trailing-edge modulated boost converter in the s-domain, $G_{\mathrm{vd\_dis\_bst\_trail}}(s)$, as shown in (17) shown at the bottom of this page.

Based on (5), the coefficient of s^2 term in the denominator of (17) can be approximated as the following equation:

$$1-\frac{1}{2}\left((1-D_y)\frac{R_c}{L}+\frac{1}{R_{\mathrm{Ld}}C}\right)T_s+\left(\frac{1}{4}+\frac{2}{\pi^2}\right)\times\frac{(1-D_y)^2}{LC}T_s^2\approx 1. \tag{18}$$

Letting $s=j\omega$, for the frequency range below $f_{\mathrm{s}}/2$, the coefficients of the s^3 and s^4 terms in the denominator of (17) satisfy the following inequalities:

$$\begin{aligned}&\frac{T_s^2}{\pi^2}\left((1-D_y)\frac{R_c}{L}+\frac{1}{R_{\mathrm{Ld}}C}-\frac{(1-D_y)^2}{LC}T_s\right)\omega^3\\&<\frac{T_s^2}{\pi^2}\left((1-D_y)\frac{R_c}{L}+\frac{1}{R_{\mathrm{Ld}}C}-\frac{(1-D_y)^2}{LC}T_s\right)(0.5\omega_s)\omega^2\\&=\frac{1}{\pi}\left((1-D_y)\frac{R_c}{L}T_s+\frac{T_s}{R_{\mathrm{Ld}}C}-\frac{(1-D_y)^2}{LC}T_s^2\right)\omega^2<<\omega^2\end{aligned} \tag{19}$$

$$\begin{aligned}\frac{T_s^4}{\pi^4}\frac{(1-D_y)^2}{LC}\omega^4&<\frac{T_s^4}{\pi^4}\frac{(1-D_y)^2}{LC}(0.5\omega_s)^2\omega^2\\&=\frac{T_s^2}{\pi^2}\frac{(1-D_y)^2}{LC}\omega^2<<\omega^2\end{aligned} \tag{20}$$

As shown in (19) and (20), the s^3 and s^4 terms are relatively small compared with the s^2 term, and thus can be omitted.

Finally, the expression of the duty-cycle-to-output-voltage transfer function, $G_{\mathrm{vd\_dis\_bst\_trail}}(s)$, can be simplified as (21) shown at the bottom of this page.

Following the same procedure, the duty-cycle-to-output-voltage transfer function, $G_{\mathrm{vd}}(s)$, for all basic converters using the trailing-edge and leading-edge modulation can be derived, as shown in (22)–(24) as shown at the bottom of this page, where subscripts "bu", "bst," and "bb" denote buck, boost, and buck–boost converter, subscript "dis" denotes discrete-time modeling, and m is 1 for leading-edge modulated converters, and is 0 for trailing-edge modulated converters.

As expected for the buck converter, which is not affected by the type of modulation, the expression of $G_{\mathrm{vd\_dis\_bu}}(s)$ shown in (22) makes no distinction of leading-edge or trailing-edge modulation.

To verify the validity of the proposed approximate modeling method, the Bode diagrams of G_{vd} before and after application of the proposed approximation are shown in Fig. 4, where the circuit parameters of the three converters are given in the Appendix. From Fig. 4, the Bode plots of the approximate transfer functions match well with the original ones (without approximation) up to half of the switching frequency, confirming the validity of the approximate discrete-time modeling method. Meanwhile, it is observed that for the buck converter, G_{vd} is independent of the modulation, whereas for the boost and buck–boost converters, the leading-edge modulation clearly causes a phase lead in G_{vd} as compared to the trailing-edge modulation, as shown in the Bode plots of $G_{\mathrm{vd\_lead}}$ and $G_{\mathrm{vd\_trail}}$.

IV. Stability Analysis of DC–DC Converters With Leading-Edge and Trailing-Edge Modulations

From (23), the duty-cycle-to-output-voltage transfer functions of the leading-edge and trailing-edge modulated boost

$$\begin{aligned}&G_{\mathrm{vd\_dis\_bst\_trail}}(s)\\&=\frac{V_{\mathrm{in}}}{LC}\frac{\left[1-0.5sT_s+\left(\frac{sT_s}{\pi}\right)^2\right]\left[1+s\left(-\frac{L}{(1-D_y)^2R_{\mathrm{Ld}}}+0.5\left(1-D_y\right)T_s\right)+\left(\frac{sT_s}{\pi}\right)^2\right]}{\frac{T_s^4}{\pi^4}\frac{(1-D_y)^2}{LC}s^4+\frac{T_s^2}{\pi^2}\left((1-D_y)\frac{R_c}{L}+\frac{1}{R_{\mathrm{Ld}}C}-\frac{(1-D_y)^2}{LC}T_s\right)s^3\\&\quad+\left[1-\frac{1}{2}\left((1-D_y)\frac{R_c}{L}+\frac{1}{R_{\mathrm{Ld}}C}\right)T_s+\left(\frac{1}{4}+\frac{2}{\pi^2}\right)\frac{(1-D_y)^2}{LC}T_s^2\right]s^2+\left[(1-D_y)\frac{R_c}{L}+\frac{1}{R_{\mathrm{Ld}}C}-\frac{(1-D_y)^2}{LC}T_s\right]s+\frac{(1-D_y)^2}{LC}}\end{aligned} \tag{17}$$

$$G_{\mathrm{vd\_dis\_bst\_trail}}(s)=\frac{V_{\mathrm{in}}}{LC}\left[1-0.5sT_s+\left(\frac{sT_s}{\pi}\right)^2\right]\cdot\frac{1+s\left(-\frac{L}{(1-D_y)^2R_{\mathrm{Ld}}}+0.5\left(1-D_y\right)T_s\right)+\left(\frac{sT_s}{\pi}\right)^2}{s^2+s\left[(1-D_y)\frac{R_c}{L}+\frac{1}{R_{\mathrm{Ld}}C}-\frac{(1-D_y)^2}{LC}T_s\right]+\frac{(1-D_y)^2}{LC}} \tag{21}$$

$$G_{\mathrm{vd\_dis\_bu}}(s)=\frac{V_{\mathrm{in}}}{LC}\left[1-0.5sT_s+\left(\frac{sT_s}{\pi}\right)^2\right]\frac{1+s\left(CR_c+0.5T_s\right)+\left(\frac{sT_s}{\pi}\right)^2}{s^2+s\left(\frac{R_c}{L}+\frac{1}{R_{\mathrm{Ld}}C}-\frac{T_s}{LC}\right)+\frac{1}{LC}} \tag{22}$$

$$G_{\mathrm{vd\_dis\_bst}}(s)=\frac{V_{\mathrm{in}}}{LC}\left[1-0.5sT_s+\left(\frac{sT_s}{\pi}\right)^2\right]\cdot\frac{1+s\left[m\left(\frac{CR_c}{1-D_y}+D_yT_s\right)-\frac{L}{(1-D_y)^2R_{\mathrm{Ld}}}+\frac{(1-D_y)T_s}{2}\right]+\left(\frac{sT_s}{\pi}\right)^2}{s^2+s\left[(1-D_y)\frac{R_c}{L}+\frac{1}{R_{\mathrm{Ld}}C}-\frac{(1-D_y)^2}{LC}T_s\right]+\frac{(1-D_y)^2}{LC}} \tag{23}$$

$$G_{\mathrm{vd\_dis\_bb}}(s)=\frac{V_{\mathrm{in}}}{LC}\left[1-0.5sT_s+\left(\frac{sT_s}{\pi}\right)^2\right]\cdot\frac{1+s\left[m\left(\frac{CR_c}{1-D_y}+D_yT_s\right)-\frac{D_yL}{(1-D_y)^2R_{\mathrm{Ld}}}+\frac{(1-D_y)T_s}{2}\right]+\left(\frac{sT_s}{\pi}\right)^2}{s^2+s\left[(1-D_y)\frac{R_c}{L}+\frac{1}{R_{\mathrm{Ld}}C}-\frac{(1-D_y)^2}{LC}T_s\right]+\frac{(1-D_y)^2}{LC}} \tag{24}$$

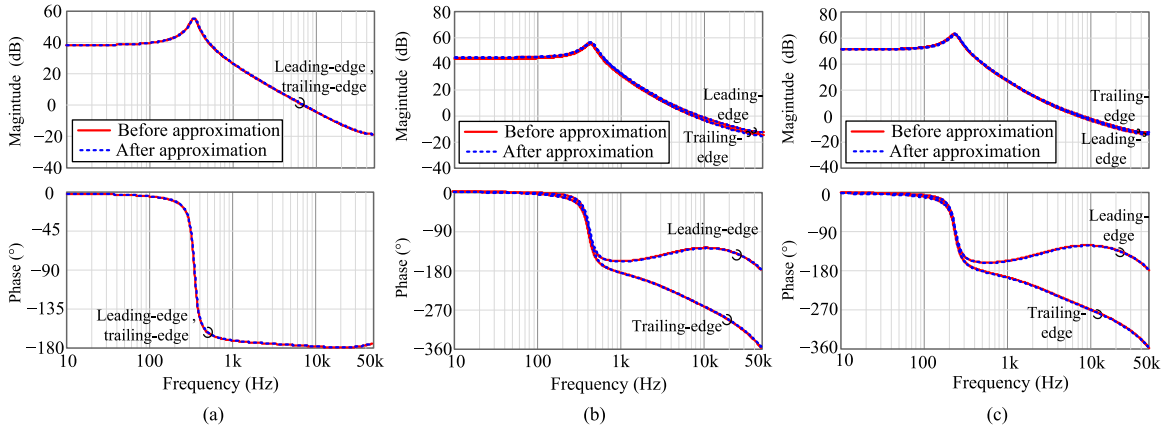

Fig. 4. Bode diagrams of duty-cycle-to-output-voltage transfer function $G_{\mathrm{vd\_dis}}(s)$, before and after application of approximate discrete-time modeling method for (a) buck converter, (b) boost converter, and (c) buck–boost converter.

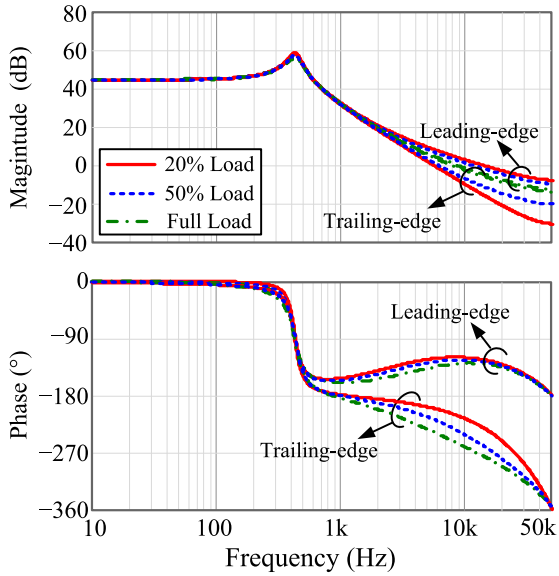

Fig. 5. Bode diagrams of duty-cycle-to-output-voltage transfer function $G_{\mathrm{vd\_dis\_bst}}(s)$ of boost converters at different loads.

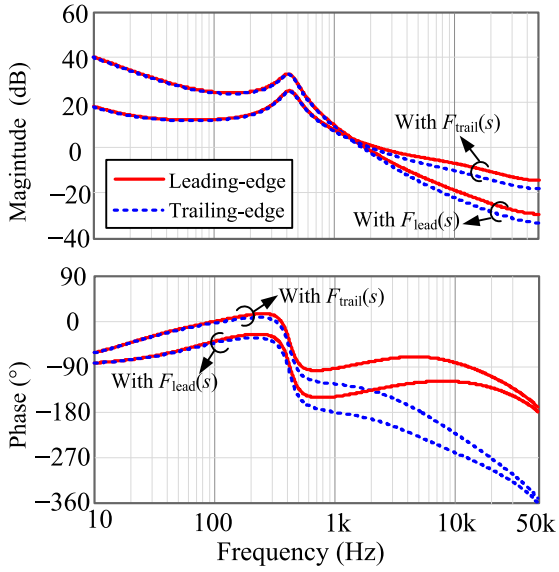

Fig. 6. Bode diagrams of loop gain $T_{\mathrm{dis\_bst}}(s)$ for boost converter using the controllers of $F_{\mathrm{lead}}(s)$ and $F_{\mathrm{trail}}(s)$.

converters differ mainly in the numerator term, i.e.,

$$1+s\left[m\left(\frac{CR_c}{1-D_y}+D_yT_s\right)-\frac{L}{(1-D_y)^2R_{\mathrm{Ld}}}+\frac{(1-D_y)\,T_s}{2}\right]+\left(\frac{sT_s}{\pi}\right)^2\triangleq 1+\frac{2\zeta sT_s}{\pi}+\left(\frac{sT_s}{\pi}\right)^2. \tag{25}$$

Comparing with the standard quadratic expression, the damping ratio ζ can be identified as

$$\zeta=\frac{\pi}{2}\left[m\left(\frac{CR_c}{(1-D_y)T_s}+D_y\right)-\frac{L}{(1-D_y)^2R_{\mathrm{Ld}}T_s}+\frac{1-D_y}{2}\right]. \tag{26}$$

Note that when $\zeta<0$, the zeros of (25) are on the right half-plane, which introduces a phase lag at high frequencies, and the smaller the ζ, the larger the phase lag. This phase lag would affect the stability of the converter. As seen from (26), it can be found that ζ in the leading-edge modulated converter is larger than in the trailing-edge modulated converter. Thus, the boost converter has improved stability when the leading-edge modulation is adopted, as illustrated in Fig. 4(b).

Fig. 5 gives the Bode diagrams of $G_{\mathrm{vd\_dis\_bst}}(s)$ for the leading-edge and trailing-edge modulated boost converters under different load conditions. As seen, ζ decreases as the load becomes heavier. Therefore, to guarantee a sufficient stability margin of the boost converter, the controller should be designed at full load.

Since the approximate discrete-time model has been translated to the s-domain, the closed-loop design can be accomplished using any standard control design procedure [22]–[24], and will be omitted here. For the same cutoff frequency and phase margin, the closed-loop control parameters for the leading-edge and trailing-edge modulated converters are different. By setting f_c at 2 kHz, and the phase margin as 45°, the controller for the leading-edge modulated converter $F_{\mathrm{lead}}(s)$

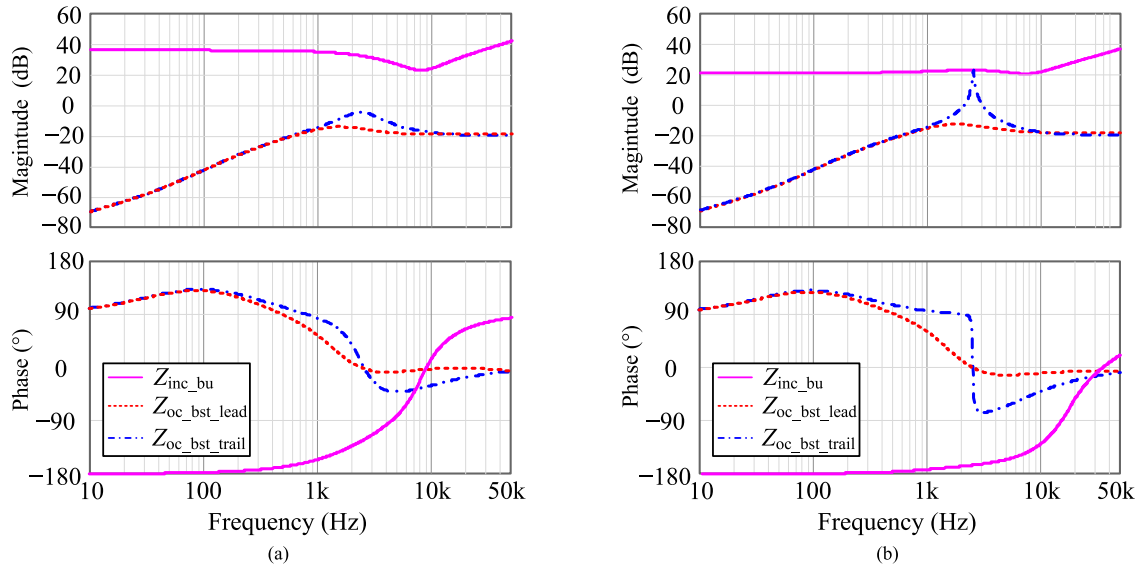

Fig. 7. Bode diagrams of closed-loop input and output impedances in a cascaded system of boost converter and buck converter at (a) 20% load and (b) full load.

is designed as

$$F_{\text{lead}}(s) = \left(4.375 + \frac{2190}{s}\right)\frac{s+10048}{s+15700}. \tag{27}$$

Likewise, the controller for the trailing-edge modulated converter $F_{\text{trail}}(s)$ is

$$F_{\text{trail}}(s) = \left(20.8 + \frac{2512.7}{s}\right)\frac{s+2413}{s+65400}. \tag{28}$$

To investigate the effect of PWM on the stability of the converters, we use the same set of closed-loop parameters in our analysis. Fig. 6 shows the loop gain of the boost converter with different control functions. As seen from Fig. 6, when adopting $F_{\text{lead}}(s)$, the boost converter is stable under leading-edge modulation, but becomes unstable under trailing-edge modulation. Moreover, as seen from Fig. 6, when adopting $F_{\text{trail}}(s)$, the boost converter is stable under both leading-edge and trailing-edge modulation. Also, the boost converter under leading-edge modulation is more stable, as evidenced by the larger phase margin.

V. Analysis of Input and Output Impedances Under Different Types of PWM

A. Closed-Loop Input and Output Impedances Based on the Approximate Discrete-Time Model

The open-loop input impedance of a dc–dc converter is defined as the ratio of the small-signal input voltage to the small-signal input current at constant duty cycle. The open-loop output impedance is the ratio of the small-signal output voltage to the small-signal output current at constant duty cycle. Since the duty cycle is the same regardless of the type of PWM used, the open-loop impedances are independent of the modulation method and the average technique suffices in deriving the open-loop impedances [8]. Specifically, the open-loop input impedance of the basic converters is of the following form:

$$Z_{\text{in}}(s) = \frac{R_{\text{Ld}}}{M^2}\frac{LCs^2 + \left(R_cC + \frac{L}{R_{\text{Ld}}}\right)s + 1}{1 + R_{\text{Ld}}Cs} \tag{29}$$

where M represents the voltage transfer ratio which is equal to D_{y}, $1/(1-D_{\text{y}})$, and $D_{\text{y}}/(1-D_{\text{y}})$ for the buck, boost, and buck–boost converters, respectively.

The open-loop output impedance of the buck converter is expressed as

$$Z_{\text{o\_bu}}(s) = \frac{sL + s^2LCR_c}{LCs^2 + \left(R_cC + \frac{L}{R_{\text{Ld}}}\right)s + 1} \tag{30}$$

and the open-loop output impedances of the boost and buck–boost converters share the same expression, i.e.,

$$\begin{aligned} Z_{\text{o\_bst}}(s) &= Z_{\text{o\_bb}}(s) \\ &= \frac{s^2LCR_c + sL + sR_c^2C(1-D_y)D_y + R_c(1-D_y)D_y}{LCs^2 + \left[(1-D_y)R_cC + \frac{L}{R_{\text{Ld}}}\right]s + (1-D_y)^2}. \end{aligned} \tag{31}$$

Using the approximate discrete-time modeling method and (29), the closed-loop input impedance can be found as [25]

$$Z_{\text{inc}}(s) = \frac{1}{-\frac{M^2}{R_{\text{Ld}}}\frac{T_{\text{dis}}(s)}{1+T_{\text{dis}}(s)} + \frac{1}{Z_{\text{in}}(s)}\frac{1}{1+T_{\text{dis}}(s)}} \tag{32}$$

where T_{dis} is the loop gain derived from the approximate method. Furthermore, the closed-loop output impedance is obtained as

$$Z_{\text{oc}}(s) = \frac{Z_o(s)}{1+T_{\text{dis}}(s)}. \tag{33}$$

B. Stability of Cascaded Systems

According to the stability criterion for cascaded converter systems [25], [26], if both the source converter and the load

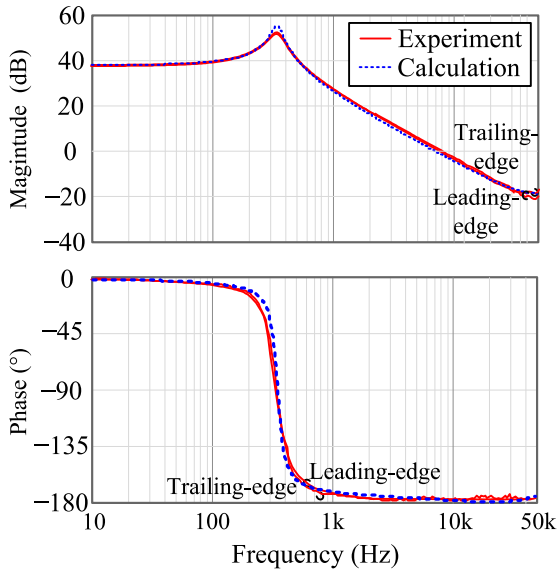

Fig. 8. Bode diagrams of calculated and measured duty-cycle-to-output-voltage transfer function for the buck converter, $G_{\mathrm{vd\_dis\_bu}}$, showing identical behavior for leading-edge and trailing-edge modulation.

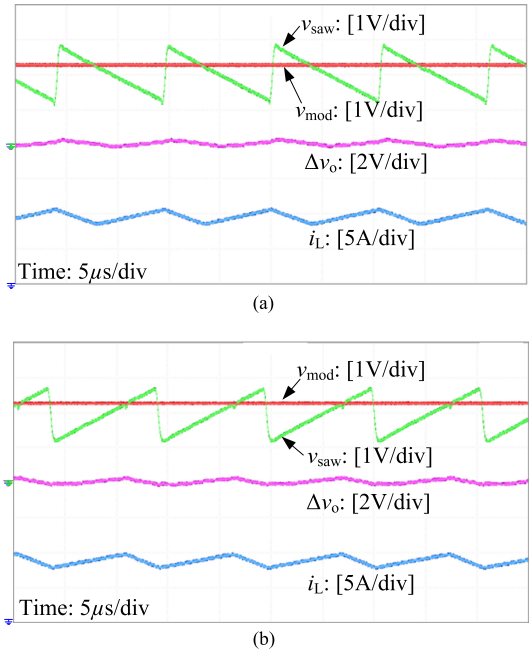

Fig. 9. Experimental waveforms of buck converter with (a) leading-edge modulation and (b) trailing-edge modulation.

converter are stable individually, the cascaded system is stable if the ratio of the source converter's output impedance $Z_{\mathrm{oc}}(s)$ and the load converter's input impedance $Z_{\mathrm{inc}}(s)$, $Z_{\mathrm{oc}}(s)/Z_{\mathrm{inc}}(s)$, satisfies the Nyquist stability criterion in the entire frequency range. From (32) and (33), it should be clear that the difference in $G_{\mathrm{vd\_dis}}(s)$ for the leading-edge and trailing-edge modulated converters will make the closed-loop input and output impedances different for the two modulation cases. Thus, the type of PWM used will affect the stability of the cascaded system. For the purpose of illustration, we take a cascaded system consisting of a boost converter and a buck converter as an example. The parameters of the buck and boost converters are given in the Appendix.

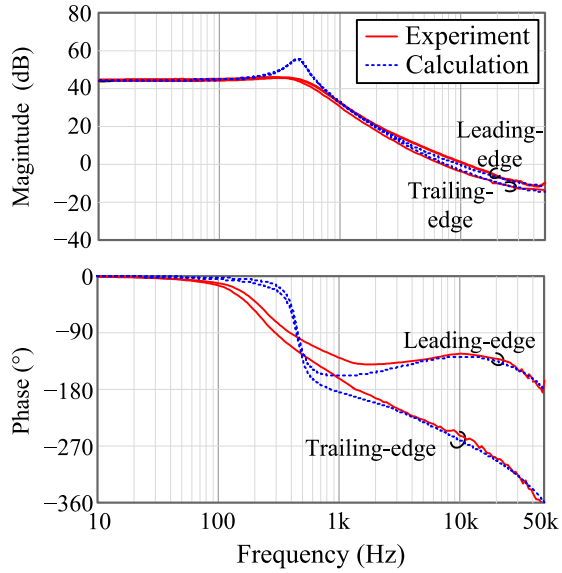

Fig. 10. Bode diagrams of calculated and measured duty-cycle-to-output-voltage transfer function for the boost converter, $G_{\mathrm{vd\_dis\_bst}}(s)$.

Generally speaking, the load converter can be regarded as a constant power load, and its closed-loop impedance behaves as a negative resistor [25], which is not affected by the type of PWM used, i.e.,

$$Z_{\mathrm{inc}}(s) \approx -R_{\mathrm{Ld}} / M^2. \tag{34}$$

As a result, only the effect of PWM on $Z_{\mathrm{oc}}(s)$ of the source converter is significant and should be considered. Since the peak value of Z_{oc} appears around the cutoff frequency [27], its value can be expressed as

$$\begin{aligned} |Z_{\mathrm{oc}}(j2\pi f_c)| &= \left| \frac{Z_o(j2\pi f_c)}{1 + T_{\mathrm{dis}}(j2\pi f_c)} \right| \\ &= \frac{|Z_o(j2\pi f_c)|}{|1 - \cos(\mathrm{PM}) - j\sin(\mathrm{PM})|} \\ &= \frac{|Z_o(j2\pi f_c)|}{\sqrt{2 - 2\cos(\mathrm{PM})}}. \end{aligned} \tag{35}$$

Obviously, there is a negative correlation between $|Z_{\mathrm{oc}}(j2\pi f_c)|$ and the phase margin. Based on the analysis above, with the same controller, the trailing-edge modulated boost converter has a lower phase margin than the leading-edge modulated case. This gives a higher peak value of $Z_{\mathrm{oc\_trail}}$, meaning that the converter is less stable if the trailing-edge modulation is adopted for the source converter.

Let the control function be $F_{\mathrm{bst}}(s)$, which is specifically designed as

$$F_{\mathrm{bst}}(s) = \left(12.18 + \frac{19130}{s}\right) \frac{s + 7815}{s + 31570}. \tag{36}$$

With this controller, the boost converter is stable under both leading-edge and trailing-edge modulations. Moreover, the buck converter employs the trailing-edge modulation, and the control

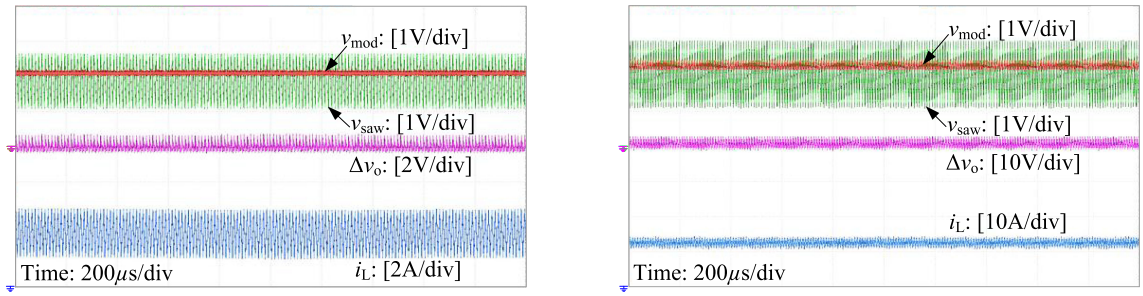

Fig. 11. Experimental waveforms of leading-edge modulated boost converter with controller $F_{\rm lead}(s)$ at (a) 20% load and (b) full load.

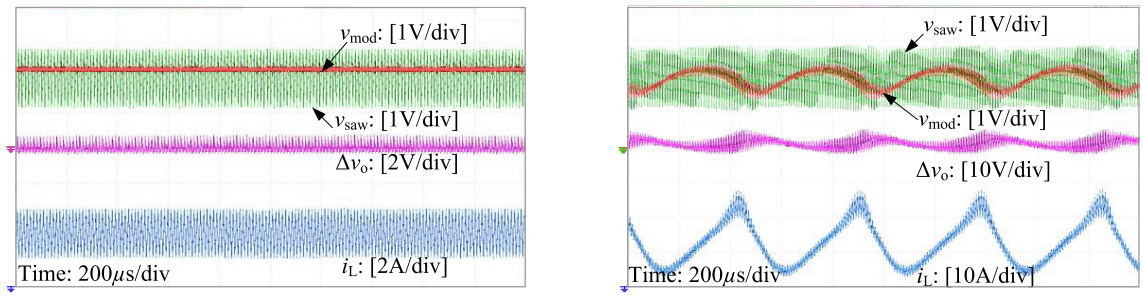

Fig. 12. Experimental waveforms of trailing-edge modulated boost converter with controller $F_{\rm lead}(s)$ at (a) 20% load and (b) full load.

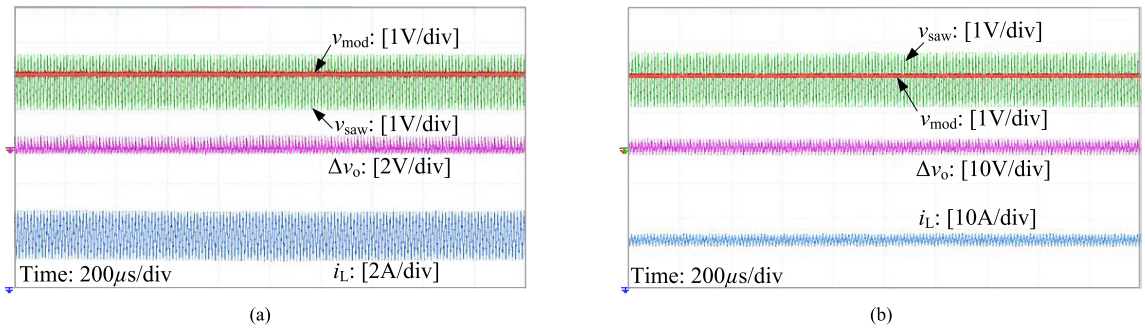

Fig. 13. Experimental waveforms of leading-edge modulated boost converter with controller $F_{\rm trail}(s)$ at (a) 20% load and (b) full load.

function is given by

$$F_{\rm bu}(s) = \left(59.4 + \frac{352955}{s}\right)\frac{s+6447}{s+116100}. \qquad (37)$$

Fig. 7 gives the Bode diagrams of $Z_{\rm inc\_bu}(s)$ and $Z_{\rm oc\_bst}(s)$ at 20% load and full-load conditions, respectively. As shown here, when the leading-edge modulation is adopted for the source boost converter, $Z_{\rm oc\_bst\_lead}(s)$ and $Z_{\rm inc\_bu}(s)$ do not intersect at either light load or full load. When the trailing edge is employed for the boost converter, $Z_{\rm oc\_bst\_trail}(s)$ and $Z_{\rm inc\_bu}(s)$ intersect at 2.5 kHz with a phase difference exceeding 180° under full-load condition, but do not intersect at 20% load. Therefore, the cascaded system is predicted to be stable if the leading-edge modulation is used in the boost converter, but is unstable at full-load condition if the trailing-edge modulation is applied, and the system will oscillate at a frequency of 2.5 kHz. Clearly, the type of PWM adopted will impact the stability of the cascaded system. With the same controller, it is more beneficial for the cascaded system to adopt the leading-edge modulation in its source converter.

VI. Experimental Verification

Three prototypes, namely a buck converter, a boost converter, and a cascaded system of buck and boost converters, are constructed for verification of the proposed modeling method. The circuit parameters are shown in the Appendix, and all the controllers are implemented with analog circuits.

A. Experimental Results of Buck Converter

Fig. 8 shows the Bode diagrams of the calculated (from the model) and measured duty-cycle-to-output-voltage transfer function $G_{\rm vd\_dis\_bu}$. The close resemblance of the calculated and measured results verifies the validity of the model. Furthermore, the results verify that the type of PWM used does not affect the

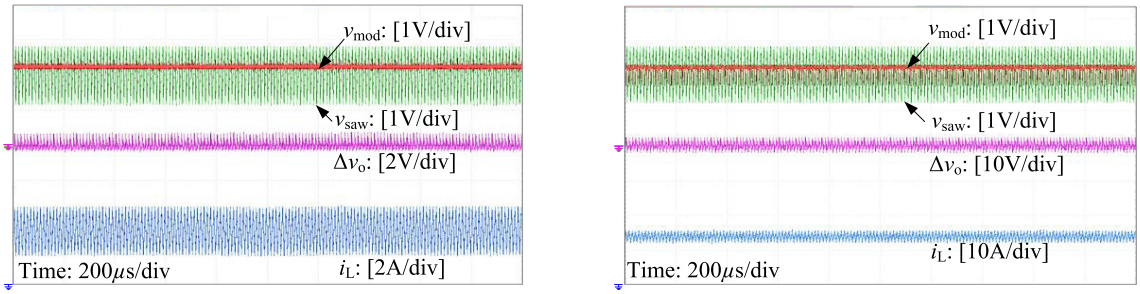

Fig. 14. Experimental waveforms of trailing-edge modulated boost converter with controller $F_{\rm trail}(s)$ at (a) 20% load and (b) full load.

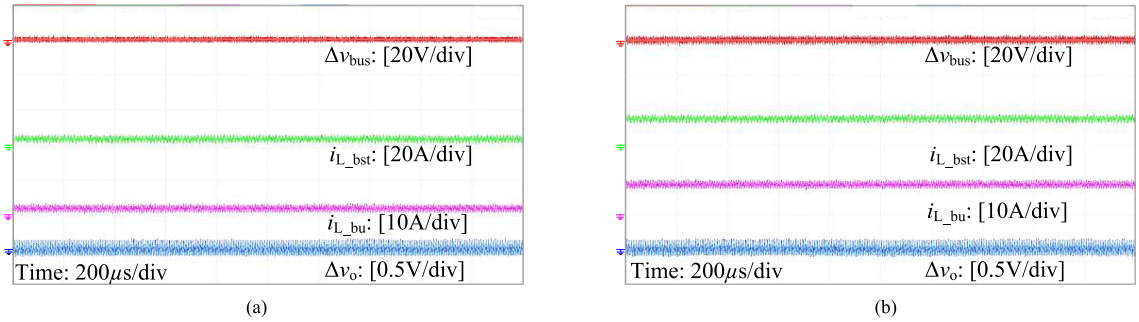

Fig. 15. Experimental waveforms of the cascaded system when boost converter is leading-edge modulated. (a) 20% load. (b) Full load.

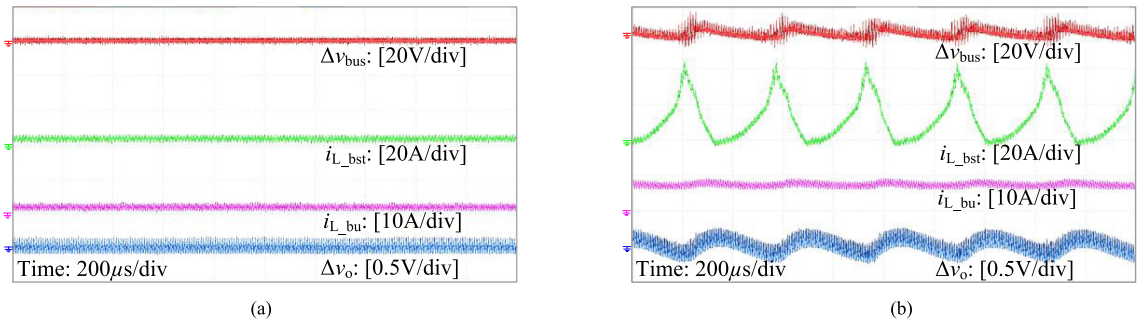

Fig. 16. Experimental waveforms of the cascaded system when boost converter is trailing-edge modulated. (a) 20% load. (b) Full load.

duty-cycle-to-output-voltage transfer function, as predicted by the model.

Taking $F_{\rm bu}(s)$ in (37) as the control function, the experimental steady-state waveforms of the leading-edge and trailing-edge modulated buck converters are given in Fig. 9. Obviously, the converter is stable with either modulation methods, consistent with the analysis.

B. Experimental Results of Boost Converter

Fig. 10 shows the Bode diagrams of the calculated and measured duty-cycle-to-output-voltage transfer function $G_{\rm vd\_dis\_bst}$. Again, the close resemblance of the calculated and measured results verifies the proposed modeling method. Moreover, it can be observed that the phase of the trailing-edge modulated converter lags that of the leading-edge modulated converter's, which is consistent with our analysis.

Taking $F_{\rm lead}(s)$ as the control function, the experimental steady-state waveforms at 20% load and full load are shown in Figs. 11 and 12, respectively. Here, the boost converter is stable with either PWM methods at 20% load, but oscillates at full load when the trailing-edge modulation is adopted.

Taking $F_{\rm trail}(s)$ as the control function, moreover, the experimental steady-state waveforms at 20% load and full load are shown in Figs. 13 and 14, respectively. As seen, the boost converter is stable at any load regardless of the type modulation adopted.

The experimental results shown in Figs. 11–14 are in good agreement with the analysis, validating the proposed approximate discrete-time modeling method for predicting stability of the boost converter.

C. Experimental Results of Cascaded System of Boost and Buck Converters

Experimental results for a cascaded system consisting of a boost converter and a buck converter are shown in Figs. 15 and 16. We see that the cascaded system is stable when the boost

converter adopts the leading-edge modulation (see Fig. 15), and it becomes unstable at full load when the boost converter adopts the trailing-edge modulation (see Fig. 16), and the oscillation frequency is 2.6 kHz, which is consistent with the analysis.

VII. Conclusion

The discrete-time model can accurately capture the effects of PWM on the behavior of dc–dc converters, but the method generally results in rather complex forms of transfer functions in the z-domain, which are not convenient to apply in closed-loop control design. In view of the low applicability of the discrete-time model, we propose in this paper an approximate discrete-time modeling method based on the low-pass characteristics of dc–dc converters, and convert the relevant transfer functions to the s-domain, which can be readily and conveniently applied in the closed-loop control design. Using the proposed model, we show that the buck converter is unaffected by the type of PWM used. Moreover, for the boost and buck–boost converters, the phase margin of the loop gain is wider when the leading-edge PWM is used. Furthermore, the effect of the use of leading-edge or trailing-edge PWM on the input and output impedances is analyzed. It is found that for a cascaded system of converters, the use of leading-edge PWM in the source or upstream converter offers the advantage of improved stability.

Appendix

For the buck, boost, and buck–boost converters in this paper, the rated output power $P_{\rm o} = 500$ W, the switching frequency $f_{\rm s} = 100$ kHz, the amplitude of sawtooth carrier $V_{\rm m} = 1.75$ V, and the voltage feedback coefficient $H = 0.05$. The other main circuit parameters of these three converters are given in Tables A1–A3.

TABLE A1
Parameters of the Buck Converter

Parameter	Symbol	Value	Parameter	Symbol	Value
Input votlage	$V_{\rm in}$	80 V	Output capacitor	C	220 μF
Output voltage	$V_{\rm o}$	54 V	Capacitor ESR	$R_{\rm c}$	10 mΩ
Inductor	L	95 μH			

TABLE A2
Parameters of the Boost Converter

Parameter	Symbol	Value	Parameter	Symbol	Value
Input votlage	$V_{\rm in}$	36 V	Output capacitor	C	300 μF
Output voltage	$V_{\rm o}$	80 V	Capacitor ESR	$R_{\rm c}$	0.1 Ω
Inductor	L	95 μH			

TABLE A3
Parameters of the Buck–Boost Converter

Parameter	Symbol	Value	Parameter	Symbol	Value
Input votlage	$V_{\rm in}$	36 V	Output capacitor	C	470 μF
Output voltage	$V_{\rm o}$	80 V	Capacitor ESR	$R_{\rm c}$	68 mΩ
Inductor	L	60 μH			

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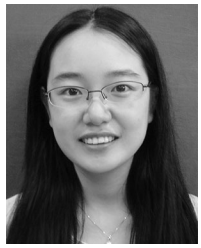
Xin Li received the B.S. degree in electrical engineering and automation, in 2012, from Nanjing University of Aeronautics and Astronautics, Nanjing, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include modeling and control of dc–dc converters and cascaded power system.

Xinbo Ruan (M'97–SM'02–F'16) was born in Hubei Province, China, in 1970. He received the B.S. and Ph.D. degrees in electrical engineering from Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1991 and 1996, respectively.

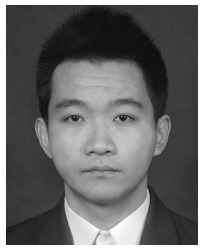
In 1996, he joined the Faculty of Electrical Engineering Teaching and Research Division, NUAA, where he became a Professor in the College of Automation Engineering in 2002 and has been engaged in teaching and research in the field of power electronics. From August to October 2007, he was a Research Fellow in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong, China. Since March 2008, he has been also with the School of Electrical and Electronic Engineering, Huazhong University of Science and Technology, China. He is a Guest Professor with Beijing Jiaotong University, Beijing, China, Hefei University of Technology, Hefei, China, and Wuhan University, Wuhan, China. He is the author or co-author of 9 books and more than 200 technical papers published in journals and conferences. His main research interests include soft-switching dc-dc converters, soft-switching inverters, power factor correction converters, modeling the converters, power electronics system integration and renewable energy generation system.

Prof. Ruan was a recipient of the Delta Scholarship by the Delta Environment and Education Fund in 2003 and was a recipient of the Special Appointed Professor of the Chang Jiang Scholars Program by the Ministry of Education, China, in 2007. From 2005 to 2013, he served as Vice President of the China Power Supply Society, and since 2008, he has been a member of the Technical Committee on Renewable Energy Systems within the IEEE Industrial Electronics Society. Currently, he serves as an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, the IEEE TRANSACTIONS ON POWER ELECTRONICS, the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS ON POWER ELECTRONICS, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-II. He is an IEEE Fellow.



Qian Jin (S'14) received the B.S. and Ph.D. degrees in electrical engineering and automation from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 2011 and 2017, respectively.

Her research interests include envelope tracking power supplies and dc–dc converters.



Mengke Sha received the B.S. degree in electrical engineering, in 2015, from Nanjing University of Aeronautics and Astronautics, Nanjing, China, where he is currently working toward the M.S. degree in electrical engineering.

His research interests include modeling and control of dc–dc converters.

Chi K. Tse (M'90–SM'97–F'06) received the B.Eng. (First Class Hons.) degree in electrical engineering and the Ph.D. degree in electrical engineering from the University of Melbourne, Melbourne, VIC, Australia, in 1987 and 1991, respectively.

He is currently the Chair Professor at Hong Kong Polytechnic University, Hong Kong, China, where he was the Head of the Department of Electronic and Information Engineering from 2005 to 2012.

Dr. Tse was awarded a number of research and industry awards, including Prize Paper Awards by the IEEE TRANSACTIONS ON POWER ELECTRONICS in 2001 and 2015, RISP Journal of Signal Processing Best Paper Award in 2014, Best Paper Award by *International Journal of Circuit Theory and Applications* in 2003, two Gold Medals at the International Inventions Exhibition in Geneva in 2009 and 2013, a Silver Medal at the International Invention Innovation Competition in Canada in 2016, and a number of recognitions by the academic and research communities, including honorary professorship by several Chinese and Australian universities, Chang Jiang Scholar Chair Professorship, IEEE Distinguished Lectureship, Distinguished Research Fellowship by the University of Calgary, Gledden Fellowship, and International Distinguished Professorship-at-Large by the University of Western Australia. While with the Hong Kong Polytechnic University, he received the President's Award for Outstanding Research Performance twice, Faculty Research Grant Achievement Award twice, Faculty Best Researcher Award, and several teaching awards. He serves and has served as an Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II (2016–2017), the IEEE CIRCUITS AND SYSTEMS MAGAZINE (2012–2015), the IEEE CIRCUITS AND SYSTEMS SOCIETY NEWSLETTER (since 2007), an Associate Editor of three IEEE Journal/Transactions, an Editor of *International Journal of Circuit Theory and Applications*, and he is on the editorial boards of a few other journals. He also serves as panel member of Hong Kong Research Grants Council and NSFC, and member of several professional and government committees.