Analysis on Synchronous Rectifier Control to Improve Regulation Capability of High-Frequency *LLC* Resonant Converter

Keon-Woo Kim, *Student Member, IEEE*, Han-Shin Youn, *Student Member, IEEE*, Jae-Il Baek, *Student Member, IEEE*, Yeonho Jeong, *Student Member, IEEE*, and Gun-Woo Moon, *Member, IEEE*

***Abstract*—A new synchronous rectifier (SR) control method is proposed to improve the light-load regulation capability of high-frequency *LLC* resonant converter. The proposed control method applies the extended SR turn-on time, which results in the negative current flowing through SRs, and the light-load regulation of the *LLC* resonant converter can be achieved by the negative current. The design guideline of the extended SR turn-on time is presented based on the precise analysis and the equivalent circuit modeling of the *LLC* resonant converter. In addition, the switching loss and gate driving loss can be reduced because the output voltage can be regulated at low switching frequency. The validity of a proposed control method is confirmed by the experimental results of a prototype converter with 330–380 VDC input and 750 W (12 V/62.5 A) output.**

***Index Terms*—High frequency, high power density, light-load regulation, *LLC* resonant converter, low profile, parasitic capacitance, planar transformer (PT), synchronous rectifier (SR) control.**

I. Introduction

RECENTLY, high power density of power systems has become a very important issue in many fields such as LED drivers, flat TVs, server powers, and electric vehicle battery chargers [1]–[5]. Although high power density can be achieved with reducing the size of the transformers and the inductors by increasing a switching frequency, high switching frequency can be a burden for large switching losses. Therefore, to minimize the switching losses, the soft-switching converters having zero-voltage-switching (ZVS) and zero-current-switching (ZCS) capability should be applied. Among the soft-switching converters, an *LLC* resonant converter could be a great candidate due to wide ZVS range of the primary switches and ZCS characteristic of the synchronous rectifiers (SRs) [6]–[9]. In addition, a planar transformer (PT) is also a great solution for high power density due to low height and small volume of transformer [10]–[12]. Moreover, PT has a large surface area, which improves the heat dissipation capability, thus it is suitable for high power density converters. Therefore, the *LLC* resonant converter with PT is widely used for high power density converters, as shown in Fig. 1.

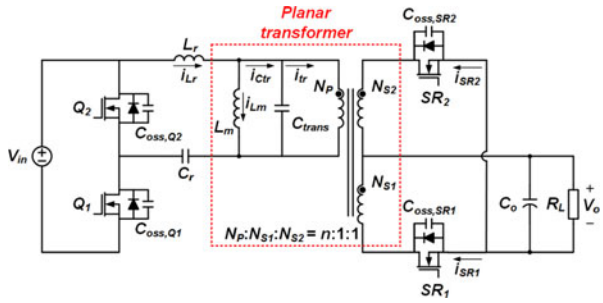

Fig. 1. Circuit diagram of the *LLC* resonant converter considering the parasitic capacitors.

However, despite the advantage of low profile and good heat dissipation capability, PT leads to serious regulation problem for the *LLC* resonant converter due to large parasitic capacitance [13]–[15]. When PT is utilized, a printed circuit board (PCB) should be used as the windings of PT [16]. Each layer in PCB contains the primary or secondary turns of the transformer, and every turns are overlapped for high power density. Overlapping winding layers result in large parasitic capacitance between each layers, and it can be modeled by the transformer parasitic capacitor $C_{\rm trans}$, as shown in Fig. 1 [14]. Large parasitic capacitance leads to unwanted behavior of the voltage gain, and Fig. 2 presents the voltage gain of the *LLC* resonant converter at no-load conditions by considering the parasitic capacitors. Due to large $C_{\rm trans}$, the voltage gain of the *LLC* resonant converter is increased, and the switching frequency becomes higher to regulate the output voltage [17], [18]. Even worse, if $C_{\rm trans}$ is too large, the output voltage cannot be regulated. Moreover, the output capacitor of SR $C_{\rm oss,SR}$ also exacerbates the light-load regulation problem. Especially, for high output current applications such as server powers and telecommunication applications, many SRs should be utilized in parallel to reduce the conduction

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K.-W. Kim, J.-I. Baek, Y. Jeong, and G.-W. Moon are with Korea Advanced Institute of Science and Technology, Daejeon 34141 South Korea (e-mail: rainbowdot@kaist.ac.kr; dpi1067@kaist.ac.kr; yh.jeong@kaist.ac.kr; gwmoon@kaist.ac.kr).

H.-S. Youn is with Hyundai Motor Company, Hwaseong, South Korea (e-mail: hanshin.youn@hyundai.co.kr).

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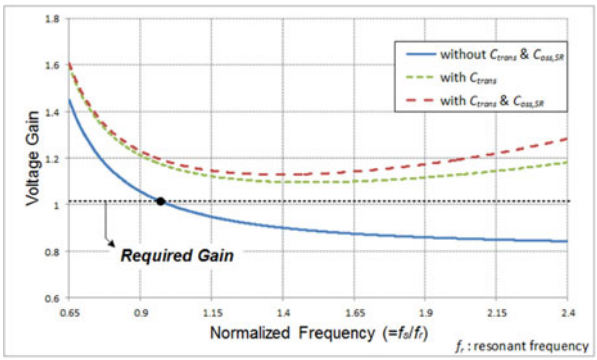


Fig. 2. Voltage gain of the *LLC* resonant converter at no-load conditions with the parasitic capacitors.

loss of the secondary side rectifiers. Due to the parallel connection of SRs, $C_{\mathrm{oss,SR}}$ becomes larger, and it results in a severe regulation problem of the *LLC* resonant converter.

To regulate the output voltage, many papers have been studied [18]–[24]. The work in [19] uses a dummy load to avoid the operation under light-load conditions. Due to simple implementation, the dummy load is widely used in many applications. However, since the dummy load consumes the constant power loss, efficiency is decreased. In [20] and [21], the burst mode strategy is developed in order to improve the light-load regulation capability. However, because of large C_{trans} and $C_{\mathrm{oss,SR}}$, the burst mode operation region should be extended in the case of high-frequency operation with PT and SRs. Therefore, the extended region for the burst mode operation leads to a large ripple output voltage, or a large output capacitor size is required, which reduces the power density. The works in [22] and [23] solved the light-load regulation problem through the phase-shifted gate signals between the primary switch legs. Although this method can regulate the output voltage without additional components and losses, it is only available on the full-bridge inverter structure. Saket *et al.* [18] and Pahlevaninezhad *et al.* [24] proposed a new PCB winding layout to minimize C_{trans} of PT. Although the new PCB winding layout can successfully reduce C_{trans}, their effectiveness is limited to the case of large $C_{\mathrm{oss,SR}}$.

To solve the aforementioned problem, this paper proposes a new SR control method without additional components. Based on the mathematical analysis of the *LLC* resonant converter, the design guideline of the SR turn-on time t_{SR} is presented to achieve the output voltage regulation with the proposed control method under light-load conditions including no-load conditions. In addition, since the proposed control method can regulate the output voltage under the lower switching frequency, the switching loss and gate driving loss are reduced and the efficiency is improved. The operation and performance of the proposed control method are verified by a prototype with 330–380 VDC input and 750 W (12 V/62.5 A) output.

II. Analysis of *LLC* Resonant Converter With Parasitic Capacitors

A. Concept of Proposed Control Method

In the conventional *LLC* resonant converter, the output voltage V_o is regulated by using pulse frequency modulation (PFM) control, which is changing the switching frequency f_s under entire load conditions, and SRs are turned ON while the secondary side current passing through SRs i_{SR} flows from source to drain, as shown in Fig. 3(a). On the other hand, the proposed control method regulates V_o by extending t_{SR}, and i_{SR} can flow through a channel resistor of SR from drain to source during the negative conduction period t_{neg}, as shown in Fig. 3(b). Due to the negative current, the power can be transferred from output to the primary side of the *LLC* resonant converter, and it can reduce the voltage gain.

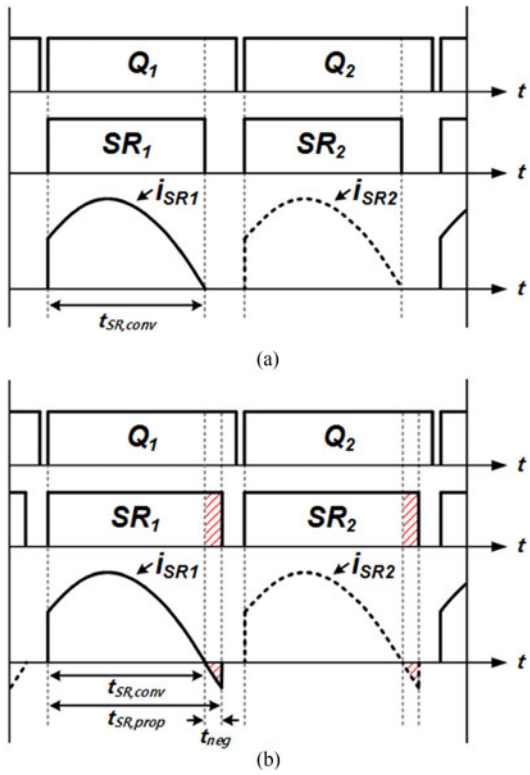


Fig. 3. SR current waveforms. (a) Using the conventional control method. (b) Using the proposed control method.

According to the increase of C_{trans} and $C_{\mathrm{oss,SR}}$, the larger energy is required to charge and discharge parasitic capacitors, and i_{SR} has the bigger positive value when SR is turned ON. Therefore, under the same f_s and load conditions, the positive conduction period of SR is shortened, and t_{neg} can be more extended compared with the *LLC* resonant converter with small C_{trans} and $C_{\mathrm{oss,SR}}$. Since t_{neg} can be more extended, the light-load regulation capability can be increased due to the increased negative current.

Fig. 4 shows a conceptual control diagram for the proposed control method. Under heavy-load conditions, the conventional control method is used, which means that V_o is regulated by PFM control. According to the decrease of load conditions, f_s is increased to regulate V_o. When f_s reaches the designed frequency limit point $f_{s,\mathrm{design}}$, t_{neg} control is used. Since the voltage gain is increased according to the decrease of load conditions, t_{neg} should be increased to regulate V_o over entire load conditions if f_s is constant. Since the converter has the largest voltage gain at no-load conditions, t_{neg} should be designed with a maximum value named as $t_{\mathrm{neg,max}}$.

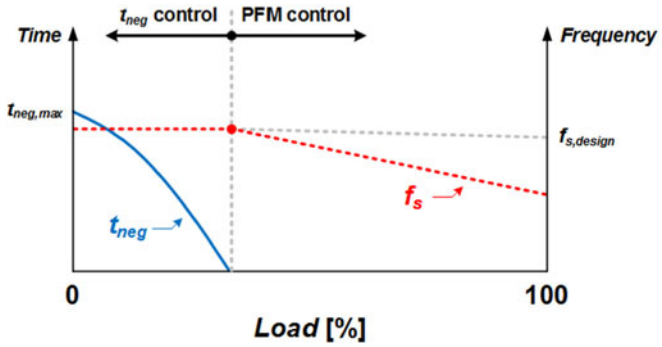


Fig. 4. Conceptual control diagram for the proposed control method.

B. Equivalent Circuit Modeling

The equivalent circuit of the *LLC* resonant converter can be derived through the fundamental harmonic approximation (FHA) [25], [26]. The rectifier, output filter, and load can be modeled as an equivalent resistance by using FHA method. However, FHA method is not suitable methodology for the *LLC* resonant converter with large parasitic capacitance of PT and SRs because charging and discharging period of the parasitic capacitors cannot be negligible. In order to analysis the *LLC* resonant converter with large parasitic capacitors, the new method has been previously researched [27]–[29]. The previous papers have used the rectifier compensated first harmonic approximation (RCFHA) method. In this method, instead of using the resistive impedance, a combination of the resistive and capacitive impedance is employed to model the rectifier, output filter, and load. In order to apply the capacitive impedance from the parasitic capacitors, $C_{\mathrm{oss,SR}}$ is first reflected to the primary side of the *LLC* resonant converter. Then, C_{trans} and $C_{\mathrm{oss,SR}}$ can be simplified to the total parasitic capacitor C_{pa}, and it can be calculated as follows:

$$C_{\mathrm{pa}} = C_{\mathrm{trans}} + \frac{2n_{\mathrm{SR}} C_{\mathrm{oss,SR}}}{n^2} \tag{1}$$

where n_{SR} is the number of SRs in parallel and n is a transformer turns ratio.

Meanwhile, in the case of the *LLC* resonant converter with the proposed control method, RCFHA method cannot be directly utilized to obtain the equivalent circuit due to the negative current flowing through SRs. This paper presents the improved RCFHA method to analyze the *LLC* resonant converter with the proposed control method. Through using this method, the equivalent circuit can be obtained considering C_{pa} and the negative current flowing through SRs. For simple analysis, the following assumptions have been made:

1) the output capacitor is large enough that V_o is constant;
2) it has no transformer dc-offset current because of the symmetric duty of the primary switches and SRs;
3) the primary current flowing through PT i_{Ctr} is the pure sinusoidal waveform.

Based on the assumptions, the key waveforms of the *LLC* resonant converter with the proposed control method are represented in Fig. 5. When the power is transferred to the output, the voltage across C_{pa}, $v_{C\mathrm{pa}}$ is clamped to nV_o, and after the

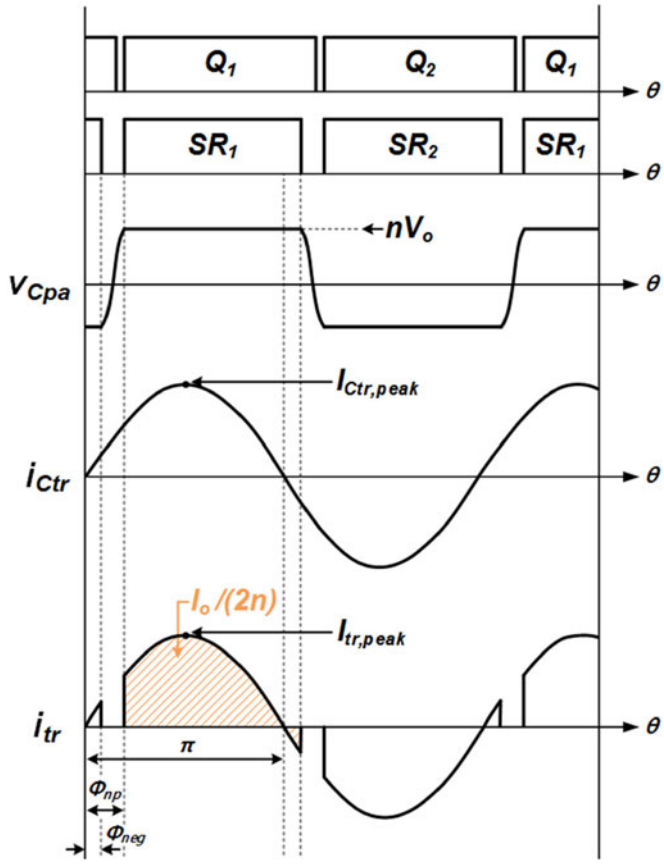


Fig. 5. Key waveforms of the *LLC* resonant converter with the proposed control method.

powering periods, C_{pa} is being charged or discharged. According to RCFHA method, $v_{C\mathrm{pa}}$ is only clamped when the positive current flow through SRs. However, $v_{C\mathrm{pa}}$ is still clamped when the negative current flows through SRs, thus the fundamental frequency component of $v_{C\mathrm{pa}}$ is changed. Moreover, the equivalent impedance model of the *LLC* resonant converter is changed because it is obtained with the fundamental frequency component of $v_{C\mathrm{pa}}$. Therefore, the fundamental frequency component of $v_{C\mathrm{pa}}$ should be calculated with considering the negative current flows through SRs. Fig. 6(a) shows the equivalent circuit of the resonant elements when $v_{C\mathrm{pa}}$ is clamped. During this period, the output capacitor is connected in parallel with the magnetizing inductor, and the output capacitor can be represented as voltage source. According to the Fourier series analysis, a fundamental component of $v_{C\mathrm{pa}}$ when the voltage is clamped, $v_{C\mathrm{pa,clamp(1)}}$ can be expressed as follows:

$$v_{C\mathrm{pa,clamp(1)}} = \frac{2}{\pi}\int_{\phi_{\mathrm{np}}}^{\pi+\phi_{\mathrm{neg}}} (nV_o)e^{-j\theta}d\theta \tag{2}$$

where Φ_{neg} is the negative conduction angle, Φ_{np} is the non-positive conduction angle, and the relation between Φ_{neg} and Φ_{np} is calculated in the appendix.

Using (A1), a boundary condition of $v_{C\mathrm{pa}}$ at Φ_{np} can be obtained, and Φ_{neg} can be calculated from (A2). Therefore,

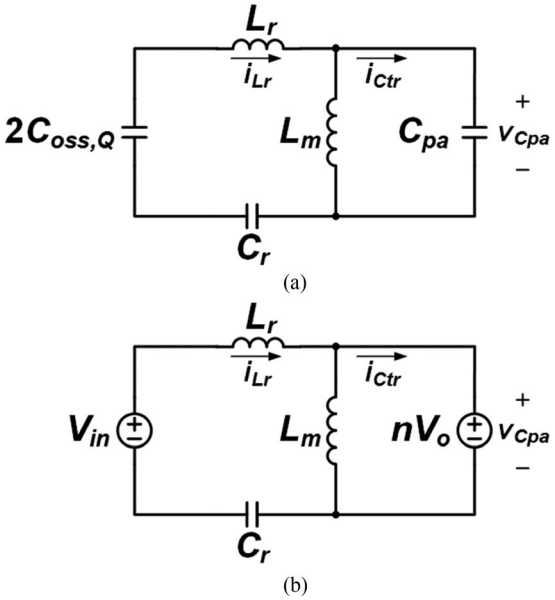


Fig. 6. Equivalent circuit of the resonant elements. (a) When $v_{C\,\mathrm{pa}}$ is clamped. (b) When $v_{C\,\mathrm{pa}}$ is charged.

$v_{C\,\mathrm{pa}}(\Phi_{\mathrm{np}})$ can be described as follows:

$$v_{C\,\mathrm{pa}}\left(\phi_{\mathrm{np}}\right) = nV_o = \frac{I_{\mathrm{Ctr,peak}}}{4\pi f_s C_{\mathrm{pa}}}\left(\cos\phi_{\mathrm{neg}} - \cos\phi_{\mathrm{np}}\right) \tag{3}$$

where $I_{\mathrm{Ctr,peak}}$ is the peak value of i_{Ctr}.

By substituting (3) into (2), $v_{C\mathrm{pa,clamp}(1)}$ can be calculated as follows:

$$v_{C\mathrm{pa,clamp}(1)} = \frac{jI_{\mathrm{Ctr,peak}}}{2\pi^2 f_s C_{\mathrm{pa}}}(\cos\phi_{\mathrm{neg}} - \cos\phi_{\mathrm{np}}) \times (-e^{-j\phi_{\mathrm{np}}} - e^{-j\phi_{\mathrm{neg}}}). \tag{4}$$

Since the operation of charging and discharging of C_{pa} is similar, only the charging operation will be considered. Fig. 6(b) shows the equivalent circuit of the resonant elements when C_{pa} is charged. During this period, both SRs are turned OFF, and $v_{C\mathrm{pa}}$ is changed. By using the similar procedure, the fundamental component of $v_{C\mathrm{pa}}$ when the voltage is charged, $v_{C\mathrm{pa,charge}(1)}$ can be obtained as follows:

$$\begin{aligned} v_{C\mathrm{pa,charge}(1)} &= \frac{2}{\pi}\int_{\phi_{\mathrm{neg}}}^{\phi_{\mathrm{np}}} \left\{ -nV_o \right. \\ &\quad \left. + \frac{I_{\mathrm{Ctr,peak}}}{2\pi f_s C_{\mathrm{pa}}}\left(\cos\phi_{\mathrm{neg}} - \cos\theta\right)\right\} e^{-j\theta}d\theta \\ &= \frac{2nV_o}{j\pi}\phi_A + \frac{I_{\mathrm{Ctr,peak}}}{\pi^2 f_s C_{\mathrm{pa}}}\left\{\frac{\phi_{\mathrm{neg}} - \phi_{\mathrm{np}}}{2}\right. \\ &\quad \left. + j\left(\frac{e^{-2\phi_{\mathrm{neg}}} - e^{-j2\phi_{\mathrm{np}}}}{4} + \phi_A\cos\phi_{\mathrm{neg}}\right)\right\} \end{aligned} \tag{5}$$

where $\Phi_A = \mathrm{e}^{-j\Phi\mathrm{np}} - \mathrm{e}^{-j\Phi\mathrm{neg}}$.

The fundamental component of the voltage across C_{pa}, $v_{C\mathrm{pa}(1)}$ can be calculated by summing (4) and (5). After simplifying the equation, $v_{C\mathrm{pa}(1)}$ is expressed as follows:

$$\begin{aligned} v_{C\mathrm{pa}(1)} = \frac{I_{\mathrm{Ctr,peak}}}{4\pi^2 f_s C_{\mathrm{pa}}}\{&S - 4\sin\phi_{\mathrm{neg}} - 2\left(\phi_{\mathrm{np}} - \phi_{\mathrm{neg}}\right) \\ &+ j\left(C - 4\cos\phi_{\mathrm{neg}} + 2\right)\} \end{aligned} \tag{6}$$

where $S = \sin(2\Phi_{\mathrm{np}}) + \sin(2\Phi_{\mathrm{neg}})$ and $C = \cos(2\Phi_{\mathrm{np}}) + \cos(2\Phi_{\mathrm{neg}})$.

The fundamental component of i_{Ctr}, $i_{\mathrm{Ctr}(1)}$ can also be calculated by the Fourier series analysis, and it is given as follows:

$$i_{\mathrm{Ctr}(1)} = \frac{2}{\pi}\int_0^{\pi} I_{\mathrm{Ctr,peak}}\sin\left(\theta\right)e^{-j\theta}d\theta = -jI_{\mathrm{Ctr,peak}}. \tag{7}$$

From (6) and (7), an equivalent impedance Z_{eq}, which is the combination of the resistive and capacitive impedance, can be obtained as follows:

$$\begin{aligned} Z_{\mathrm{eq}} = \frac{1}{4\pi^2 f_s C_{\mathrm{pa}}}\big[&j\left\{S - 4\sin\phi_{\mathrm{neg}} - 2\left(\phi_{\mathrm{np}} - \phi_{\mathrm{neg}}\right)\right\} \\ &- \left(C - 4\cos\phi_{\mathrm{neg}} + 2\right)\big]. \end{aligned} \tag{8}$$

An equivalent resistor R_{eq} can be modeled as the real term in Z_{eq}, and it can be simplified as follows:

$$R_{\mathrm{eq}} = \frac{\sin^2\phi_{\mathrm{np}} + \sin^2\phi_{\mathrm{neg}} + 2\cos\phi_{\mathrm{neg}} - 2}{2\pi^2 f_s C_{\mathrm{pa}}}. \tag{9}$$

An equivalent capacitance C_{eq} can be derived from the imaginary term in Z_{eq}, and it can be simplified as follows:

$$C_{\mathrm{eq}} = \frac{\pi C_{\mathrm{pa}}}{\left(\phi_{\mathrm{np}} - \phi_{\mathrm{neg}}\right) - \sin\phi_{\mathrm{np}}\cos\phi_{\mathrm{np}} - \sin\phi_{\mathrm{neg}}\cos\phi_{\mathrm{neg}} + 2\sin\phi_{\mathrm{neg}}}. \tag{10}$$

Finally, the equivalent circuit of the *LLC* resonant converter using the proposed control method is shown in Fig. 7. The values of the equivalent passive components are given by (9) and (10).

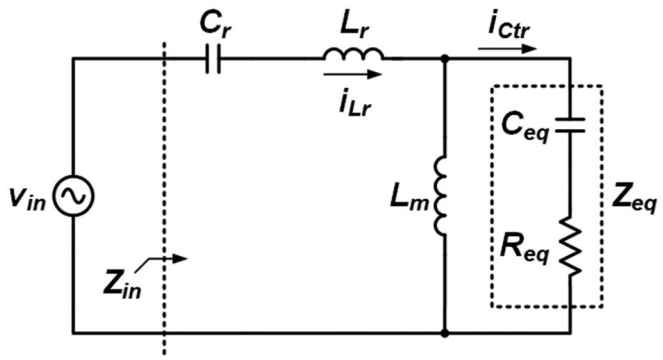


Fig. 7. Equivalent circuit of the *LLC* resonant converter using the proposed control method.

C. Voltage Gain

Voltage gain of the *LLC* resonant converter using the proposed control method can be obtained based on the equivalent circuit presented in Fig. 7. First, an input impedance $Z_{\mathrm{in}}(j\omega_s)$, and the

fundamental components of the input resonant current $i_{Lr(1)}$ can be obtained as follows:

$$Z_{\text{in}}(j\omega_s) = j\omega_s L_r + \frac{1}{j\omega_s C_r} + \frac{j\omega_s L_m \left(R_{\text{eq}} + \frac{1}{j\omega_s C_{\text{eq}}}\right)}{R_{\text{eq}} + j\omega_s L_m + \frac{1}{j\omega_s C_{\text{eq}}}} \tag{11}$$

$$i_{Lr(1)} = \frac{2V_{\text{in}}}{\pi \left|Z_{\text{in}}\left(j\omega_s\right)\right|} \tag{12}$$

where V_{in} is the input voltage, C_r is the resonant capacitance, L_r is the resonant inductance, L_m is the magnetizing inductance, and ω_s is the angular switching frequency.

Relationship between $i_{Lr(1)}$ and $I_{\text{Ctr,peak}}$ is determined by the impedance ratio between L_m and Z_{eq}, and $I_{\text{Ctr,peak}}$ can be solved as follows:

$$I_{\text{Ctr,peak}} = \left|\frac{j\omega_s L_m}{R_{\text{eq}} + 1/\left(j\omega_s C_{\text{eq}}\right) + j\omega_s L_m}\right| i_{Lr(1)}. \tag{13}$$

Under the steady-state conditions, the average output current I_o is the amount of current transfer to the secondary side of the transformer, thus the dashed area in Fig. 5 can be represented as $I_o/2n$. Since the peak value of the current flow into the primary side of the transformer $I_{\text{tr,peak}}$ is the same with $I_{\text{Ctr, peak}}$, I_o can be expressed as follows:

$$\begin{aligned} I_o &= \frac{1}{\pi}\int_{\phi_{\text{np}}}^{\pi+\phi_{\text{neg}}} nI_{\text{tr,peak}} \sin\theta d\theta \\ &= \frac{nI_{\text{Ctr,peak}}\left(\cos\phi_{\text{neg}} + \cos\phi_{\text{np}}\right)}{\pi}. \end{aligned} \tag{14}$$

Using (11)–(14), the voltage gain of the *LLC* resonant converter using the proposed control method M_{prop} is calculated as follows:

$$\begin{aligned} M_{\text{prop}} = \frac{2nR_L I_o}{V_{\text{in}}} &= \frac{4n^2 R_L}{\pi^2}\frac{\left(\cos\phi_{\text{neg}} + \cos\phi_{\text{np}}\right)}{\left|Z_{\text{in}}\left(j\omega_s\right)\right|} \\ &\times \left|\frac{j\omega_s L_m}{R_{\text{eq}} + 1/\left(j\omega_s C_{\text{eq}}\right) + j\omega_s L_m}\right| \end{aligned} \tag{15}$$

where R_L is the load resistance.

Using (15) with $\Phi_{\text{neg}} = 0$, the voltage gain of the *LLC* resonant converter using the conventional control method can be obtained, and the voltage gain according to the load conditions is represented in Fig. 8(a). It is clear that the voltage gain is increased according to the decrease of load conditions. At 5% load and no-load conditions, the voltage gain of the converter cannot reach the required gain due to large C_{pa}. Fig. 8(b) shows the voltage gain of the *LLC* resonant converter according to $t_{\text{neg,max}}$ at no-load conditions when the proposed control method is used. According to the increase of $t_{\text{neg,max}}$, the voltage gain is decreased, and it enables the light-load regulation with low f_s.

III. Design Guideline of Proposed Control Method

When f_s reaches $f_{s,\text{design}}$, the converter starts to operate with the proposed control method. In order to ensure V_o regulation over the entire load conditions, the design for $f_{s,\text{design}}$ is important. Especially, to achieve high efficiency, $f_{s,\text{design}}$ should be as small as possible with ensuring the light-load regulation.

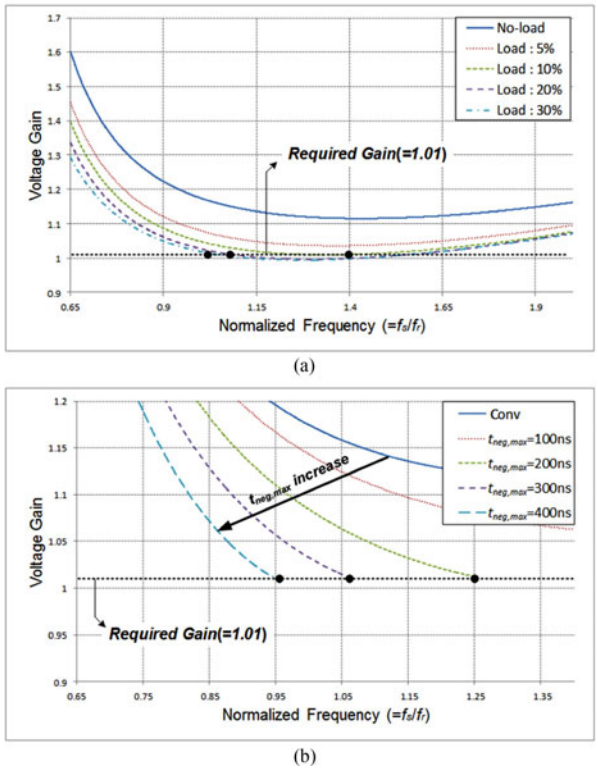


Fig. 8. Voltage gain of the *LLC* resonant converter. (a) According to the load conditions. (b) According to $t_{\text{neg,max}}$ at no-load conditions.

Since the converter has the largest voltage gain at no-load conditions, $f_{s,\text{design}}$ should be designed to regulate V_o at no-load conditions.

Although the negative current flowing through SRs can help to decrease V_o, the voltage gain cannot reach the required gain when the negative current is insufficient. Fig. 9(a) shows that the minimum $t_{\text{neg,max}}$ to regulate V_o is 165 ns, and the voltage gain reaches the required gain when f_s is 815 kHz, which is $f_{s,\text{design}}$. According to the increase of $t_{\text{neg,max}}$, the voltage gain reaches the required gain with lower f_s, and the lower $f_{s,\text{design}}$ can increase efficiency by reducing the switching loss and gate driving loss. However, the negative current flowing through SRs has the maximum value when t_{SR} is the same with the primary switch turn-on time t_Q because t_{SR} cannot be extended more than t_Q. Since t_Q is inversely proportional to f_s, f_s is limited when $t_Q = t_{\text{SR}}$, which is marked as the circles with the dotted line in Fig. 9(a). Moreover, the limited point of f_s is decreased according to the increase of $t_{\text{neg,max}}$, because t_{SR} is increased according to the increase of $t_{\text{neg,max}}$. For example, at $t_{\text{neg,max}} = 450$ ns in Fig. 9(a), the voltage gain cannot satisfy the required gain due to the limited f_s. Therefore, $t_{\text{neg,max}}$ cannot be extended more than 400 ns. As a result, to regulate V_o with the proposed control method, $f_{s,\text{design}}$ can be selected from 530 to 815 kHz. Fig. 9(b) shows the control diagram when $f_{s,\text{design}}$ is 530 and 815 kHz. It is shown that when $f_{s,\text{design}}$ is small, at same load conditions, the converter can operate with the smallest switching loss and gate driving loss. Therefore, $f_{s,\text{design}}$ should be designed as 530 kHz for high efficiency.

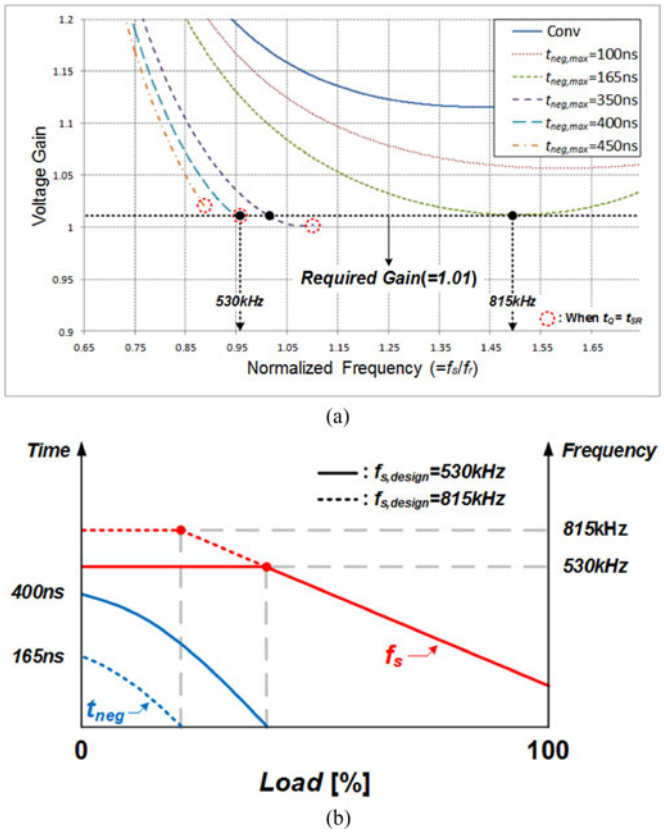


Fig. 9. (a) Design examples of the proposed control method according to $t_{\mathrm{neg,max}}$. (b) Control diagram when $f_{s,\mathrm{design}}$ is 530 and 815 kHz.

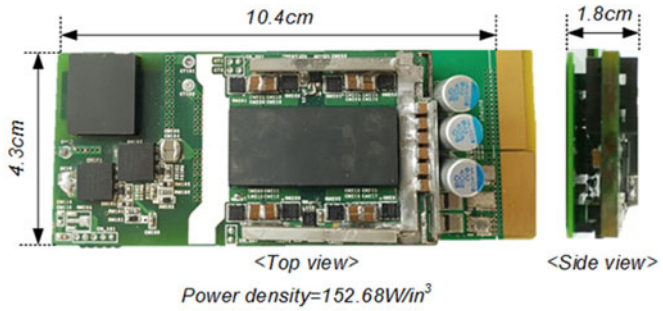


Fig. 10. Prototype of the *LLC* resonant converter with the PT.

TABLE I
COMPONENTS LIST OF PROTOTYPE

Primary switch (Q_1, Q_2)	TPH3208LD (650 V, 20 A)
Synchronous rectifier (SR_1, SR_2)	BSZ034N04LS (40 V, 40 A, 4 in parallel)
Magnetizing inductor (L_m)	30 μH
Resonant inductor (L_r)	6.8 μH
Resonant capacitor (C_r)	12.2 nF
Output capacitor of primary switch ($C_{\mathrm{oss},Q1}$, $C_{\mathrm{oss},Q2}$)	82 pF
Output capacitor of SR ($C_{\mathrm{oss,SR1}}$, $C_{\mathrm{oss,SR2}}$)	900 pF × 4
Parasitic capacitor of PT (C_{trans})	495 pF

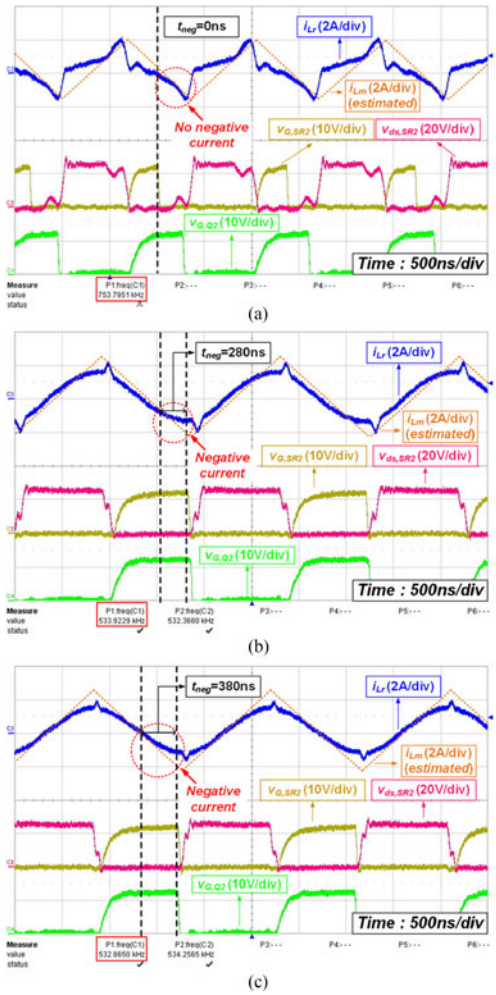
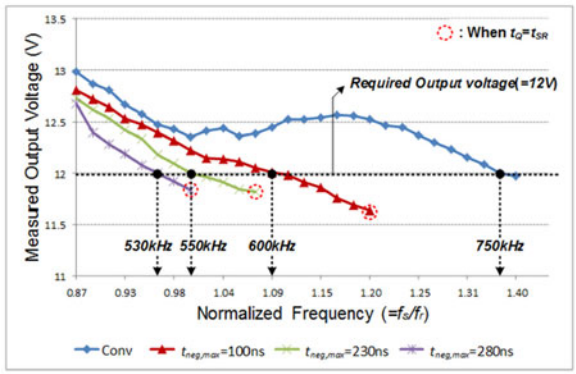


Fig. 11. Experimental waveforms of the *LLC* resonant converter. (a) Using the conventional control method at 10% load conditions. (b) Using the proposed control method at 10% load conditions. (c) Using the proposed control method at no-load conditions.

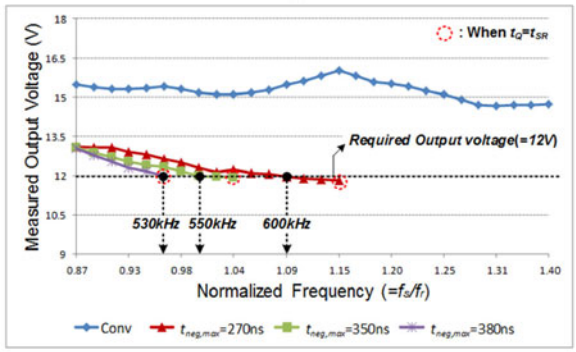
IV. EXPERIMENTAL RESULTS

The proposed control method is implemented with 750 W *LLC* resonant converter with a Texas Instruments digital power controller UCD3138064, as shown in Fig. 10, and the design specification is as follows. Input voltage = 330–380 VDC, output voltage = 12 V, rated output power = 750 W, resonant frequency = 550 kHz, and power density = 152.68 W/in^3. The detailed component list is presented in Table I.

Fig. 11 shows the experimental waveforms of the *LLC* resonant converter under light-load conditions. Fig. 11 shows the experimental waveforms of the *LLC* resonant converter under light-load conditions. Assume the estimated waveform as dotted orange color is the current of L_m. Fig. 11(a) and (b) is different, due to the negative current flowing through SRs. In Fig. 11(a) and (b), V_o can be regulated at 10% load conditions. However, when the proposed control method is utilized, the converter can regulate V_o with smaller f_s compared with the conventional control method. At no-load conditions, as shown in Fig. 11(c), V_o can only be regulated with the proposed control method, and $t_{\mathrm{neg,max}}$ is 380 ns when $f_{s,\mathrm{deisgn}}$ is 530 kHz, which is the simi-



(a)



(b)

Fig. 12. Measured output voltage of the *LLC* resonant converter according to $t_{\mathrm{neg,max}}$. (a) At 10% load conditions. (b) At no-load conditions.

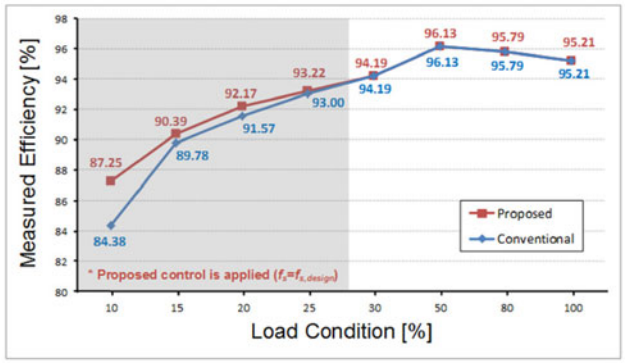


Fig. 13. Measured efficiency of the *LLC* resonant converter.

lar result compared with the theoretical analysis. Fig. 12 shows the measured output voltage of the *LLC* resonant converter according to $t_{\mathrm{neg,\,max}}$. In the conventional control method, V_o can be regulated when f_s is 750 kHz, and efficiency is low due to large switching loss. The proposed control method can regulate V_o with higher efficiency due to the lower f_s by extending t_{neg}. With the conventional control method, V_o is not regulated. However, with the proposed control method, V_o regulation can be achieved. It is clear that the negative current flowing through SRs in the *LLC* resonant converter can improve the light-load regulation capability.

Fig. 13 shows the measured efficiency of the *LLC* resonant converter at nominal input voltage, 380 V. Above 30% load conditions, due to the same operation, efficiency is the same with the conventional and proposed control method. In this paper, f_s reaches $f_{s,\mathrm{design}}$, which is 530 kHz, at 30% load conditions. Therefore, under 30% load conditions, the converter operates with the proposed control method, and efficiency with the proposed control method can be improved by reducing f_s. In the proposed control method, V_o can be regulated by using the negative current flowing through SRs instead of increasing f_s. Although the conduction loss in SRs is slightly increased, high efficiency can be achieved by reducing the switching loss and gate driving loss.

V. Conclusion

This paper proposes the SR control method to solve the light-load regulation problem of the *LLC* resonant converter. Based on the mathematical analysis, the modified ac equivalent circuit model and the voltage gain of the *LLC* resonant converter are presented. When t_{SR} is extended to flow the negative current through SRs, the voltage gain of the *LLC* resonant converter is reduced. Compared with the conventional control method, the proposed control method operates with lower f_s, and it can reduce the switching loss and gate driving loss. Therefore, it can achieve high efficiency under light-load conditions. Moreover, there are no additional components to utilize the proposed control method, and it can achieve high power density. Consequently, the proposed control method is suitable for high output current applications requiring high power density such as server powers and telecommunication applications.

Appendix

According to Fig. 5, $v_{C\mathrm{pa}}$ is divided into two intervals. During the first interval, $v_{C\mathrm{pa}}$ is charged or discharged, and during the second interval $v_{C\mathrm{pa}}$ is clamped, thus $v_{C\mathrm{pa}}$ can be expressed as follows:

$$v_{C\mathrm{pa}}(\theta) = \begin{cases} -nV_o + \frac{I_{\mathrm{Ctr,peak}}}{2\pi f_s C_{\mathrm{pa}}}\left(\cos\phi_{\mathrm{neg}} - \cos\theta\right), & \text{for } \phi_{\mathrm{neg}} \le \theta < \phi_{\mathrm{np}} \\ nV_o, & \text{for } \phi_{\mathrm{np}} \le \theta < \pi + \phi_{\mathrm{neg}}. \end{cases} \tag{A1}$$

According to (14) and (A1), Φ_{np} can be calculated by eliminating $I_{\mathrm{Ctr,peak}}$, and it can be derived as follows:

$$\phi_{\mathrm{np}} = \cos^{-1}\left(\cos\phi_{\mathrm{neg}}\frac{\pi - 2n^2\omega_s R_L C_{\mathrm{pa}}}{\pi + 2n^2\omega_s R_L C_{\mathrm{pa}}}\right). \tag{A2}$$

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Keon-Woo Kim (S'16) received the B.S. and M.S. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015 and 2017, respectively. He is currently working toward the Ph.D. degree at KAIST.

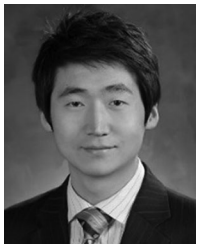
His main research interests include dc/dc converters, analog/digital control, server power system, and high-efficiency converter topologies.

Han-Shin Youn (S'14) received the B.S. degree in electrical engineering from Hanyang University, Seoul, South Korea, in 2009, and the M.S. and Ph.D. degrees in Department of Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea in 2011 and 2017, respectively.

He has worked as a Research Engineer in Hyundai Motor Company, Hwaseong, Korea, since 2017. His main research interests are AC/DC converters, DC/DC converters, drive system, and digital control method.

Jae-Il Baek (S'14) received the B.S. degree in electronics and electrical engineering from Sungkyunkwan University, Suwon, South Korea, in 2007, the M.S. degree from the Department of Electrical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2015. He is currently working toward the Ph.D. degree at KAIST.

His research interests include power electronics, particularly dc/dc converters, ac/dc converters, LED driver, battery chargers, and digital control approach of converters.



Yeonho Jeong (S'13) was born in South Korea, in 1982. He received the B.S. degree in the electronics and electrical engineering from Dankook University, Seoul, South Korea, in 2008, the M.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2014. He is currently working toward the Ph.D. degree at KAIST, Daejeon, South Korea.

From 2008 to 2015, he was a Research Engineer in the Power Advanced Development Group for the server power system in Samsung Electro-Mechanics, Suwon, South Korea. Since 2015, he has been a Senior Research Engineer for developing server power system in Solu-M, Yongin, South Korea. His main research-interests include dc/dc converters, power factor correction ac/dc converters, the sever power supply, and digital control approach for power converters.

Gun-Woo Moon (S'92–M'00) received the M.S. and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 1992 and 1996, respectively.

He is currently a Professor in the Department of Electrical Engineering, KAIST. His research interests include modeling, design and control of power converters, soft-switching power converters, resonant inverters, distributed power systems, power factor correction, electric drive systems, driver circuits of plasma display panels, and flexible ac transmission systems.

Dr. Moon is a member of the Korean Institute of Power Electronics, Korean Institute of Electrical Engineers, Korea Institute of Telematics and Electronics, Korea Institute of Illumination Electronics and Industrial Equipment, and Society for Information Display.