A High-Efficiency Integrated Multimode Battery Charger With an Adaptive Supply Voltage Control Scheme

Pang-Jung Liu, *Member, IEEE* and Lin-Hao Chien

***Abstract*—A high-efficiency multimode battery charger with an adaptive supply voltage (ASV) control scheme is presented in this paper. The proposed battery charger includes a charging circuit and a dc–dc buck converter. The charging circuit automatically switches among trickle current (TC), constant-current (CC), and constant-voltage (CV) modes corresponding to the battery voltage while the buck converter with ASV control generates an ASV to closely track the battery voltage, leading to significant reduction in the power loss of the charging circuit. To further enhance the efficiency of the battery charger, zero-current detection and nonswitching control schemes are employed to decrease the power consumption of the buck converter in TC and CV modes. The battery charger was implemented with a 0.35-μm CMOS 2P4M process. The experimental results are shown to verify the theoretical analysis of the proposed charger. The maximum efficiency of the overall system is 88.3%, and the maximum efficiency improvement between the proposed charger and the conventional linear charger with fixed supply voltage is up to 11.6%.**

***Index Terms*—Adaptive supply voltage (ASV), battery, charger, constant current (CC), constant voltage (CV), dc–dc converter.**

I. Introduction

In recent years, battery-powered portable devices such as smart phones and tablets have been increasingly popular. Lithium-ion (Li-ion) batteries are extensively adopted in portable gadgets due to their high energy density, small size, and low self-discharge [1]–[3]. However, the life cycles of Li-ion batteries are easily affected by the overcharging control and charging method [4], [5]. Thus, the design of a Li-ion battery charger requires the following properties:

1) depending on the remnant charge, the charger should automatically switch to an appropriate charging mode for preventing battery damage and reducing charging time;
2) for maximum energy storage, the charged battery voltage should be as close to the rated voltage as possible without overcharging;
3) the power conversion efficiency of the charger should be as high as possible during the whole charging procedure.

In general, the charging procedure of Li-ion batteries includes trickle current (TC) mode, constant-current (CC) mode, and constant-voltage (CV) mode. TC mode is employed to preclude battery damage with a small charging current when the battery is deeply discharged [2], [6]. To reduce charging time, a large constant charging current is adopted in CC mode. The charging current is continuously decreased in CV mode to achieve a rated voltage and avoid overcharging.

Generally, the charger system can be separated into two categories: switching- or linear-based charger [5]–[14]. The switching-based charger has relatively higher conversion efficiency, but it requires higher component counts and it trades off accuracy for efficiency [11]. In contrast, a linear-based charger has the advantages of compact size, ripple freeness, and high accuracy. However, a linear-based charger suffers considerable power loss when the battery voltage is low. To alleviate this drawback of the linear-based charger, several different approaches for a variable supply voltage had been presented [11], [13], [14]. Fig. 1(a) shows a low dropout (LDO) regulator connected with a charger in series [14]. Although the LDO regulator can be integrated into a chip without discrete components, the power loss of the power transistor $M_{\rm ldo}$ is also appreciable when there is a large voltage difference between the input voltage $V_{\rm in}$ and battery voltage $V_{\rm bat}$. Fig. 1(b) illustrates another method for a variable supply voltage [10]. Through the negative feedback of the operational amplifier $A_{\rm sw}$ and resistance kR, the variable supply voltage $V_{\rm sup,var}$ is equal to $V_{\rm bat}$ plus $V_{\rm const}$. Thus, the voltage value across the power transistor M_p is equal

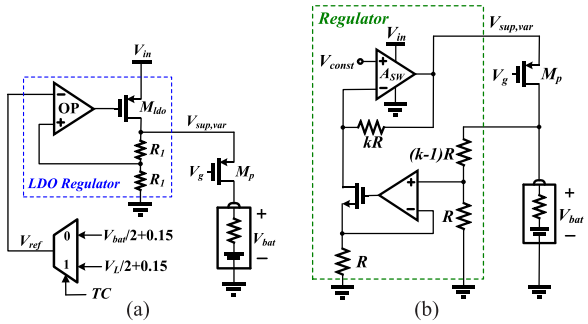

Fig. 1. Conventional variable supply voltage technologies with (a) LDO regulator and (b) operational amplifier.

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to $V_{\rm const}$, so as to significantly reduce power loss on power transistor M_p. However, there is considerable power consumption in the output-stage transistor of the operational amplifier $A_{\rm sw}$ when the voltage difference between voltages $V_{\rm in}$ and $V_{\rm sup,var}$ is large. In [13], Yang *et al.* mentioned a scheme where a dc–dc buck converter could be used to provide a variable supply voltage for enhancing the efficiency of a charger. However, this effective scheme was not implemented in this reference.

To ensure the advantageous high accuracy and ripple freeness of the proposed charger, a compact linear-based charging circuit is presented in this paper. With simple circuitry, the proposed charging circuit realizes TC, CC, and CV modes and automatically switches among operation modes corresponding to the battery voltage. To mitigate the drawback of low charging efficiency under low battery voltage, an adaptive supply voltage (ASV) control scheme is employed. An ASV generated by a dc–dc converter is used as the voltage source for the charging circuit. The ASV tracks and is slightly larger than the battery voltage, so the power loss of the charging circuit is reduced significantly. However, the overall efficiency of the proposed charger is also influenced by the dc–dc converter. Hence, zero-current detection and nonswitching control schemes are presented to reduce the power consumption of the dc–dc converter in TC and CV modes. Furthermore, the battery charger allows charging batteries in series and provides an overcharge protection scheme. After this introduction, the rest of the paper is organized as follows. In Section II, a conventional linear charger with fixed supply voltage is reviewed briefly. Sections III and IV address the proposed charger and its implementation. Section V describes the small-signal analysis of the proposed charger. Finally, experimental results and conclusions are given in Section VI and VII, respectively.

II. Conventional Linear Charger With Fixed Supply Voltage

In this section, a conventional linear charger is reviewed briefly. A linear charger with fixed supply voltage and its conceptual waveforms are shown in Fig. 2. The voltage difference $V_{\rm diff}$ between the supply voltage and the battery voltage can be expressed as

$$V_{\rm diff} = V_{\rm sup,fix} - V_{\rm bat}. \tag{1}$$

Voltage $V_{\rm diff}$ is large when the battery voltage is low. Thus, large power loss is generated by the linear charger under low battery voltage. When the charger starts to charge the battery with different charging currents, voltage $V_{\rm diff}$ decreases continuously with different slopes, leading to smaller power loss of the charger. The power efficiency of the charger with fixed voltage can be formulated as

$$\begin{aligned}\eta_{\rm charger,fix} &= \frac{V_{\rm bat} I_{\rm charge}}{(V_{\rm sulp,fix} - V_{\rm bat})\, I_{\rm charge} + V_{\rm bat} I_{\rm charge} + V_{\rm sulp,fix} I_q} \\ &\approx \frac{V_{\rm bat}}{V_{\rm sulp,fix}}\end{aligned} \tag{2}$$

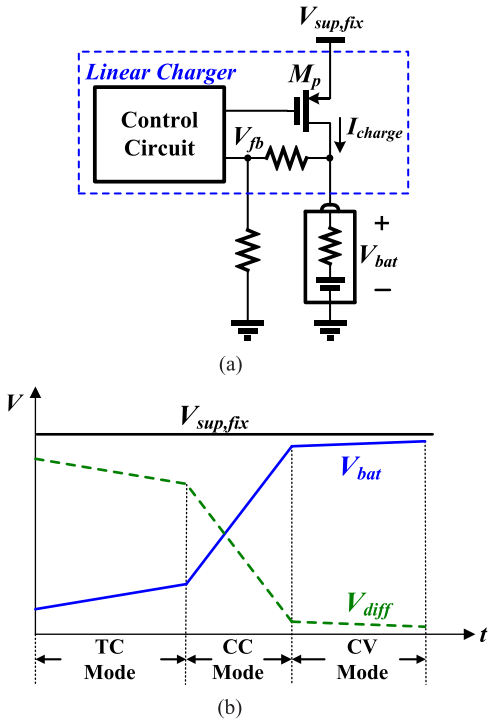

Fig. 2. (a) Conventional linear charger with fixed supply voltage and (b) its conceptual waveforms.

where $I_{\rm charge}$ and I_q are the charging current and the quiescent current of the control circuit, respectively. I_q is always much smaller than $I_{\rm charge}$, so the efficiency of the linear charger is about $V_{\rm bat}/V_{\rm sulp,fix}$. To reduce power loss of the linear charger during the whole charging procedure, the supply voltage should track and be slightly larger than the battery voltage.

III. Integrated Battery Charger With ASV Control Scheme

A. Concept of ASV Control Scheme

The system block diagram of the proposed charger integrated circuit is shown in Fig. 3(a). The battery charger includes a charging circuit and a dc–dc switching converter. The charging circuit provides TC, CC, and CV charging modes and automatically switches among different operation modes depending on the battery voltage. To enhance the power efficiency of charging circuit during the whole charging procedure, a dc–dc switching converter is employed. By using the information of battery voltage $V_{\rm bat}$, the dc–dc converter generates an ASV $V_{\rm sup,asv}$ for the charging circuit. The ASV $V_{\rm sulp,asv}$ follows and is slightly higher than the battery voltage, leading to high power efficiency of the charging circuit for the entire charging procedure based on (2). The conceptual waveforms of the charger with ASV control are illustrated in Fig. 3(b). It is noted that the voltage difference $V_{\rm diff}$ between supply voltage $V_{\rm sup,asv}$ and battery voltage $V_{\rm bat}$ is larger at the beginning of the charging procedure because the charging circuit requires a minimum supply voltage for normal operation. Voltage difference $V_{\rm diff}$ continues decreasing in TC mode. Nevertheless, the overall efficiency of the proposed

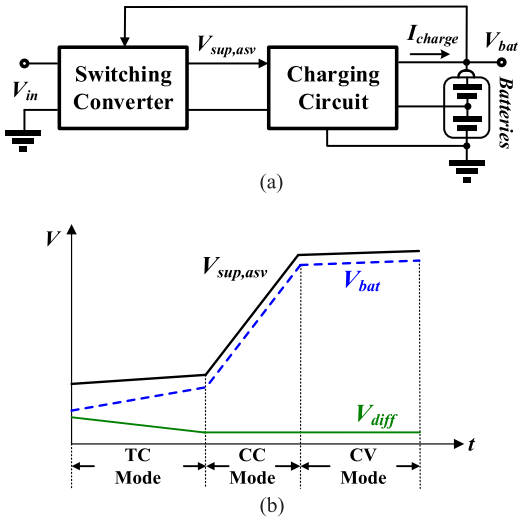

Fig. 3. (a) Multimode battery charger with ASV control and (b) its conceptual waveforms.

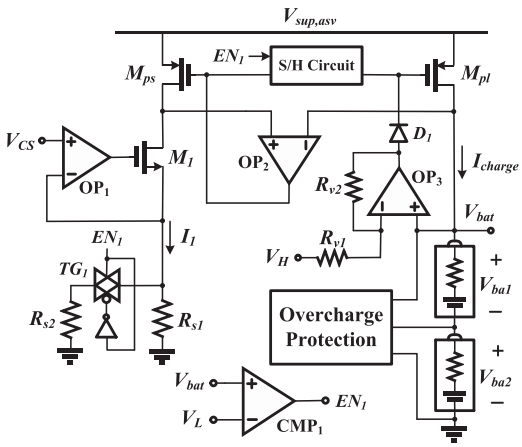

Fig. 4. Schematic diagram of the proposed charging circuit.

charger is also influenced by the switching converter, and it can be written as

$$\eta_{\text{charger,ASV}} = \eta_{\text{charging}} \times \eta_{\text{switch}} \approx \frac{V_{\text{bat}}}{V_{\text{dc,avs}}} \times \eta_{\text{switch}}. \quad (3)$$

Thus, the efficiency of the dc–dc converter should be maintained as high as possible. Hence, zero-current detection and nonswitching control schemes are adopted to reduce power loss of the dc–dc converter in TC and CV modes, respectively.

B. Multimode Battery Charging Circuit

The charging circuit with overcharge protection is shown in Fig. 4. The current loop is regulated by operational amplifiers OP_1 and OP_2 while the voltage loop is regulated by operational amplifier OP_3. At the start of the charging procedure, when battery voltage V_{bat} is lower than a predefined voltage V_L, transmission gate TG_1 is turned OFF. Furthermore, diode D_1 is turned OFF due to low battery voltage. Thus, the voltage loop does not influence the charging current. When the charging circuit operates in TC mode, a negative feedback loop is established by operational amplifier OP_1 and transistor M_1, so current I_1 is equal to V_{CS}/R_{s1}. Through a current mirror composed of transistors M_{ps} and M_{pl}, the charging current I_{charge} is enlarged to be 1000 times of I_1 and then charges the two batteries in series. Operational amplifier OP_2 and transistor M_{ps} force the drain voltages of transistors M_{ps} and M_{pl} to be identical, so as to enhance the accuracy of the charging current.

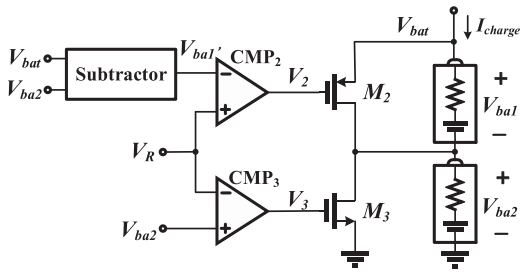

Fig. 5. Schematic diagram of the overcharge protection circuit.

Once the charging procedure enters CC mode, transmission gate TG_1 is turned ON, and then resistors R_{s1} and R_{s2} are in parallel. It results in larger current I_1 and charging current I_{charge}. It is possible to produce a current spike in current I_1 during the turn-on transition of the transmission gate. After passing through the current mirror, the charging current could damage batteries. To preclude this issue, a sample-and-hold (S/H) circuit is used. The charging circuit switches to CV mode when the battery voltage approaches a predefined voltage V_H. In CV mode, the output voltage of operational amplifier OP_3 is high enough to turn ON diode D_1 to charge the parasitic capacitance at the gate terminal of power transistor M_{pl}. It leads to a gradually decreasing the charging current. Therefore, TC, CC, and CV charging modes can be realized with simple circuitry.

Even though the two batteries are charged with the same current, the required charging times of the two batteries are different due to different battery parameters. Thus, an overcharge protection circuit is required as shown in Fig. 5. By subtracting voltage V_{ba2} from voltage V_{bat}, the information of voltage V_{ba1} can be obtained. Two comparators CMP_2 and CMP_3 are used to determine whether the two battery voltages reach the rated voltage V_R or not. Before the two battery voltages approach the rated voltage, transistors M_2 and M_3 are turned OFF. Assuming voltage V_{ba1} reaches V_R first, voltage V_2 is pulled down to a low level. Thus, transistor M_2 is turned ON and charging current I_{charge} follows through M_2 and then delivers energy to battery 2. On the other hand, the charging current provides energy for battery 1 through transistor M_3. Hence, the overcharge protection of the two batteries can be achieved.

C. DC–DC Converter With ASV and Nonswitching Operation Mode Controls

The schematic diagram of the dc–dc buck converter with ASV and nonswitching control schemes is shown in Fig. 6. To achieve the ASV control, the battery voltage V_{bat} and a reference signal V_{ref} are added with different weightings by a reference adder. Thus, an adaptive reference signal $V_{\text{ref,asv}}$ is generated. $V_{\text{ref,asv}}$

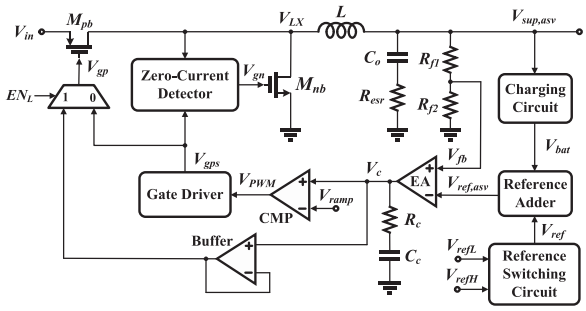

Fig. 6. Schematic diagram of dc–dc converter with ASV and nonswitching controls.

is connected to the inverting input of the error amplifier, resulting in a varying duty cycle value and the ASV $V_{\mathrm{sup,asv}}$. Based on ASV control, supply voltage $V_{\mathrm{sup,asv}}$ should be slightly higher than battery voltage V_{bat}, but the supply voltage must also be higher than a minimum voltage level for ensuring good operation of the charging circuit. Furthermore, the rising slopes of $V_{\mathrm{sup,asv}}$ in TC and CC modes are different because distinct charging currents are applied. Therefore, two reference signals V_{refL} and V_{refH} are used. Signal V_{refL} is for low battery voltage, and signal V_{refH} is adopted when the charging circuit enters CC mode. The reference switching circuit is employed to switch between the two reference signals for preventing overshoot and ringing issues of the ASV.

When the charging circuit is in TC mode, since the buck converter provides a few tens mA, the inductor current could become negative, leading to additional power loss. To alleviate this issue, a zero-current detector is used to turn OFF power transistor M_{nb} to prevent output capacitor C_o from discharging energy. When the battery voltage V_{bat} is charged up to a high level, the voltage across power transistor M_{pl} of the charging circuit is reduced significantly. Thus, if the buck converter still uses a switching operation control, the overall efficiency of the proposed charger would be lower than that of the conventional linear charger. Furthermore, the charging time in CV mode occupies a notable portion of the total charging time [8]. Under the considerations, a nonswitching operation control is adopted to keep power transistor M_{pb} ON and power transistor M_{nb} OFF. Since signal EN_{L} is in the high state, the value of gate voltage V_{gp} is determined by the error amplifier EA. On the other hand, gate voltage V_{gn} is maintained at zero level because the V_c level is always larger than the amplitude of ramp signal V_{ramp}. By using the zero-current detector and nonswitching operation control, the efficiency of the buck converter can be kept as high as possible, so can the efficiency of the battery charger.

IV. Circuit Implementation

To realize the battery charger with ASV, a reference switching circuit, a reference adder, and a zero-current detector are utilized. Detailed circuit-level implementations of these function blocks are described in this section.

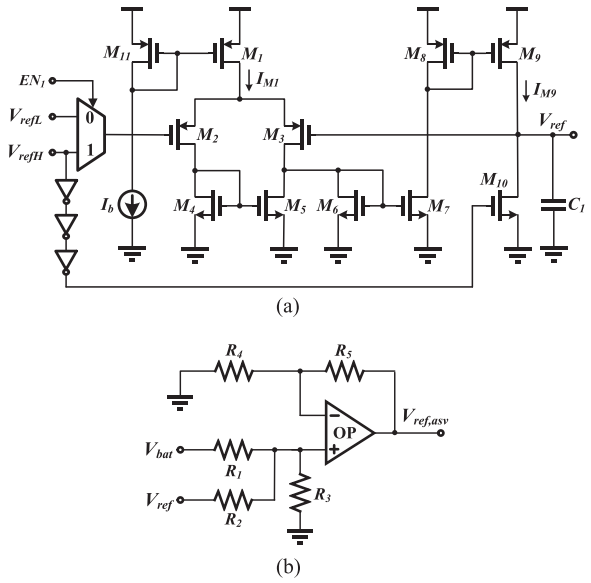

Fig. 7. Schematic diagram of (a) reference switching circuit and (b) reference adder.

A. Reference Switching Circuit and Reference Adder

The schematic diagram of the reference switching circuit shown in Fig. 7(a) is used to prevent overshoot and ringing in the ASV during the start-up period and the interchanging transition between the two reference signals. Before the buck converter is in operation, signal $V_{\mathrm{ref}H}$ should be at about zero value, so that transistor M_{10} is turned ON to discharge capacitor C_1. This action makes sure the reference voltage V_{ref} is reset from zero before the start-up process. After the buck converter is powered ON, $V_{\mathrm{ref}H}$ is changed to the predefined value. Signal $V_{\mathrm{ref}L}$ is connected to the gate of transistor M_2 when the battery voltage is lower than V_L. Then, most of current I_{M1} flows through transistors M_3 and M_5, resulting in the rising drain voltage of M_6. Subsequently, current I_{M9} charges capacitor C_1, so that the reference voltage V_{ref} increases linearly and slowly until V_{ref} approaches $V_{\mathrm{ref}L}$, then current I_{M9} becomes zero and the charging stops. When the charging circuit enters CC mode, the gate of transistor M_2 is connected to $V_{\mathrm{ref}H}$. Similarly, reference voltage V_{ref} will be charged to $V_{\mathrm{ref}H}$ slowly. The reference adder shown in Fig. 7(b) is a noninverting amplifier with two input signals V_{ref} and V_{bat}. The adaptive reference signal $V_{\mathrm{ref,asv}}$ can be calculated as

$$V_{\mathrm{ref,avs}} = \frac{R_1\left(R_2+R_3\right)\left(R_4+R_5\right)}{R_1R_4\left(R_2+R_3\right)+R_2R_3R_4}V_{\mathrm{bat}} + \frac{R_2\left(R_1+R_3\right)\left(R_4+R_5\right)}{R_2R_4\left(R_1+R_3\right)+R_1R_3R_4}V_{\mathrm{ref}}. \quad (4)$$

Hence, the ASV is influenced by the battery voltage and reference voltage.

B. Zero-Current Detector

Since no current sensor is used in the buck converter, signal V_{LX} is adopted to realize the zero-current detector, as shown in

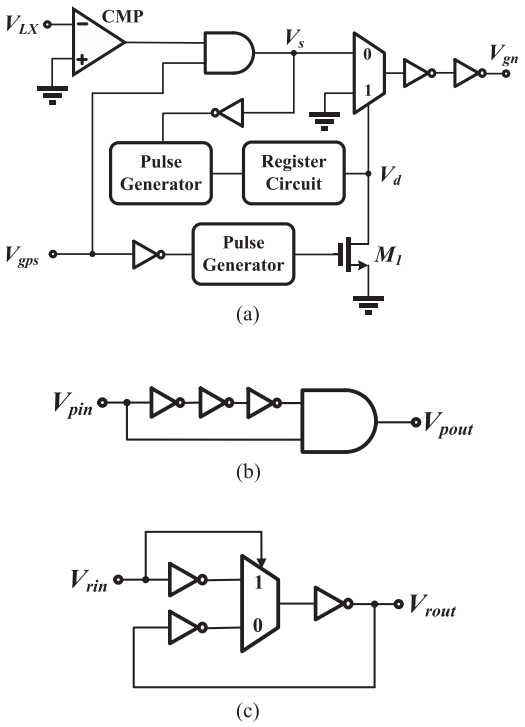

Fig. 8. (a) Zero-current detector block diagram, (b) pulse generator, and (c) register circuit.

Fig. 8(a). When the driving signal $V_{\rm gps}$ changes to a low state, after passing through an inverter and a pulse generator, as shown in Fig. 8(b), a pulse signal is produced to turn ON transistor M_1. It results in the zero level of signal V_d. Meanwhile, signal V_s is at a low state due to the low level of $V_{\rm gps}$. Once the power transistor M_{pb} is turned OFF and the inductor current flows through the body diode of power transistor M_{nb}, signal V_s becomes at a high level which turns ON power transistor M_{nb}. Subsequently, the inductor current passes through power transistor M_{nb} and decreases continuously. When the inductor current becomes negative, signal V_{LX} is larger than zero which turns OFF power transistor M_{nb} due to the low state of signal V_s. However, signal V_{LX} will suffer ringing while the inductor current is back to zero, and thus power transistor M_{nb} will be turned ON again, leading to additional power loss. To prevent this issue, a pulse generator and register circuit are employed to maintain the status of V_d. When V_s switches to a low level, a pulse is sent to the register circuit. V_d changes to a high state when the input signal of the register circuit shown in Fig. 8(c) is at a high level. The output signal of the register circuit is kept in the previous state when its input signal becomes zero. In other words, by using the register circuit, V_d is maintained at a high level once V_s becomes in a low state. Thus, the gate driving signal V_{gn} is kept at zero level. The V_d state changes to a low level when the driving signal $V_{\rm gps}$ becomes at a low state. Then, the operation of the zero-current detector will repeat again.

C. *Operational Amplifier* $\rm OP_2$ *of the Charging Circuit*

Operational amplifier $\rm OP_2$ used in the charging circuit is shown in Fig. 9 [15]. Since the battery voltage is charged from a low level to a high level, operational amplifier $\rm OP_2$ should operate well given a large range of input signals. Thus, to maintain the accuracy of the charging current, n- and p-type differential pairs are adopted in $\rm OP_2$ to realize a full range of input swing. Moreover, a folded cascade architecture composed of transistors M_3 to M_{12} is used to enhance voltage gain.

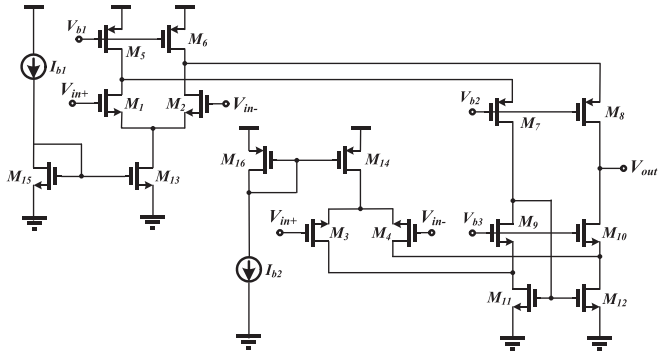

Fig. 9. Schematic diagram of operational amplifier $\rm OP_2$.

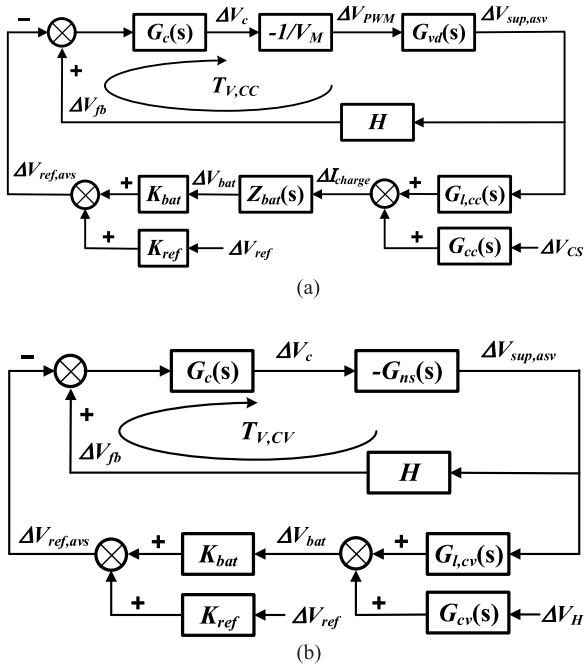

Fig. 10. Small-signal block diagram of the battery charger operating in (a) CC and (b) CV modes.

V. Small-Signal Analysis of the Proposed Charger

Fig. 10(a) shows the small-signal block diagram of the proposed charger operating in CC mode for analyzing the system stability and ASV effect. Block $G_{vd}(s)$ is the duty cycle-to-ASV transfer function when the buck converter operates in CCM operation, and it can be expressed as [16]

$$G_{vd}(s) = V_{\rm in}\frac{1 + sC_oR_{esr}}{1 + s\left(C_oR_{esr} + L/R_L\right) + s^2LC_o} \tag{5}$$

where R_L is the equivalent input resistance of the charging circuit. V_M is the amplitude of ramp signal $V_{\rm ramp}$ and

H is determined by the feedback resistors and is equal to $R_{f2}/(R_{f1}+R_{f2})$. $G_c(s)$ is the transfer function of the error amplifier and can be derived as

$$G_c(s) = G_m R_o \frac{1+sC_cR_c}{1+sC_c(R_o+R_c)} \tag{6}$$

where G_m and R_o are the transconductance and output resistance of the error amplifier, respectively. Thus, the voltage loop gain $T_{V,\mathrm{CC}}(s)$ can be formulated as

$$T_{V,\mathrm{CC}}(s) = HG_c(s)G_{vd}(s)/V_M. \tag{7}$$

$G_{l,\mathrm{cc}}(s)$ is the ASV-to-charging current transfer function when the charging circuit operates in CC operation, and it can be written as

$$G_{l,\mathrm{cc}}(s) = \frac{g_{m,pl}}{1+A_{v,\mathrm{op2}}(g_{m,ps}r_{o,ps})} \frac{1}{1+sC_{g,ps}R_{o,\mathrm{op2}}} \tag{8}$$

where $g_{m,pl}$ is the transconductance of power transistor M_{pl} in the charging circuit and $A_{v,\mathrm{op2}}$ is the voltage gain of operational amplifier OP_2. $g_{m,ps}$ and $r_{o,ps}$ are the transconductance and output resistance of transistor M_{ps}, respectively. $C_{g,ps}$ is the gate capacitance of M_{ps} and $R_{o,\mathrm{op2}}$ is the output resistance of OP_2. Due to the feedback loop, the distribution of the ASV can be reduced significantly. Block $Z_{\mathrm{bat}}(s)$ is the impedance of the two batteries in series. $G_{\mathrm{cc}}(s)$ is the reference voltage-to-charging current transfer function when the charging circuit is in CC operation, and it can be formulated as

$$G_{\mathrm{cc}}(s) = \frac{1000\cdot V_{CS}}{(R_{s1}\parallel R_{s2})} \frac{1}{1+sC_{g,ps}R_{o,\mathrm{op2}}}. \tag{9}$$

Blocks K_{bat} and K_{ref} in Fig. 10(a) are the voltage gains of the reference adder corresponding to V_{bat} and V_{ref}. According to (4), K_{bat} and K_{ref} can be expressed as

$$K_{\mathrm{bat}} = \frac{R_1(R_2+R_3)(R_4+R_5)}{R_1R_4(R_2+R_3)+R_2R_3R_4} \tag{10}$$

$$K_{\mathrm{ref}} = \frac{R_2(R_1+R_3)(R_4+R_5)}{R_2R_4(R_1+R_3)+R_1R_3R_4}. \tag{11}$$

The influence on the ASV corresponding to the variation of battery voltage ΔV_{bat} is calculated as

$$\frac{\Delta V_{\mathrm{sup,asv}}}{\Delta V_{\mathrm{bat}}} = \frac{K_{\mathrm{bat}}}{H} \frac{1}{1+1/T_{V,\mathrm{CC}}(s)} \approx \frac{K_{\mathrm{bat}}}{H}. \tag{12}$$

Since the dc gain of $T_{V,\mathrm{CC}}(s)$ is always larger than 1, the ASV accurately follows the battery voltage multiplied by K_{bat}/H. Similarly, Fig. 10(b) shows the small-signal block diagram of the proposed charger operating in CV mode. Block $G_{ns}(s)$ is the gate driving signal-to-ASV transfer function when the buck converter operates with nonswitching control, and it is shown as

$$G_{ns}(s) = \frac{[R_L\parallel(1/sC_o+R_{esr})\parallel(R_{f1}+R_{f2})]}{r_{o,pb}+sL+[R_L\parallel(1/sC_o+R_{esr})\parallel(R_{f1}+R_{f2})]} \times \frac{1}{1+SC_{g,pb}R_{o,\mathrm{buf}}} \tag{13}$$

where $r_{o,pb}$ and $C_{g,pb}$ are the on-resistance and gate capacitance of power transistor M_{pb}, respectively, in the buck converter.

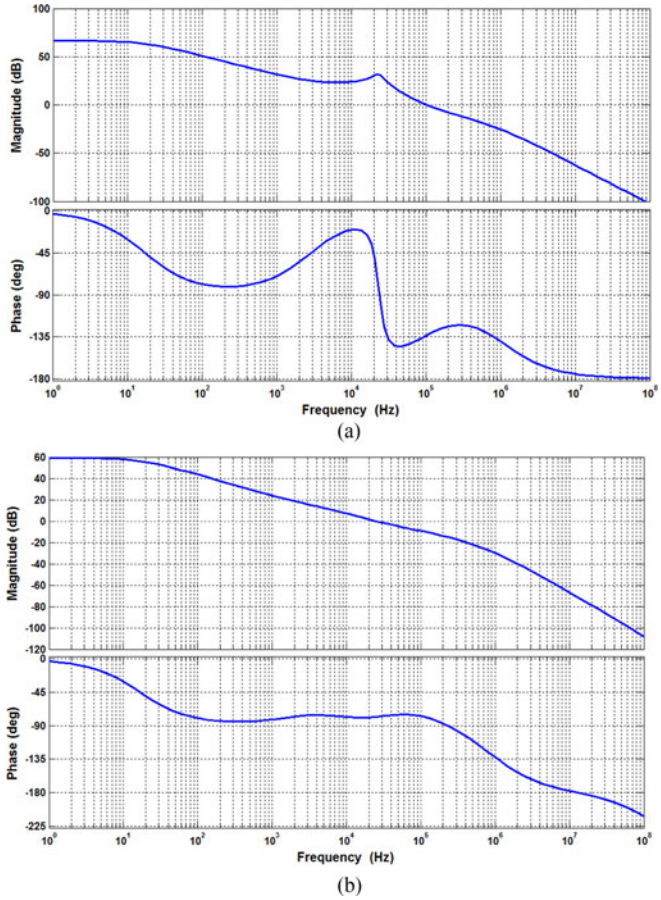

Fig. 11. Bode plots of the voltage loop gains TV,CC(s) and TV,CV(s) when buck converter operates in (a) CC and (b) CV modes.

$R_{o,\mathrm{buf}}$ is the output resistance of unit-gain buffer. Thus, the voltage loop gain $T_{V,\mathrm{CV}}(s)$ can be expressed as

$$T_{V,\mathrm{CV}}(s) = HG_c(s)G_{ns}(s). \tag{14}$$

Blocks $G_{l,\mathrm{cv}}(s)$ and $G_{\mathrm{cv}}(s)$ are the ASV-to-battery voltage transfer function and reference voltage-to-battery voltage transfer function, respectively, when the charging circuit is in CV mode, and they can be formulated as

$$G_{l,\mathrm{cv}}(s) \approx \frac{1}{1+(R_{v2}/R_{v1})} \frac{1}{1+s/p_{\mathrm{op3}}} \tag{15}$$

$$G_{\mathrm{cv}}(s) \approx \frac{1}{1+(R_{v1}/R_{v2})} \frac{1}{1+s/p_{\mathrm{op3}}} \tag{16}$$

where p_{op3} is the internal pole of OP_3. Fig. 11 shows Bode plots of the voltage loop gains $T_{V,\mathrm{CC}}(s)$ and $T_{V,\mathrm{CV}}(s)$ when the buck converter operates in CC and CV modes, where the design parameters are shown in Section VI. The phase margin is over 46° for CC and CV modes, and the Bode plot results assure us of stable operation of the buck converter due to the adequate phase margin.

VI. Experimental Results

In order to verify the circuit validity, an experimental prototype of the proposed charger was designed with an input voltage of 5.8–6.5 V, ASV of 0.2–5.7 V, maximum charging current of

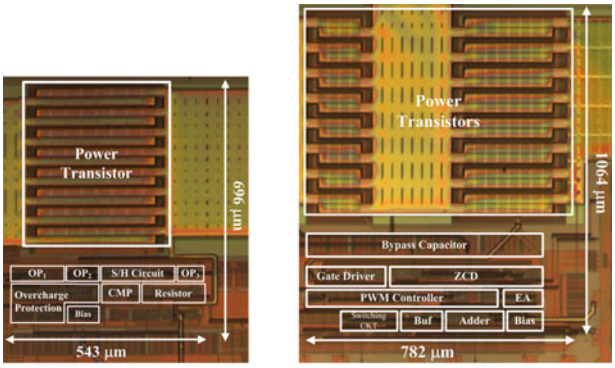

Fig. 12. Chip microphotographs of (a) charging circuit and (b) buck converter.

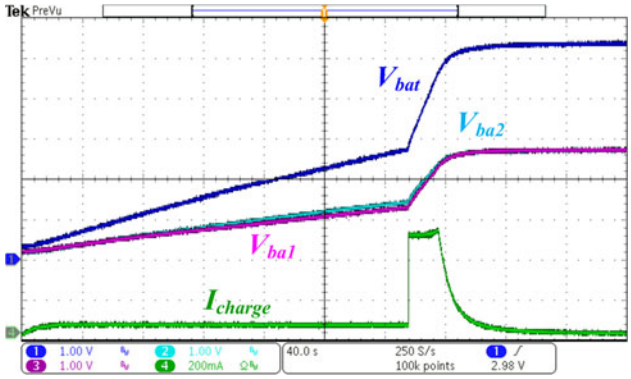

Fig. 13. Measured waveforms of the charging circuit supplied by the buck converter.

500 mA, and switching frequency of 1 MHz. The output capacitance and inductance were 10 μF and 4.7 μH, respectively. The battery charger was fabricated in a 0.35-μm CMOS process. The chip microphotographs of the charging circuit and buck converter are shown in Fig. 12 and their active areas are $543 \times 696\ \mu\mathrm{m}^2$ and $782 \times 1064\ \mu\mathrm{m}^2$. To shorten the time for testing chip functionality, two super capacitors are used as the batteries. The parameters of the super capacitor are capacitance of 10 F, rated voltage of 2.7 V, and internal resistance of 30 mΩ.

Fig. 13 shows the measured waveforms of the charging circuit supplied by the buck converter. The four waveforms in the figure from top to bottom are the battery voltage V_{bat}, voltages V_{ba1} and V_{ba2} of the two batteries, and charging current I_{charge}. Before testing, the battery voltage is discharged to around zero, so the charging circuit is in TC mode. Thus, the charging current of 50 mA is adopted and the battery voltages increase slowly. The charging current changes to 500 mA when the charging circuit enters CC mode, and then the battery voltage rises quickly. The charging circuit switches to CV mode when the battery voltage approaches the rated voltage, and then the charging current continuously decreases to zero. Fig. 14 shows the experimental waveforms of the charging circuit with different initial voltages of the two batteries for testing the overcharge protection circuit. We can clearly find that the higher battery voltage is maintained constant while the lower battery voltage continues charging until the two battery voltages are the same.

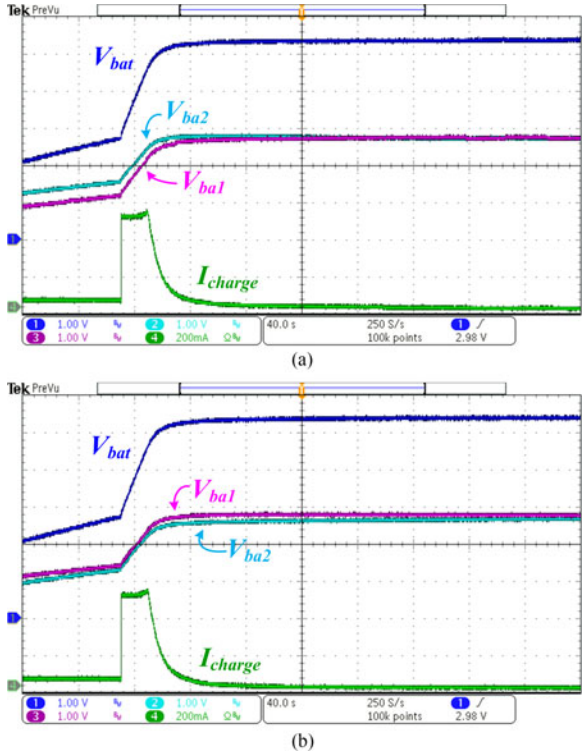

Fig. 14. Measured waveforms of the charging circuit with different initial voltages of the two batteries for (a) $V_{ba1} < V_{ba2}$ and (b) $V_{ba1} > V_{ba2}$.

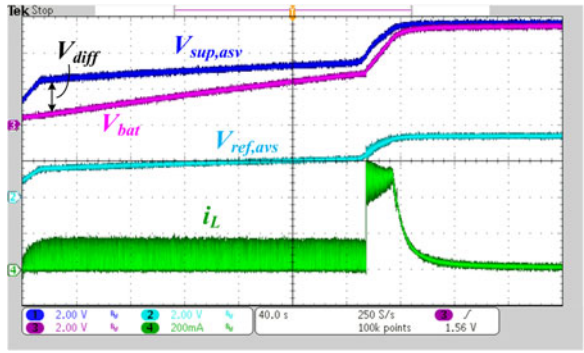

Fig. 15. Waveforms of the proposed charger.

Fig. 15 shows the waveforms of the proposed charger. The four waveforms in the figure from top to bottom are the ASV $V_{\mathrm{sup,avs}}$, battery voltage V_{bat}, adaptive reference voltage $V_{\mathrm{ref,asv}}$, and inductor current i_L. Adaptive reference voltage $V_{\mathrm{ref,asv}}$ increases from zero linearly to prevent supply voltage $V_{\mathrm{sup,asv}}$ from overshoot and inrush current during the start-up period. In TC mode, $V_{\mathrm{ref,asv}}$ rises slowly, so does the ASV. It is noted that the battery voltage starts form about zero. Since the charging circuit requires a minimum supply voltage for normal operation, voltage difference V_{diff} between $V_{\mathrm{sup,asv}}$ and V_{bat} is larger at the beginning of the charging procedure. V_{diff} continues decreasing in TC mode. Thanks to zero current detection, inductor current i_L is always larger than zero for power saving. When the charging circuit enters CC mode, the charging current becomes 500 mA, so the dc value of the inductor current also changes to 500 mA. Since $V_{\mathrm{sup,asv}}$ increases quickly, the in-

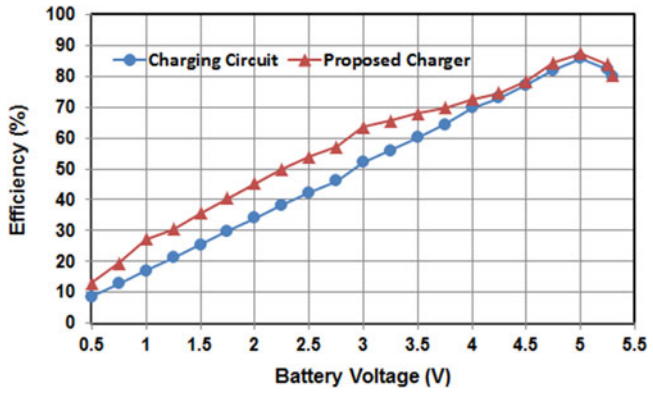

Fig. 16. Measured efficiencies of the proposed charger and charging circuit with a fixed supply voltage of 5.8 V.

ductor current ripple decreases rapidly. Moreover, $V_{\rm diff}$ is almost maintained constant. In CV mode, the buck converter operates with nonswitching mode while the inductor current becomes a stable value instead of a varying range. Voltage $V_{\rm sup,asv}$ is kept fixed, and then the inductor current decreases toward zero when the battery voltage approaches the rated voltage. It is noted that the time scale of Figs. 13 to 15 is 40 s. Fig. 16 illustrates the measured efficiencies of the proposed charger and the charging circuit with a fixed supply voltage of 5.8 V with respect to the battery voltage. The efficiency of the proposed charger is higher than that of the charging circuit and the maximum efficiency difference is up to 11.6%. It is noted that larger voltage difference between the input voltage and battery rated voltage leads to better efficiency improvement of the proposed charger.

VII. Conclusion

In this paper, an integrated battery charger composed of a charging circuit and a dc–dc buck converter with ASV control is presented. The charging circuit realizes a highly accurate and ripple-free charging current and automatically switches among TC, CC, and CV modes. The buck converter with ASV control generates an ASV to reduce redundant power loss on the charging circuit. Furthermore, nonswitching and zero current detection control schemes are adopted to reduce power loss of the dc–dc converter in CV and TC modes. The experimental results demonstrate that the theoretical analysis of the proposed charger can be verified. The maximum efficiency of the battery charger is 88.3% and the maximum efficiency improvement between the proposed charger and the charging circuit with fixed supply voltage is up to 11.6%.

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References

[1] L.-R. Chen, S.-L. Wu, D.-T. Shieh, and T.-R. Chen, "Sinusoidal-ripple current charging strategy and optimal charging frequency study for Li-ion batteries," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 88–97, Jan. 2013.

[2] K. Tae-Hoon *et al.*, "Analytical study on low-frequency ripple effect of battery charging," in *Proc. Veh. Power Propulsion Conf.*, Oct. 2012, pp. 809–811.

[3] C.-S. Lim, K.-J. Lee, N.-J. Ku, D.-S. Hyun, and R.-Y. Kim, "Dual active bridge-based battery charger for plug-in hybrid electric vehicle with charging current containing low frequency ripple," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7299–7307, Dec. 2015.

[4] M. J. Isaacson, R. P. Hollandsorth, P. J. Giampaoli, F. A. Linkowaky, A. Salim, and V. L. Teofilo, "Advanced lithium ion battery charger," in *Proc. 15th Annu. Battery Conf. Appl. Adv.*, Jan. 2000, pp. 193–198.

[5] C.-H. Lin, C.-Y. Hsieh, and K.-H. Chen, "Li-ion battery charger with smooth control circuit and built-in resistance compensator for achieving stable and fast charging," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 2, pp. 506–517, Apr. 2010.

[6] Y.-S. Hwang, S.-C. Wang, F.-C. Yang, and J.-J. Chen, "New compact CMOS Li-ion battery charger using charge-pump techniques for portable applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 4, pp. 705–712, Apr. 2007.

[7] C.-C. Tsai, C.-Y. Lin, Y.-S. Hwang, W.-T. Lee, and T. -Y. Lee, "A multimode LDO-based Li-ion battery charger in 0.35 μm CMOS technology," in *Proc. IEEE Asia-Pac. Conf. Circuits Syst.*, 2004, pp. 49–52.

[8] P.-J. Liu and C.-H. Yen, "A fast-charging switching-based charger with adaptive hybrid duty cycle control for multiple batteries," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1975–1983, Mar. 2017.

[9] G. J. M. de Sousa, C. M. T. Cruz, C. G. C. Branco, L. D. S. Bezerra, and R. P. Torrico-Bascope, "A low cost flyback-based high power factor battery charger for UPS applications," in *Proc. IEEE Brazilian Power Electron. Conf.*, 2009, pp. 783–790.

[10] M.-G. Jeong, S.-H. Kim, and C. Yoo, "Switching battery charger integrated circuit for mobile devices in a 130-nm BCDMOS process," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7943–7952, Nov. 2016.

[11] M. Chen and G. A. R. Rincon-Mora, "Accurate, compact, power efficient Li-ion battery charger circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1180–1184, Nov. 2006.

[12] Y. J. Moon, Y. S. Roh, and C. Yoo, "A 3.0-W wireless power receiver circuit with 75% overall efficiency," in *Proc. IEEE Asian Solid-State Circuit Conf.*, Nov. 2012, pp. 97–100.

[13] S.-H. Yang, J.-W. Liu, and C.-C. Wang, "A single-chip 60-V bulk charger for series Li-ion batteries with smooth charge-mode transition," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 7, pp. 1588–1597, Jul. 2012.

[14] P. H. V. Quang, T. T. Ha, and J.-W. Lee, "A fully integrated multimode wireless power charger IC with adaptive supply control and built-in resistance compensation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 1251–1260, Feb. 2015.

[15] W. Sansen, *Analog Design Essentials*. Berlin, Germany: Springer, 2006.

[16] E. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA, USA: Kluwer, 2001.

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