Synthesis and Comparative Analysis of Very High Step-Up DC–DC Converters Adopting Coupled-Inductor and Voltage Multiplier Cells

António Manuel Santos Spencer Andrade, *Student Member, IEEE*, Everson Mattos, *Student Member, IEEE*, Luciano Schuch, *Member, IEEE*, Hélio Leães Hey, *Member, IEEE*, and Mario Lúcio da Silva Martins, *Member, IEEE*

***Abstract*—A synthesis methodology for developing a set of very high step-up dc–dc converters is presented and discussed in this paper. The proposed method makes use of a boost converter as basic topology in which three step-up techniques are combined and incorporated. The studied techniques are the switched capacitors voltage multipliers (VM), the diode VMs, and the coupled-inductors. With the proposed methodology, many well-known converters are identified and two novel converters are proposed. In addition to a detailed analysis of the synthesis of each topology, a comparative analysis among of some important converters is presented. This comparison involves aspects such as voltage gain, voltage stress, component stress factor, component count, and relative cost. By means of these comparisons, the main characteristics and constraints of the analyzed converters are identified. Results from 250 W prototypes, designed according to photovoltaic ac-module specifications, are obtained experimentally to validate the theoretical analyses and point out advantages and limitations of each converter. The results demonstrate that the combination of the three studied techniques provides the best trend off on the comparative analysis carried out in this work.**

***Index Terms*—Boost converter, coupled-inductor (CI), dc–dc converter, high voltage gain, voltage multiplier (VM) cells.**

Nomenclature

PV	Photovoltaic modules.
FC	Fuel cells.
N	Coupled-inductor turns-ratio.
$D_{\mathrm{Cycle}(1,2,\ldots)}$	Duty-cycle.
M	Static voltage gain.
B	Boost.
$\mathrm{SC}(S)$	Super-lift charge pump.
$\mathrm{SC}(D)$	Dickson charge pump.
$\mathrm{SC}(F)$	Fibonacci charge pump.
$B^{\mathrm{SC}(S)}$, $B^{\mathrm{SC}(D)}$, $B^{\mathrm{SC}(F)}$	Boost converter with [$\mathrm{SC}(S)$, $\mathrm{SC}(D)$, or $\mathrm{SC}(F)$].
SO	Stacked outputs.
CO	Cascaded outputs.
PO	Parallel outputs.
$\mathrm{BCI}_{\mathrm{SO}}$, $\mathrm{BCI}_{\mathrm{CO}}$, $\mathrm{BCI}_{\mathrm{PO}}$	Coupled-inductor boost converter with (SO, CO, or PO).
VM	Voltage multiplier.
$\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{VM}}$	Coupled-inductor VM boost converter with (SO, CO, or PO).
$\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(S)}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(S)}$, $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(S)}$	Coupled-inductor $\mathrm{SC}(S)$ boost converter with (SO, CO, or PO).
$\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(F)}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(F)}$, $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(F)}$	Coupled-inductor $\mathrm{SC}(F)$ boost converter with (SO, CO, or PO).
$\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(D)}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)}$, $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(D)}$	Coupled-inductor $\mathrm{SC}(D)$ boost converter with (SO, CO, or PO).
$\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(S)+\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(S)+\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(S)+\mathrm{VM}}$	Coupled-inductor VM + $\mathrm{SC}(S)$ boost converter with (SO, CO, or PO).
$\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(F)+\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(F)+\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(F)+\mathrm{VM}}$	Coupled-inductor VM + $\mathrm{SC}(F)$ boost converter with (SO, CO, or PO).
$\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(D)+\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(D)+\mathrm{VM}}$	Coupled-inductor VM + $\mathrm{SC}(D)$ boost converter with (SO, CO, or PO).
$\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(F)+\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(F)+\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(F)+\mathrm{VM}}$	Coupled-inductor $\mathrm{SC}(F)$ + VM boost converter with (SO, CO, or PO).

Manuscript received April 6, 2017; revised July 14, 2017; accepted August 4, 2017. Date of publication August 28, 2017; date of current version March 5, 2018. This paper was supported in part by the "Conselho Nacional de Desenvolvimento Científico (CNPq)" and in part by "Coordenação de Aperfeiçoamento de Pessoal de Nível Superior (PROEX/CAPES)". Recommended for publication by Associate Editor Gerry Moschopoulos. *(Corresponding author: António Manuel Santos Spencer Andrade.)*

A. M. S. S. Andrade, L. Schuch, H. L. Hey, and M. L. da Silva Martins are with the Power Electronics and Control Research Group, Federal University of Santa Maria, Santa Maria, RS 97105-900, Brazil (e-mail: antoniom.spencer@gmail.com; schuch.prof@gmail.com; heliohey@gmail.com; mariolsm@gmail.com).

E. Mattos is with the National Institute of Space Research, Federal University of Santa Maria, Santa Maria, RS 97105-900, Brazil (e-mail: everson.mattos@inpe.br).

Digital Object Identifier 10.1109/TPEL.2017.2742900

I. Introduction

HIGH-VOLTAGE step-up dc–dc converters have been emerging in various low power single-phase applications [1], [2]. For the renewable power industry, the high-voltage

conversion ratio is of prime concern since PV modules and FC provide very low voltages compared to grid utility patterns [3]. The boost converter is a standard step-up nonisolated converter. Ideally, it can obtain high output voltage levels by simply increasing its switch duty-cycle. Nevertheless, this converter presents excessive conduction losses at extreme duty-cycles, which not only degrade the converter efficiency but tends to increase the voltage drops across the converter components, which in turn, also limit the maximum attainable voltage gain [4].

In order to overcome the limitations of ordinary step-up converters (boost, buckboost, etc.) imposed by extremely high duty-cycles, many circuit modifications and techniques have been proposed in the literature to increase their voltage gain [5]–[8].

Two winding magnetic devices are the simplest method to transfer an alternate voltage from a pair of terminals of a circuit to another with the advantage of voltage adjustment by means of the winding turns-ratio. This method is used in transformer-based dc–dc converters (such as full-bridge, forward, etc. [5]–[8]) and in coupled-inductor (CI) dc–dc converters (flyback, SEPIC, etc. [9]). In cases where isolation is not required, tapped inductors can also provide high-voltage conversion ratios [10]–[13]. On the other hand, even in nonisolated topologies, the coupled-inductor (CI) windings can be separated and connected in circuits that are far apart from each other [14]–[28]. In this way, Dreher *et al.* [25] analyzes the use of CIs to merge two dc–dc converters in order to sum their individual *M*s. On the other hand, a high CI turns ratio often results in an increase of parasitic leakage inductances. It must be taken into account that large leakage inductances lead to additional undesired stored energy, which results in voltage spikes across the semiconductors and reduction of system efficiency [26], in addition to voltage and current ringing that degrades converter electromagnetic interference performance.

Because the use of high turns ratio transformers and CIs to achieve voltage adjustment is limited by the large leakage inductances and parasitic capacitances of the magnetic devices, VM circuits (Greinacher [29], Cockcroft–Walton [30], etc.) are a common alternative to attain high voltages. The VM circuit is applied to dc–dc converters in several ways, the most usual being the replacement of the converter output rectifier by the diode-capacitor VM [31]–[44]. Another approach using a VM is to replace a middle section capacitive buffer of the dc–dc converter structure by a diode-capacitor VM [45], [46]. In both of these approaches, the VM circuit must be driven by an alternative voltage which is able to polarize directly and reversely the diodes in the ladder structure of the multiplier circuit, transferring the input voltage across the capacitors. High-voltage conversion ratios are achieved by increasing the number of VM cells. This may lead to higher voltage rating diodes and capacitors. The large component count also increases the cost and complexity of the converters.

A more concise arrangement for VM cells does not require an alternative voltage to drive the diodes. Its operation relies only on switching action. The switched capacitors (SCs) VM circuits are well-known in low power analog electronics, such as charge pump circuits [47]–[49]. For power electronic circuits, SCs are used in several converter circuits. In order to not increase the number of active devices, it commonly makes use of a single active switch and a few passive ones [47]–[54]. In some topologies, an inductor buffer is used to readily charge the capacitors of the charge pumping cell. This improved circuit has been presented as super-lift charge pumping [54]–[56]. This VM method is also limited by the number of required components and the complexity associated with the dc/dc converter.

The duality concept has been employed to produce the switched inductor approach [50], [57]. Regrettably, employing a number of inductors is more expensive and complex than a number of capacitors, which limits this technique to very few switched inductor cells.

Finally, associations of several dc/dc converters in parallel (interleaved [58]–[64]), stacked (three-level [65]–[68]), or cascade (quadratic [69]–[71]) connection have also been explored. Another noteworthy technique proposes the use of a Y-source impedance to provide high voltage gain [72]; however, its design is very complex.

To sum up, in recent years, there has been growing interest in high-frequency, high step-up voltage conversion ratio switched power converters. For this reason, a number of topologies have been presented promising wide voltage conversion at very high efficiency. They may make use of CIs, interleaved pulse width modulation (PWM) cells, VM circuits, SCs, voltage-lift circuits, and so on.

In order to provide a concise analysis among several high step-up techniques and topologies, this paper proposes a simple synthesis approach to generate new families of high step-up converters. This synthesis methodology can also provide insight into well-known high-step up techniques and their application to converters that have been in use for a long time. Additionally, a detailed comparison of five selected topologies is carried out. Among the compared converters, three of them have already been published in the literature, the CI boost converter with cascaded outputs $\mathrm{BCI_{CO}}$ {see Fig. 1(a), proposed in [15]}, the boost converter with Dickson charge pump $B^{\mathrm{SC}(D)}$ {see Fig. 1(b), proposed in [51]}, and the CI VM boost converter with cascaded outputs $\mathrm{BCI_{CO}^{VM}}$ {see Fig. 1(c), proposed in [20]}. The other two topologies have not been presented in the literature. They are the CI Dickson charge pump boost converter with cascaded outputs $\mathrm{BCI_{CO}^{SC}}(D)$ [see Fig. 1(d)] and the CI $\mathrm{VM} + \mathrm{SC}(D)$ boost converter with cascaded outputs $\mathrm{BCI_{CO}^{SC}}(D)+VM$ [see Fig. 1(e)]. Besides the static voltage gain, it takes into account some key performance aspects, such as voltage and current stresses and circuit relative costs.

This paper is organized as follows. In Section II, a synthesis description about the converters is given. The comparative theoretical analysis of the converters is presented in Section III. The comparative results are presented in Section IV. This paper concludes with a general discussion concerning the pros and cons of each evaluate topology in Section V.

II. High Voltage Gain Techniques Applied to Step-Up DC/DC Converters

To obtain a better understanding of the voltage step-up mechanism considered in this study, this section presents the general

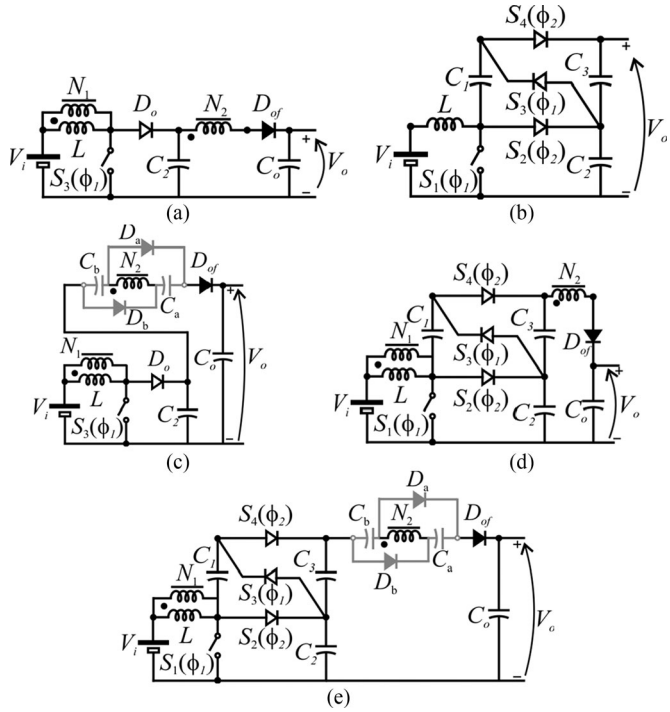

Fig. 1. High step-up dc/dc converters. (a) $\mathrm{BCI_{CO}}$ [15]. (b) $B^{\mathrm{SC}(D)}$ [51]. (c) $\mathrm{BCI_{CO}^{VM}}$ [20]. (d) $\mathrm{BCI_{CO}^{SC}}^{(D)}$. (e) $\mathrm{BCI_{CO}^{SC}}^{(D)+\mathrm{VM}}$.

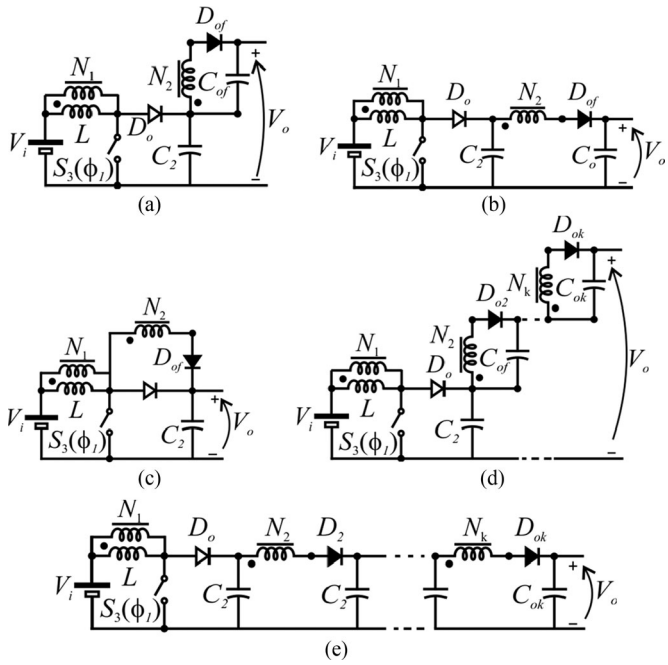

Fig. 2. Diagrams for some converters employing the coupled-inductor voltage gain technique. (a) $\mathrm{BCI_{SO}}$. (b) $\mathrm{BCI_{CO}}$. (c) $\mathrm{BCI_{PO}}$. (d) Multistacked outputs boost with coupled-inductor. (e) Multicascaded outputs boost with coupled-inductor.

characteristics of the three most well-known techniques employed to achieve a high *M*:

1) voltage adjustment by means of the turns-ratio of the magnetic device such as a transformer or a CI;
2) VM circuit; and
3) SC (charge pump) circuit.

A. Coupled-Inductor Voltage Gain Technique (CI)

Contrary to the common belief of many engineers, the CI differs by far from a two-winding transformer. The CI magnetizing inductance does store energy and, for this reason, it plays the role of an inductive buffer in the ladder structure of a power converter [73]. Thus, secondary winding can be seen as a derivation point from an inductive buffer that simply merges two converter circuits together. According to [73], dc/dc power converters are comprised by a set of components located in a well-known distribution that must agree with a set of network rules and their components are arranged in a ladder structure that can be grouped into three parts or sections named as follows, input, middle, and output sections. In [25], it is shown that replacing an inductor by a coupling inductor provides a merged topology of its former converter and an isolated one. The most well-known and studied merged converter is the CI boost converter [21], [22]. From the analyses carried out in [25], the isolated output section formed by the secondary winding of the CI can be associated with the nonisolated output in three ways, stacked, parallel, and cascade resulting in the BCI converter with stacked outputs [named $\mathrm{BCI_{SO}}$, Fig. 2(a)], the BCI with cascaded outputs [named $\mathrm{BCI_{CO}}$, Fig. 2(b)], and the BCI converter with parallel outputs [named $\mathrm{BCI_{PO}}$, Fig. 2(c)]. The parallel output association [25] yields more prominent voltage stresses and thus is not preferred. The stacked and cascade associations result in low-voltage stresses and, consequently, permit the use of low breakdown voltage devices (diodes and MOSFET) which is advantageous since low resistances can be achieved. *M* of the merged topologies from series, parallel, and cascade output associations is given by the sum of each individual converter static voltage gain. This way, it can be seen that this voltage gain approach strongly relies on the CI turns-ratio (*N*). In order to avoid a high turns-ratio, the secondary winding can be split in several windings with smaller turns-ratios [see Fig. 2(d) for a stacked multi-output BCI converter and Fig. 2(e) for a cascaded multi-output BCI converter].

M for the BCI converters with stacked, cascaded, and parallel outputs is given by the sum of each individual converter gain, as presented in Table I. The main advantage of the stacked and cascade output configurations is that the voltage stress on semiconductors depends only on each output voltage.

B. Voltage Multiplier (Cockcroft–Walton) Voltage Gain Technique (VM)

The Cockroft–Walton method of multiplying voltages is commonly used to generate high direct voltages. In general, a diode ladder structure is fed by high-frequency square waves via capacitors in series (Cockcroft–Walton [29]) or in parallel (Dickson [69]). These two approaches result in topologies that present equivalent voltage gain; however, their output impedances differ significantly.

A single half-wave (one-phase) VM cell was applied to the dc/dc switching converters Cúk and Zeta by Luo [45] giving

TABLE I
STATIC VOLTAGE GAIN

Converters	Static Voltage Gain	Converters	Static Voltage Gain
BCI	$M_{N=2} = \frac{1+ND}{1-D}$ (1)	$\mathrm{BCI}^{\mathrm{VM}}$	$M_{N=2,\,k_{\mathrm{VM}}=1} = \frac{1+N(2k_{\mathrm{VM}}-D)}{1-D}$ (2)
$B^{\mathrm{SC}(S)}$	$M_{k_{\mathrm{SC}}=1} = (\frac{2-D}{1-D})^{k_{\mathrm{SC}}}$ (3)	$\mathrm{BCI}^{\mathrm{SC}(S)}$	$M_{k_{\mathrm{SC}}=1,\,N=2} = \frac{(1-D)(2-D)^{k_{\mathrm{SC}}}+ND(1-D)^{k_{\mathrm{SC}}}}{(1-D)^{(k_{\mathrm{SC}}+1)}}$ (4)
$B^{\mathrm{SC}(F)}$	$M_{k_{\mathrm{SF}}=1} = \frac{1+k_{\mathrm{SF}}}{1-D}$ (5)	$\mathrm{BCI}^{\mathrm{SC}(F)}$	$M_{k_{\mathrm{SF}}=1,\,N=2} = \frac{1+k_{\mathrm{SF}}+ND}{1-D}$ (6)
$B^{\mathrm{SC}(D)}$	$M_{k_{\mathrm{CW}}=1} = \frac{1+k_{\mathrm{CW}}}{1-D}$ (7)	$\mathrm{BCI}^{\mathrm{SC}(D)}$	$M_{k_{\mathrm{CW}}=1,\,N=2} = \frac{(1+k_{\mathrm{CW}})+ND}{1-D}$ (8)

Converters	Static Voltage Gain
$\mathrm{BCI}^{\mathrm{VM+SC}(F)}$	$M_{N=2,\,k_{\mathrm{VM}}=1,\,k_{\mathrm{SF}}=1} = \frac{1+k_{\mathrm{SF}}(1+ND+2k_{\mathrm{VM}}N(1-D))}{1-D}$ (9)
$\mathrm{BCI}^{\mathrm{SC}(S)+\mathrm{VM}}$	$M_{k_{\mathrm{SC}}=1,\,N=2,\,k_{\mathrm{VM}}=1} = \frac{(1-D)(2-D)^{k_{\mathrm{SC}}}+ND(1-D)^{k_{\mathrm{SC}}}+2k_{\mathrm{VM}}ND(1-D)^{(k_{\mathrm{SC}}+1)}}{(1-D)^{(k_{\mathrm{SC}}+1)}}$ (10)
$\mathrm{BCI}^{\mathrm{SC}(F)+\mathrm{VM}}$	$M_{k_{\mathrm{SF}}=1,\,N=2,\,k_{\mathrm{VM}}=1} = \frac{1+k_{\mathrm{SF}}+ND+2k_{\mathrm{VM}}N(1-D)}{1-D}$ (11)
$\mathrm{BCI}^{\mathrm{SC}(D)+\mathrm{VM}}$	$M_{k_{\mathrm{CW}}=1,\,N=2,\,k_{\mathrm{VM}}=1} = \frac{(1+k_{\mathrm{CW}})+ND+2k_{\mathrm{VM}}N(1-D)}{1-D}$ (12)

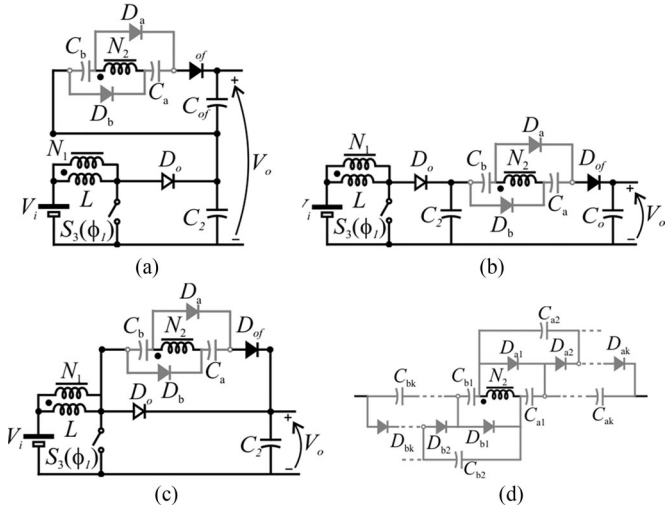

Fig. 3. Diagrams for some converters employing coupled-inductor and a voltage multiplier cell. (a) $\mathrm{BCI}^{\mathrm{VM}}_{\mathrm{SO}}$. (b) $\mathrm{BCI}^{\mathrm{VM}}_{\mathrm{CO}}$. (c) $\mathrm{BCI}^{\mathrm{VM}}_{\mathrm{PO}}$. (d) General voltage multiplier cell.

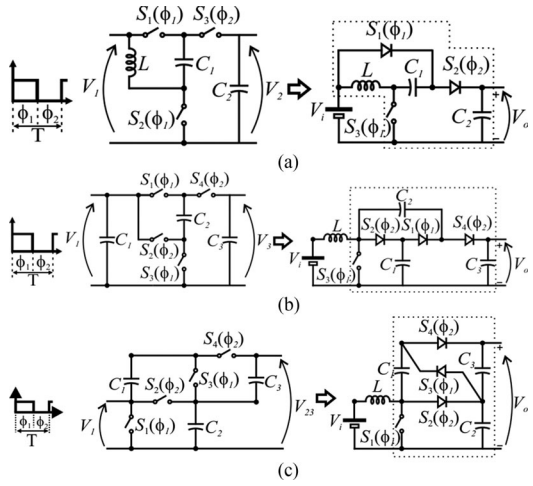

Fig. 4. Diagrams of some converters employing switched capacitor cells. (a) $B^{\mathrm{SC}(S)}$. (b) $B^{\mathrm{SC}(F)}$. (c) $B^{\mathrm{SC}(D)}$.

rise to the so called self-lift converters. Nevertheless, the static voltage gain of these converters is equal to the boost voltage gain; thus, one can point out that the main advantage of the Cúk and Zeta self-lift converters compared to the boost converter is that their output current presents a small ripple. This way, as long as this paper aims to deal with high voltage gain topologies, only the boost derived converters will be discussed in the following analyses.

On the other hand, the use of a two-phase drive (full-wave) for alternate modes of the diode ladder improves VM performance [75], [76]. Fig. 3 shows a two-phase driven single-cell Cockcroft–Walton VM that has been applied to the secondary winding of CIs of the three type BCI converters [32], yielding the stacked, cascaded, and parallel outputs VM CI boost converter configurations. These configurations are named CI VM boost converter with stacked outputs $\mathrm{BCI}^{\mathrm{VM}}_{\mathrm{SO}}$ [see Fig. 3(a)], CI VM boost converter with cascaded outputs $\mathrm{BCI}^{\mathrm{VM}}_{\mathrm{CO}}$ [see Fig. 3(b)], and CI VM boost converter with parallel outputs $\mathrm{BCI}^{\mathrm{VM}}_{\mathrm{PO}}$ [see Fig. 3(c)]respectively. The static voltage gain for the stacked, cascaded, and parallel outputs VM BCI converters is presented in Table I.

C. Switched Capacitor (Charge Pump) Voltage Gain Technique (SC)

The SC VM originated from Cockcroft–Walton circuit by using serial capacitor ladders [30]. In order to increase the maximum attainable voltage gain, a different control of the switches that provide alternately switching the state from in-serial to in-parallel and vice-versa, for the adjacent capacitors was introduced [71]. The resultant achieved voltage gain of the VM circuit is defined by the Fibonacci series and depends on the number of the switching capacitor multiplying cells. This technique has been applied to the boost converter in [54] and [51]. Fig. 4 shows the three possible SC and its respective boost converters, resulting in the boost converter with super-lift charge

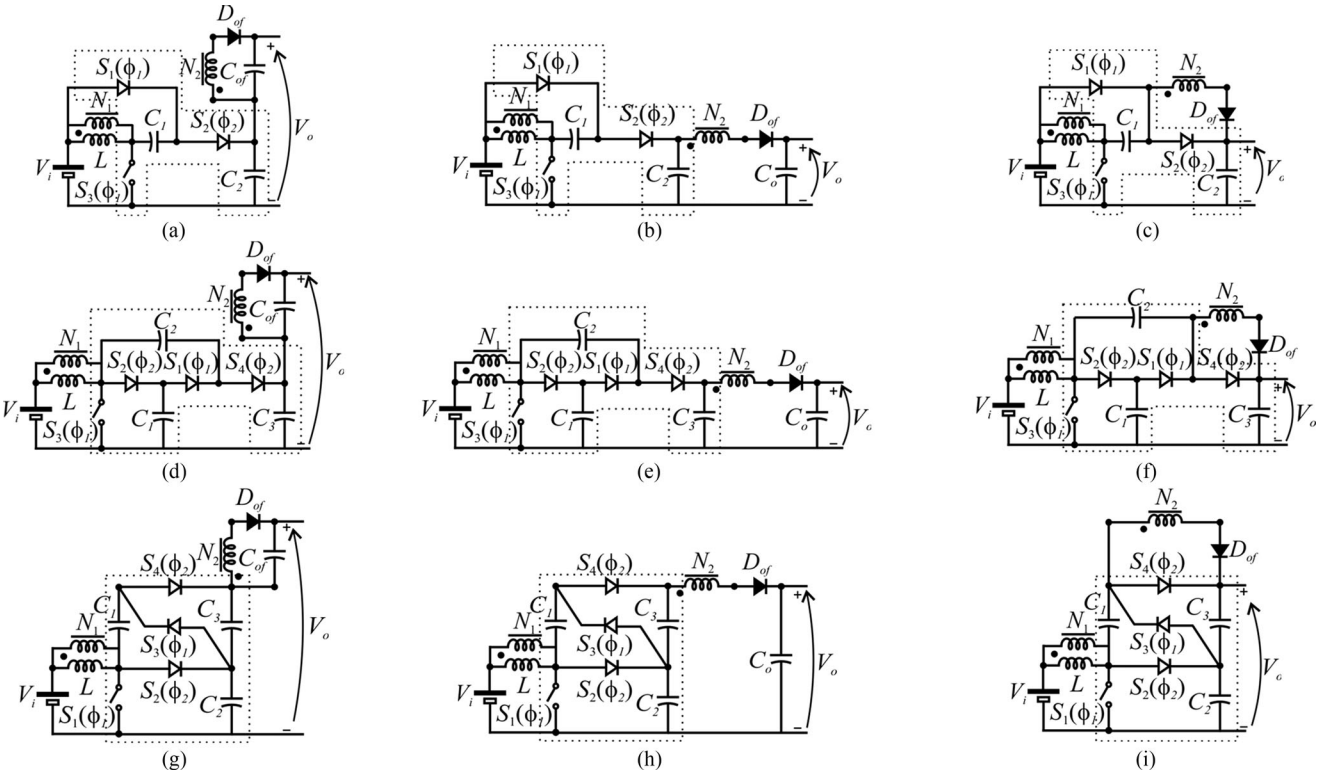

Fig. 5. Diagrams of the charge pump cells and coupled-inductor voltage gain techniques. (a) $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(S)}$. (b) $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(S)}$. (c) $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(S)}$. (d) $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(F)}$. (e) $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(F)}$. (f) $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(F)}$. (g) $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(D)}$. (h) $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)}$. (i) $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SO}(D)}$.

pump, named $B^{SC(S)}$ [see Fig. 4(a)]; the boost converter with Fibonacci charge pump, named $B^{SC(F)}$ [see Fig. 4(b)], and the boost converter with Fibonacci charge pump, named $B^{SC(D)}$ [see Fig. 4(c)]. It can be seen that Dickson and Fibonacci charge pumps consist only of switches and capacitors. This way, they can be more easily extended. On the contrary, the super-lift cell, although resembling the other SC charge pumps, requires an inductor to provide the capacitor charge [76]. Hence, it is more expensive to extend it than in charge pumps that consist of only capacitors and diodes. The static voltage gain for the super-lift, Fibonacci, and Dickson charge pumps is presented in Table I.

To improve the boost converter static voltage gain, the three abovementioned SC techniques can be combined with the CI concept. Fig. 5(a)–(c) shows a super-lift charge pump associated with stacked, cascaded, and parallel outputs of BCI converters, respectively. These topologies are, respectively, named $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(S)}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(S)}$, and $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(S)}$. In the same way, a Fibonacci charge pump associated with stacked, cascaded, and parallel outputs of BCI converters form the configurations $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(F)}$ [see Fig. 5(d)], $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(F)}$ [see Fig. 5(e)], and $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(F)}$ [see Fig. 5(f)].

Analogously, Fig. 5(g)–(i) shows a Dickson charge pump associated with stacked, cascaded, and parallel outputs of CI boost converter. These topologies are named $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(D)}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)}$, and $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(D)}$, respectively. The voltage conversion ratio for the charge pump cells with stacked, cascaded, and parallel outputs CI boost converters is presented in Table I.

To further improve the boost converter *M*, a third technique can be incorporated. Fig. 6(a)–(c) shows a super-lift charge pump associated with stacked, cascaded, and parallel outputs of VM BCI converters, respectively. These topologies are named $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(S)+\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(S)+\mathrm{VM}}$, and $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(S)+\mathrm{VM}}$. Likewise, Fig. 6(d)–(f) shows a Fibonacci charge pump associated with stacked, cascaded, and parallel outputs of VM BCI converters, respectively. These topologies are referred to as $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(F)+\mathrm{VM}}$, $\mathrm{BCI}_{CO}^{\mathrm{SC}(F)+\mathrm{VM}}$, and $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(F)+\mathrm{VM}}$. Similarly, Fig. 6(g)–(i) shows a Dickson charge pump associated with stacked, cascaded, and parallel outputs of VM BCI converter, respectively. These topologies are named $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(D)+\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+\mathrm{VM}}$, and $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(D)+\mathrm{VM}}$. *M* for the SC with stacked, cascaded, and parallel outputs VM BCI converters is presented in Table I.

On the other hand, an SC Fibonacci charge pump can be associated with the stacked, cascaded, and parallel outputs of VM BCI converters configurations, resulting in the configurations $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(F)+\mathrm{VM}}$ [see Fig. 7(a)], $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(F)+\mathrm{VM}}$ [see Fig. 7(b)], and $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(F)+\mathrm{VM}}$ [see Fig. 7(c)], respectively. The static voltage gain for stacked, cascaded, and parallel outputs VM CI boost converters with a Fibonacci charge pump is shown in Table I.

Aiming to summarize all topologies discussed in this section, Fig. 8 shows a diagram of the voltage step-up techniques and their combinations. It is worth noting that the diagram is limited to two- and three-technique combinations; however, more techniques can be combined. The more the techniques used, the more complex the circuit becomes and thus, prior to including

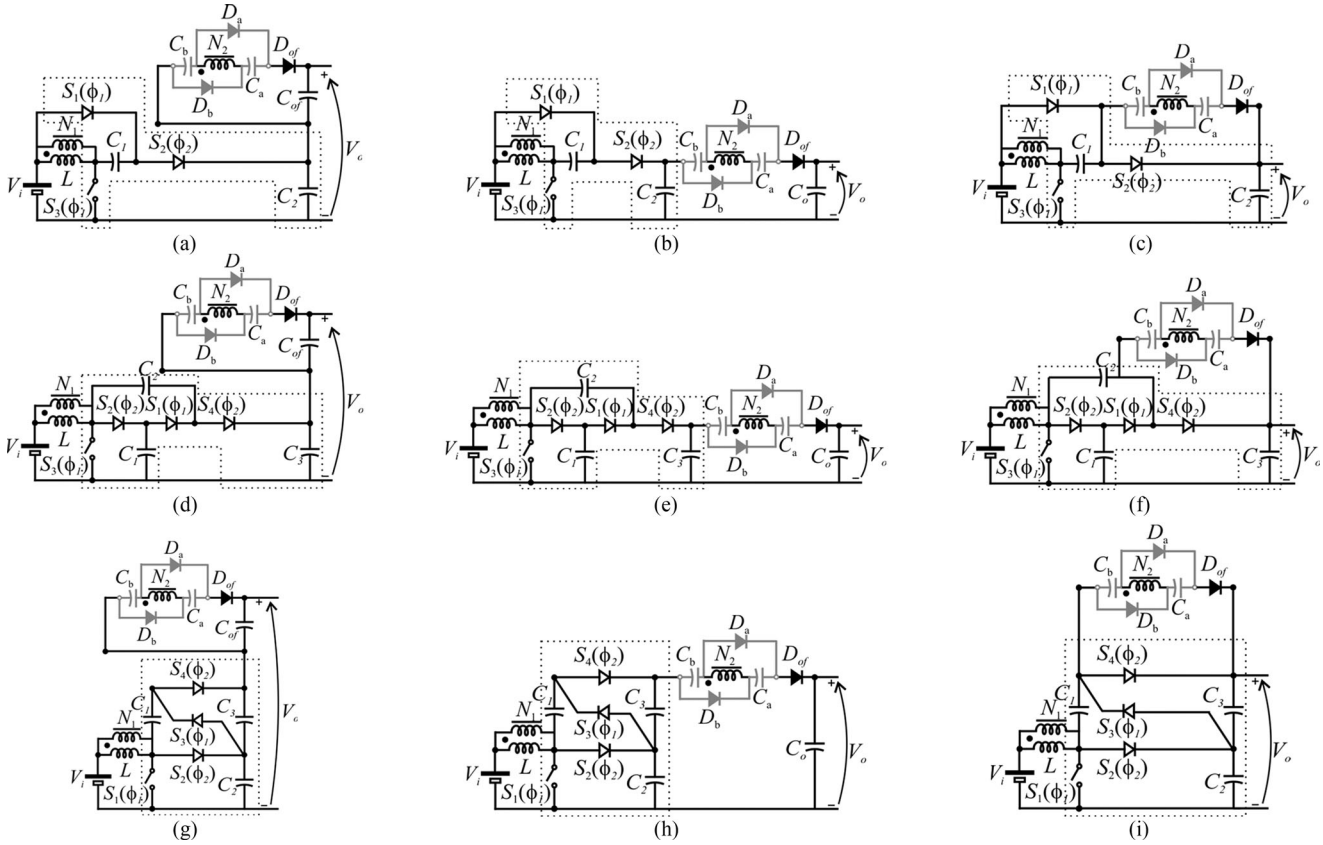

Fig. 6. Diagrams of the charge pump cells and coupled-inductor with voltage doubler cell. (a) $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(S)+\mathrm{VM}}$. (b) $\mathrm{BCI}_{\mathrm{SC}}^{\mathrm{SC}(S)+\mathrm{VM}}$. (c) $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(S)+\mathrm{VM}}$. (d) $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(F)+\mathrm{FM}}$. (e) $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(F)+\mathrm{VM}}$. (f) $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SO}(F)+\mathrm{VM}}$. (g) $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(D)+\mathrm{VM}}$. (h) $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+\mathrm{VM}}$. (i) $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(D)+\mathrm{VM}}$.

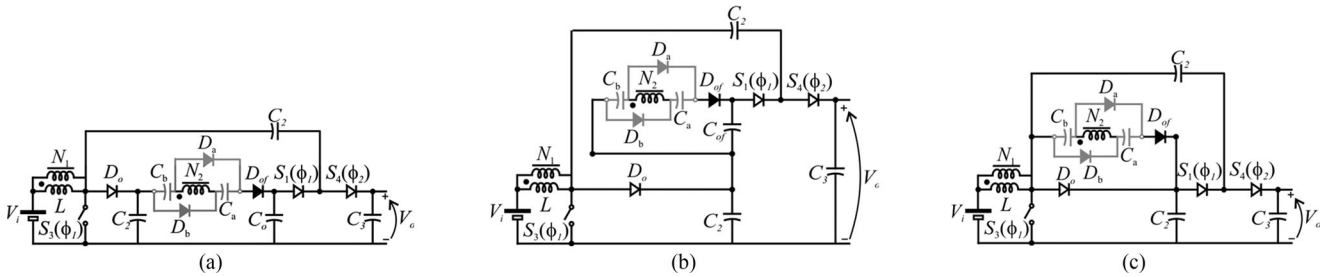

Fig. 7. Diagrams of some converters employing switched capacitor cells with voltage doubler boost. (a) $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(F)+\mathrm{VM}}$. (b) $\mathrm{BCI}_{\mathrm{SO}}^{\mathrm{SC}(F)+\mathrm{VM}}$. (c) $\mathrm{BCI}_{\mathrm{PO}}^{\mathrm{SC}(F)+\mathrm{VM}}$.

a new technique to a given circuit, the benefits and disadvantages should be analyzed. Alternatively, a single technique can be extended, i.e., a VM [VM(*h*) or VM(*f*)] can be extended to a voltage tripler or quadrupler, and so on. In the same way, charge pumps can also be extended. The CI approach does not require circuit modifications as long as the turns-ratio can simply assume different values to enhance the converter *M*. Nevertheless, voltage stresses on semiconductors can be minimized when the secondary winding is split in more parts.

Aiming to provide a general analysis of the static voltage gain of the converters mentioned in Fig. 8, Table I presents all equations for them, where k_{D} and k_{VM} are the number of cells for the VM circuits (half-wave and full-wave); k_{CW}, k_{SC}, and k_{SF} are the number of SC cells; and *N* is the CI turns-ratio.

In order to provide the numerical solution for the equations presented in Table I, these parameters are chosen as $N = k_D = 2$ and $k_{\mathrm{VM}} = k_{\mathrm{SF}} = k_{\mathrm{SC}} = k_{\mathrm{CW}} = 1$. Fig. 9 shows the results for the static voltage gain for all techniques evaluated. It can be seen that the smallest voltage gain attained is for BCI (black solid line), followed by the converters with the $B^{\mathrm{SC}(S)}$ converter. Topologies $B^{\mathrm{SC}(D)}$ and $B^{\mathrm{SC}(F)}$ have a major positive inclination, which makes them advantageous amongst the other first configurations for duty-cycles higher than 0.5. As it was expected, the second configurations provide improvement to the voltage gain, achieving higher values when compared with their first counterparts.

The highest gain attained among second configuration is $\mathrm{BCI}^{\mathrm{SC}(D)}$ and $\mathrm{BCI}^{\mathrm{SC}(F)}$ for duty-cycle values below 0.75. In

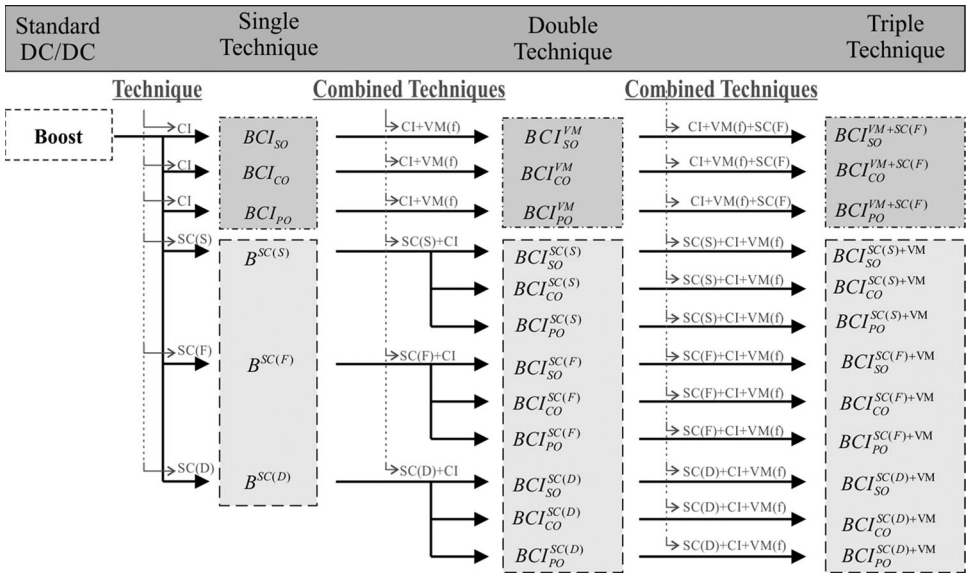

Fig. 8. Derivation of the high-voltage step-up topologies flowchart.

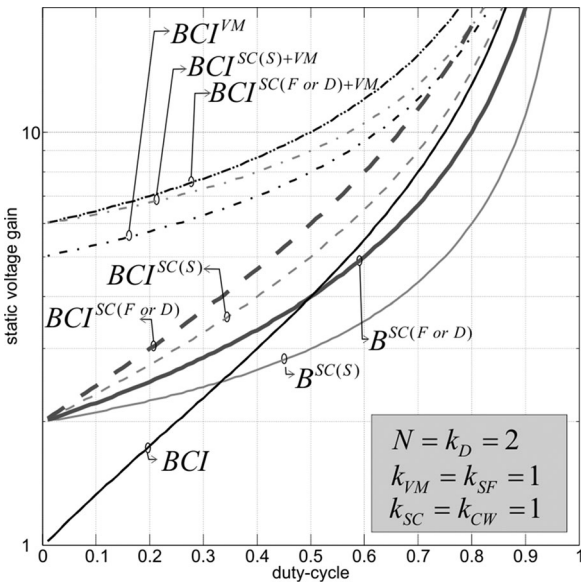

Fig. 9. Static voltage gain versus duty-cycle for configurations.

the same way, third configurations provide higher voltage gains, being the highest for $\mathrm{BCI}^{\mathrm{SC}(D)+VM}$ and $\mathrm{BCI}^{\mathrm{SC}(F)+\mathrm{VM}}$. It means that all these configurations can be seen as candidates to yield the best topology. It will depend on further analysis of other criteria to point out which one is more advantageous.

III. Theoretical Comparative Analysis

A comparative analysis is carried out among all converters shown in Fig. 1. In this analysis, the principle of operation, static voltage gain, voltage stress on components, component stress factor (CSF), component count, and relative cost are addressed.

In order to simplify the following analysis, the assumptions are shown as follows:

1) All power devices are ideal;

TABLE II
Summary of the Operation Mode of Converters

Converters	Semiconductors						
	S	D_1	D_2	D_3	D_4	D_5	D_o
$\mathrm{BCI}_{\mathrm{CO}}$	ON	OFF	–	–	–	–	OFF
	OFF	ON	–	–	–	–	ON
$B^{\mathrm{SC}(D)}$	ON	OFF	ON	OFF	–	–	OFF
	OFF	ON	OFF	ON	–	–	ON
$\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{VM}}$	ON	OFF	–	–	ON	ON	OFF
	OFF	ON	–	–	OFF	OFF	ON
$\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)}$	ON	OFF	ON	OFF	–	–	OFF
	OFF	ON	OFF	ON	–	–	ON
$\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+\mathrm{VM}}$	ON	OFF	ON	OFF	ON	ON	OFF
	OFF	ON	OFF	ON	OFF	OFF	ON

2) Capacitors $C_1 - C_o$ are large enough to consider that their voltages are constant during one switching period.
3) The turns ratio N of the CI is equal to N_2/N_1; and
4) All converters operate in a continuous conduction mode (CCM).

A. Principle of Operation

One of the main characteristics of the principle of operation of the topology is that all have two operation stages. In the first stage, the switch *S* is turned ON and the inductor L of the CI is magnetized. In the second stage, the switch *S* is turned OFF and CI is demagnetized. Table II summarizes the operation stages of all converters. Fig. 10 depicts their key waveforms.

B. Static Voltage Gain Versus Duty-Cycle

The static voltage gain of the converters can be found by applying a volt-second balance on the inductor of each converter, yielding the expressions shown in Table I. Solving the expressions (1), (7), (2), (8), and (12) for the duty-cycle, it

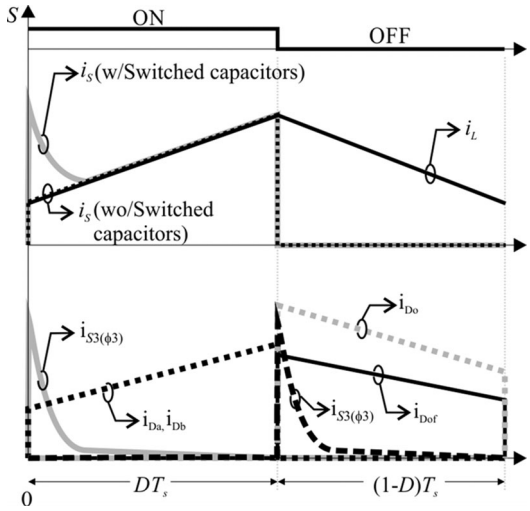

Fig. 10. Key waveforms of converters.

TABLE III
DUTY-CYCLE FOR THE CONVERTERS ANALYZED

Converters	Duty-cycle
$\mathrm{BCI_{CO}}$	$D_{\mathrm{Cycle1}} = \frac{M-1}{M+N}$ (25)
$B^{\mathrm{SC}(D)}$	$D_{\mathrm{Cycle2}} = \frac{M-(1+k_{\mathrm{CW}})}{M}$ (26)
$\mathrm{BCI_{CO}^{VM}}$	$D_{\mathrm{Cycle3}} = \frac{M-(1+2k_{\mathrm{VM}}N)}{M+N-2k_{\mathrm{VM}}N}$ (27)
$\mathrm{BCI_{CO}^{SC(D)}}$	$D_{\mathrm{Cycle4}} = \frac{M-(1+k_{\mathrm{CW}})}{M+N}$ (28)
$\mathrm{BCI_{CO}^{SC(D)+VM}}$	$D_{\mathrm{Cycle5}} = \frac{M-(1+k_{\mathrm{CW}}+2k_{\mathrm{VM}}N)}{M+N-2k_{\mathrm{VM}}N}$ (29)

can be seen that the duty-cycle definition differs for topologies $\mathrm{BCI_{CO}}$, $B^{\mathrm{SC}(D)}$, $\mathrm{BCI_{CO}^{VM}}$, $\mathrm{BCI_{CO}^{SC(D)}}$, and $\mathrm{BCI_{CO}^{SC(D)+VM}}$ (see Table III). It can be noted that the duty-cycle reduces by the increment of the parameters N, k_{CW}, and k_{VM}. Hence, in order to adjust the duty-cycle to a small value, N from topology $\mathrm{BCI_{CO}}$ must be a high value, which may enlarge the CI leakage inductance and associated losses. Likewise, to minimize the duty-cycle in topology $B^{\mathrm{SC}(D)}$, the number of VM cells (k_{CW}) must be increased, resulting in higher costs and losses as the number of semiconductor devices increases. On the other hand, topologies $\mathrm{BCI_{CO}^{VM}}$ and $\mathrm{BCI_{CO}^{SC(D)}}$ count on two techniques to achieve a low duty-cycle, which means that both parameters can share the task and, consequently, a better tradeoff between losses saving, cost, and complexity should be achieved. In the same way, topology $\mathrm{BCI_{CO}^{SC(D)+VM}}$ can count on the three techniques to minimize the duty-cycle in a more cost-effective manner. The reduction of the duty-cycle is of prime concern to reduce power stresses and losses as will be detailed in the following sections.

Aiming to provide a quantitative example for the following analyses, by choosing the parameters as $M = 10$, $N = 2$, $k_{\mathrm{VM}} = 1$, and $k_{\mathrm{CW}} = 1$, the duty-cycle of each converter of the comparison has been computed as $D_{\mathrm{Cycle1}} = 0.75$, $D_{\mathrm{Cycle2}} = 0.8$, $D_{\mathrm{Cycle3}} = 0.625$, $D_{\mathrm{Cycle4}} = 0.667$, $D_{\mathrm{Cycle5}} = 0.5$, in comparison to the boost converter whose duty-cycle would be $D_{\mathrm{boost}} = 0.9$.

TABLE IV
CONVERTERS SPECIFICATIONS

Specification	Value
Output Power P_o	250 W
Input Voltage V_i	25 V
Output Voltage V_o	250 V
Static Voltage Gain M	10
Switching Frequency fs	50 kHz

C. Component Stress Factor

The previous sections described different topologies to achieve a high-voltage conversion ratio (M). It has been shown that for the same M, their operating duty-cycles are also distinct. Thus, in order to address the actual benefits acheived with each high-voltage technique, the CSF is evaluated. The CSF analysis provides numerical scores for each component type in each topology for a specific set of operation conditions, allowing an apples-to-apples comparison of topologies [79], [80]. In order to compute the voltage stress factor, a set of specifications that define an operating point from an actual application are presented in Table IV. The electrical specifications are based on an ordinary ac-module application considering the requirements for the solar panel (for instance the Kyocera KD250GH-4FB2) and the grid (127 V). It is worth to note that a 50 kHz switching frequency has been chosen for all evaluated topologies to ensure a good trade-off between power density $(> text 0.2 W/cm^3)$ and efficiency $(> 96\%)$. On the other hand, instead of optimizing each converter for its critical operating frequency (as proposed by [81]), the same frequency is used for all converters to ensure that they will use semiconductors of the same technology.

In the following analyses, for semiconductors, switches, and diodes, the total CSFs S_SCSF and S_DCSF are expressed, respectively, by

$$\text{Total } S_S\text{CSF} = \sum_{\text{Switch}} S_S\text{CSF}_i \tag{13}$$

$$\text{Total } S_D\text{CSF} = \sum_{\text{Diodes}} S_D\text{CSF}_i. \tag{14}$$

Concerning inductors and CIs, the total winding CSF (WCSF) is given by

$$\text{Total WCSF} = \sum_{\text{Windings}} \text{WCSF}_i. \tag{15}$$

In addition, the total capacitor CSF (CCSF) is given by

$$\text{Total CCSF} = \sum_{\text{Capacitors}} \text{CCSF}_i. \tag{16}$$

Assuming the operating conditions specified in Table V, the CSF is calculated for all components, providing the Total CSF for each converter.

Fig. 11(a) shows the results for the total CSF of each topology from the comparative analysis and the boost converter. It can be seen that besides being a simpler topology, the boost converter presents the highest stress factor, reaching a value of 110. The

TABLE V
CONVERTER OPERATING CONDITIONS AND SPECIFICATIONS

Converter	Parameters				
	D_{Cycle}	Inductors	Capacitors	Switches	Diodes
$\mathrm{BCI_{CO}}$	0.75	L: 100 μH (77 083*) R_{dc}: 112 mΩ	C_2: 9 μF (0.15 Ω) C_{o}: 18 μF (0.15 Ω)	IRFP250N 200 V/ 30 A (0.075 Ω, 650 pF) (82 ns, 102 ns) 0.95 °C/W	STPSC4H065 650 V/4 A (0.61 Ω) 1.8 °C/W
$B^{\mathrm{SC}(D)}$	0.8	L: 100 μH (77 083*) R_{dc}: 112 mΩ	$C_{1,2,3}$: 9 μF (0.15 Ω)	IRFP250N 200 V/ 30 A (0.075 Ω, 650 pF) (82 ns, 102 ns) 0.95 °C/W	STPSC4H065 650 V/4 A (0.61 Ω) 1.8 °C/W
$\mathrm{BCI_{CO}^{VM}}$	0.625	L: 100 μH (77 083*) R_{dc}: 112 mΩ	$C_{1,2,3}$: 7.6 μF (0.15 Ω) $C_{\mathrm{a,b}}$: 1.5 μF (0.15 Ω) C_{o}: 3.3 μF (0.15 Ω)	IRFP250N 200 V/30 A (0.075 Ω, 650 pF) (82 ns, 102 ns) 0.95 °C/W	STPSC4H065 650 V/4 A (0.61 Ω) 1.8 °C/W
$\mathrm{BCI_{CO}^{SC(D)}}$	0.667	L: 100 μH (77 083*) R_{dc}: 112 mΩ	$C_{1,2,3}$: 7.6 μF (0.15 Ω) C_{o}: 3.3 μF (0.15 Ω)	IRFP150N 100 V/ 42 A (0.015 Ω, 450 pF) (66 ns, 96 ns) 0.95 °C/W	MBR20200CT 200 V/20 A (0.22 Ω) 2.0 °C/W
$\mathrm{BCI_{CO}^{SC(D)+VM}}$	0.5	L: 100 μH (77 083*) R_{dc}: 112 mΩ	$C_{1,2,3}$: 7.6 μF (0.15 Ω) $C_{\mathrm{a,b}}$: 1.5 μF (0.15 Ω) C_{o}: 3.3 μF (0.15 Ω)	IRFP150N 100 V/ 42 A (0.015 Ω, 450 pF) (66 ns, 96 ns) 0.95 °C/W	MBR20200CT 200 V/20 A (0.22 Ω) 2.0 °C/W

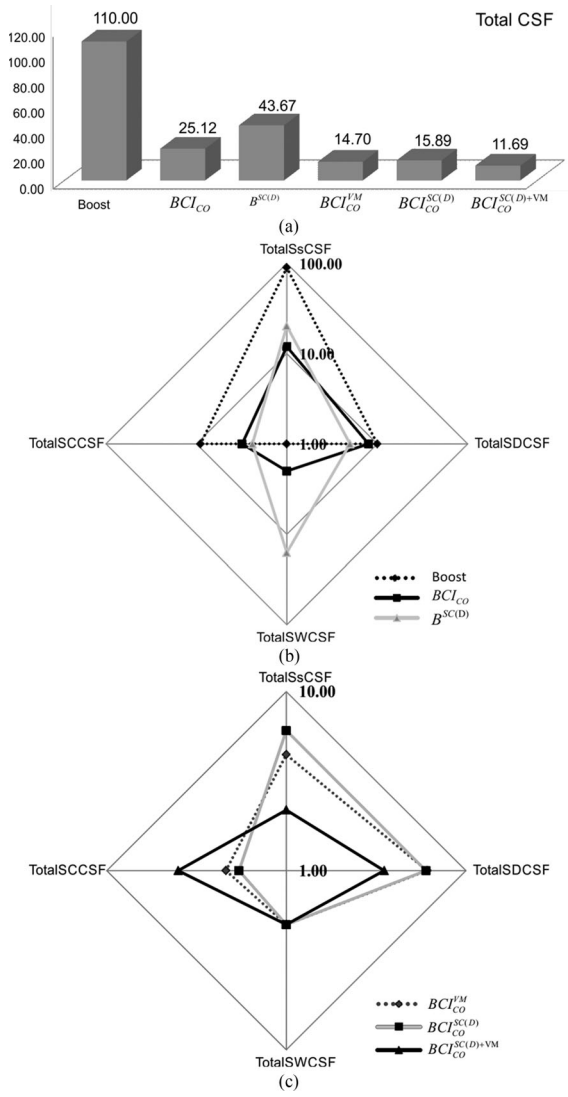

Fig. 11. Diagrams for the component stress factor. (a) Total component stress factor by a converter. (b) Boost, $\mathrm{BCI_{CO}}$ and $B^{\mathrm{SC}(D)}$ converters. (c) $\mathrm{BCI_{CO}^{VM}}$, $\mathrm{BCI_{CO}^{SC(D)}}$, and $\mathrm{BCI_{CO}^{SC(D)+VM}}$ converters.

adoption of a single voltage step-up technique is provided by topologies $\mathrm{BCI_{CO}}$ and $B^{\mathrm{SC}(D)}$ that achieve 25.12 and 43.67, respectively. From Fig. 11(b), it can be seen that stresses on the switch (Total S_{S}CSF) are reduced expressively for $\mathrm{BCI_{CO}}$ and $B^{\mathrm{SC}(D)}$, the latter being higher than the former. This can be explained by the fact that in topology $B^{\mathrm{SC}(F)}$, the SC discharges through the switch while in $\mathrm{BCI_{CO}}$, no additional current passes through the switch. On the other hand, capacitor (total SCCSF) and diode (total S_D CSF) stresses are lower in topology $B^{\mathrm{SC}(D)}$. The magnetic device winding stresses also increase in $\mathrm{BCI_{CO}}$ and $B^{\mathrm{SC}(D)}$ converters. The inclusion of two voltage step-up techniques is evaluated by topologies $\mathrm{BCI_{CO}^{VM}}$ and $\mathrm{BCI_{CO}^{SC(D)}}$ that achieve total CSF factors of 14.70 and 15.89, respectively, which still represent a significant reduction. Fig. 11(c) points out that stresses on the switch (total S_SCSF) are continuously reduced, reaching a minimum value for $\mathrm{BCI_{CO}^{SC(D)+VM}}$. The minimum stress on diodes is also obtained for $\mathrm{BCI_{CO}^{SC(D)+VM}}$. The winding stress factor is the same for $\mathrm{BCI_{CO}^{VM}}$ and $\mathrm{BCI_{CO}^{SC(D)}}$; however, the capacitor stress factor is smaller for $\mathrm{BCI_{CO}^{SC(D)}}$.

D. Current and Voltage Stress on Semiconductor Components

In this section, the current and voltage stresses across the semiconductor devices are evaluated. The current and voltage stresses on the semiconductors and the total stress voltage factor for switch and diodes are expressed in Table VI.

The total current stress on the switch $(\mathrm{TC}_S S)$ and the total current stress on the diodes $(\mathrm{TC}_D S)$ are the sum of the stresses across each switch and each of the converter diodes [82]. They are calculated, respectively, by

$$\mathrm{TC}_S S = \sum_{S_1}^{S_n} \mathrm{SC}_S \tag{17}$$

$$\mathrm{TC}_D S = \sum_{D_1}^{D_n} \mathrm{SC}_D. \tag{18}$$

TABLE VI
CURRENT AND VOLTAGE STRESSES ACROSS SEMICONDUCTOR DEVICES

Converter	Switch	Diodes D_1, D_2 D_3, and D_o	Diodes $D_{\rm of}$, D_4, and D_5	$\mathrm{TC}_S S$	$\mathrm{TC}_D S$	Switch	Diodes D_1, D_2 D_3, and D_o	Diodes $D_{\rm of}$, D_4, and D_5	$\mathrm{TV}_S S$	$\mathrm{TV}_D S$
		Current stresses				Voltage stresses				
Boost	(36)	–	(38)	$0.95I_i$	$0.32I_i$	$\frac{1}{1-D_{\rm boost}}V_i$	–	$\frac{1}{1-D_{\rm boost}}V_i$	$10V_i$	$10V_i$
$\mathrm{BCI}_{\rm CO}$		–		$0.87I_i$	$0.75I_i$	$\frac{1}{1-D_{\rm Cycle1}}V_i$	–	$\frac{N}{1-D_{\rm Cycle1}}V_i$	$4V_i$	$8V_i$
$B^{\mathrm{SC}(D)}$		(38)		$0.90I_i$	$0.45I_i$	$\frac{1}{1-D_{\rm Cycle2}}V_i$	$\frac{1}{1-D_{\rm Cycle2}}V_i$	$\frac{1}{1-D_{\rm Cycle2}}V_i$	$5V_i$	$15V_i$
$\mathrm{BCI}_{\rm CO}^{\rm VM}$		–		$0.79I_i$	$1.22I_i$	$\frac{1}{1-D_{\rm Cycle3}}V_i$	–	$\frac{N}{1-D_{\rm Cycle3}}V_i$	$2.67V_i$	$18.65V_i$
$\mathrm{BCI}_{\rm CO}^{\mathrm{SC}(D)}$		(38)		$0.82I_i$	$0.87I_i$	$\frac{1}{1-D_{Cycle4}}V_i$	$\frac{1}{1-D_{Cycle4}}V_i$	$\frac{N}{1-D_{Cycle4}}V_i$	$3V_i$	$15V_i$
$\mathrm{BCI}_{\rm CO}^{\mathrm{SC}(D)+\mathrm{VM}}$		(38)		$0.74I_i$	$1.30I_i$	$\frac{1}{1-D_{\rm Cycle5}}V_i$	$\frac{1}{1-D_{\rm Cycle5}}V_i$	$\frac{N}{1-D_{\rm Cycle5}}V_i$	$2V_i$	$18V_i$

It can be seen that the current stress across the switch S is a function of the converter input current (I_i) and duty-cycle. Hence, since the duty-cycle is defined in Table III for each converter, it can be observed that it will be smaller for the smaller duty-cycle. This way, a decrease of current stress may result in a reduction on their conduction losses.

The total voltage stress on the switch ($\mathrm{TV}_S S$) and the total voltage stress on the diodes ($\mathrm{TV}_D S$) are the sum of the stresses across each switch and each of the converter diodes [82]. They are calculated, respectively, by

$$\mathrm{TV}_S S = \sum_{S_1}^{S_n} \mathrm{SV}_S \tag{19}$$

$$\mathrm{TV}_D S = \sum_{D_1}^{D_n} \mathrm{SV}_D \tag{20}$$

where SV_S and SV_D are the voltage stress on the switch and diodes, respectively, S switch, D diodes, and $1 \ldots n$ number of components.

It can be seen that the voltage stress across the switch *S* is a function of the converter input voltage (V_i) and duty-cycle. Hence, since the duty-cycle is defined in Table III for each converter, it can be observed that it will be smaller for the smaller duty-cycle. In other words, the inclusions of voltage step-up techniques reduce the converter duty-cycle and, consequently, the switch stresses are also reduced. This feature is important for MOSFET technology as long as the ON state resistance of these transistors is proportional to their breakdown voltage.

Finally, the current stress on the inductor L is given by (41) for simple inductor converters, and can also be approximate by it for all CI topologies. It can be observed that it is a function of the input current ($I_i = P_i/V_i$), the input voltage V_i, inductance L, switching frequency f_s, and duty-cycle. This way, as long as inductance *L* is designed by a specific current ripple, keeping all operating specifications identical for all evaluated topologies, the current stress will be exactly the same.

Conversely, the voltage stress across the capacitors of each topology can be computed by (44). It can be seen that it is identical to the voltage stress of its neighbor diode, according to Table III.

E. Converter Estimated Losses and Efficiencies

The component stresses were evaluated in the previous sections, showing that the reduction in duty-cycle provides lower stresses. In this section, the main loss mechanisms for the topologies in analysis are evaluated in order to verify the effectiveness of the inclusion of step-up voltage techniques in the reduction of converter losses and, consequently, the improvement of converter efficiency.

It is assumed that all topologies will operate under the specifications presented in Table IV. Hence, the converters' active and passive components are designed according to ordinary switching power supply design methodologies, such as those described in power electronics text books (for instance [81]). Taking into account that the topologies operate in CCM and applying the abovementioned reference design, the values for all components of each converter are also summarized in Table V. Electric current and voltage variables of the converters were obtained using PSIM simulation software. The switching losses are obtained considering the switching behavior with piecewise linear approximations and, thus applying the simple integral equation of device voltage and current variables during the switching intervals as

$$P_{\rm Sw} = 0.5 f_s V_s \left[I_s \left(t_{\rm off} + t_{\rm on} \right) + C_{\rm oss} \right] \tag{21}$$

where $t_{\rm on}$ and $t_{\rm off}$ were estimated by the rise and fall times provided in the device manufacture datasheet. Additionally, the turn-ON capacitive losses are included as long as this loss mechanism is significant to MOS gate devices.

Semiconductor conduction losses can be separated into switch ON-state losses (27) and diode conduction losses (28)

$$P_{\rm Scon} = {I_{S\_\rm rms}}^2 R_{\rm DS(on)} \tag{22}$$

where $I_{S_{\rm rms}}$ is the switch root mean square (rms) current and $R_{\rm DS(on)}$ is the MOSFET ON-state resistance obtained from device static characteristics provided by manufacture datasheet information

$$P_D = \sum_{k=1}^{K} {I_{D\rm rms(k)}}^2 r_{D(k)} \tag{23}$$

where $I_{D\rm rms}$ is the rms current and r_D is the conduction resistance of the kth converter diode. Resistance r_D is calculated

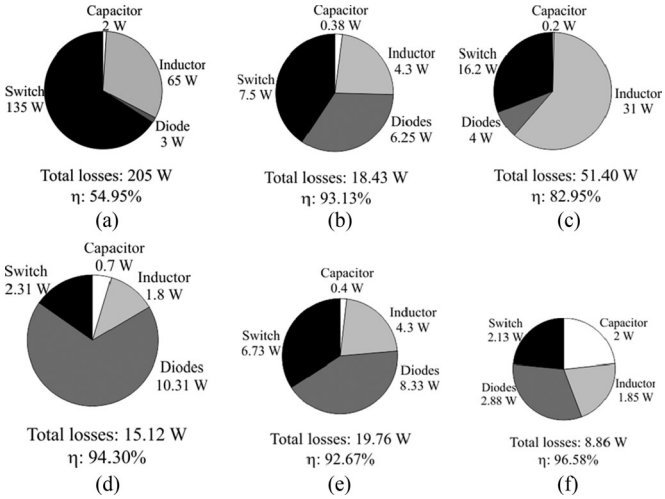

Fig. 12. Power converter loss distribution and efficiencies. (a) Boost. (b) $\mathrm{BCI}_{\mathrm{CO}}$. (c) $B^{\mathrm{SC}(D)}$. (d) $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{VM}}$. (e) $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)}$. (f) $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+\mathrm{VM}}$.

from diode static characteristics given by the manufacture datasheet.

As long as the copper wire diameters obey the limits imposed by the skin effect, magnetic device losses for inductors and CIs can be categorized into copper and core losses, as suggested by expression (29). Additionally, the leakage inductance of CIs that are effectively in series with a switching element lose their stored energy when the switch turns OFF. This energy must be added as an additional inductor loss if no circuit technique is used to recycle the energy

$$P_L = \sum_{j=1}^{J} r_{L(j)} {I_{L\mathrm{rms}(j)}}^2 + \sum_{h}^{H} \left(a {B_{\mathrm{pk}(h)}}^b {f_s}^c\right) A_{e(h)} l_{e(h)} + \frac{1}{2} f_s L_k {I_{L\mathrm{peak}}}^2 \tag{24}$$

where $I_{L\mathrm{rms}}$ is the rms current of the jth magnetic device winding; B_{pk} is the ac magnetic flux density for the hth magnetic device core; and l_e is the core medium path length MPL and A_e is the transversal core area, both given in the manufacture core information [83]. Eq. (25)–(29) are shown in the Table III.

Finally, capacitor losses can be regarded as the power dissipated due to their equivalent series resistance (ESR). These losses can be summarized as

$$P_C = \sum_{g=1}^{G} {I_{C\mathrm{rms}(g)}}^2 \mathrm{ESR}_{(g)} \tag{30}$$

where $I_{C\mathrm{rms}}$ is the rms current and ESR the measured resistance of the gth capacitor.

Total estimated losses and their distribution, for all evaluated converters, are shown in Fig. 12.

The estimated efficiency is given by

$$\eta = P_o / (P_o + (P_{\mathrm{scon}} + P_{\mathrm{Sw}} + P_D + P_L + P_C)). \tag{31}$$

From Fig. 12(a), it can be noted that in the boost converter, the higher duty-cycle value of 0.9 yields large losses on the switch and inductor, with losses reaching 205 W and an estimated efficiency of only 54.95%. Fig. 12(b) shows that the losses on switch and inductor are greatly reduced with the inclusion of the CI. However, the duty-cycle reduction is accompanied by an increase in diode and capacitor losses. However, in general, the losses for $\mathrm{BCI}_{\mathrm{CO}}$ are 18.43 W, with an estimated efficiency of 93.13%. When the CI is replaced by the VM ($B^{\mathrm{SC}(D)}$), inductor losses are more prominent and the total losses are 51.40 W, giving an efficiency of 82.95%, showing that the CI is more effective than the VM alone. In Fig. 12(d), the breakdown losses of converter $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{VM}}$ show that switch and inductor losses can be further reduced with the inclusion of two voltage step-up techniques. With this approach, the total losses reach 15.12 W with an estimated efficiency of 94.30%. Analogously, Fig. 12(e) shows that converter $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)}$ yields a total of 19.76 W of losses and an efficiency of 92.67%. The major losses on the switch are caused by the capacitor's high charging currents. Finally, in Fig. 12(f), converter $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$ presents a reduction of the inductor losses since the leakage energy is recycled by the secondary winding VM. This way, even though capacitor losses increase, the total losses are smaller for this topology, with 8.86 W of losses and efficiency of 96.58% achieved. It can also be noted that losses are more equally distributed when compared to other converters.

F. Component Count and Relative Cost

As demonstrated in the previous sections, the inclusion of one, two, and three voltage step-up techniques improved the performance of the converters. However, there are drawbacks since each voltage step-up technique relies on the addition of some passive circuit components such as, capacitors, inductors, and diodes. In order to measure this disadvantage, Fig. 13(a) shows a comparison of the component count of the converters. As can be seen, the boost and $\mathrm{BCI}_{\mathrm{CO}}$ converter have the smallest number of components while the $\mathrm{BCI}_{CO}^{SC(D)+VM}$ converter has the largest component count.

The ratings of electrical device cost are dictated by various agreements and regulations. The continuous current rating and the voltage rating are directly used to design the eletrical device, so the relative cost can be estimated.

The relative cost of the switch is

$$\mathrm{CR}_S = \frac{I_S V_S}{I_{S\_b} V_{S\_b}} 100 \tag{32}$$

where I_S is the switch current rating, which is the rms current given in Appendix A; V_S is the switch voltage rating, which is the maximum voltage given in Appendix A; I_{S_b} is the switch current rating of the boost converter, which is the rms current given in Appendix A; and V_{S_b} is the switch voltage rating of the boost converter, which is the maximum voltage given in Appendix A.

The relative cost of the diodes is

$$\mathrm{CR}_D = \frac{I_D V_D}{I_{D\_b} V_{D\_b}} 100 \tag{33}$$

where I_D is the diode current rating, which is the rms current given in Appendix A; V_D is the switch voltage rating, which is the maximum voltage given in Appendix A; I_{D_b} is the diode

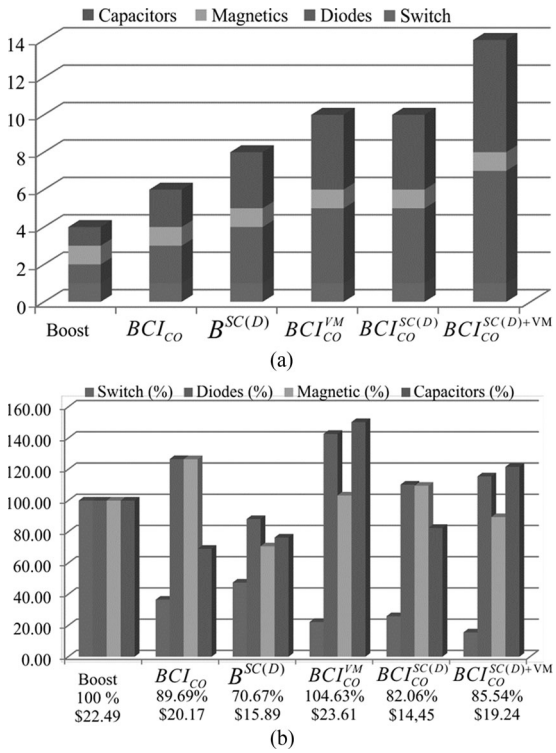

Fig. 13. Value (a) Component count. (b) Relative cost (% and US$).

current rating of the boost converter, which is the rms current given in Appendix A; and V_{D_b} is the diode voltage rating of the boost converter, which is the maximum voltage given in Appendix A.

The relative cost of the inductor

$$\mathrm{CR}_L = \frac{I_L V_L}{I_{L\_b} V_{L\_b}} 100 \tag{34}$$

where I_L is the inductor current rating, which is the rms current given in Appendix A; V_L is the switch voltage rating, which is the rms voltage of the inductor $V_{L\,\mathrm{rms}} = \frac{V_i}{\sqrt{1-D}}$; I_{L_b} is the diode current rating of the boost converter, which is the rms current given in Appendix A; V_{L_b} is the diode voltage rating of the boost converter, which is the rms voltage of the inductor.

The relative cost of the capacitors is

$$\mathrm{CR}_C = \frac{I_C V_C}{I_{C\_b} V_{C\_b}} 100 \tag{35}$$

where I_C is the capacitor current rating, which is the rms current given in Appendix A; V_C is the capacitor voltage rating, which is the maximum voltage given in Appendix A; I_{C_b} is the capacitor current rating of the boost converter, which is the rms current given in Appendix A; V_{C_b} is the capacitor voltage rating of the boost converter, which is the maximum voltage given in Appendix A.

In order to establish a cost to the boost converter prototype, the price of the boost components has been evaluated as follows [84]. The MOSFET IRFP450PBF and the diode STPSC4H065B have been choosen and thier cost is US$2.78 and US$1.61, respectively. The toroidal magnetic core 597700 from Magnetics and the electrolytic capacitor C4A THBW4900A3LJ have been chosen to implement the inductor and the output capacitor and thier cost is US$1.91 and US$8.69, repectively. For all other materials and components, a factor of 50% of the components mentioned above has been used. This way, the cost for the other prototypes also has been evaluated using the relative cost percentual, as can be seen in Fig. 14(b).

Based on these variables together with the parameters presented in Table V, Fig. 13(b) shows the relative device cost of each converter. It can be observed that the converter cost is lower than those of the other converters, which is an important feature for manufacturing large-scale production.

Table VII shows a summary of the main characteristics from all converters discussed in this section. The converters are graded as the best, in-between, and worst. Hence, one can easily address the better performance just by algebraically summing the occurrences of "best" and "worst" for each topology. It can be verified that topology presents better performance for the single PV module dc/dc converter application analyzed in this work. For other applications, or even different electric specifications, the results may vary and, thus, the performance may change from those presented in Table VII.

IV. Experimental Results

In order to verify the effectiveness of the converters shown in Fig. 1, five 250 W prototypes for $\mathrm{BCI}_{\mathrm{CO}}$, $B^{\mathrm{SC}(D)}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{VM}}$, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)}$, and $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$ converters were built in the lab. The main components and parameters of the prototypes are summarized in Table IV. Besides the converter hardware, the additional specifications for the set-up are the input voltage source E4360A from Agilent; electronic load 3252 A from PRODIGIT; and PWM generator DSP TMS320F28335 from TI. The measurement equipment included the oscilloscope Tektronix Encore MD03000 and the power meter Yokogawa WT1800.

Fig. 14 shows the following waveforms for the five prototypes: PWM control signal at MOSFET gate–source terminals V_{gs} (upper trace), output voltage V_o (middle-upper trace), capacitor C_2 voltage V_{C2} (middle-lower trace), and input voltage V_i (lower trace). From Fig. 15(a), it can be seen that, for the prototype of the $\mathrm{BCI}_{\mathrm{CO}}$ converter, for an input voltage of 25 V and a duty-cycle of approximately 0.75, the voltage across C_2 reaches 100 V while the output voltage reaches 250 V, confirming the designed voltage gain equal to 10. Fig. 14(b) shows that, for the same voltage gain in the prototype of the $B^{\mathrm{SC}(D)}$ converter, the voltage across C_2 reaches 125 V at a duty-cycle of 0.8. On the other hand, Fig. 14(c) shows that the $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{VM}}$ prototype has a reduction of the voltage across C_2, achieving 67 V as well as a duty-cycle reduction ($D = 0.625$). From Fig. 14(d), it can be seen that for the $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)}$ prototype, the voltage across C_2 increases slightly, reaching 75 V at a duty-cycle of 0.667. Finally, Fig. 14(e), for the $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$ prototype, shows that the voltage across C_2 reaches only 50 V at a duty-cycle of 0.5.

In order to assess the voltage stress on the semiconductor, Fig. 15 shows the following waveforms: a PWM control signal at MOSFET gate–source terminals V_{gs} (upper trace), voltage across the MOSFET drain–source terminals (middle-upper trace), voltage across anode–cathode terminals of diode D_{of} . $V_{D\mathrm{of}}$

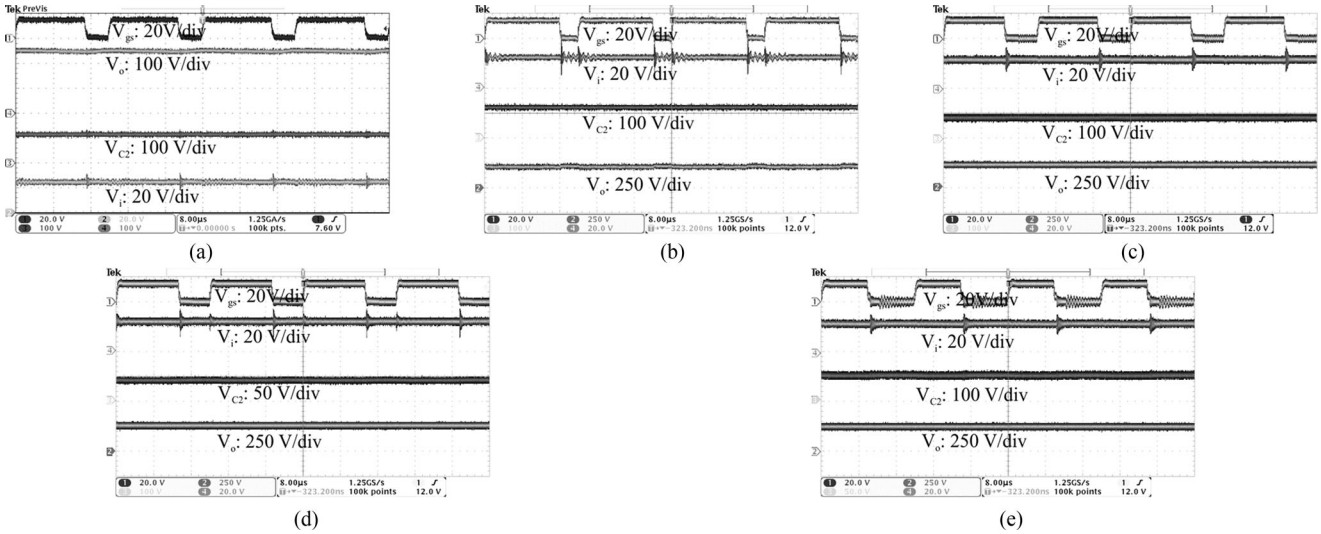

Fig. 14. Waveforms of $V_{\rm gs}$, V_o, V_{C2}, V_i for (a) $\mathrm{BCI_{CO}}$, (b) $B^{\mathrm{SC}(D)}$, (c) $\mathrm{BCI_{CO}^{VM}}$, (d) $\mathrm{BCI_{CO}^{SC}}(D)$, and (e) $\mathrm{BCI_{CO}^{SC}}(D)+\mathrm{VM}$.

TABLE VII
SUMMARY OF CHARACTERISTICS OF THE EVALUATED CONVERTERS

Converters	Features				
	Static Voltage Gain	CSF	Component Count	Relative Cost	Efficiency
$\mathrm{BCI_{CO}}$	Worst	In-between	Best	Worst	In-between
$B^{\mathrm{SC}(D)}$	In-between	Worst	In-between	Best	Worst
$\mathrm{BCI_{CO}^{VM}}$	In-between	In-between	In-between	In-between	In-between
$\mathrm{BCI_{CO}^{SC}}(D)$	In-between	In-between	In-between	In-between	In-between
$\mathrm{BCI_{CO}^{SC}}(D)+\mathrm{VM}$	Best	Best	Worst	In-between	Best

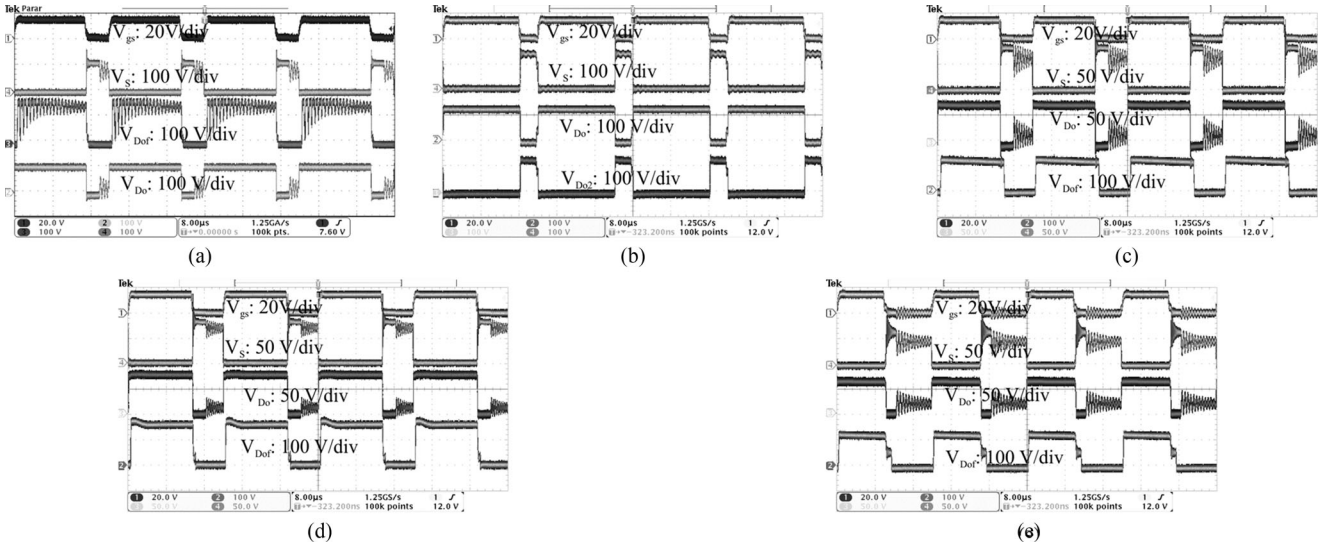

Fig. 15. Waveforms of $V_{\rm gs}$, V_s, $V_{D\rm of}$, and V_{Do} for (a) $\mathrm{BCI_{CO}}$, (b) $B^{\mathrm{SC}(D)}$, (c) $\mathrm{BCI_{CO}^{VM}}$, (d) $\mathrm{BCI_{CO}^{SC}}(D)$, and (e) $\mathrm{BCI_{CO}^{SC}}(D)+\mathrm{VM}$.

(middle-lower trace), and across anode–cathode terminals of diode D_o . V_{Do} (lower trace). Fig. 15(a) shows that for the $\mathrm{BCI_{CO}}$ prototype, the voltage stresses are higher for diode $D_{\rm of}$ (180 V) and equal for the MOSFET (100 V) and diode D_o (100 V). In Fig. 15(b) ($B^{\mathrm{SC}(D)}$ prototype), it can be seen that all voltage stresses are higher, reaching 125 V for both diode D_o and MOSFET; and 250 V for diode D_{o2}. Fig. 15(c) of the $\mathrm{BCI_{CO}^{VM}}$ prototype shows that voltage stresses decrease to 67 V for diode D_o and MOSFET, reaching 125 V across diode $D_{\rm of}$. On the other hand, for the $\mathrm{BCI_{CO}^{SC}}(D)$ prototype [see Fig. 15(d)] they

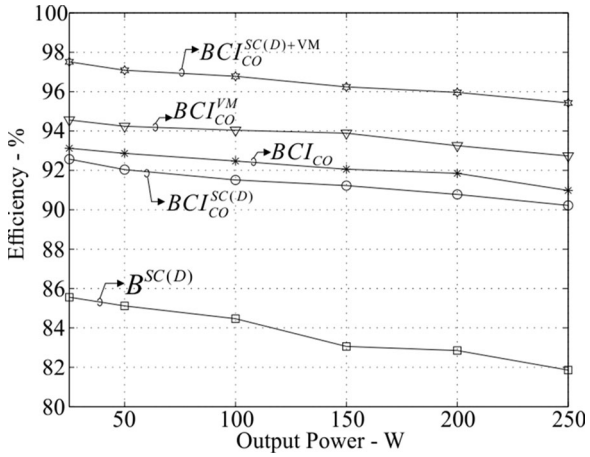

Fig. 16. Efficiency of topologies for different output powers.

are higher, reaching 75 V for MOSFET and diode D_o and 150 V across diode $D_{\rm of}$. The smallest voltage stresses are presented by the $\rm BCI_{CO}^{SC(D)+VM}$ prototype [see Fig. 15(e)] with 50 V stress across both MOSFET and diode D_o and 100 V across diode $D_{\rm of}$.

Fig. 16 shows the measured efficiency of the prototypes evaluated experimentally as a function of output power. As can be seen, the $\rm BCI_{CO}^{SC(D)+VM}$ prototype presents the highest efficiency, reaching 95.8% at full-load and maintaining an efficiency above 96% from zero to 200 W of load. The second highest efficiency is achieved by the $\rm BCI_{CO}^{VM}$ prototype. This topology provides a 92.73% efficiency at full-load and maintains an efficiency above 94% from zero to 150 W of load. The third highest efficiency is achieved by the $B^{\rm SC(F)}$ prototype, with 90.98% efficiency at full-load and maintaining efficiency above 92% from zero to 150 W of load. The $\rm BCI_{CO}^{SC(D)}$ prototype presents the fourth highest efficiency, with a full-load efficiency of 90.42% and an efficiency higher than 91% from zero to 150 W of load. The lowest efficiency is presented by the $B^{\rm SC(F)}$ prototype.

V. Conclusion

This paper presented and discussed a novel synthesis methodology for developing very high step-up dc–dc converters. The methodology is based on the boost converter with the inclusion of three different voltage step-up techniques: CI; the VM circuit; and SCs also referred as charge pumps. Aiming to address the advantages and limitations for the converters derived from the proposed synthesis methodology, a comparative analysis among of some important converters has been carried out. It comprised aspects such as voltage gain, voltage stress, CSF, component count, and relative cost. Results from 250 W prototypes designed according to PV ac-module specifications have been obtained experimentally to validate the theoretical analyses. The results demonstrate that topology "CI VM Dickson charge pump boost converter with cascaded outputs" presents better performance for the single PV module dc/dc converter application analyzed in this work. Hence, the combination of the three studied techniques provides the best trend off on the comparative analysis carried out in this work.

Appendix A

Generalized equations are represented for the converters shown in Fig. 1.

The rms value of the switch current is given by

$$I_{s\_\rm rms} = \sqrt{D_{\rm Cycle}} I_i \left(1-D_{\rm Cycle}\right) \sqrt{1+\frac{1}{12}\left(\frac{D_{\rm Cycle} V_i}{f\, L\, I_i}\right)^2} + \alpha \tag{36}$$

where the input current is $I_i = P_i/V_i$; the parameter α is given by $\alpha = \frac{1}{2}\left(\frac{V_{C2}-V_{C1}}{R_{\rm DS(on)}+\rm RSE} e^{-\frac{DT_S}{(R_{\rm DS(on)}+\rm RSE)(C_1+C_2)}}\right)$, or it is zero for the converters without SCs.

The maximum voltage across the switch is given by

$$V_{s\_\max} = V_i (1-D_{\rm Cycle})^{-1}. \tag{37}$$

From (36) and (37), the $S_{\rm S}$CSF is calculated from (18).

To calculate the CSF of diodes, the rms value for the diode currents, disregarding the capacitor discharge, can be given by

$$I_{D\_\rm rms} = \sqrt{(1-D_{\rm Cycle})}\frac{I_i}{\beta}\sqrt{1+\frac{1}{12}\left(\frac{D_{\rm Cycle} V_i}{f\, L\, I_i}\right)^2} \tag{38}$$

where $\beta = 2N$ for the diodes of VM cells; otherwise, $\beta = 1$.

On the other hand, the diode currents of SCs are

$$I_{D\_\rm rms} = 0.5\left(V_{C2} - V_{C1} e^{-\frac{D_{\rm Cycle} T_S}{\left(R_{\rm DS(on)}+\rm RSE\right)(C_1+C_2)}}\right)\left(R_{\rm DS(on)} + \rm RSE\right)^{-1}. \tag{39}$$

The maximum voltage of diodes is

$$V_{s\_\max} = \chi V_i (1-D_{\rm Cycle})^{-1} \tag{40}$$

where $\chi = N$ for diode $D_{\rm of}$; $\chi = 2N$ for diodes of VM cells, and $\chi = 1$ for the other diodes.

From this, it is possible to calculate the $S_{\rm D}$CSF using (19).

To calculate the CSF of the inductor, the rms current is given by

$$I_{L\_\rm rms} = I_i \sqrt{1+0.33(\Delta i/I_i)^2} \tag{41}$$

where $\Delta_i = D_{\rm Cycle} V_i/(f\, L)$.

While the maximum voltage of the inductor is

$$V_{L\_\max} = \delta V_i \tag{42}$$

where $\delta = N$ for the secondary CI and $\delta = 1$ for the primary CI or inductor.

From this, the S_W CSF is calculated using (20).

Finally, to calculate the CSF of capacitors, the rms current is given by

$$I_{C\_\rm rms} = I_{\rm in}\left(1-D_{\rm Cycle}\right)\sqrt{\varphi}\,(\varepsilon)^{-1} \tag{43}$$

where $\varepsilon = ND$ for the capacitors of VM cells and C_o and $\varepsilon = 1$ for the other capacitors while the maximum voltages of capacitors are

$$V_{C\_\max} = \gamma V_i \tag{44}$$

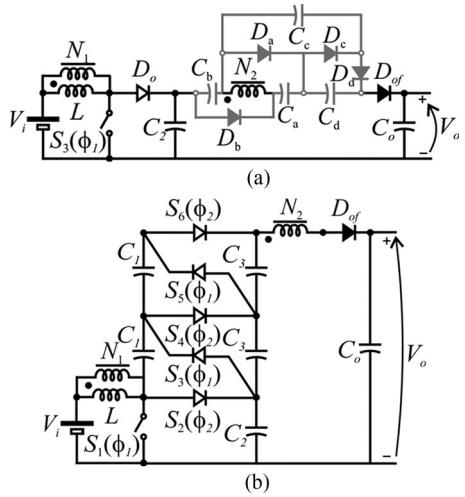

Fig. 17. Other possible variations. (a) $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{VM}}$. (b) $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$.

where $\gamma = N$ for the capacitors of VM cells, $\gamma = ND_{\mathrm{Cycle}}(1-D_{\mathrm{Cycle}})^{-1}$ for the capacitor C_o, and $\gamma = (1-D_{\mathrm{Cycle}})^{-1}$ for the other capacitors.

From this, S_CCSF is calculated using (21).

APPENDIX B

In Section III-D, the current and voltage stress on components has been discussed for the five topologies presented in Fig. 1. Since these converters make use of one, two, or three different voltage step-up techniques, the component count of each topology is different from the others. Thus, intending to make a comparison according to the converters component count, this section presents two novel circuits both with the same component count as the CI VM + SC(D) boost converter with cascaded outputs $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$ [see Fig. 1(e)]. The two converters are $\mathrm{BCI}_{\mathrm{CO}}^{2VM}$ [see Fig. 17(a)] and $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$ [see Fig. 17(b)]. The former is derived from an expansion of the VM circuit of $\mathrm{BCI}_{\mathrm{CO}}^{VM}$ [see (Fig. 1(c)], and the latter is derived from an expansion of the Dickson SC circuit of $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)}$ [see Fig. 1(d)]. Table VII summarizes the main parameters of the three topologies. It can be seen that the number of switches, capacitors, diodes, and windings in the CI is exactly the same for all converters. The static voltage gain for each topology is also provided. The static voltage gain for the $\mathrm{BCI}_{\mathrm{CO}}^{2VM}$ converter is obtained from (2) by using the parameter $k_{\mathrm{VM}} = 1.5$. Analogously, the static voltage gain for the $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$ converter is obtained from (8) by using the parameter $k_{\mathrm{CW}} = 2$. Compared to the static voltage of the $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$ converter, it can be shown that the converter $\mathrm{BCI}_{\mathrm{CO}}^{2VM}$ always achieves slightly higher value for any given duty-cycle. On the other hand, the converter $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$ only achieves *M* with higher values, for duty-cycles between 0.75 and the unity.

Comparing the topologies for the same operating specifications defined in Section III, the following duty-cycle has been computed, $D_{\mathrm{cycle6}} = 0.375$ and $D_{\mathrm{cycle7}} = 0.583$, for $\mathrm{BCI}_{\mathrm{CO}}^{2VM}$ and $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$, respectively. This way, the current and voltage stresses across the semiconductor devices are evaluated.

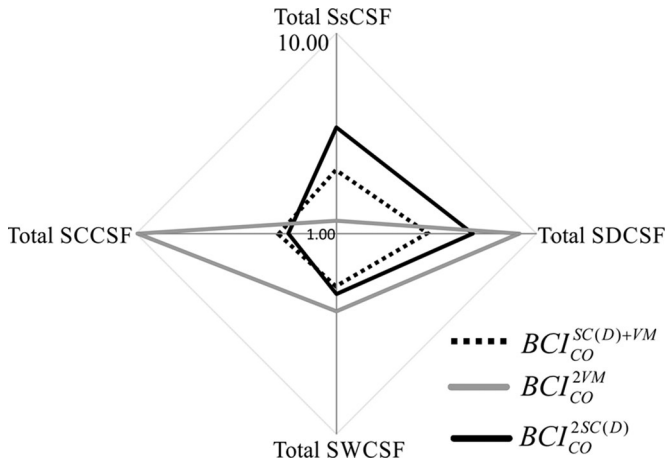

Fig. 18. Diagram for the component stress factor.

TABLE VIII
TOPOLOGIES WITH THE SAME COMPONENT COUNT

	$\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+\mathrm{VM}}$	$\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{VM}}$	$\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$
Parameter	Fig. 1(e)	Fig. 17(a)	Fig. 17(b)
No. of switches	1	1	1
No. of diodes	6	6	6
No. of capacitors	6	6	6
No. of windings	2	2	2
Value of constant	$k_{\mathrm{VM}} = \mathrm{k_{CW}} = 1$	$k_{\mathrm{VM}} = 1.5$	$\mathrm{k_{CW}} = 2$
Static voltage gain M	(12)	$\frac{1+N(3-D_{\mathrm{cycle}})}{1-D_{\mathrm{cycle}}}$	$\frac{3+ND_{\mathrm{cycle}}}{1-D_{\mathrm{cycle}}}$

Fig. 18 shows the CSF of each converter presented in Table VIII. It can be seen that the CSF of switches, capacitors, diodes, and windings in the CI. Comparing the topologies for the same operating specifications defined in Section III, the following S_SCSF have been computed: 1) Total S_SCSF $= 2.13$ for $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$; 2) Total S_SCSF $= 1.16$ for $\mathrm{BCI}_{\mathrm{CO}}^{2VM}$; and 3) Total S_SCSF $= 3.39$ for $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$. To evaluate the current and voltage stress across the diodes, S_DCSF have been computed and results are 1) Total S_DCSF $= 2.88$ for $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$; 2) Total S_DCSF $= 8.2$ for $\mathrm{BCI}_{\mathrm{CO}}^{2VM}$; and 3) Total S_DCSF $= 4.8$ for $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$. The stress concerning the windings of the CI, the SWCSF have been computed, yielding in 1) Total S_WCSF $= 1.85$ for $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$; 2) Total S_WCSF $= 2$ for $\mathrm{BCI}_{\mathrm{CO}}^{2VM}$; and 3) Total S_WCSF $= 2.44$ for $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$. Finally, to stress of the capacitor, S_CCSF have been computed as 1) Total S_CCSF $= 2$ for $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$; 2) Total S_CCSF $= 1.74$ for $\mathrm{BCI}_{\mathrm{CO}}^{2VM}$; and 3) Total S_CCSF $= 9.88$ for $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$. As it can be seen by Fig. 18, the $\mathrm{BCI}_{\mathrm{CO}}^{2VM}$ converter presents the small S_SCSF. Nevertheless, all the other evaluated factors increase, which may jeopardize the benefits of it. On the contrary, $\mathrm{BCI}_{\mathrm{CO}}^{2\mathrm{SC}(D)}$ presents small S_CCSF; meanwhile, $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$ presents small S_WCSF and S_DCSF. Thus, it may be concluded that in general, the stresses are smaller for the $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)+VM}$ converter. Hence, in spite of adding components to provide the

same component count to $\mathrm{BCI}_{\mathrm{CO}}^{VM}$ and $\mathrm{BCI}_{\mathrm{CO}}^{\mathrm{SC}(D)}$, the use of three different voltage step-up techniques still provides best performance concerning the CSF.

REFERENCES

[1] K. C. Tseng, C. A. Cheng, and C. T. Chen, "High step-up interleaved boost converter for distributed generation using renewable and alternative power sources," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 713–722, Jun. 2017.

[2] X. Hu, G. Dai, L. Wang, and C. Gong, "A three-state switching boost converter mixed with magnetic coupling and voltage multiplier techniques for high gain conversion," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2991–3001, Apr. 2016.

[3] H. Liu, F. Li, and J. Ai, "A novel high step-up dual switches converter with coupled inductor and voltage multiplier cell for a renewable energy system," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4974–4983, Jul. 2016.

[4] N. Vázquez, F. Medina, C. Hernández, J. Arau, and E. Vázquez, "Double tapped-inductor boost converter," *IET Power Electron.*, vol. 8, no. 5, pp. 831–840, May 2015.

[5] A. Mohammadpour, L. Parsa, M. H. Todorovic, R. Lai, R. Datta, and L. Garces, "Series-input parallel-output modular-phase dc–dc converter with soft-switching and high-frequency isolation," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 111–119, Jan. 2016.

[6] S. Y. Cho, I. O. Lee, J. K. Kim, and G. W. Moon, "A new standby structure based on a forward converter integrated with a phase-shift full-bridge converter for server power supplies," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 336–346, Jan. 2013.

[7] J. H. Lee, T. J. Liang, and J. F. Chen, "Isolated coupled-inductor integrated dc–dc converter with non-dissipative snubber for solar energy applications," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3337–3348, Jul. 2014.

[8] T. J. Liang, J. H. Lee, S. M. Chen, J. F. Chen, and L. S. Yang, "Novel isolated high-step-up dc–dc converter with voltage lift," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1483–1491, Apr. 2013.

[9] H. Hu *et al.*, "A three-port flyback for PV microinverter applications with power pulsation decoupling capability," *IEEE Trans. Power Electron.*, vol. 27, no. 9, pp. 3953–3964, Sep. 2012.

[10] A. Abramovitz, J. Yao, and K. Smedley, "Unified modeling of PWM converters with regular or tapped inductors using TIS-SFG approach," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1702–1716, Feb. 2016.

[11] D. A. Grant, Y. Darroman, and J. Suter, "Synthesis of tapped-inductor switched-mode converters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1964–1969, Sep. 2007.

[12] W. Li and X. He, "ZVT interleaved boost converters for high-efficiency, high step-up dc–dc conversion," *IET Electr. Power Appl.*, vol. 1, no. 2, pp. 284–290, Mar. 2007.

[13] W. Li and X. He, "High step-up soft switching interleaved boost converters with cross-winding-coupled inductors and reduced auxiliary switch number," *IET Power Electron.*, vol. 2, no. 2, pp. 125–133, Mar. 2009.

[14] C. Y. Yang, M. C. Chen, T. H. Ho, J. Y. Lin, Y. C. Hsieh, and H. J. Chiu, "High step-up voltage-doubling dc-dc converter with coupled inductors," in *Proc. IEEE 8th Int. Power Electron. Motion Control Conf.*, 2016, pp. 429–432.

[15] Q. Zhao and F. C. Lee, "High-efficiency, high step-up dc –dc converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 65–73, Jan. 2003.

[16] K. C. Tseng and T. J. Liang, "Novel high-efficiency step-up converter," *IEE Proc. Electr. Power Appl.*, vol. 151, no. 2, pp. 182–190, Mar. 2004.

[17] A. A. A. Freitas, F. L. Tofoli, E. M. S. Júnior, S. Daher, and F. L. M. Antunes, "High-voltage gain dc–dc boost converter with coupled inductors for photovoltaic systems," *IET Power Electron.*, vol. 8, no. 10, pp. 1885–1892, Oct. 2015.

[18] L. Schmitz, R. F. Coelho, and D. C. Martins, "High step-up high efficiency dc-dc converter for module-integrated photovoltaic applications," in *Proc. IEEE 13th Braz. Power Electron. Conf. 1st Southern Power Electron. Conf.*, 2015, pp. 1–6.

[19] S. M. Chen, T. J. Liang, L. S. Yang, and J. F. Chen, "A boost converter with capacitor multiplier and coupled inductor for ac module applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1503–1511, Apr. 2013.

[20] K. I. Hwu, W. Z. Jiang, and L. C. Yang, "High-step-up single-switch dc–dc converter with low voltage spike," *IET Power Electron.*, vol. 8, no. 12, pp. 2504–2510, Dec. 2015.

[21] I. Laird and D. D. Lu, "High step-up dc/dc topology and MPPT algorithm for use with a thermoelectric generator," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3147–3157, Jul. 2013.

[22] R. J. Wai, C. Y. Lin, C. Y. Lin, R. Y. Duan, and Y. R. Chang, "High efficiency power conversion system for kilowatt-level stand-alone generation unit with low input voltage," *IEEE Trans. Ind. Electron.*, vol. 55, no. 10, pp. 3702–3714, Oct. 2008.

[23] Z. Chen and J. Xu, "High boost ratio dc–dc converter with ripple-free input current," *Electron. Lett.*, vol. 50, no. 5 pp. 353–355, Feb. 2014.

[24] Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "Novel high step-up dc–dc converter for distributed generation system," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1473–1482, Apr. 2013.

[25] J. R. Dreher, F. Marangoni, J. L. R. Ortiz, M. L. da S. Martins, H. T. Camara, and L. D. Flora, "High step-up voltage gain integrated dc/dc converters," in *Proc. IEEE 3rd Inter. Symp. Power Electron. Distrib. Gener. Syst.*, 2012, pp. 125–132.

[26] W. J. Cha, Y. W. Cho, J. M. Kwon, and B. H. Kwon, "Highly efficient microinverter with soft-switching step-up converter and single-switch modulation inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 6, pp. 3516–3523, Jun. 2015.

[27] K. C. Tseng, J. Z. Chen, J. T. Lin, C. C. Huang, and T. H. Yen, "High step-up interleaved forward-flyback boost converter with three-winding coupled inductors," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4696–4703, Sep. 2015.

[28] R. J. Wai, C. Y. Lin, R. Y. Duan, and Y. R. Chang, "High-efficiency dc-dc converter with high voltage gain and reduced switch stress," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 354–364, Feb. 2007.

[29] F. Hwang, Y. Shen, and S. H. Jayaram, "Low-ripple compact high-voltage dc power supply," *IEEE Trans. Ind. Appl.*, vol. 42, no. 5, pp. 1139–1145, Sep./Oct. 2006.

[30] A. H. Falkner, "Generalised Cockcroft-Walton voltage multipliers," *Electron. Lett.*, vol. 9, no. 25, pp. 585–586, 1973.

[31] J. Wang, S. W. H. de Haan, and J. A. Ferreira, "Detailed derivation and minimization of the equivalent parasitic capacitances of a high-voltage multiplier based on the complete model," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 362–372, Jan./Feb. 2015.

[32] L. Muller and J. W. Kimball, "High gain dc–dc converter based on the Cockcroft–Walton multiplier," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6405–6415, Sep. 2016.

[33] M. Uno and K. Tanaka, "Single-switch multioutput charger using voltage multiplier for series-connected lithium-ion battery/supercapacitor equalization," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3227–3239, Aug. 2013.

[34] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and Roger Gules, "Voltage multiplier cells applied to non-isolated dc–dc converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 871–887, Mar. 2008.

[35] K. C. Tseng, C. C. Huang, and C. A. Cheng, "A high step-up converter with voltage-multiplier modules for sustainable energy applications," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 3, no. 4, pp. 1100–1108, Dec. 2015.

[36] L. W. Zhou, B. X. Zhu, Q. M. Luo, and S. Chen, "Interleaved non-isolated high step-up dc/dc converter based on the diode–capacitor multiplier," *IET Power Electron.*, vol. 7, no. 2, pp. 390–397, Feb. 2014.

[37] Y. Hu, W. Xiao, W. Li, and X. He, "Three-phase interleaved high-step-up converter with coupled-inductor-based voltage quadrupler," *IET Power Electron.*, vol. 7, no. 7, pp. 1841–1849, Jul. 2014.

[38] T. Nouri, S. H. Hosseini, E. Babaei, and J. Ebrahimi, "Interleaved high step-up dc–dc converter based on three-winding high-frequency coupled inductor and voltage multiplier cell," *IET Power Electron.*, vol. 8, no. 2, pp. 175–189, Feb. 2015.

[39] W. Li, Y. Zhao, Y. Deng, and X. He, "Interleaved converter with voltage multiplier cell for high step-up and high-efficiency conversion," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2397–2408, Sep. 2010.

[40] C. S. Leu and M. H. Li, "A novel current-fed boost converter with ripple reduction for high-voltage conversion applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2018–2023, Jun. 2010.

[41] C. S. Leu, P. Y. Huang, and M. H. Li, "A novel dual-inductor boost converter with ripple cancellation for high-voltage-gain applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1268–1273, Apr. 2011.

[42] C. S. Leu and P. Y. Huang, "A novel voltage doubler rectifier for high output voltage applications," in *Proc. Int. Power Electron. Conf.*, 2010, pp. 2082–2085.

[43] T. J. Liang, S. M. Chen, L. S. Yang, J. F. Chen, and A. Ioinovici, "Ultra-large gain step-up switched-capacitor dc-dc converter with coupled inductor for alternative sources of energy," *IEEE Trans. Circuits Syst.—I: Regul. Pap.*, vol. 59, no. 4, pp. 864–874, Apr. 2012.
[44] Y. Tang, T. Wang, and Y. He, "A switched-capacitor-based active-network converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2959–2968, Jun. 2014.
[45] F. L. Luo, "Six self-lift dc-dc converters, voltage lift technique," *IEEE Trans. Ind. Electron.*, vol. 48, no. 6, pp. 1268–1272, Dec. 2001.
[46] F. L. Luo, "Seven self-lift dc-dc converters, voltage lift technique," *IEE Proc. Electr. Power Appl.*, vol. 148, no. 4, pp. 329–338, Jul. 2001.
[47] T. Tanzawa, "Innovation of switched-capacitor voltage multiplier: P. 1: A brief history," *IEEE Solid-State Circuits Mag.*, vol. 8, no. 1, pp. 51–59, 2016.
[48] T. Tanzawa, "Innovation of switched-capacitor voltage multiplier: P. 2: Fundamentals of the charge pump," *IEEE Solid-State Circuits Mag.*, vol. 8, no. 2, pp. 83–92, 2016.
[49] B. P. Baddipadiga and M. Ferdowsi, "A high-voltage-gain dc-dc converter based on modified Dickson charge pump voltage multiplier," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7707–7715, Oct. 2015.
[50] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc–dc PWM converters," *IEEE Trans. Circuits Syst. I: Regul. Pap.*, vol. 55, no. 2, pp. 687–696, Mar. 2008.
[51] D. F. Cortez, G. Waltrich, J. Fraigneaud, H. Miranda, and I. Barbi, "DC–DC converter for dual-voltage automotive systems based on bidirectional hybrid switched-capacitor architectures," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 3296–3304, May 2015.
[52] M. Chen, K. Li, J. Hu, and A. Ioinovici, "Generation of a family of very high dc gain power electronics circuits based on switched-capacitor-inductor cells starting from a simple graph," *IEEE Trans. Circuits Syst. I: Regul. Pap.*, vol. 63, no. 12, pp. 2381–2392, Dec. 2016.
[53] B. Wu, S. Li, K. M. Smedley, and S. Singer, "A family of two-switch boosting switched-capacitor converters," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5413–5424, Oct. 2015.
[54] F. L. Luo and H. Ye, "Positive output cascade boost converters," *IEE Proc. Electr. Power Appl.*, vol. 151, no. 5, pp. 590–606, Sep. 2004.
[55] F. L. Luo and H. Ye, "Positive output super-lift converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 105–113, Jan. 2003.
[56] K. I. Hwu and T. J. Peng, "High-voltage-boosting converter with charge pump capacitor and coupling inductor combined with buck-boost converter," *IET Power Electron.*, vol. 7, no. 1, pp. 177–188, Jan. 2014.
[57] S. M. Chen, M. L. Lao, Y. H. Hsieh, T. J. Liang, and K. H. Chen, "A novel switched-coupled-inductor dc–dc step-up converter and its derivatives," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 309–314, Jan. 2015.
[58] M. C. Mira, Z. Zhang, A. Knott, and M. A. E. Andersen, "Analysis, design, modeling, and control of an interleaved-boost full-bridge three-port converter for hybrid renewable energy systems," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1138–1155, Feb. 2017.
[59] Y. F. Wang, L. K. Xue, C. S. Wang, P. Wang, and W. Li, "Interleaved high-conversion-ratio bidirectional dc–dc converter for distributed energy-storage systems - Circuit generation, analysis, and design," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5547–5561, Aug. 2016.
[60] K. C. Tseng and C. C. Huang, "High step-up, high efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1311–1319, Mar. 2014.
[61] W. Li, Y. Zhao, J. Wu, and X. He, "Interleaved high step-up converter with winding-cross-coupled inductors and voltage multiplier cells," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 133–143, Jan. 2012.
[62] S. Dwari and L. Parsa, "An efficient high-step-up interleaved dc–dc converter with a common active clamp," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 66–78, Jan. 2011.
[63] W. Li, W. Li, X. He, D. Xu, and B. Wu, "General derivation law of nonisolated high-step-up interleaved converters with built-In transformer," *IEEE Trans. Ind. Electron.*, vol. 59, no. 3, pp. 1650–1661, Mar. 2012.
[64] C. M. Lai, C. T. Pan, and M. C. Cheng, "High-efficiency modular high step-up interleaved boost converter for dc-microgrid applications," *IEEE Trans. Ind. Appl.*, vol. 48, no. 1, pp. 161–171, Jan./Feb. 2012.
[65] B. Poorali, H. M. Jazi, and E. Adib, "Single-core soft-switching high step-up three-level boost converter with active clamp," *IET Power Electron.*, vol. 9, no. 14, pp. 2692–2699, Mar. 2016.
[66] Y. Zhang, J. T. Sun, and Y. F. Wang, "Hybrid boost three-level dc–dc converter with high voltage gain for photovoltaic generation systems," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3659–3664, Aug. 2013.
[67] L. F. Costa, S. A. Mussa, and I. Barbi, "Multilevel boost dc-dc converter derived from basic double-boost converter," in *Proc. 15th Eur. Conf. Power Electr. Appl.*, 2013, pp. 1–10.
[68] F. L. de Sá, D. R. Caballero, and S. A. Mussa, "A new dc-dc double boost quadratic converter," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, 2013, pp. 1–10.
[69] O. L. Santos, L. M. Salamero, G. Garcia, H. V. Blavi, and D. A. Z. Prada, "Steady-state analysis of inductor conduction modes in the quadratic boost converter," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2253–2264, Mar. 2017.
[70] S. Zhang, J. Xu, and P. Yang, "A single-switch high gain quadratic boost converter based on voltage-lift-technique," in *Proc. 10th Int. Power Energy Conf.*, 2012, pp. 71–75.
[71] X. Hu and C. Gong, "A high voltage gain dc–dc converter integrating coupled-inductor and diode–capacitor techniques," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 789–800, Feb. 2014.
[72] Y. P. Siwakoti, P. C. Loh, F. Blaabjerg, and G. E. Town, "Y-source impedance network," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3250–3254, Jul. 2014.
[73] K. H. Liu and F. C. Lee, "Topological constraints on basic PWM converters," in *Proc. 19th IEEE Power Electron. Spec. Conf.*, 1988, pp. 164–172.
[74] J. A. Starzyk, Y. W. Jan, and F. Qiu, "A dc–dc charge pump design based on voltage doublers," *IEEE Trans. Circuits Syst. – I: Fundam. Theory Appl.*, vol. 48, no. 3, pp. 350–359, Mar. 2001.
[75] Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "Novel high step-up dc–dc converter with coupled-inductor and switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 998–1007, Feb. 2012.
[76] Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "Novel high step-up dc–dc converter with coupled-inductor and switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 998–1007, Feb. 2012.
[77] T. Tanzawa, "On two-phase switched-capacitor multipliers with minimum circuit area," *IEEE Trans. Circuits Syst. - I: Regul. Pap.*, vol. 57, no. 10, pp. 2602–2608, Oct. 2010.
[78] F. L. Luo and H. Ye, "Hybrid split capacitors and split inductors applied in positive output super-lift Luo-converters," *IET Power Electron.*, vol. 6, no. 9, pp. 1759–1768, Jun. 2013.
[79] E. Wittenbreder, "Topology selection by the numbers – Part one," Power Electron. Technol., Mar. 2006, pp. 32–36.
[80] E. Wittenbreder, "Topology selection by the numbers – part two," Power Electron. Technol., Apr. 2006, pp. 28–32.
[81] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Secaucus, NJ, USA: Kluwer, 2001.
[82] J. F. Ardashir, M. Sabahi, S. H. Hosseini, F. Blaabjerg, E. Babaei, and G. B. Gharehpetian, "Transformerless inverter with charge pump circuit concept for PV application," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. PP, no. 99, pp. 1–1, 2017.
[83] Powder Core Catalog Magnetics, Jul. 2016. [Online]. Available: www.mag-inc.com
[84] Farnell element14 | Electronic Component Distributors, Jul. 2017. [Online]. Available: http://www.newark.com

António Manuel Santos Spencer Andrade (S'15) was born in Ribeira Grande, Cabo Verde, in 1989. He received the Bachelor of Science degree in Automation and Control Engineering from the University of Caxias do Sul (UCS) in 2012, and the M.S. degree in electrical engineering in 2015 from the Federal University of Santa Maria, Santa Maria, Brazil, where he is currently working toward the Ph.D. degree.

His research interests include renewable energy, dc–dc converters, and microinverters.

Mr. Andrade is a member of the Brazilian Power Electronics Society and several IEEE Societies.

Everson Mattos (S'17) was born in Criciúma, Brazil. He received the B.Eng. and Specialization from Federal University of Santa Catarina, and the M.Sc. degree in electrical engineering from Federal University of Santa Maria.

His research interest focuses on electrical power system for nano- and picosatellites.

Luciano Schuch (S'03–M'06) received the B.S., M.S., and Ph.D. degrees from the Federal University of Santa Maria (UFSM), Santa Maria, Brazil, in 1999, 2001, and 2007, respectively, all in electrical engineering (subarea power electronics).

Since 2009, he has been with the UFSM, where he is currently a Professor. His research interests include photovoltaic systems, UPS, and high-performance power converters.

Hélio Leães Hey (M'88) received the B.S. degree from the Catholic University of Pelotas, Pelotas, Brazil, in 1985, and the M.S. and Ph.D. degrees from the Federal University of Santa Catarina, Santa Catarina, Brazil, in 1987 and 1991, respectively.

From 1989 to 1993, he was with the Federal University of Uberlândia, Uberlândia, Brazil. Since 1994, he has been with the Federal University of Santa Maria, Santa Maria, Brazil, where he is currently a Full Professor. His research interests include high-frequency power conversion, power factor correction techniques, and renewable energy applications.

Mario Lúcio da Silva Martins (M'10) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Federal University of Santa Maria (UFSM), Santa Maria, Brazil, 1999, 2002, and 2008, respectively.

In 2012, he joined the Department of Electronics and Computation, UFSM, Brazil. His research interests include UPS and power converters for renewable energy.

Dr. Martins is a member of the Brazilian Power Electronics Society and several IEEE Societies.