Single-Phase LED Drivers With Minimal Power Processing, Constant Output Current, Input Power Factor Correction, and Without Electrolytic Capacitor

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***Abstract*—High-power light-emitting diodes (LEDs) having properties of high luminous efficacy and long life span are becoming a major light source for general illumination. To fully utilize the advantages of LED in lighting applications, the offline power supply that drives the LED should possess the following features: high efficiency, long life span, high input power factor, and (COC). In this paper, high efficiency is achieved by using a minimal power processing (MPP) configuration. Near perfect power factor correction (PFC) is achieved by a simple dual-output discontinuous-conduction-mode (DCM) pulse-width-modulated (PWM) front-end converter. One output of the front-end converter is connected to the LED load using a control switch. The other output is connected directly to a dc storage capacitor cascaded with a downstream DCM PWM converter driving the same LED load to achieve COC driving. The power flow is controlled to achieve the required MPP that can also reduce the storage capacitance by balancing only the ac input ripple power and the dc output power without power recycling. Thus, the design requires no electrolytic capacitor, hence extending the system life span. The achievement of input PFC, MPP, and COC requires design tradeoff among design freedom, ease of control and component count. LED drivers having all these properties are developed, designed, and tested.**

***Index Terms*—Electrolytic capacitor, flicker-free, minimal power processing, offline light-emitting diode (LED) driver, power factor correction (PFC).**

I. Introduction

With the attractive luminous efficacy and long life span, light-emitting diodes (LEDs) are widely used in many commercial, domestic, and industrial applications. To fully utilize the advantages of LED in lighting applications, the power supply that drives the LED should be of high efficiency and long life span, and having high input power factor and delivering constant output current (COC) [1]. The requirements of power factor correction (PFC) and COC necessitate the use of an energy storage capacitor for handling the imbalance between the input ripple power at double line frequency and the output constant power, with minimal power processing (MPP) [2]–[4]. To make the life span of the LED driver comparable with the LEDs, the use of a high charge density but relatively shorter life span electrolytic capacitor should be avoided.

An important design aspect of LED drivers is the multiple design goals and their tradeoffs. Specifically, the charge storage capacitance can be reduced either by operating it at a higher voltage with the same power storage or relaxing the requirement of input power factor and/or the output current regulation with reduced power storage. A single-stage design can hardly avoid the use of large storage capacitance [1], [5] due to the low degree of freedom in optimizing input PFC, COC, MPP and the reduction of charge storage capacitor. An integrated multiple-stage design allows the storage capacitor to be isolated from the LED load and at the same time permits the use of smaller capacitance at the expense of a higher capacitor voltage ripple. However, an integrated multiple-stage converter may have low overall conversion efficiency [1]. By allowing the controls of MPP, PFC, and COC to be less precise, other converter constraints can be optimized and the use of a shared switch can be achieved [6], [7]. However, such implementation also incurs higher output current ripple, which reduces the life span of the LEDs being driven. Given the importance of lighting applications and their huge power consumption, high power factor and efficiency are still the crucial design factors.

The two-independent-stage configuration shown in Fig. 1(a) can achieve better input PFC, COC, and efficiency, compared to other integrated configurations [1], [8]–[10]. In this design, a front-end PFC converter is cascaded with a dc–dc regulator, with a storage capacitor buffering the power imbalance. It is, thus, a 2-power-stage (2-PS) converter. The overall efficiency η_α is simply the product of the average efficiency η_1 of the PFC converter and that of the dc–dc converter η_2, i.e.,

$$\eta_\alpha = \eta_1 \eta_2. \tag{1}$$

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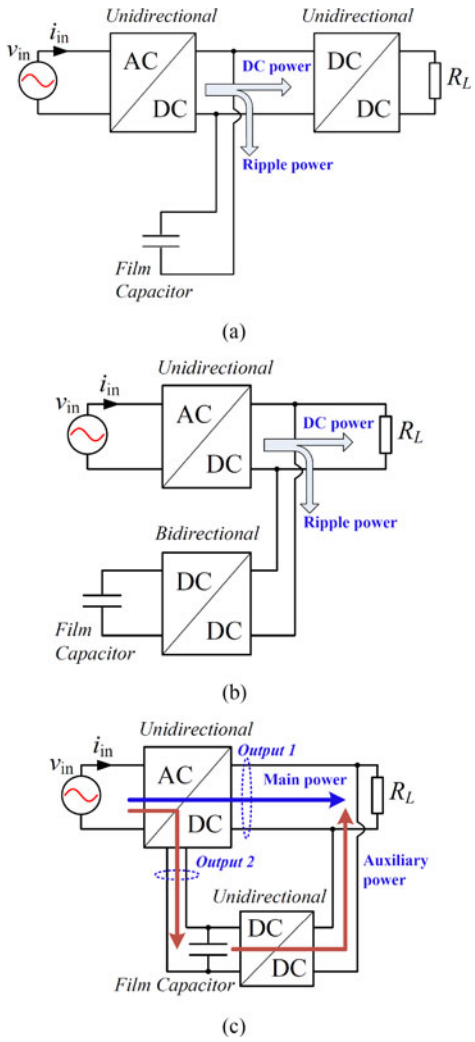

Fig. 1. LED drivers and power processing stages: (a) two-stage design, (b) n_β-power-stage design, and (c) n_χ-power-stage design.

The two-stage design can be optimized for MPP by directly forwarding power to the load, and the ripple power is compensated by connecting the output with a bidirectional converter and a capacitor storage [11]–[15], as shown in Fig. 1(b). In this type of 2-PS with MPP design, the best overall efficiency is

$$\eta_\beta = k_1\eta_1 + (1-k_1)\eta_1\eta_{2_f}\eta_{2_b} \tag{2}$$

where $k_1 = 1 - \frac{1}{\pi}$ is the maximum portion of power directly delivered to the load by the PFC stage, η_{2_f} and η_{2_b} are the efficiencies of the forward and backward power conversions of the bidirectional converter, respectively. The number of effective power processing stages of the converter shown in Fig. 1(b), denoted by n, can be determined from an energy-flow-path analysis [16]. Specifically, for the 2-PS configuration, if the efficiency of each stage is identically η_i, then $\eta_\alpha = \eta_i^{n_\alpha}$ and $n = n_\alpha = 2$. Similarly, for the 2-PS with MPP configuration, (2) becomes

$$n = n_{\beta,\min} = k_1 + (1-k_1)3 = 1.64. \tag{3}$$

Another power flow optimized 2-PS design with MPP is shown in Fig. 1(c), which uses a PFC stage with dual outputs. One output directly delivers power to the load, and the other output delivers power to the charge storage capacitor. The charge stored in the capacitor is converted to the load via a power converter. The maximum overall efficiency is

$$\eta_\chi = k_1\eta_1 + (1-k_1)\eta_1\eta_2. \tag{4}$$

Thus, we have $n = n_{\chi,\min} = 1.32$. In this way, based on the energy-flow-path analysis, a converter can generally be identified as an n-PS converter for a unified topological comparison. The parallel PFC converters described in [17]–[20] have been targeted for PFC regulator applications with no consideration of LED driving requirements. The basic concept, however, is applicable to LED drivers [21]–[24]. A specific example of an $n_{\chi,\min}$-PS converter was reported by Chen and Hui [21].

In this paper, an efficient offline LED driver based on the structure shown in Fig. 1(c) is developed, achieving input PFC, COC, the smallest number of power processing stages with $n = 1.32$, i.e., an $n_{\chi,\min}$-PS converter, and without electrolytic capacitor. The charge storage capacitor can be minimized using a tighter yet simple control technique to forward only the necessary power. Detailed comparison of existing topologies for LED drivers will be given in Section II. Our proposed LED driver will be described in Section III, implemented in Section IV, and evaluated in Section V. Finally, Section VI concludes the paper.

II. Comparison of LED Drivers

The 2-PS offline LED driver can be designed with the desired properties of the absence of electrolytic capacitor, high input power factor, and constant current output [8]–[10]. However, in terms of efficiency, it is a 2-PS converter, and in terms of the number of active switches, it needs at least two. Improvement on efficiency has been proposed by adopting an n_β-PS design [13]–[15] and n_χ-PS design [21], [22] with the number of active switches increased to three. On the other hand, the number of active switches can be reduced by integrating the stages at the expense of compromising input power factor or output regulation. However, these integrated two-stage LED drivers [6], [7] are still 2-PS designs that have no topological advantage in improving efficiency. In this section, we will compare the offline LED drivers in terms of

1) design without an electrolytic capacitor;
2) driver and control complexity;
3) losses due to parasitic elements.

A summary is given in Table I.

A. Capacitance Reduction

The 2-PS LED driver can readily achieve a design without an electrolytic capacitor, thanks to the storage capacitor being isolated from the input power factor and output current regulation. The storage capacitance can be further reduced if the input power factor can be compromised by allowing third-order harmonics [9] or the COC is controlled with pulse-width-modulated (PWM) dimming and/or bilevel dimming [10]. The n_β-PS and n_χ-PS offline LED drivers can retain similar merits of the two-stage design for the reduction of the storage capacitance. Moreover, the output capacitance in parallel with the LED string can

TABLE I
COMPARISON OF ELECTROLYTIC CAPACITOR-LESS LED DRIVERS

Classification		2-PS[8]–[10]	ISD[6], [7]	n_β-PS[13]–[15]	n_χ-PS[21], [22]
Topological number of processing stages		2	2	1.64	1.32
Minimum number of active switches		2	1	3	3
Control complexity		Medium	Low	High	High
Achieving both high PFC and COC		Easy	Difficult	Easy	Easy
Capacitance reduction	Narrow Input Range	Excellent	Good	Good	Good
	Wide Input Range	Excellent	Medium	Good	Good
Line current harmonics injection		Easy*	Difficult	Easy	Easy
Output PWM dimming		Easy#	Difficult	Difficult	Easy

Key: *verified in [9]; # verified in [10]; ISD denotes integrated stage design.

be used solely for removing converter switching ripples, and is, therefore, relatively small.

Due to the limited control freedom of a single switch in the integrated two-stage LED driver, double line-frequency ripple power cannot be completely eliminated at the output. Instead, the ripple power may be mitigated by designing the storage capacitor with a higher voltage or larger capacitance [6], making it harder to eliminate the electrolytic capacitor. Moreover, to achieve better output current regulation, the extra output current control in [7] may cause unstable converter operation. Also, without the extra control freedom provided by more active switches such as in 2-PS, n_β-PS design, or n_χ-PS design, control techniques like third-order harmonics injection [9] and PWM dimming and/or bilevel dimming [10] are not applicable.

B. Driver and Control Complexities

The single-switch integrated two-stage offline LED drivers have the lowest complexity in terms of active switch driving and control. For some specific applications, where the input voltage range is narrow and some double line-frequency ripple output currents are allowed, they have the lowest cost and size.

The control of two to three active switches in 2-PS, n_β-PS design, and n_χ-PS design is more complicated. Efforts have been made to remove one active switch for the n_χ-PS design [23], [24]. However, either the input power factor or output current regulation must be significantly compromised.

Compared with 2-PS offline LED drivers, the n_β-PS design described in [13]–[15] requires an extra sensor for its output current loop, and the n_χ-PS design described in [21], [22] requires an extra line voltage sensor for the timing control of charging and discharging of the storage capacitor.

C. Losses Due to Parasitic Elements

In general, the efficiency of various types of offline LED drivers can be compared in terms of the value of n in an n-PS configuration by using the energy-flow-path analysis [16]. However, different configurations may involve different sets of parasitic elements that may incur extra power losses. Efforts have been made to minimize such losses. Specifically, the energy stored in the leakage inductance of the integrated configuration described in [6] has been recycled to the storage capacitor, the energy stored in the leakage inductance of the n_χ-PS design in [21] can be recycled via the one-stage power path and is dissipated in the two-stage power path, and the energy stored in the leakage inductance of the n_χ-PS design in [22] is completely dissipated.

III. LED DRIVER ARCHITECTURE

In this section, a single-phase LED driver architecture with PFC and COC is developed using the $n_{\chi,\min}$-PS design shown in Fig. 1(c). The first stage PFC converter can be chosen from some simple nonisolated PWM converters, as shown in Fig. 2, some of which have pulsating current source (PCS) outputs [26]. Among these topologies, the buck PFC converter shown in Fig. 2(a) cannot sink input current when the rectified line voltage is lower than the output voltage, leading to a lower power factor. The boost PFC converter shown in Fig. 2(b) and its bridgeless versions as shown in Fig. 2(d) and (e) are widely implemented in high-power applications, operating in continuous conduction mode. When operating in discontinuous conduction mode (DCM), the average input current of the boost PFC converter, like the buck converter, depends on both the input and output voltages. Thus, the input resistance at constant duty cycle varies with the input-to-output voltage ratio, degrading the PFC performance. In contrast, the DCM operated buck–boost PFC converter shown in Fig. 2(c) and its isolated version, i.e., flyback PFC converter, are suitable for low-power applications with an automatic PFC function and a simple duty cycle control, eliminating the need for line current sensors.

The PFC converters shown in Fig. 2(b)–(e) can be readily modified by adding an extra diode for each extra output to form multiple-output converters. Specifically, the output of inductor L_m can be regarded as a PCS that is connected to each output using a diode as a passive switch. The proportion of power flowing to each output can be controlled with one or more active switch(es), as explained in Section IV.

At the input side, the line voltage $v_{\rm in}$ and power factor corrected current $i_{\rm in}$ with line angular frequency ω are

$$v_{\rm in} = V_m \sin \omega t, \text{ and} \tag{5}$$

$$i_{\rm in} = I_m \sin \omega t. \tag{6}$$

The output power of PCS is given by

$$\begin{aligned} p_{\rm PCS} &= \eta_1 p_{\rm in} \approx p_{\rm in} = v_{\rm in} i_{\rm in} \\ &= \frac{1}{2} V_m I_m - \frac{1}{2} V_m I_m \cos 2\omega t \end{aligned} \tag{7}$$

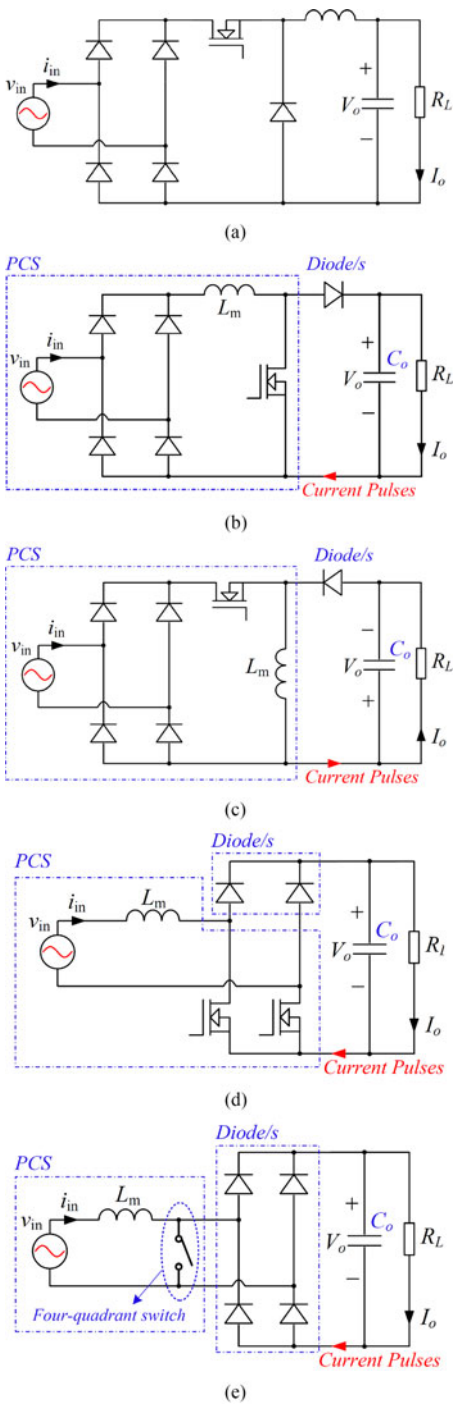

Fig. 2. Active nonisolated PFC converters: (a) Buck PFC, (b) boost PFC, (c) buck–boost PFC, (d) bridgeless boost PFC, and (e) bridgeless PFC converters with a four-quadrant switch.

which is simply a summation of a dc power $p_{\rm dc}$ and a second-order ac power $p_{2\omega}$ given by

$$p_{\rm dc} = \frac{1}{2} V_m I_m, \text{ and} \tag{8}$$

$$p_{2\omega} = -\frac{1}{2} V_m I_m \cos 2\omega t. \tag{9}$$

The 2-PS LED driver, shown in Fig. 1(a), can be implemented with a single output PCS by using one of the topologies given in

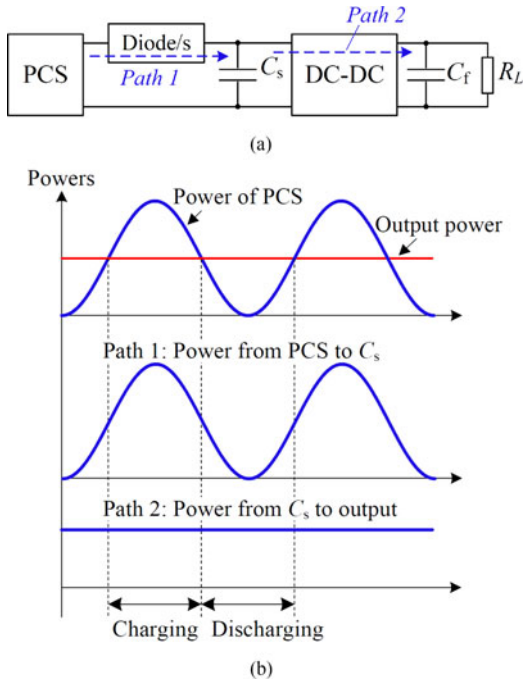

Fig. 3. Power flow of a traditional two-stage LED driver: (a) block diagram and (b) power waveforms.

Fig. 2(b)–(e), and its block diagram can be redrawn as shown in Fig. 3(a). Here, the output power $p_{\rm PCS}$ from PCS flows to C_s via Path 1. The downstream dc–dc converter is controlled to deliver $p_{\rm dc}$ via path 2. Capacitor C_s stores power when $p_{\rm PCS} > p_{\rm dc}$ and releases power when $p_{\rm PCS} < p_{\rm dc}$. The power waveforms are given in Fig. 3(b). Obviously, the power is processed twice with efficiency given by (1).

To minimize repeated power processing, the n_χ-PS design shown in Fig. 1(c) is implemented using a two-output PCS. The additional output provides a direct power flow path from PCS to the LED load. Two typical designs are presented in Fig. 4(a) and (b). For the design of Fig. 4(a), a smaller capacitance C_s can be used due to its higher operating voltage. Furthermore, an extra power flow switch is connected between one output terminal of the PCS and the lower voltage output terminal, i.e., C_f in Fig. 4(a) and C_s in Fig. 4(b). Fig. 4(c) shows the desired power flows paths 1, 2, and 3. Comparing power flows shown in Figs. 3(b) and 4(c), it can be observed that $k_1 = 1 - \frac{1}{\pi}$ in (4) and only $\frac{1}{\pi}$ of the total power is processed by the unidirectional dc–dc converter. This saves the cost of thermal management and reduces the power rating of devices.

Using the block diagrams shown in Fig. 4, two families of the n_χ-PS design can be synthesized as shown in Fig. 5 for low output voltage applications and in Fig. 6 for high output voltage applications. The structure shown in Fig. 5(a) has been used in electric vehicle charging as a three-level quasi-two-stage single-phase PFC converter [27].

IV. Implementation of n_χ-PS LED Driver

This section describes the implementation of a low-power and small-charge-storage-capacitance LED driver based on the

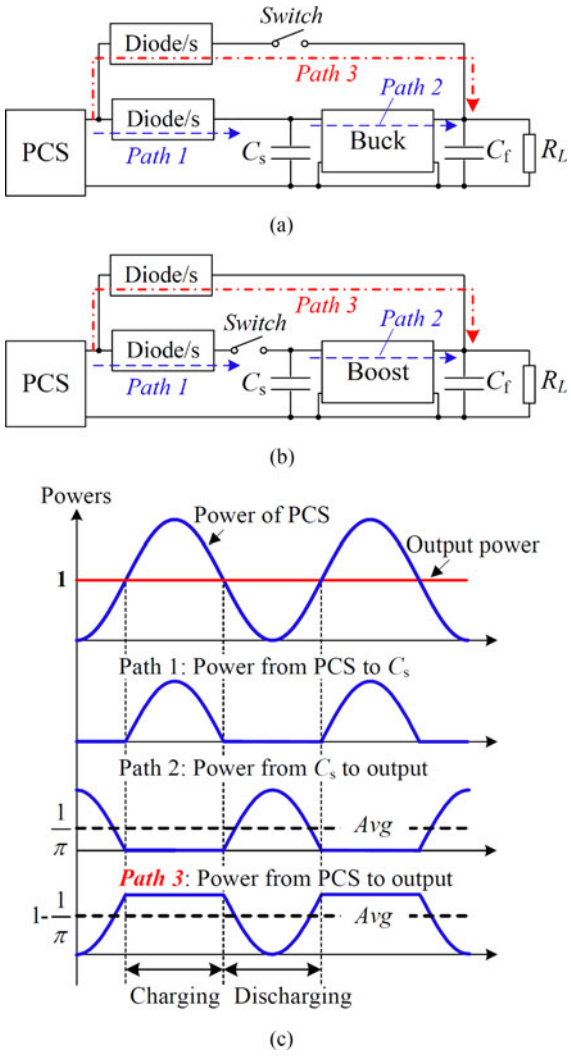

Fig. 4. Configuration of the n_χ-PS LED driver: (a) low output voltage design, (b) high output voltage design, and (c) desired power flow waveforms within a line period.

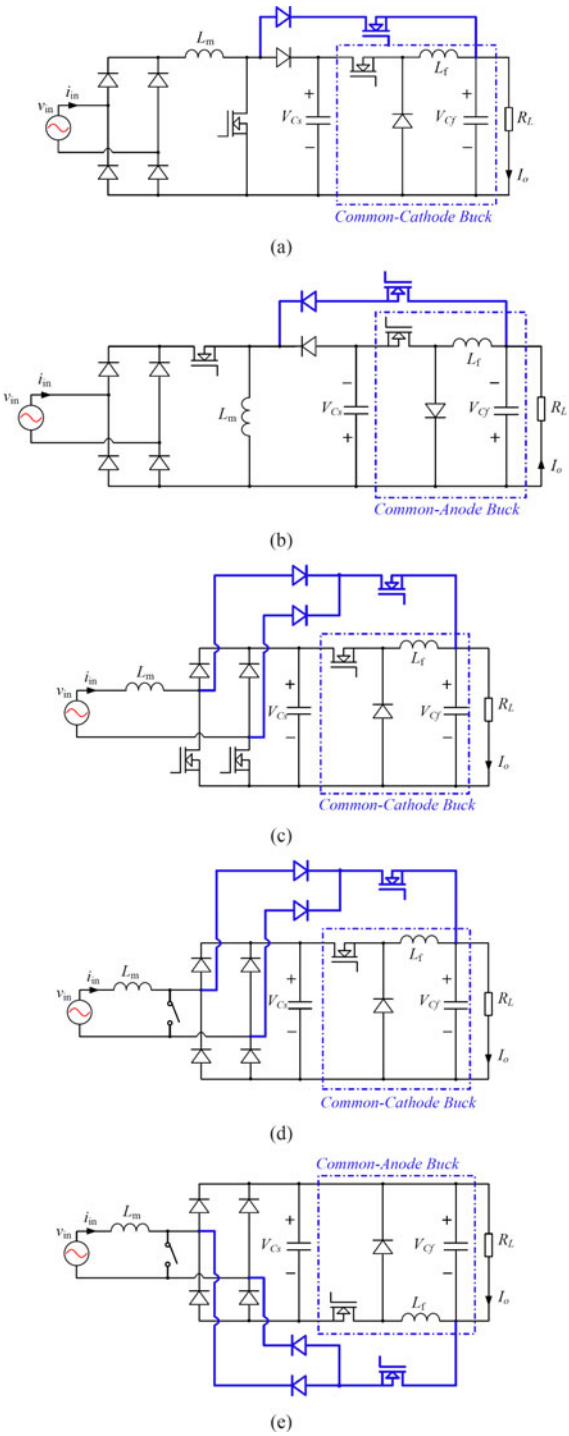

Fig. 5. Family of low voltage output n_χ-PS converters. (a) Boost PFC and common-cathode buck cascaded converter. (b) Buck–boost PFC and common-anode buck cascaded converter. (c) Bridgeless boost PFC and common-cathode buck converter. (d) Bridgeless four-quadrant switch PFC and common-cathode buck converter. (e) Bridgeless four-quadrant switch PFC and common-anode buck converter.

circuit shown in Fig. 5(b). The details of this nonisolated LED drivers are shown in Fig. 7(a). The PFC stage is a buck–boost converter that provides two outputs. The averaged voltage of the storage capacitor C_s from one of its directly connected output is fed back for control [21]. Inductor L_m, operating in DCM, provides a native input unity power factor as long as the voltage loop is slow enough to keep the duty cycle of the main switch Q_m constant within a line period. The second stage is a common-anode buck converter with a small current filtering capacitor C_f. The inductor L_f of this buck converter also operates in DCM such that diode $D_{\rm buck}$ is zero-current turned off. The output current sensed by a small resistor $R_{\rm sense}$ will be regulated by the combined action of $Q_{\rm byp}$ and $Q_{\rm buck}$ to fullfil the desired COC requirement and the power flow condition to be described in the next section.

Comparing with a topologically similar implementation reported in Valipour *et al.* [23], although one less switch is used, it has less design freedom and cannot be programmed to achieve the desired power flow. On the other hand, the design of Chen and Hui [21] has a higher power density, thanks to the use of a single integrated transformer. However, the control of power flow is complicated due to the time-multiplex control of two pairs of switches for charging and discharging of the mutual inductor of the flyback transformer and the need for

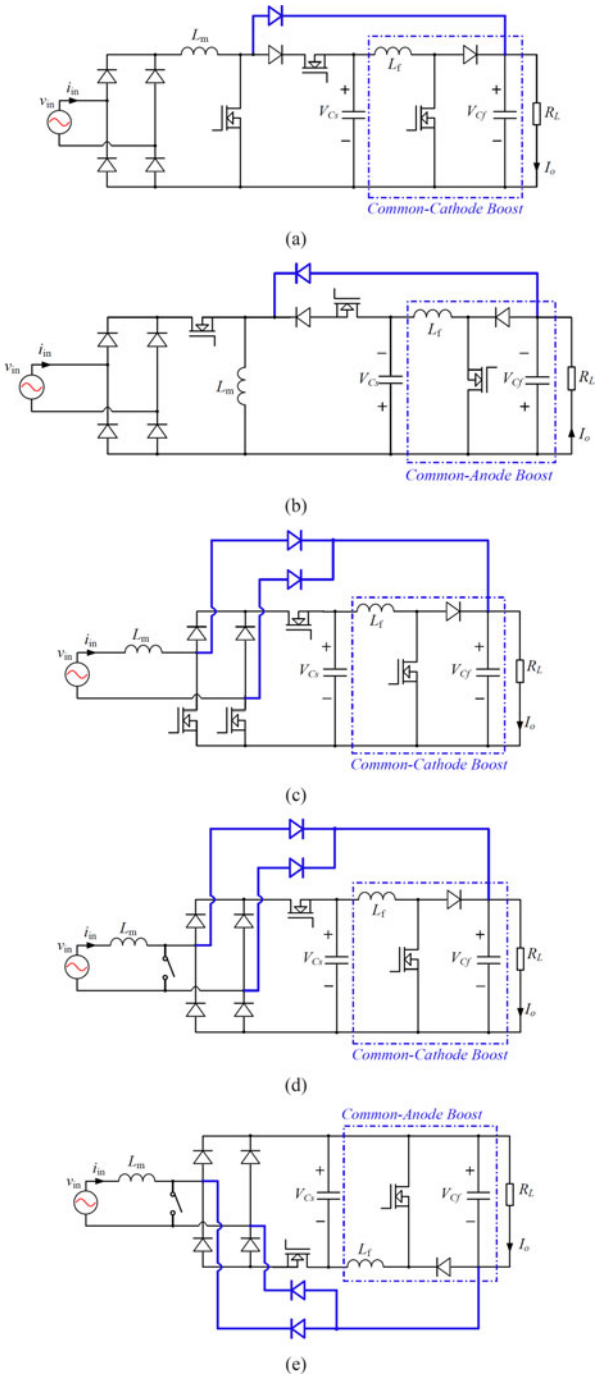

Fig. 6. Family of high voltage output n_χ-PS converters. (a) Boost PFC and common-cathode buck cascaded converter. (b) Buck–boost PFC and common-anode buck cascaded converter. (c) Bridgeless boost PFC and common-cathode buck converter. (d) Bridgeless four-quadrant switch PFC and common-cathode buck converter. (e) Bridgeless four-quadrant switch PFC and common-anode buck converter.

maintaining DCM operation simultaneously. Furthermore, the control adopted in [21] for distinguishing the operating modes during charging and discharging of the charge storage capacitor as shown in Figs. 4(c) or 7(b) is achieved by comparing the rectified input line voltage and its averaged value. The precision of this approach depends on the assumption of lossless power conversion and requires sensing the input line voltage.

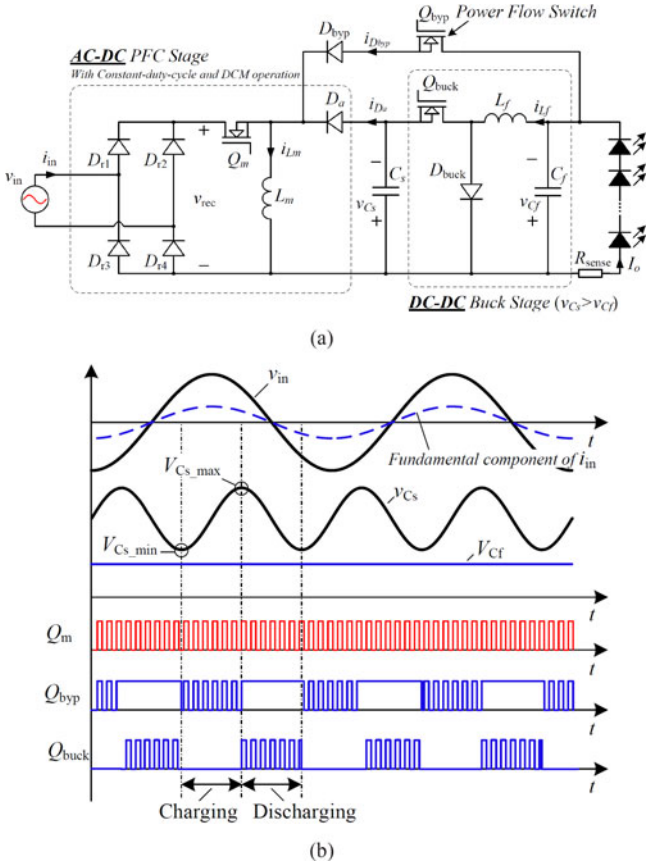

Fig. 7. (a) Proposed nonisolated n_χ-PS LED driver and its (b) operating waveforms.

A. Control Strategy With Carrier Disposition

A novel control strategy based on carrier disposition is proposed here as shown in Fig. 8(a). Compared with the control strategy of the traditional two-stage LED driver, only one extra comparator for $Q_{\rm byp}$ is needed. In this modulation scheme, a single sawtooth carrier is added to three independent dc-biased voltages to form three falling-edge synchronized sawtooth waveforms, i.e., v_{tr1}, v_{tr2p}, and v_{tr2n}. The modulation signal v_{m1} shown in Fig. 8(a) is compared with v_{tr1} to generate the driving signal for switch Q_m. Switches $Q_{\rm buck}$ and $Q_{\rm byp}$ are controlled in a coordinated manner. For simplicity, the lowest value of v_{tr2p} and the highest value of v_{tr2n} are fixed at 0 V. When v_{m2} is negative, it is compared with v_{tr2n} to generate the on–off driving signal for $Q_{\rm byp}$, and at the same time $Q_{\rm buck}$ stays open. When v_{m2} is positive, it is compared with v_{tr2p} to generate the on–off driving signal for $Q_{\rm buck}$, and at the same time $Q_{\rm byp}$ is kept closed.

Four possible operating states can be identified depending on the voltage level of v_{m2} as shown in Fig. 8(b).

1) State 1, as shown in Fig. 9(a): The duty cycle of $Q_{\rm byp}$ is lower than that of Q_m. The combined switch of $D_{\rm byp}$ and $Q_{\rm byp}$ is masked by $D_{\rm byp}$, which is off. The energy from PCS is fully stored in C_s.

2) State 2, as shown in Fig. 9(b): The duty cycle of $Q_{\rm byp}$ is larger than that of Q_m, and $Q_{\rm byp}$ is turned off before i_{Lm} falls

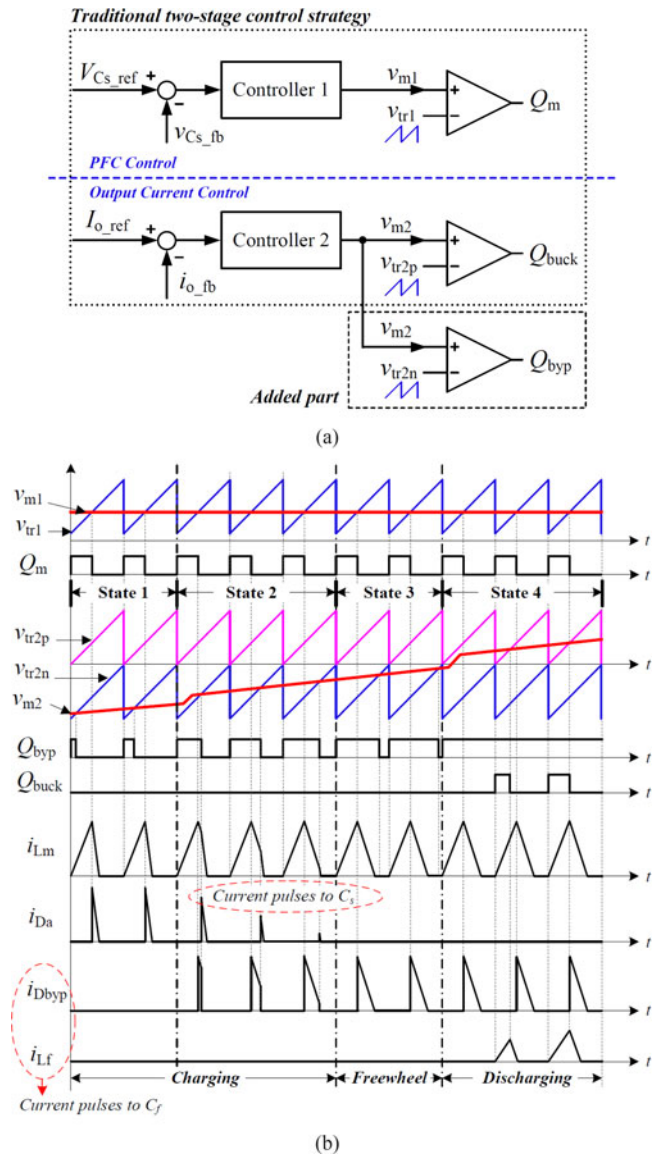

Fig. 8. (a) Proposed control strategy based on carrier disposition; (b) waveforms.

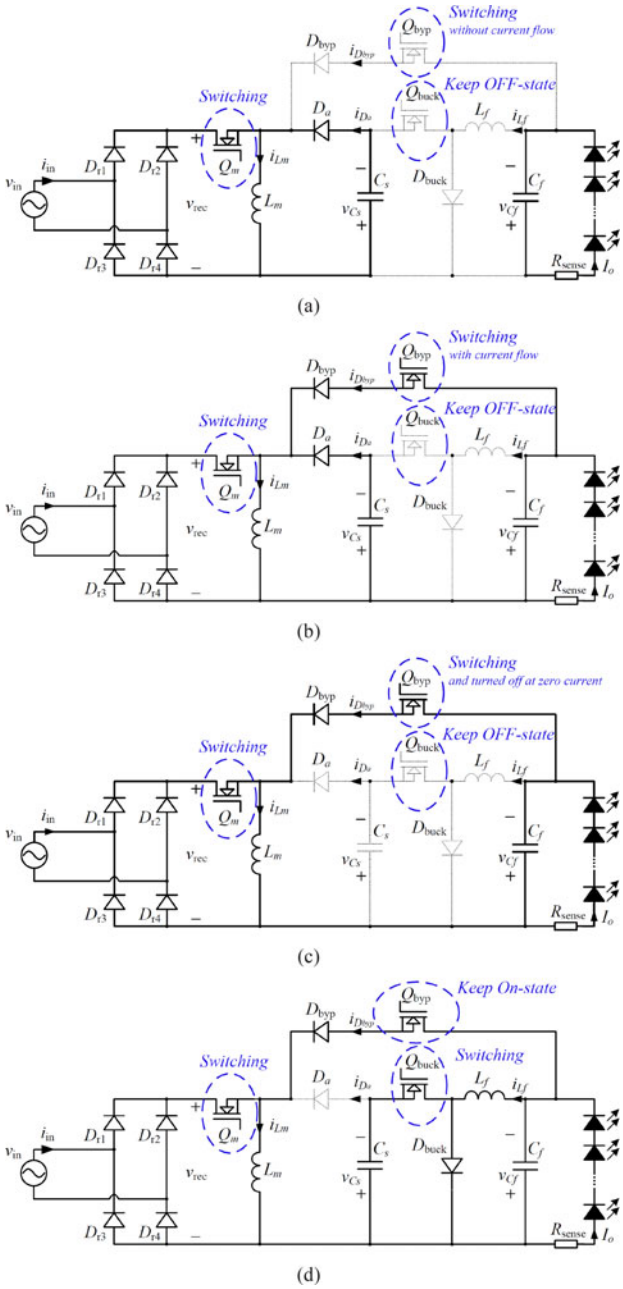

Fig. 9. Operating states of LED driver within a line cycle: (a) State 1, (b) state 2, (c) state 3, and (d) state 4.

to zero. The current from PCS first flows to the output load and later to the charge storage capacitor. The time duration of the current pulse from PCS to C_s decreases as v_{m2} increases.

3) State 3, as shown in Fig. 9(c): The value of v_{m2} is still negative. $Q_{\rm byp}$ is turned off after i_{Lm} falls to zero. The time duration of the current pulse from PCS to C_s decreases to zero upon further increase in v_{m2}.

4) State 4, as shown in Fig. 9(d): The value of v_{m2} becomes positive. $Q_{\rm byp}$ is kept closed to maximize the power transfer from PCS directly to the load. Meanwhile, any increase in v_{m2} will increase the duty cycle of $Q_{\rm buck}$, which delivers more power from C_s to the output load.

As observed from Fig. 8(b), the total output current ($i_{D_{\rm byp}}$ and i_{L_f}) increases with increasing v_{m2} in states 2 and 4, and is kept unchanged in states 1 and 3. As a result, the output current can be controlled using the output v_{m2} of controller 2 and the error current $(I_{o\_\rm ref} - i_{o\_\rm fb})$. As the output current does not change in states 1 and 3, when a fast controller is used, the output transient response can be analyzed without consideration of states 1 and 3. Detailed analysis of states 2 and 4 will be performed in the following sections.

B. Analysis of Charging Operation in State 2

In this subsection, we consider the charging operation of the buck–boost PFC converter. With a given input power $P_{\rm in}$, the steady-state duty cycle of Q_m is given by

$$D_m = \frac{2}{V_m}\sqrt{P_{\rm in} L_m f_s} \tag{10}$$

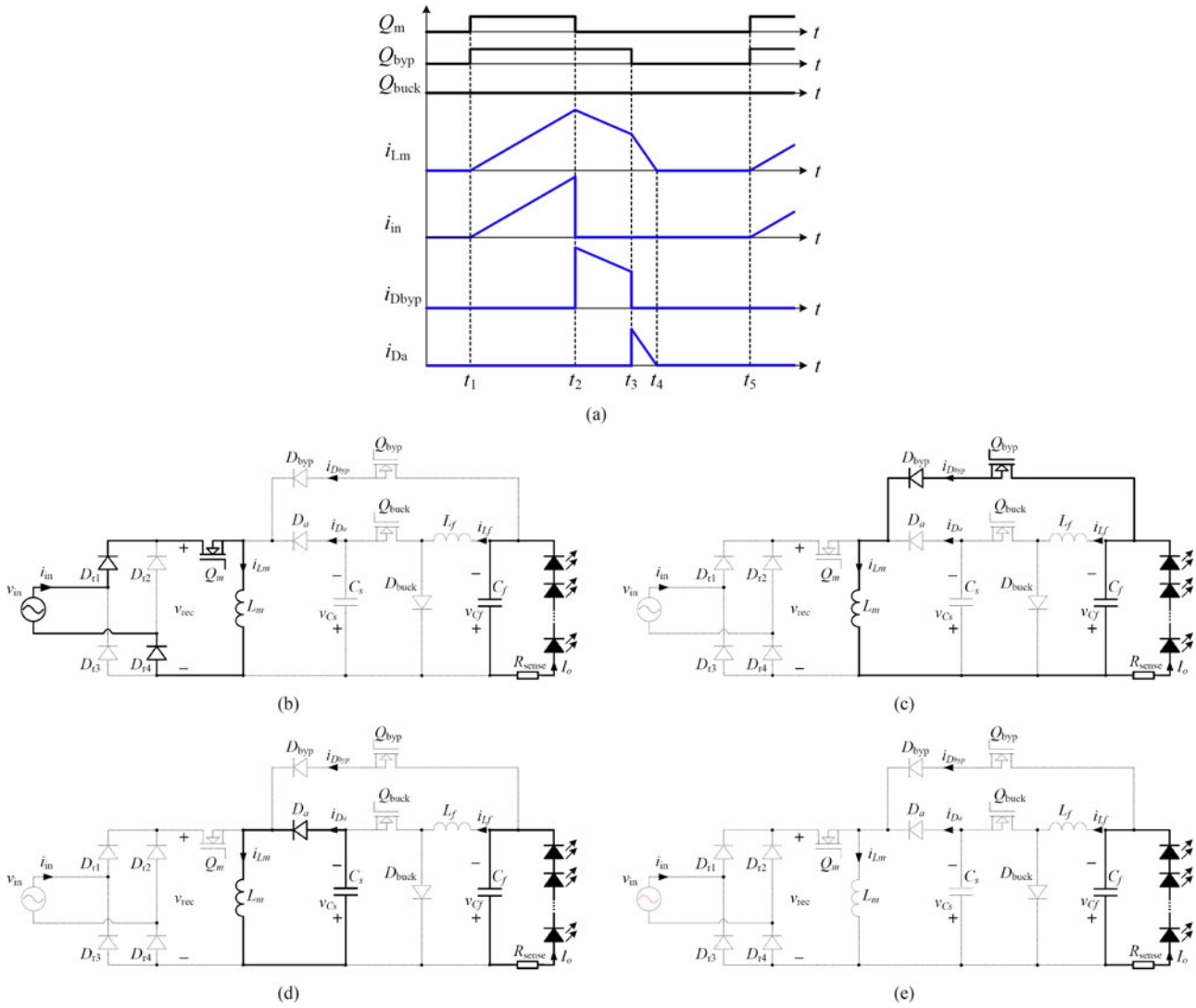

Fig. 10. (a) Switching waveforms within a switching period of State 2. Current flow in subintervals within (b) $[t_1, t_2]$, (c) $[t_2, t_3]$, (d) $[t_3, t_4]$, and (e) $[t_4, t_5]$.

where V_m is the amplitude of the line voltage in (5) and f_s is the switching frequency. The peak value of the PFC inductor current i_{L_m} is a function of time given by

$$i_{\text{pk\_}L_m} = \frac{D_m}{L_m f_s} |v_{\text{in}}| = \frac{V_m D_m}{L_m f_s} |\sin \omega t| . \tag{11}$$

The time-domain analysis of the charging operation is presented in Fig. 10. The period between t_1 and t_5 in Fig. 10(a) is divided into four subintervals.

1) $[t_1, t_2]$ *as shown in Fig. 10(b):* Q_m and Q_{byp} are turned on at $t = t_1$. Inductor current i_{L_m} charges up linearly by the line voltage and attains a peak value $i_{\text{pk\_}L_m}$ at $t = t_2$ according to (11). The output paths are blocked by D_{byp} and D_a even though Q_{byp} is turned on.

2) $[t_2, t_3]$ *as shown in Fig. 10(c):* Q_m is turned off at $t = t_2$. As $v_{C_f} < v_{C_s}$, D_{byp} is on and D_a is off. The current of i_{L_m} will flow to output capacitor C_f through D_{byp} and Q_{byp}. Current i_{L_m} decreases at a rate of $\frac{V_{C_f}}{L_m}$. The transferred energy to the output can be calculated as

$$\begin{aligned} e_{\text{byp\_charge}} &= \frac{1}{2} L_m \Delta i_{L_m}^2 \\ &= \frac{V_{C_f}}{f_s} \left(D_{\text{byp}} - D_m\right) i_{\text{pk\_}L_m} \\ &\quad - \frac{V_{C_f}^2}{2 L_m f_s^2} \left(D_{\text{byp}} - D_m\right)^2 . \end{aligned} \tag{12}$$

3) $[t_3, t_4]$ *as shown in Fig. 10(d):* Switch Q_{byp} is turned off at $t = t_3$. Current i_{L_m} flows to C_s through D_a and decreases at a rate of $\frac{V_{C_s}}{L_m}$. Only C_f provides energy for the load.

4) $[t_4, t_5]$ *as shown in Fig. 10(e)*: Current i_{L_m} falls to zero at $t = t_4$ and stay there until t_5. Diodes D_a and D_{byp} are off during this interval.

Only during the interval of $[t_2, t_3]$, energy is transferred from inductor L_m to output. Within a switching period, the energy consumed by the load can be calculated as

$$e_{\text{ld}} = \frac{P_o}{f_s} \tag{13}$$

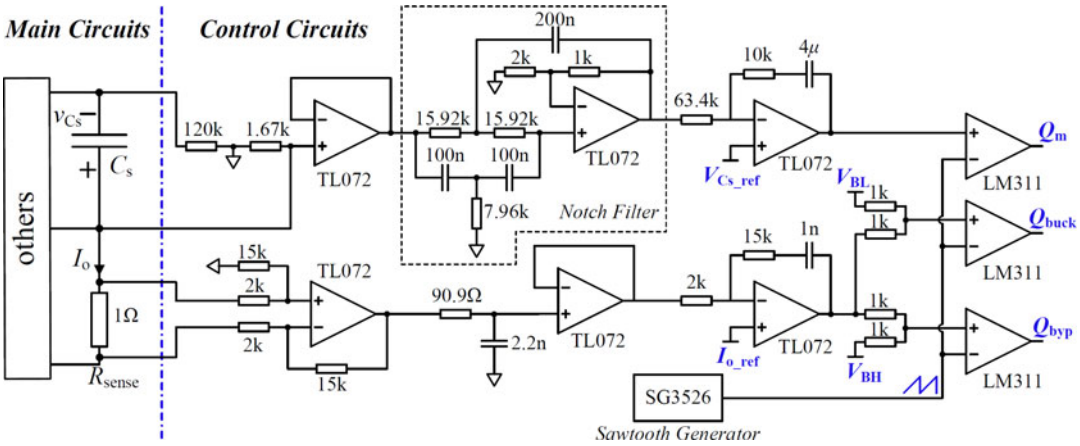

Fig. 11. Detailed circuit diagram of the control circuit. Since double line frequency ripple is significant for electrolytic-capacitor-less design, a notch filter is used for better rejection of the double line frequency ripple.

and the peak energy of inductor L_m at $t = t_2$ can be calculated with (11) as

$$e_{\text{pk}\_L_m} = \frac{1}{2} L_m i^2_{\text{pk}\_L_m} = \frac{V_m^2 D_m^2}{2 L_m f_s^2} \sin^2 \omega t. \tag{14}$$

Substituting (10) into (14), it has

$$e_{\text{pk}\_L_m} = \frac{2P_{\text{in}}}{f_s} \sin^2 \omega t = \frac{P_{\text{in}}}{f_s} - \frac{P_{\text{in}}}{f_s} \cos 2\omega t. \tag{15}$$

As long as

$$e_{\text{pk}\_L_m} \geq e_{\text{ld}} \tag{16}$$

the inductor can provide sufficient energy for load consumption, and can charge the capacitor C_s with the excess energy in State 2. Condition (16) is also applicable during transient of load switching, i.e., $P_{\text{in}} \neq \frac{P_o}{\eta}$, where η is the measured efficiency at steady state.

C. Analysis of Discharging Operation in State 4

When $e_{\text{pk}\_L_m} < e_{\text{ld}}$, the circuit is in state 4, as shown in Fig. 9(d), discharging the energy from capacitor C_s to the load. The buck–boost PFC converter and the DCM buck converter are delivering power to the load in parallel.

The energy provided by the buck–boost PFC converter, $e_{\text{pk}\_L_m}$, can be calculated from (14). Within a switching period, the energy difference can be calculated as

$$e_{\text{gap}} = e_{\text{ld}} - e_{\text{pk}\_L_m} \tag{17}$$

and the energy provided by the DCM buck converter is given by

$$e_{\text{buck}} = \frac{V_{C_s} - V_{C_f}}{2 L_f f_s^2} V_{C_s} D^2_{\text{buck}}. \tag{18}$$

Consequently, using the proposed control with D_{buck} as the control variable, the energy difference can be nullified, i.e., $e_{\text{buck}} = e_{\text{gap}}$.

V. Verification

An experimental prototype is constructed according to the control circuit given in Fig. 11 and the parameter values given in Table II. A photograph of the main circuit board is shown in Fig. 12.

TABLE II
Main Parameters of the Proposed LED Driver

Parameters	Values
Grid input voltage v_{in}	110% ± 20% VAC
Grid frequency f	50 Hz
Input inductor $L_{\text{in}}{}^*$	2 × 470 μH
Input capacitor $C_{\text{in}}{}^*$	100 nF/400 V
Switching frequency f_s	100 kHz
Inductor in PFC stage L_m	200 μH
Storage capacitor C_s	3 × 2.2 μF/400 V
Filtering inductor in buck stage L_f	50 μH
Filtering capacitor in buck stage C_f	3 × 2.2 μF/100 V
Maximum power capacity $P_{o\,\max}$	16 W
Diodes $D_{r1} - D_{r4}$, D_{byp}, D_a, D_{buck}	MUR160G
MOSFETs Q_a, Q_{byp}, Q_{buck}	IPA60R385CP
Measured LED VI points	85.1 V @ 190 mA 82.0 V @ 110 mA 78.0 V @ 30 mA

Key: ${}^*L_{\text{in}}$ and C_{in} constitute an input LC filter

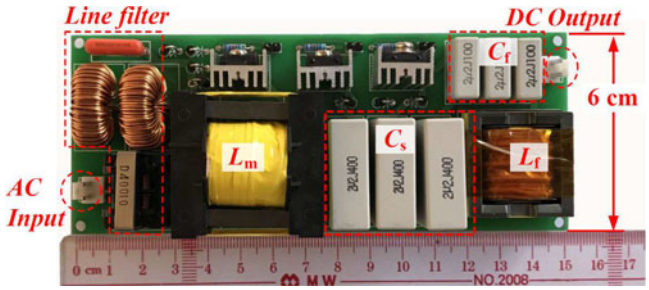

Fig. 12. Photograph of main circuit board.

Fig. 13(a) shows the measured input and output waveforms of the converter. High input power factor and constant output dc driving current are achieved. Fig. 13(b) shows the measured control waveforms of the converter, demonstrating smooth transition of power splitting using the carrier disposition technique. Fig. 13(c) and (d) show the enlarged waveforms during state 2 of

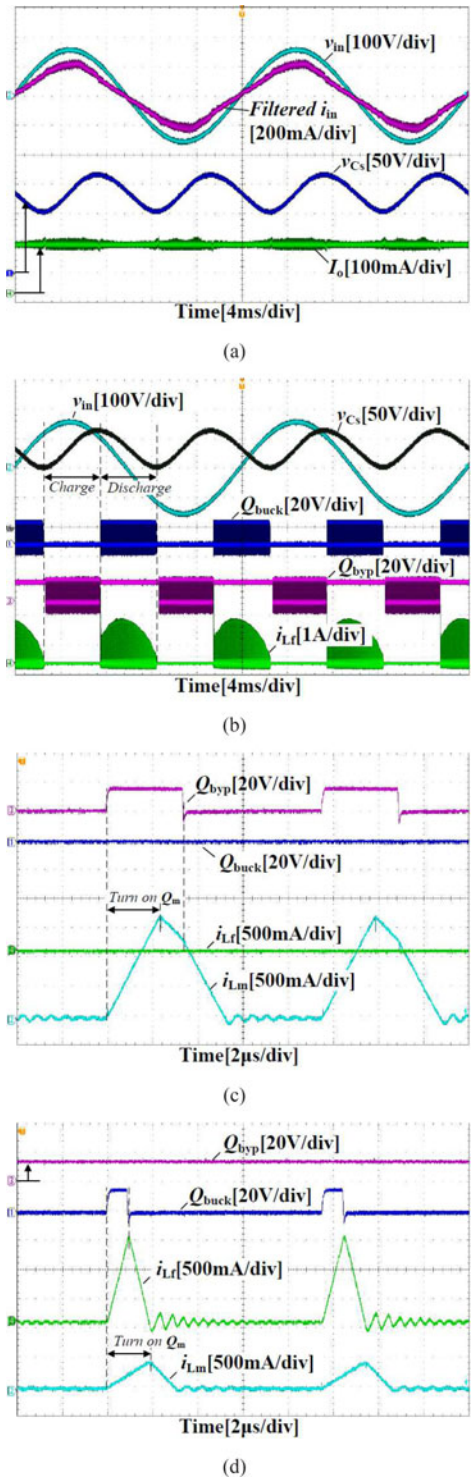

Fig. 13. Key experimental waveforms of the LED driver.

charging and state 4 of discharging of C_f, respectively. Fig. 14 shows the portion of power directly delivered to the load that k_1 is close to the theoretical value of $1 - \frac{1}{\pi} \approx 0.682$.

Measured power factors at various output currents and input voltages are shown in Fig. 15. At $V_{\text{in}} = 110$ V, harmonic contents of the grid current are shown in Fig. 16(a) and (b) for $I_o = 50$ mA and $I_o = 160$ mA, respectively. The measured

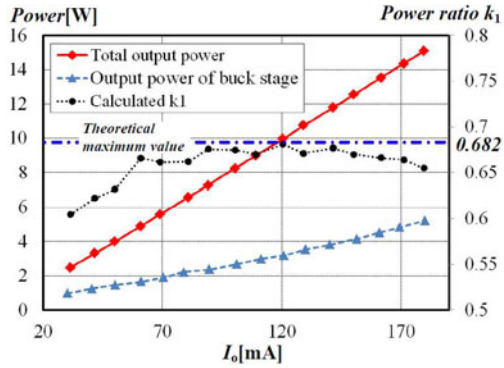

Fig. 14. Experimental measurement of k_1 in (4), which is obtained from the ratio of power of the buck converter versus the total power outputting to the LED string.

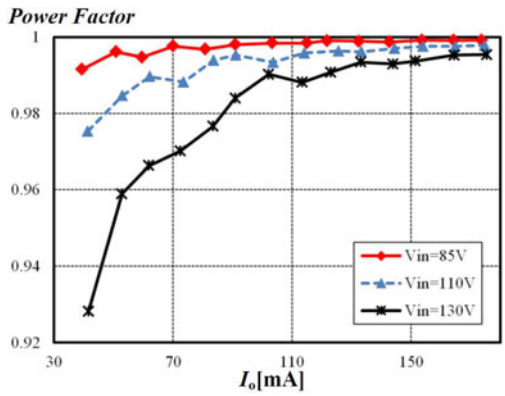

Fig. 15. Measured power factor at various output currents.

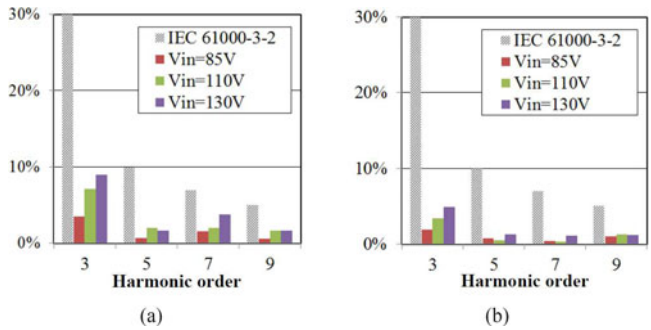

Fig. 16. IEC 61000-3-2 Class C limits and input harmonic contents at (a) $I_o = 50$ mA and (b) at $I_o = 160$ mA .

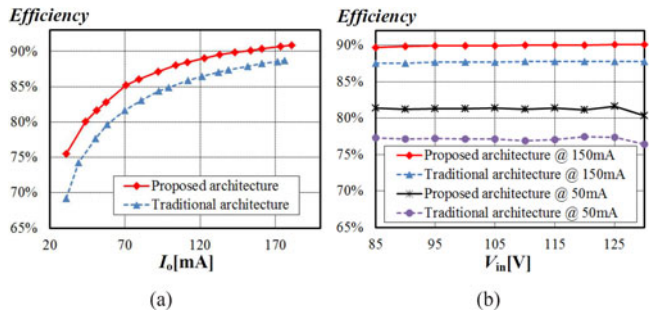

Fig. 17. Comparison of efficiency of the LED driver and the traditional two-stage converter at (a) $V_{\text{in}} = 110$ V and (b) $I_o = 50$ and 150 mA.

TABLE III
LOSS BREAKDOWN @ $V_{\rm in} = 110$ V AND $I_o = 150$ MA

Measured Prototype		Proposed Driver	2-Stage Counterpart
Overall efficiency		89.69%	87.34%
Overall loss		1.46 W	1.83 W
AC–DC stage	Efficiency	90.98%	90.10%
	Loss	1.27 W	1.43 W
	Loss weighting	86.99%	78.14%
DC–DC Buck Stage	Efficiency	95.72%	96.93%
	Loss	0.19 W	0.40 W
	Loss weighting	13.01%	21.86%

efficiencies of the proposed converter and a traditional two-stage implementation [by removing diode $D_{\rm byp}$ and switch $Q_{\rm byp}$ shown in Fig. 7(a)] are given in Fig. 17. A loss breakdown of the proposed LED driver and its two-stage counterpart is given in Table III.

VI. CONCLUSION

In this paper, an LED offline driver is designed based on a minimum power processing structure. The LED driver is chosen from a family of converters having input PFC and output controlled dc constant current. The LED driver is designed with a control using the technique of carrier disposition for seamless splitting of the input power into two paths. An optimal portion of the input power goes to the dc output and the rest to a storage buffering path connected to the dc output. Since the storage capacitor is operated at a much higher voltage than the output voltage, a small nonelectrolytic capacitor can be used. The design of the LED driver has been verified experimentally.

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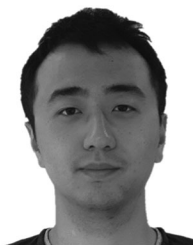

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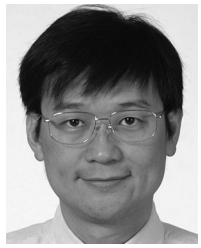

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