Resonant Multi-input/Multi-output/Bidirectional ZCS Step-Down DC–DC Converter With Systematic Synthesis for Point-to-Point Power Routing

Masoud Jabbari and Mozafar Sharifian Dorcheh

***Abstract*—A new resonant zero-current switching (ZCS) multi-input/multi-output (MIMO) converter is presented. The proposed converter routes power from every desired input port to every desired output port independently. Capability of bidirectional operation is also provided. All semiconductor devices operate under the soft-switching conditions independent from operating voltage and output power. Power budgeting for the inputs, individually voltage regulation for the outputs, and internal voltage balancing for the bidirectional ports are attained with few power-element count. The system is synthesized systematically based on a topology belonging to the family of switched-resonator converters (SwRCs). No transformer is utilized, and common ground exists between all ports. The concept of route matrix is developed to determine the power multiplexing paths. This method greatly simplifies the analysis, design, and control of the proposed system. Mathematical formulation based on route matrix is given in detail. Circuit analysis, design procedure, and five different designs along with simulation and experimental results are presented.**

***Index Terms*—Bidirectional converter, multi-input/multi-output (MIMO) converter, multiport converter, resonant power conversion, soft switching, switched-resonator converter (SwRC), zero-current switching (ZCS).**

I. Introduction

SWITCHING converters are widely employed for electric power conversions. Power density, efficiency, and electromagnetic interference (EMI) compatibility should be enhanced in a modern converter. For these purposes, soft-switching techniques are developed successfully [1]–[9]. The method of zero-current switching (ZCS) is simple and well adopted with the power converters. Moreover, full-range soft switching can be attained and control method is not complicated [6]. In resonant converters, a resonant tank provides soft-switching conditions by shaping the switch voltage and/or current. These converters are featured by their power density [5]–[6], [10]. Switched-resonator converters (SwRCs) are resonant converters adopting forward-conducting bidirectional-blocking (FCBB) switch with a resonant *LC* network [5]–[8]. SwRCs enjoy the advantages of ZCS operation and few element number.

Converters with multi-input (MI) ports are utilized to accommodate several voltage sources. These converters are often employed in renewable energy utilities such as photovoltaic (PV) cells [11], wind turbines [12], fuel cells [13], and hybrid electric vehicles (HEV) [14]. In [15], some general rules for developing MI converters are studied. Especially using FCBB switch is considered. Power budgeting (programming the power flow of each input source) is presented in [16] and [17]. In [18], a simple configuration of series-connected double-input converter with bootstrap circuit is presented, which gives proper reliability and robustness. However, the number of input ports are fixed and many active elements should be employed. In [14], [16], and [19], MI converter is based on a multiwinding transformer. Asa *et al*. [19] adopt an asymmetric series resonant converter (SRC) with an MI transformer. However, the transformer should be used if galvanic isolation is required. Otherwise, it is a bulky component that increases the converter volume and cost. In [20], a transformerless MI converter is presented, which can provide buck and boost operation with few element count. However, limitations are imposed on the modulation index and the converter is not soft switching.

Multi-output (MO) power supplies provide different regulated voltage levels and are frequently used in the modern electronic systems. In an enhanced MO converter, the problem of cross-regulation should be perfectly obviated [21]–[24]. Similar to MI converters, employing a multiwinding transformer gives a systematic approach at the cost of employing an expensive bulky component [25]. A transformerless systematic synthesis based on positive buck–boost converter (PBBC) is presented in [26], which enjoys the advantage of pulsewidth modulation (PWM) control. However, it is not soft switching and every port includes a bulky inductor. Behjati and Davoudi [17] present another systematic architecture based on PBBC with FCBB switch where power is multiplexed and only one bulky inductor is utilized. But this method is again hard switching and the system is very sensitive to the gate signals. In [9], the converter is soft switching; however, the configuration is complicated and coupled inductors ought to be used.

This paper presents a new transformerless resonant multiport topology with systematic synthesis, which is illustrated in Fig. 1. Bidirectional ports can be added to the interface with rechargeable energy storage elements. The architecture is based on the

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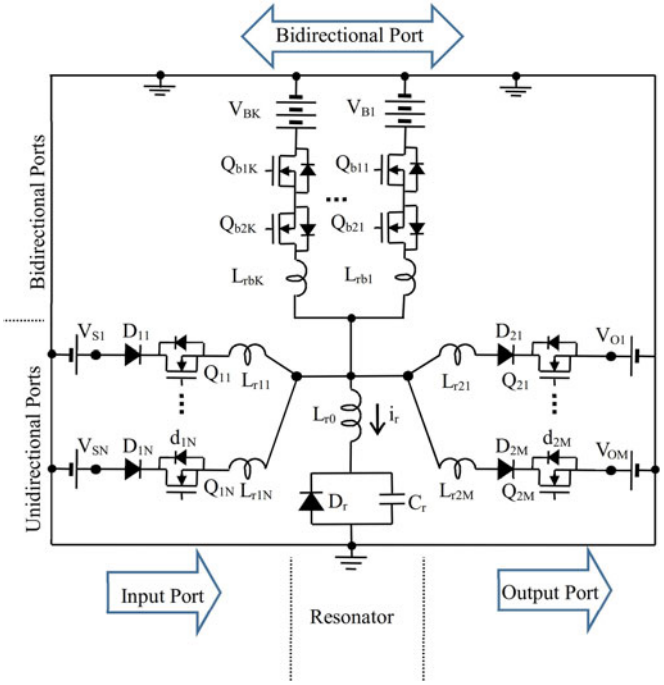

Fig. 1. Proposed transformerless resonant multiport topology (except L_{r0}, other inductors are optional).

SwRC structure which provides full-range ZCS conditions for all switches. Each input/output port is a single branch link connected to a resonator via an FCBB switch. The inductors L_{r11} to L_{r1N} at the input, L_{21} to L_{r2M} at the output, and L_{rb1} to L_{rbk} at the bidirectional ports are optional. The switches multiplex power between all the ports via the shared resonator. Thus, power can be routed from every desired input/bidirectional port to every desired output/bidirectional port arbitrarily. The concept of route matrix is introduced, and the mathematical formulation based on it is developed. The presented formalism greatly simplifies the converter analysis and design. It is shown that power budgeting for the input sources can be programmed. The output ports are independent from each other, and therefore, cross-regulation problem is obviated. Analyses and design procedures for five different conditions are presented. Simulation and experimental results verify the integrity of operation and analysis.

II. General Architecture

A general architecture for an MIMO power multiplexer is shown in Fig. 2. Since the connection of every port is only to a FCBB switch, this architecture is probably the simplest topology, which gives the capability of arbitrary power routing. Since the voltage levels for input ports (V_{S1} to V_{SN}) or for output ports (V_{O1} to V_{OM}) are different, FCBB switches must be employed to avoid short-circuit fault. The interface is the shared part of the converter. The interface circuit proposed in this paper is shown in Fig. 3, which is, in fact, a high-frequency series resonant tank. The diode D_r stabilizes its operation [5]. By substituting the circuit of Fig. 3 in Fig. 2, the general synthesis presented in Fig. 1 is developed.

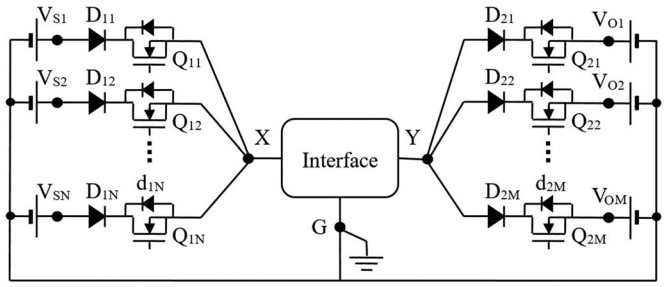

Fig. 2. General architecture of MIMO power multiplexer.

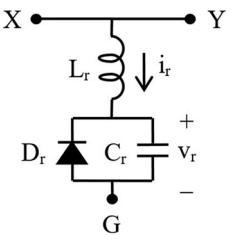

Fig. 3. Proposed interface circuit.

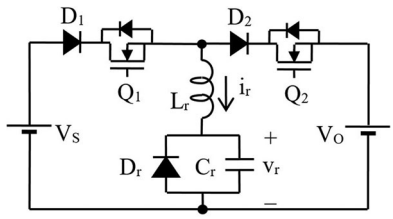

Fig. 4. SISO Buck-G SwRC.

III. SISO Topology

Buck-G SwRC, which is, in fact, the single-input single-output (SISO) version of Fig. 2, is shown in Fig. 4 where "G" represents its topology formation. The sets of D_1-Q_1 and D_2-Q_2 create FCBB switches. The resonator is a series-resonant tank (L_r and C_r) and a stabilizer (D_r). This converter is a step-down resonant voltage regulator belongs to the subgroup SwRC-g5 [5]. Detailed modal analysis of this converter is presented in [7], and its underlying operation principles are illustrated in [5]. To have a complete discussion, the operation of Buck-G is presented here briefly.

For simplicity, it is assumed that all elements are ideal and the circuit is in steady state. The output filtering capacitor is assumed large enough, and thus, the output section is modeled by the voltage source V_O. The voltage of C_r is defined resonant voltage v_r, and the current of L_r is defined resonant current i_r. Initially, v_r and i_r are both zero and all semiconductor devices are OFF. As shown in Fig. 5, at the first mode Q_1 is turned on, and thus, a resonance starts between L_r and C_r. Due to L_r, Q_1 is turned on at ZCS.

After one-half cycle, v_r reaches $2V_S$ and i_r sets at zero. Due to D_1, C_r cannot be discharged to V_S, and thus, Q_1 is turned off at ZCS. An energy equal to $E = \frac{1}{2}C_r(2V_S)^2$ is now stored in C_r. In the next mode, Q_2 is turned on, and therefore, C_r

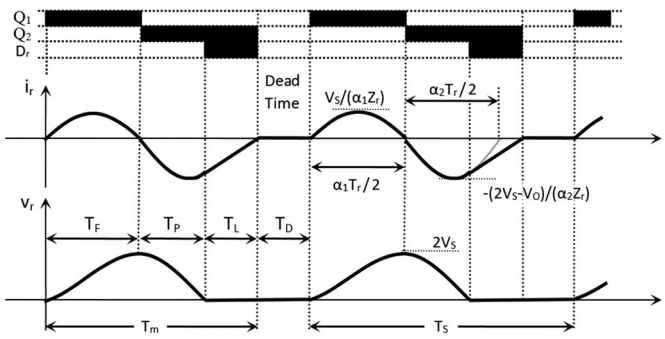

Fig. 5. Typical waveforms of SISO Buck-G SwRC.

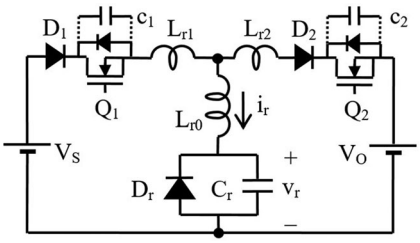

Fig. 6. SISO Buck-G SwRC with parasitic capacitances and additional inductors.

discharges to the output via a resonance with L_r. Due to L_r, Q_2 is turned on at ZCS. When $V_O < V_S, v_r$ reaches zero at a time where i_r is nonzero. Then, D_r becomes forward biased at ZVS and i_r continues through it. Finally, i_r reaches zero and, Q_2 and D_r are both turned off at ZCS. Due to D_2, C_r cannot be charged by V_O. The total energy E drained from V_S in the first mode is now pumped to the output, and v_r and i_r have been set at zero as well. The last interval is a dead-time that by adjusting its duration the rate of energy transfer is controlled to attain the required output voltage gain $A = V_O/V_S$. By satisfying the energy conservation principle as $E = 2C_r V_S^2 = V_O^2/R \times T_S$, the voltage conversion ratio is obtained as $A = S^{1/2}$, where $S = 2RC_r f_S$ is the scale- actor [7], $R = V_O^2/P_{\text{out}}$ is the load resistance, P_{out} is the converter output power, and $f_S = T_S^{-1}$ is the switching frequency. According to the presented analysis, a full soft-switching operation is achieved independent from the operating voltages and load current. An important feature is that v_r and i_r are set at zero at the end of each switching cycle independent of V_S, V_O, and P_{out}. This feature greatly simplifies the operation of Buck-G in confront of multiple input/output ports. In fact, the system is memoryless, which means operation of the converter in a cycle is not affected by the previous cycles. This feature also enables implementation of a one-cycle control, which results in very fast dynamics and high output voltage quality [7].

As shown in Fig. 6, practically, each switch has a parasitic parallel capacitance (output capacitance C_{oss}). In the circuit of Fig. 4, by turning Q_1 ON, a spiky current flows through the output capacitance of Q_2, which is a well-known phenomenon of the bridge structures. To obviate it, a small series inductor is added, as depicted in Fig. 6 (L_{r1} and L_{r2}) [27]. Adding these inductors does not change the operation of Buck-G discussed earlier, except that when Q_1 is ON, the tank inductance is $L_{r1} + L_{r0}$ and when Q_2 is ON, it would be $L_{r2} + L_{r0}$. Since in the MI and/or MO configuration of Fig. 2 the output capacitances of all switches are stacked, the total value of the parasitic capacitance can be problematic. Thus, the circuit of Fig. 6 is considered for extending the SISO configuration. More significantly, by adding these inductors, the power rating of each port can be managed since L_{r1} and L_{r2} change the tank characteristic impedance. This issue is supportive when high voltage diversity exists. The following parameters are defined for the circuit of Fig. 6, where ω_r is the tank angular frequency and Z_r is the characteristic impedance:

$$\omega_r = \frac{1}{\sqrt{L_{r0} \cdot C_r}} \qquad f_r = \frac{1}{T_r} = \frac{\omega_r}{2\pi} \tag{1}$$

$$Z_r = \sqrt{L_{r0}/C_r} \tag{2}$$

$$\begin{cases} \alpha_1 = \sqrt{1 + L_{r1}/L_{r0}} \\ \alpha_2 = \sqrt{1 + L_{r2}/L_{r0}} \end{cases}. \tag{3}$$

According to the analyses presented in [7], the equations describe operation of the circuit of Fig. 6 are derived as following. According to Fig. 5, T_F, T_P, T_L, and T_D are the durations of operating modes obtained as below, where *A* is the dc voltage gain $A = V_O/V_S$

$$\frac{T_F}{T_r} = \frac{\alpha_1}{2} \tag{4}$$

$$\frac{T_P}{T_r} = \alpha_2 \times \left[\frac{1}{2} - \frac{1}{2\pi}\cos^{-1}\frac{A}{2-A}\right] \tag{5}$$

$$\frac{T_L}{T_r} = \alpha_2 \times \frac{\sqrt{1-A}}{\pi A}. \tag{6}$$

According to Fig. 5, the switching period is $T_S = T_m + T_D$, where $T_m = T_F + T_P + T_L$, and T_D is the duration of dead-time mode. When T_D is zero (dead-time is not inserted), $T_S = T_m$, and thus, the switching frequency is at maximum. This situation is named as the maximum power delivery condition. The converter voltage gain at this condition is denoted by A_m, which represents the maximum attainable voltage gain. A_m is determined by the ratio of the load resistance to the tank characteristics impedance. By defining the function $\theta(x, y, z)$ as (7), T_m is calculated by (8). The normalized load *r* is defined as (9). Then, the maximum attainable voltage gain A_m as a function of *r* is expressed by (10), e.g., for $\alpha_1 = \alpha_2 = 1.05\,(L_{r1} = L_{r2} = L_r/10)$ and $r = 1, A_m$ is obtained as 0.5, which means in the absence of dead-time, $V_O = V_S/2$. Inserting dead-time would reduce the voltage gain

$$\theta(x, y, z) = \frac{\pi x}{2} + \frac{y}{2}\left[\pi + \frac{2\sqrt{1-z}}{z} - \cos^{-1}\frac{z}{2-z}\right] \tag{7}$$

$$\frac{\pi T_m}{T_r} = \theta(\alpha_1, \alpha_2, A) \tag{8}$$

$$r = \frac{R}{Z_r} = \frac{V_O^2}{P_{\text{out}} Z_r} \tag{9}$$

$$r = A_m^2 \cdot \theta(\alpha_1, \alpha_2, A_m). \tag{10}$$

As illustrated in Fig. 5, the peak currents of Q_1 and Q_2 are, respectively, as $V_S/(\alpha_1 Z_r)$ and $(2V_S - V_O)/(\alpha_2 Z_r)$. As a result, the current stresses of the switches can be independently controlled by adjusting α_1 and α_2. When Q_1 is turned on, a resonance starts between the circuit inductances and the output parasitic capacitance of Q_2 (which is denoted by c_2 in Fig. 6). Then a sinusoidal current flows through c_2. Similarly, when Q_2 is turned ON, a sinusoidal current flows through c_1. Since in a reasonable design c_1 and c_2 are much less than C_r, their effects on the converter voltage gain are negligible. The peak of currents passing through c_1 and c_2 are obtained as follows. Thus, α_1 and α_2 also determine the maximum currents flow through the parasitic capacitances c_1 and c_2

$$I_{c1} = \frac{2V_S - V_O}{\sqrt{\frac{L_{r1}+L_{r2}}{c_1}}} \tag{11}$$

$$I_{c2} = \frac{V_S}{\sqrt{\frac{L_{r1}+L_{r2}}{c_2}}}. \tag{12}$$

IV. General Configuration

As illustrated in Fig. 1, migration from the SISO topology of Fig. 6 to the MIMOB topology is simple. The MIMOB converter has *N* input, *M* output, and *K* bidirectional ports. To drain energy from the voltage source V_{Sn}, the switch Q_{1n} is turned on and then C_r is charged up to $2V_{Sn}$. Next, the energy stored in C_r is delivered to V_{Om} by turning Q_{2m} on. Consequently, the power can be routed from each arbitrary input port to each arbitrary output port. Since after each switching cycle, v_r and i_r are set at zero (as proven previously), all switching cycles are independent from each other. Therefore, in each switching cycle, the multiport converter of Fig. 1 exactly behaves as the SISO converter of Fig. 6. The inductors L_{r11} to L_{r1N}, L_{r21} to L_{r2M} and L_{rb1} to L_{rbK} provide more degrees of freedom for designer. The required number of bidirectional ports can be added. Q_{b11} along with the antiparallel diode of Q_{b21} create an FCBB switch, and so on, for Q_{b21} and the antiparallel diode of Q_{b11}. To charge V_{B1} from V_{Sn}, first Q_{1n} is turned on and then Q_{b21}. To transfer energy from V_{B1} to V_{Om}, first Q_{b11} is turned on and then Q_{2m}. Obviously, soft-switching conditions are provided for all switches at all conditions.

V. Route Matrix

In the MIMOB converter, *switching pattern* is defined as a sequence of switching signals repeated periodically. For example, consider an MIMOB converter that includes one input, two output, and one bidirectional ports. An instance of the switching pattern is demonstrated in Fig. 7, where the power is routed as: 1) V_{S1} to V_{O1}; 2) V_{S1} to V_{O2} two times; 3) V_{S1} to V_{B1}; 4) V_{B1} to V_{O2}; and 5) dead-time.

As shown in Fig. 7, T_m is the switching cycle duration of each routing, T_M is the interval in which the converter is active, and T_D is the dead-time. For Fig. 1 (*N* input, *M* output, and *K* bidirectional ports), the route matrix $\mathbf{\Gamma}$ is defined as (13). This matrix has $(N + K)$ rows and $(M + K)$ columns. The rows show input ports and the columns are for the output

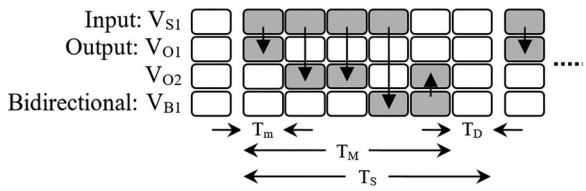

Fig. 7. Example for switching pattern.

ports. Bidirectional ports exist in rows as well as columns. The entries of this matrix Γ_{ij} indicate the number of times which power is transferred from each input/bidirectional port to each output/bidirectional port during one switching pattern. In the earlier example, $\mathbf{\Gamma} = \left[\begin{smallmatrix}1 & 2 & 1\\ 0 & 1 & 0\end{smallmatrix}\right]$. According to (13), four processes exist: 1) V_{Si} supplies V_{Oj}; 2) V_{Si} charges the energy storage element V_{Bk} (battery); 3) V_{Bk} supplies V_{Oj}; and 4) internal energy exchange between V_{Bi} and V_{Bj} (for voltage balancing [28]). Obviously, V_{Bk} to V_{Bk} (V_{Bk} discharges and charges itself) is possible but is not reasonable and thus the corresponding coefficients at $\mathbf{\Gamma}$ are set zero

$$\mathbf{\Gamma} = \begin{array}{c} \\ V_{S1} \\ \vdots \\ V_{SN} \\ V_{B1} \\ \vdots \\ V_{BK} \end{array} \begin{array}{c} \begin{array}{cccccc} V_{O1} & \cdots & V_{OM} & V_{B1} & \cdots & V_{BK} \end{array} \\ \begin{bmatrix} \bullet & & \bullet & \bullet & & \bullet \\ & \ddots & & & \ddots & \\ \bullet & & \bullet & \bullet & & \bullet \\ \bullet & & \bullet & 0 & & \bullet \\ & \ddots & & & \ddots & \\ \bullet & & \bullet & \bullet & & 0 \end{bmatrix} \end{array}. \tag{13}$$

The coefficients α are defined as (14). Since the bidirectional branches are IO ports, V, U, and β are defined as (15)–(18), e.g., in the earlier example, $V_1 = V_{S1}, V_2 = V_{B1}, U_1 = V_{O1}, U_2 = V_{O2}$, and $U_3 = V_{B1}$. Thus, V_i shows an input port, which is at the ith row of $\mathbf{\Gamma}$ and U_i shows an output port, which is at the jth column of $\mathbf{\Gamma}$

$$\begin{cases} \alpha_{1i} = \sqrt{1 + L_{r1i}/L_{r0}}, & i = 1, \ldots, N \\ \alpha_{2j} = \sqrt{1 + L_{r2j}/L_{r0}}, & j = 1, \ldots, M \\ \alpha_{bk} = \sqrt{1 + L_{rbk}/L_{r0}}, & k = 1, \ldots, K \end{cases} \tag{14}$$

$$V_i = \begin{cases} V_{Si}, & \text{if } i \le N \\ V_{B(i-N)}, & \text{otherwise} \end{cases}, \quad i = 1, \ldots, (N + K) \tag{15}$$

$$U_j = \begin{cases} V_{Oj}, & \text{if } j \le M \\ V_{B(j-M)}, & \text{otherwise} \end{cases}, \quad j = 1, \ldots, (M + K) \tag{16}$$

$$\beta_{1i} = \begin{cases} \alpha_{1i}, & \text{if } i \le N \\ \alpha_{b(i-N)}, & \text{otherwise} \end{cases}, \quad i = 1, \ldots, (N + K) \tag{17}$$

$$\beta_{2j} = \begin{cases} \alpha_{2j}, & \text{if } j \le M \\ \alpha_{b(j-M)}, & \text{otherwise} \end{cases}, \quad j = 1, \ldots, (M + K). \tag{18}$$

Within one switching pattern, the total energy drained from the input source V_i is E_{Ii} as (19), and the total energy delivered to the output port U_j is E_{Oj} as (20). $\theta_M = \pi T_M/T_r$ is given

by (21) where T_M is shown in Fig. 7 and $T_{m,ij}$ is the switching duration of routing from V_i to U_j

$$E_{I\,i} = 2C_r V_i^2 \sum_{j=1}^{M+K} \Gamma_{ij} \tag{19}$$

$$E_{O\,j} = 2C_r \sum_{i=1}^{N+K} \Gamma_{ij} V_i^2 \tag{20}$$

$$\theta_M = \sum_{i=1}^{N+B} \sum_{j=1}^{M+B} \Gamma_{ij}\theta\left(\beta_{1i}, \beta_{2j}, \frac{U_j}{V_i}\right) = \frac{\pi}{T_r} \sum_{i=1}^{N+B} \sum_{j=1}^{M+B} \Gamma_{ij} T_{m,ij}. \tag{21}$$

When $T_D = 0$, the system sets at maximum power delivery condition and $T_S = T_M$. Then, the maximum power can be drained from the input source V_i is $P_{MIi} = E_{Ii}/T_M$ as (22). Similarly, P_{MOj} is the maximum power that can be delivered to U_j and is given by (23)

$$P_{MI\,i} = \frac{V_i^2 \sum_{j=1}^{M+K} \Gamma_{ij}}{Z_r \theta_M} \tag{22}$$

$$P_{MO\,j} = \frac{\sum_{i=1}^{N+K} \Gamma_{ij} V_i^2}{Z_r \theta_M}. \tag{23}$$

VII. Design Methods

A. Design Method

The tank characteristics impedance Z_r controls the converter power rating, and its characteristics frequency ω_r ascertains switching frequency. Z_r is determined by satisfying maximum power delivery condition at the minimum of source voltage and maximum of the output power. The employed technology, especially transition times of the switches, limits ω_r. At least one of the inductors of Fig. 1 can be omitted without affecting the system operation.

Design I (SISO converter): Consider a 225-W SISO converter for input voltage range of 170–220 V, the output voltage of $V_O = 150$ V, and 20% overdesign. Assume that the converter efficiency is 94%.

Solution I: Equation (23) is rewritten as (24), which can be simplified to (25). Then, according to (8), (26) is obtained. By multiplying (25) by (26) and simplifying, (27) is achieved. Maximum switching frequency is chosen $T_m^{-1} = 250$ kHz, and then $C_r = 20$ nF is attained. For $\alpha_{11} = \alpha_{21} = 1\,(L_{r11} = L_{r21} = 0)$, L_r is calculated as 20 μH. A complete set of experimental waveforms and curves of this converter is presented in [5]. As shown in [5], since $L_{r11} = L_{r21} = 0$, current spikes are created at turn-on instants of the switches. To limit these current spikes, proper values of α_{11} and α_{21} are calculated by using (11) and (12). Experimental waveforms of such converter are demonstrated in [7]

$$\frac{225 \times 1.2}{0.94} = \frac{\Gamma_{11} \times 170^2}{Z_r \times \Gamma_{11} \times \theta\left(\alpha_{11}, \alpha_{21}, \frac{150}{170}\right)} \tag{24}$$

$$Z_r \times (1.57\alpha_{11} + 1.63\alpha_{21}) \cong 100\,\Omega \tag{25}$$

$$\frac{\pi T_m}{T_r} = 1.57\alpha_{11} + 1.63\alpha_{21} \tag{26}$$

$$\frac{T_m}{C_r} = 200\,\Omega. \tag{27}$$

Design II (Single-input MO converter): Consider a 250-W single-input double-output (1I2O) converter for $V_{S1} = 200$ V, $V_{O1} = 100$ V, $P_{MO1} = 100$ W, $V_{O2} = 150$ V, and $P_{MO2} = 150$ W. Initially, it is assumed that all circuit elements are ideal, and then 20% overdesign is taken into account.

Solution II: Equation (23) for each output port is rewritten as (28). Thus, $\Gamma_{12}/\Gamma_{11} = 3/2$, and therefore, $\Gamma_{11} = 2$ and $\Gamma_{12} = 3$ are proper. Equation (8) is rewritten as (29), where $\alpha_{11} = 1$ is chosen. The current stress of Q_{12} is $(2 \times 200 - 100)/(\alpha_{21} Z_r)$ and that of Q_{22} is equal to $(2 \times 200 - 150)/(\alpha_{22} Z_r)$. Since both loads currents are equal $(100/100 = 150/150)$, the current stresses of both Q_{12} and Q_{22} are also set equal which results in $\alpha_{21} = 1.2\alpha_{22}$. By applying $T_r = 4\,\mu$s and $\alpha_{22} = 1.05$, then $Z_r = 41.22\,\Omega$ is obtained. With 20% overdesign Z_r is set at 34.35 Ω. Finally, the circuit elements are calculated as $C_r = 18.5$ nF, $L_{r0} = 21.9\,\mu$H, $L_{r11} = 0$, $L_{r21} = 12.9\,\mu$H, and $L_{r22} = 2.2\,\mu$H. The experimental results of this converter are illustrated in Section VIII

$$100 = \frac{\Gamma_{11} \times 200^2}{Z_r \theta_M} \qquad 150 = \frac{\Gamma_{12} \times 200^2}{Z_r \theta_M} \tag{28}$$

$$\pi T_{m,11}/T_r = 1.57 + 2.37\alpha_{21}$$

$$\pi T_{m,12}/T_r = 1.57 + 1.77\alpha_{22}. \tag{29}$$

Design III (Multi-input single-output converter): A 200-W double-input single-output (2I1O) converter for $V_{S1} = 240$ V, $V_{S2} = 160$ V, and $V_{O1} = 150$ V is considered. It is required to program the converter for power budgeting as $P_{MI1} = 120$ W and $P_{MI2} = 80$ W.

Solution III: Equation (22) for each input port is rewritten as (30). Thus, $\Gamma_{21}/\Gamma_{11} = 3/2$, and thus, $\Gamma_{11} = 2$ and $\Gamma_{21} = 3$ are proper. Equation (8) is rewritten as (31), where, as a degree of freedom, $\alpha_{21} = 1$ is chosen. To have identical switching durations, $T_{m,11}$ and $T_{m,21}$ are both set equal to 10 μs. By using $\alpha_{11} = 1.05$, then $\alpha_{12} = 1.31$, $f_r = 116$ kHz, $Z_r = 52.6\,\Omega, C_r = 26.1$ nF, $L_{r0} = 72.2\,\mu$H, $L_{r11} = 7.4\,\mu$H, and $L_{r21} = 51.7\,\mu$H are obtained

$$120 = \frac{\Gamma_{11} \times 240^2}{Z_r \theta_M} \qquad 80 = \frac{\Gamma_{21} \times 160^2}{Z_r \theta_M} \tag{30}$$

$$\pi T_{m,11}/T_r = 1.57\alpha_{11} + 2$$

$$\pi T_{m,21}/T_r = 1.57\alpha_{12} + 1.59. \tag{31}$$

Design IV (MIMO converter): With the proposed converter, it is possible to have both input power budgeting and individually regulated outputs simultaneously. The design is still

quite simple. For instance, consider a 200-W double-input double-output (2I2O) converter. The input voltage sources are $V_{S1} = 240$ V and $V_{S2} = 160$ V; and the desired output voltages are $V_{O1} = 150$ V and $V_{O2} = 100$ V. The required power budgeting is $P_{MI1} = 120$ W and $P_{MI2} = 80$ W, and the output power ratings are $P_{MO1} = 150$ W and $P_{MO2} = 50$ W. It is assumed that all elements are ideal.

Solution IV: Equations (22) and (23) are, respectively, rewritten as (32) and (33). Then, $\Gamma_{11} = 23, \Gamma_{12} = 5, \Gamma_{21} = 27$, and $\Gamma_{22} = 15$ are obtained. Therefore, a switching pattern at full-load includes $23 + 5 + 27 + 15 = 70$ switching cycles, where, for instance, in 23 cycles power is transferred from V_{S1} to V_{O1}. To have a smooth operation, these 23 cycles are distributed appropriately in the switching pattern. The solution is continued exactly the same as previous examples and the circuit elements are calculated as $f_r = 200$ kHz, $Z_r = 37.84\,\Omega$, $C_r = 1$ nF, $L_{r0} = 1.4\,\mu$H, $L_{r11} = 0\,\mu$H, $L_{r12} = 1.75\,\mu$H, $L_{r21} = 3.65\,\mu$H, and $L_{r22} = 0.14\,\mu$H

$$120 = \frac{240^2 \times (\Gamma_{11} + \Gamma_{12})}{Z_r \theta_M} \qquad 80 = \frac{160^2 \times (\Gamma_{21} + \Gamma_{22})}{Z_r \theta_M} \tag{32}$$

$$150 = \frac{240^2 \Gamma_{11} + 160^2 \Gamma_{21}}{Z_r \theta_M} \qquad 50 = \frac{240^2 \Gamma_{12} + 160^2 \Gamma_{22}}{Z_r \theta_M}. \tag{33}$$

Design V (SISO bidirectional converter): Since the proposed converter is step down, the constraint of $V_S > V_B > V_O$ must be held. However, holding this constraint is not restrictive for many applications. A SISOB converter for the input voltage source $V_S = 60$ V, the battery nominal voltage $V_B = 48$ V, and the output voltage $V_O = 36$ V is considered for this design. The maximum output power is 36 W where additional 12 W should be provided also for battery charging during the normal condition.

Solution V: The parameters are set as $V_1 = V_S, V_2 = U_2 = V_B$, and $U_1 = V_O$. To control the converter, the route matrix $\mathbf{\Gamma}$ is determined at run-time and configures the converter according to the circumstances. For the normal condition $V_S \geq 60$ V power is transferred from V_S to V_O and the battery can be charged. The converter parameters, in this condition marked by superscript (1), are $\mathbf{\Gamma}^{(1)}$ and $\theta_M^{(1)}$. The other condition is input voltage failure where $V_S < 60$ V in which the power transmission from V_S is terminated and the battery has to feed the load. The parameters at this condition are denoted as $\mathbf{\Gamma}^{(2)}$ and $\theta_M^{(2)}$. In the normal condition, $P_{MO1} = 36$ W and $P_{MO2} = 12$ W, and thus, (23) is rewritten as (34), which yields to $\Gamma_{11}^{(1)} = 3, \Gamma_{12}^{(1)} = 1, \Gamma_{21}^{(1)} = \Gamma_{22}^{(1)} = 0$, and $Z_r \theta_M^{(1)} = 300\,\Omega$. In the condition of $V_S < 60$ V, (23) is rewritten as (35), and therefore, $\Gamma_{21}^{(2)} = 1, \Gamma_{11}^{(2)} = \Gamma_{12}^{(2)} = \Gamma_{22}^{(2)} = 0$, and $Z_r \theta_M^{(2)} = 64\,\Omega$. According to (17) and (18), $\beta_{11} = \alpha_{11}, \beta_{21} = \alpha_{21}$, and $\beta_{12} = \beta_{22} = \alpha_{b1}$. Then, by using (21) and simplifying, (36) is obtained. Since $\theta_M^{(1)}/\theta_M^{(2)} = 300/64$, (36) is reduced to (37). A design can be as $\alpha_{b1} = 1, \alpha_{11} = 1.4$, and $\alpha_{21} = 1.48$. Finally, Z_r is determined as $15.27\,\Omega$

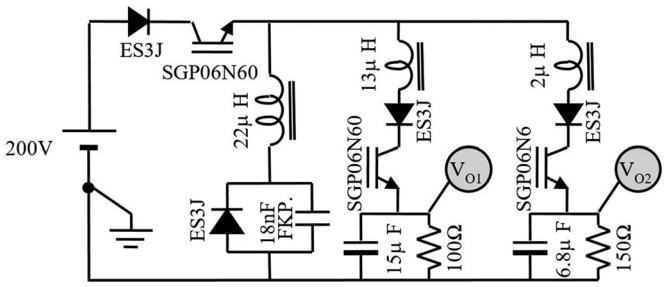

Fig. 8. Implemented resonant 250 W 1I2O Buck-G.

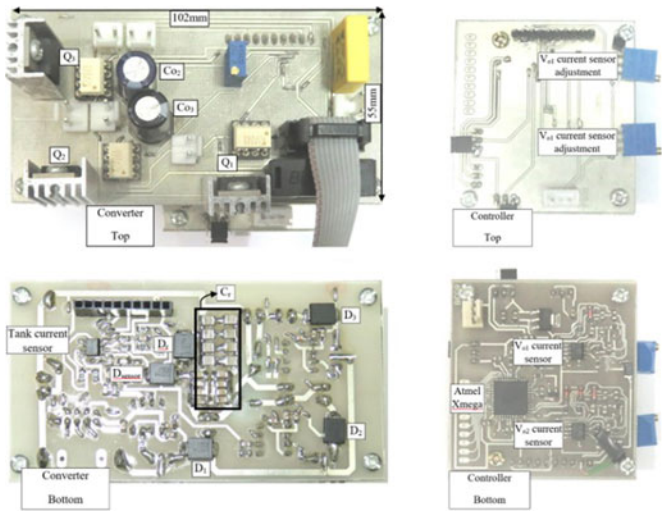

Fig. 9. Photo of the implemented prototype.

$$36 = \frac{60^2 \Gamma_{11}^{(1)}}{Z_r \theta_M^{(1)}} \qquad 12 = \frac{60^2 \Gamma_{12}^{(1)}}{Z_r \theta_M^{(1)}} \tag{34}$$

$$36 = \frac{48^2 \Gamma_{21}^{(2)}}{Z_r \theta_M^{(2)}} \tag{35}$$

$$\theta_M^{(1)} = 6.28\alpha_{11} + 6.18\alpha_{21} + 1.71\alpha_{b1}$$

$$\theta_M^{(2)} = 1.57\alpha_{b1} + 1.77\alpha_{21} \tag{36}$$

$$6.28\alpha_{11} = 5.65\alpha_{b1} + 2.13\alpha_{21}. \tag{37}$$

VIII. Experimental Results

For Design II performed in Section VII, the converter schematic is illustrated in Fig. 8. The resonant passive elements were calculated previously and the semiconductor devices are selected according to their current and voltage stresses. The employed switches are 06N60 since IGBT is more compatible with the presented ZCS operation [6]. The prototype is shown in Fig. 9 where an ATMEL XMega is used as the controller (ATxmega32A4U).

The output voltage ripple ΔV_O is at maximum when the load is at minimum. The worst condition is zero load wherein the

TABLE I
VOLTAGE REGULATION ERROR IN PERCENTAGE VERSUS OUTPUT POWER

$U_{j,vre}$ (%)		Output power of V in Watts						
		5	25	50	75	100	125	150
Output power of V_{O1} in Watts	5	0.47	0.47	0.46	0.47	0.46	0.46	0.47
		0.47	0.42	0.37	0.32	0.27	0.22	0.17
	25	0.43	0.42	0.42	0.36	0.38	0.40	0.40
		0.47	0.42	0.36	0.32	0.27	0.22	0.16
	50	0.37	0.36	0.36	0.35	0.36	0.33	0.34
		0.46	0.42	0.37	0.32	0.27	0.16	0.16
	75	0.30	0.29	0.28	0.30	0.26	0.28	0.28
		0.46	0.42	0.37	0.32	0.21	0.10	0.15
	100	0.24	0.24	0.24	0.23	0.17	0.18	0.18
		0.46	0.42	0.37	0.24	0.27	0.09	0.15

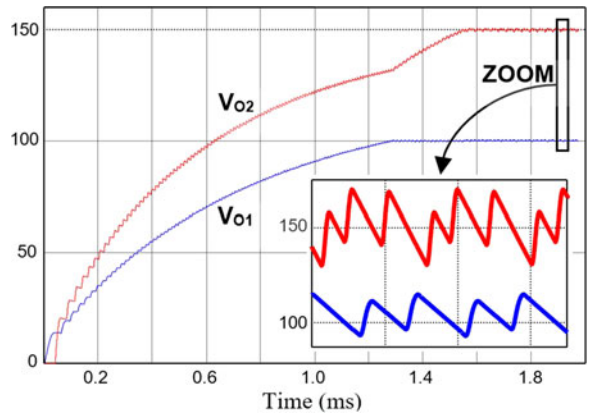

Fig. 10. Output voltage (V) at full load: startup and steady state.

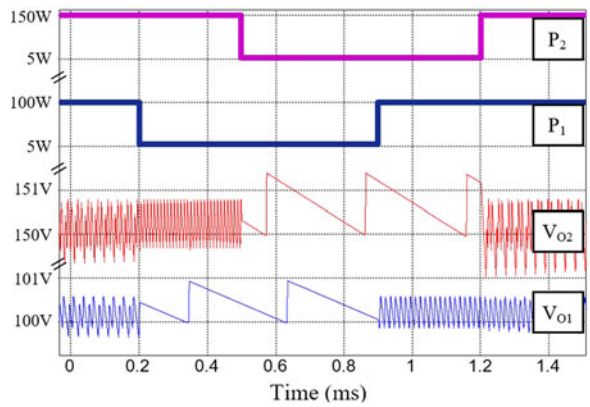

Fig. 11. Dynamics operation: load-step response.

peak-to-peak output voltage ripple is given by $\Delta V_{OPP}/V_O = 2C_r/(C \cdot A^2)$ [5]. In Fig. 8, C_1 and C_2 are determined for maximum 1% peak-to-peak output voltage ripple.

Voltage regulation error which is defined as $U_{j,vre} = |U_{j,\text{avg}} - U_{j,d}|/U_{j,d}$ versus output power is presented in Table I. In each cell of this table, the top value is the voltage regulation error of V_{O1} in percentage and the bottom value is that of V_{O2}. The voltage regulation error in all conditions is less than one half of the output voltage ripple, which indicates an independent regulation for both output ports ($U_{j,vre} < 0.5\%$).

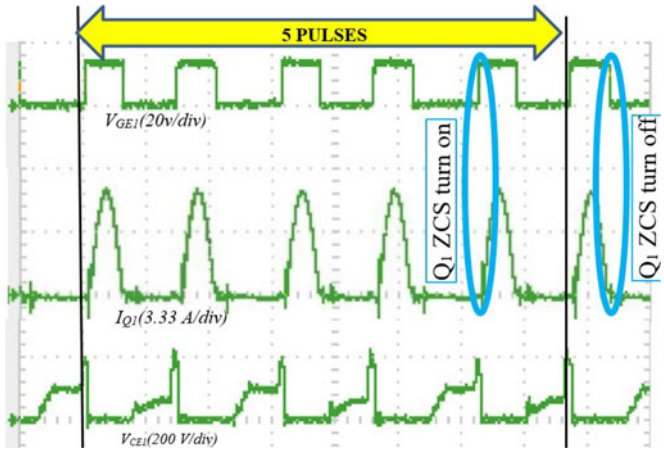

Fig. 12. Q1 soft-switching waveforms, time (5 μs/div).

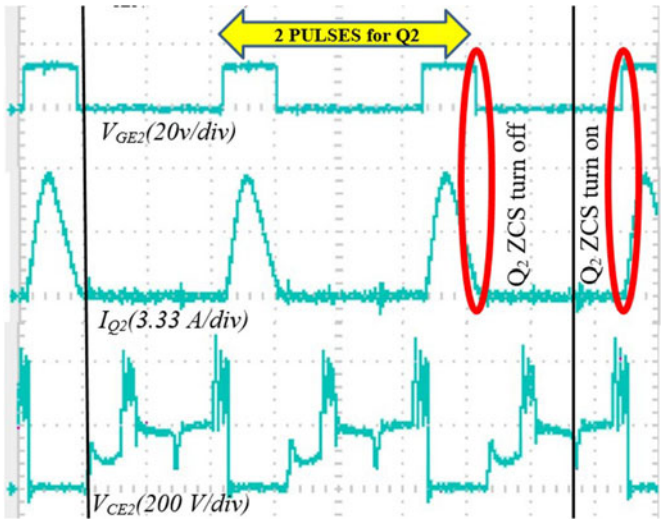

Fig. 13. Q2 soft-switching waveforms, time (5 μs/div).

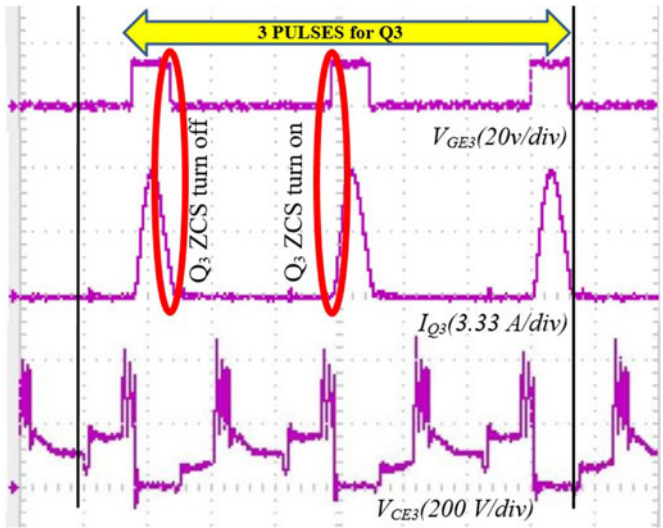

Fig. 14. Q3 soft-switching waveforms, time (5 μs/div).

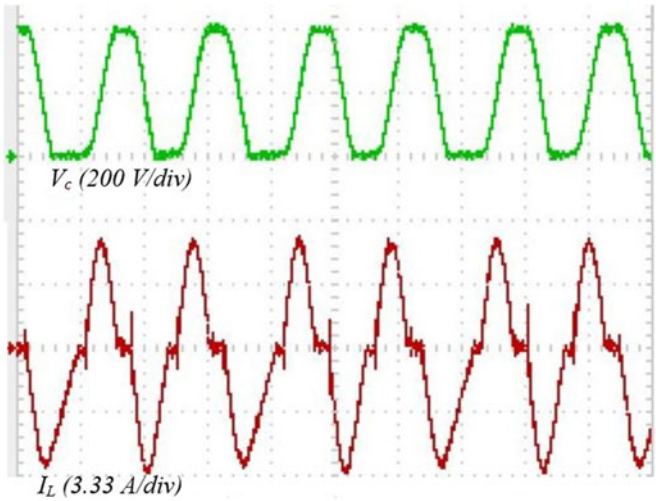

Fig. 15. State variables of the resonant tank, time $(5\,\mu s/\text{div})$.

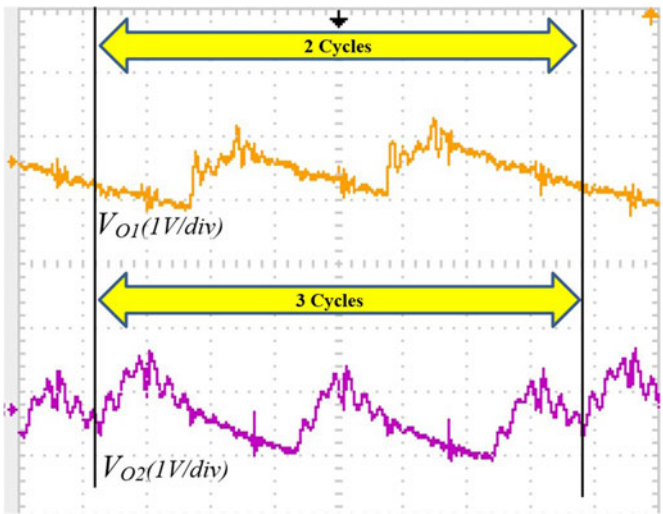

Fig. 16. Output voltage ripples, time $(5\,\mu s/\text{div})$.

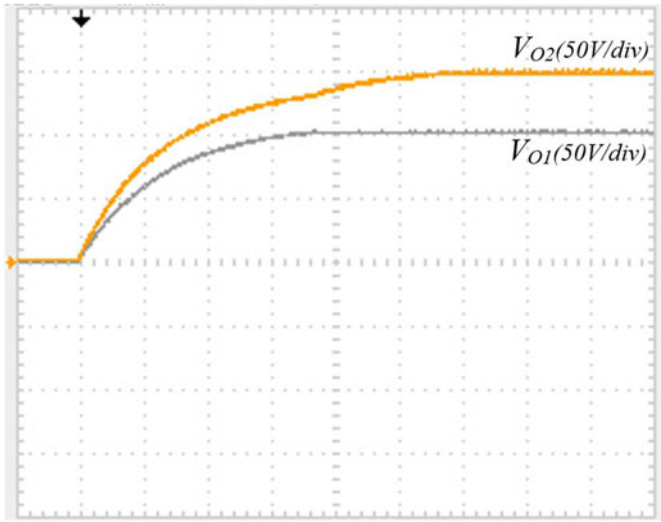

Fig. 17. Startup until settling time of both output at full load, time $(500\,\mu s/\text{div})$.

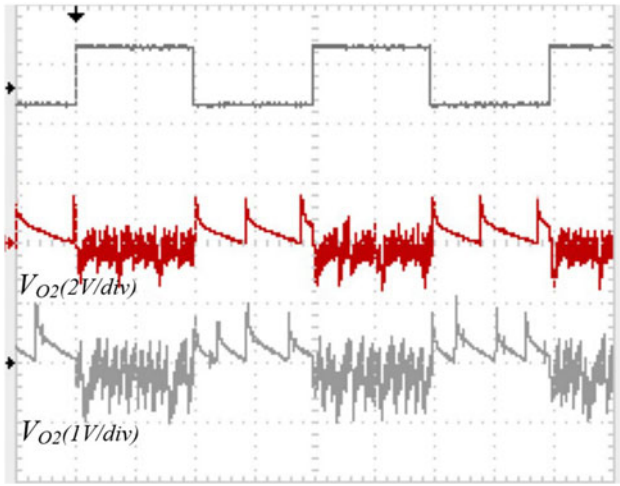

Fig. 18. Both output load responses of change load, time $(250\,\mu s/\text{div})$.

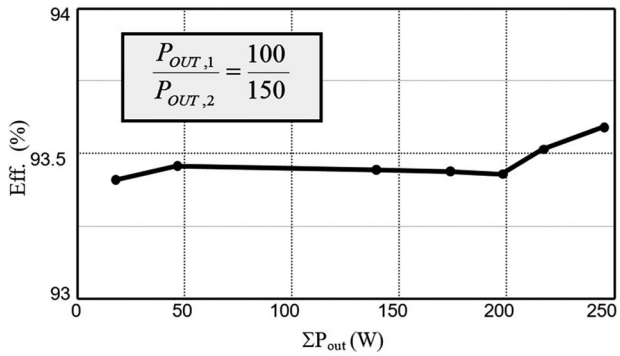

Fig. 19. Measured efficiency versus output power.

Fig. 10 shows the simulation results for the output voltages at startup and steady state. During the startup time, V_{O1} and V_{O2} increase simultaneously; first, V_{O1} reaches to its desired value 100 V and then V_{O2} reaches to 150 V. The total startup time is less than 1.5 ms, without any voltage overshoot before the settling time. Output voltage ripples at steady state are also illustrated. Fig. 11 presents the converter dynamic operation in confront of abrupt load variations (load-step response). According to this figure, both output voltages are free of overshoot/undershoot with peak-to-peak voltage ripple less than or equal to the desired values.

The experimental waveforms are presented in Figs. 12–19. Figs. 12, 13, and 14 show soft-switching operations of Q_1, Q_2, and Q_3, respectively. Accordingly, ZCS turn-on and ZCS turn-off are attained for all switches. The waveforms are synchronized, and each screen includes the captured traces of gate–emitter voltage, collector current, and collector–emitter voltage, respectively, from the top. A switching pattern is a frame containing five switching cycles (see Fig. 12), in which in two switching cycles, power is transferred to port 1 (see Fig. 13) and in three cycles, power is routed to port 2 (see Fig. 14). State variables of the resonant tank v_r and i_r are presented in Fig. 15. For both ports and output voltage ripples are illustrated in

Fig. 16. Dynamics of the converter are presented in Figs. 18 and 19. Output voltage of both output ports during startup until settling time are illustrated in Fig. 17. The achieved soft-start profiles comply with the aforementioned discussions. Fig. 18 shows the load responses of both output terminals versus abrupt load changing from 10% to full load and vice versa. The top trace is the converter total output power (25–250 W), and the second and third traces are the corresponding output voltage waveforms of output ports V_{O1} and V_{O2} in ac mode (output voltage ripples). According to this figure, both output voltages are kept within the 1% band, which has been determined as the maximum peak-to-peak output voltage ripple. The converter efficiency curve is presented in Fig. 19. Since the converter always operates in discontinuous conduction mode, the efficiency is almost constant.

IX. Conclusion

A new transformerless resonant multiport converter is presented. Systematic synthesis, point-to-point power routing, common ground between all ports, bidirectional operation capability, and few element number are the advantages of the proposed converter. Experimental results from a 250-W laboratory prototype confirm the integrity of the proposed converter and the presented theoretical analysis.

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