Research on a 4000-V-Ultrahigh-Input-Switched-Mode Power Supply Using Series-Connected MOSFETs

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***Abstract*—A 4000-V-ultrahigh-input voltage-switched-mode power supply (UHV-SMPS) using series-connected MOSFETs is designed in this paper. The main contributions of the proposed scheme include the common-mode interference modeling of the multiswitch structure, voltage balance of the switches and driving method. First, the common-mode interference of UHV-SMPS is evaluated by a high-frequency equivalent model of the proposed scheme. Then, a detailed multiswitch common-mode electromagnetic interference mathematical model is derived and the interference quantity is calculated according to the coupling of series-connected switches. Second, a new mathematical regulation for passive snubber circuit is proposed to realize input voltage balance. Through the regularity of the equivalent parasitic capacitances, the design of compensatory capacitance and voltage balance can realized with ease. Third, a novel driving method based on integrated pulse transformer is proposed. It can achieve both good consistency to the gate signals of MOSFETs and ultrahigh isolation voltage in the wide range input applications. Finally, the experimental results obtained from a 300–4000 V wide range input prototype verified the feasibility of the proposed scheme and accuracy of the theoretical analysis.**

***Index Terms*—Common-mode (CM) interference, series connected, ultrahigh input, voltage balance.**

NOMENCLATURE

$V_{\rm in}$	Input voltage.
$V_{\rm out}$	Output voltage.
$V_{\rm gs}$	Driver output voltage.
$V_1 \sim V_n$	Interference sources' voltages of *N* MOSFETs.
$V_{\rm ds}$	Voltage between drain and source of MOSFET.
P_o	Maximum output power.
$C_{\rm in}$	Input capacitance.
$C_{\rm out}$	Output capacitance.
$C_{\rm ds1} \sim C_{{\rm d}sn}$	Parasitic capacitance of MOSFETs.
$C_{s1} \sim C_{sn}$	Distributed capacitance between the drain and the grounding heat sink of MOSFETs.
$C_{\rm ps}$	Stray capacitance between the primary side and the secondary side of the main transformer.
C_p	Distributed capacitance in the primary winding of the main transformer.
$C_{\rm eq}$	Equivalent capacitance in drain and source.
$C_{\rm com}$	Dynamic compensatory capacitance of MOSFET.
$C_{\rm offset}$	Benchmark compensation capacitance.
C_0	Blocking capacitance.
$C_{q1} \sim C_{qn}$	Displacement capacitance.
R_0	Drive resistance.
$R_{\rm OFF}$	Leakage resistance of MOSFET.
$R_1, C_1, D_1 \sim D_n$	*RCD* absorbing resistance, capacitance, diodes.
$S_1 \sim S_n$	Serialization of MOSFETs.
$D_{o1} \sim D_{\rm on}$	Serialization of rectifier diodes.
D	Duty cycle.
$D_{11}, D_{12} \sim D_{n1}, D_{n2}$	Zener diodes of the driving circuit.
T_r, T_f	Rising time and falling time of $V_{\rm ds}$.
v	Switching frequency.
n	Number of switches connected in series.
m	Ratio of main transformer.

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I. INTRODUCTION

IN RECENT years, the demand of ultrahigh dc voltage input auxiliary power supply is steadily growing. For example, in high-speed electrical railway traction, in coalmining industry applications, in solid-state transformers or in modular multilevel converter high-voltage direct current system (MMC-HVdc), the input voltage of auxiliary power supply is up to 2000–4000 V or even higher [1]–[3]. To fabricate this kind of power supply,

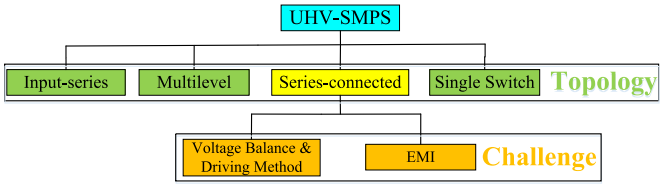

Fig. 1. Topologies and challenges of UHV-SMPS.

the very high voltage stress has to be faced with first. So, how to deal with such high input voltage becomes a serious problem [4], [5].

Nowadays, there are various solutions to overcome this challenge [6]–[24]. The methods can be divided into four groups, which are based upon input-series converters, multilevel converters, single switch with ultrahigh voltage, and series-connected switches, as shown in Fig. 1. First, using input-series converters is a popular solution. The authors in [6]–[8] reported a converter with input-series-output-parallel structure which could be used under very high input voltage. But this topology is complicated with poor reliability because of its multiple magnetic devices. And it is expensive in industry applications. In order to achieve active input voltage sharing capability, in [9], an integrated transformer is used instead of traditional multiple transformers. However, the integrated magnetics transformer is hard to design, especially when the number of series modules increased. Second, choosing multilevel dc/dc converter is another solution. However, this kind of topology is not suitable to the high-input low-power applications like 4000 V input [10], [11]. And as the number of "level" increases, the control of the whole system becomes more complex [12], [13]. Third, some scholars introduced a single corresponding voltage-level MOSFET to construct a high-voltage converter (like choosing 6300 V MOSFET for 4000 V input voltage application). While it is possible to realize electrical isolation and voltage conversion, the cost of such voltage level MOSFET is very high. Moreover, its switching characteristic is poor and it has very large $R_{\mathrm{ds(on)}}$ which will cause much loss [14]. The final option is taking power switches in series connection. The advantages are listed as follows: 1) it is a simplified and feasible structure with a single main transformer without complicated integration of series-modules; 2) it could achieve high breakdown voltage by using low-voltage MOSFET while having a better switching characteristic; and 3) it has low control complexity and low cost [15]–[24]. However, there are still two challenges in switch-series connection topology to be faced up. They are voltage balance problem and electromagnetic interference (EMI) issue.

As for series-connected switches structure, the main challenge is how to ensure an equal voltage sharing among them during static and dynamic transient states. Various voltage balance methods have been introduced, such as using vertical structure, active gate control circuit, active clamping circuit, and passive snubber circuit. In [15], a vertical structure is built for the series-connected switches based on the influence of parasitic capacitances to the power circuit physical architecture. However, this vertical structure is complex and inconvenient for engineering. In [16] and [17], the reported active gate control circuit could control the dynamic voltage sharing among the switches during switching transitions. However, it is complicated and may increase the stray capacitance in the gate driver circuit. In [18]–[22], an active clamping circuit is connected across the collector and gate of IGBT. However, the longtime conduction of the active clamping circuit as well as frequent actions of the active clamping circuit will inevitably result in high switching loss of the system. And the driving signals cannot achieve good consistency. It is because each switch needs a drive circuit. Moreover, optical feedback signals of each switch may be different. The passive snubber circuit is also widely used [23]–[26]. However, the resistor–capacitance circuit for dynamic sharing is insufficient because of the influence of parasitic capacitances to the power circuit physical architecture [23], [24]. Moreover, the *RC* snubber loss and switching loss would be large and the regulation of resistor–capacitance circuit design is sightless, disorder, and not universal [25], [26].

Another challenge is the high-frequency EMI produced by high du/dt of the switches. Because of the ultrahigh input voltage and multiswitch structure, the EMI issue becomes more serious than the traditional converter. For example, in the application of MMC-HVDC system, the interference will be conducted to the submodule's control and drive circuits. This will lead to serious damage to the voltage balance circuit as well as the stability of the whole system [25]. In [27], a series-parallel-connected topology of SiC MOSFETs is reported. A buck converter based on the MOSFETs' serialization is derived in [28]. They all realize good voltage balance characteristic. However, the EMI performance of switches connected in series was omitted. A new EMI simulation model and filter design method for flyback converter is reported in [29]. Rahmani *et al.* [30] presented an EMI analysis method for dual-switch flyback converter based on zero-current soft-switching mode. However, there is no further modeling and analysis for the EMI mechanism of series-connected switches.

In this paper, an auxiliary power supply with ultrahigh input voltage based on the serialization of SiC MOSFETs is proposed, which can be used as MMC-HVDC auxiliary power supply. In this scheme, the novelty can be listed as follows.

1) A high-frequency equivalent model for multiswitch system based on the ultrahigh-input voltage-switched-mode power supply (UHV-SMPS) is proposed. By means of the proposed model, the common-mode (CM) interference of UHV-SMPS is evaluated. A detailed multiswitch CM EMI mathematical model has been derived for the first time. The novelty of the proposed model lies in that it found the coupling difference between single-switch condition and multiswitch condition. Then, the interference quantity can be calculated according to the coupling of series-connected switches. The proposed multiswitch model can be used not only in the high-voltage auxiliary power supply, but also in other system with more than one cascade switches. It is an effective method to predict the conducted EMI emission among those switches.
2) A new mathematical regulation for passive snubber circuit is proposed to realize input voltage balance. It is

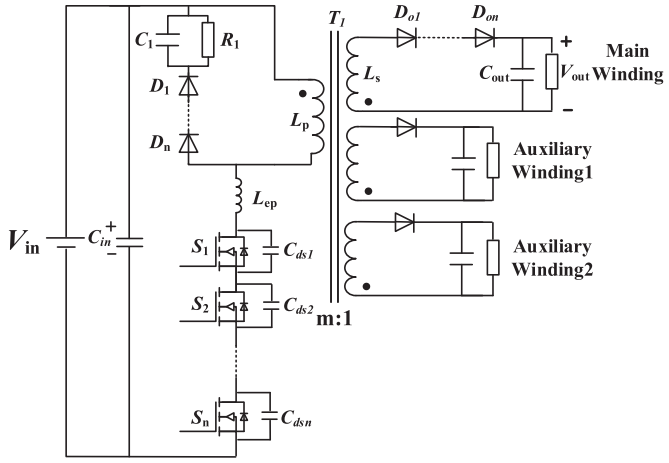

Fig. 2. Topology of the proposed UHV-SMPS.

according to the voltage unbalance causes of the series-connected MOSFETs. Through the regularity of the equivalent parasitic capacitances, the compensatory capacitance can be designed and the voltage balance can be achieved easily. Traditional trial-and-error design procedure turns out to be a mathematical analysis process.

3) A novel driving method based on integrated pulse transformer with multiple secondary windings is proposed. It can achieve both good consistency to the gate signals of MOSFETs and ultrahigh isolation voltage. By making use of the displacement capacitance, the driver output voltage $V_{\rm gs}$ is independent of the duty cycle *D*. So, this method is suitable for applications with wide range input voltage and multiple switches connected in series.

The rest of this paper is organized as follows. Section II gives the topology of the proposed UHV-SMPS and its working principle is presented. In Section III, the CM interference coupling mechanism of UHV-SMPS is analyzed and the quantitative analysis of the serialization of switches to EMI is given. Design considerations of the voltage balance for the MOSFETs in series and the pulse transformer integration driving method for the multiswitch are discussed in Section IV. Finally, in Section V, a wide range ultrahigh voltage auxiliary power supply for MMC-HVDC based on the serialization of SiC MOSFETs is designed and tested.

II. Ultrahigh Input Topology and Its Working Principle

A. Proposed Topology

The flyback converter is widely used in small- and medium-power circuits because of its advantages, such as its simplicity, providing multichannel dc output efficiently, lower EMI, having a more stable output when the input voltage fluctuations within a wide range. The topology of the proposed UHV-SMPS based on the serialization of the SiC MOSFETs is shown in Fig. 2.

The primary side of the circuit is composed of input capacitance $C_{\rm in}$, *RCD* absorbing circuit (R_1, C_1, D_1–D_n), a main transformer T_1 with leakage inductor $L_{\rm ep}$, serialization of MOSFETs $S_1 \sim S_n$, the parasitic capacitance of MOSFETs $C_{\rm ds1}$–$C_{{\rm d}sn}$. And the secondary side of the circuit includes one main output winding and several auxiliary windings which send power to the control and drive parts of the UHV-SMPS. The main winding needs serialization of rectifier diodes D_{o1}–$D_{\rm on}$ because of the large reflection voltage from primary side when MOSFETs are turned off and an output capacitance C_o.

B. Working Principle

The working principle of the proposed UHV-SMPS is analyzed as follows. To simplify the analysis, it is assumed that: 1) the auxiliary windings of the secondary side are neglected; 2) the series-connected MOSFETs S_1–S_n, the diodes of *RCD* D_1–D_n, and the rectifier diodes D_{o1}–$D_{\rm on}$ are turned on and off synchronously. The proposed UHV-SMPS operates in six modes whose equivalent circuits are shown in Fig. 3(a)–(f) and the time-related main waveforms of circuit are shown in Fig. 3(g).

Mode 1 [see Fig. 3(a), $t_0 \le t < t_1$]: at t_0, S_1–S_n are turned on, the input current $I_{\rm in}$ running through primary side of the main transformer T_1 which stores energy by the increasing of core flux, and L_p is charged by $V_{\rm in}$. During this time, the diodes D_{o1}–$D_{\rm on}$ and D_1–D_n are reverse blocked. C_1 is discharging through R_1, and $C_{\rm out}$ provides power to the load.

Mode 2 [see Fig. 3(b), $t_1 \le t < t_2$]: at t_1, when S_1–S_n are turned off, $C_{\rm ds1}$–$C_{{\rm d}sn}$ are charged and their voltages are increasing. At t_2

$$V_{C_{\rm ds1}} = V_{C_{\rm ds2}} = \cdots = V_{C_{{\rm d}sn}} = \frac{V_{\rm in} + mV_{\rm out}}{n} \tag{1}$$

and the voltage across primary side of the main transformer T_1 is $-mV_{\rm out}$ (*m* is the ratio of T_1). C_1 is discharging through R_1, and $C_{\rm out}$ provides power to the load.

Mode 3 [see Fig. 3(c), $t_2 \le t < t_3$]: at t_2, the diodes D_{o1}–$D_{\rm on}$ are turned on, and the main transformer T_1 releases energy from the primary side L_p to the secondary side L_s by the reduction of core flux. After t_2, the voltage across primary side of T_1 is fixed at $-mV_{\rm out}$, and $C_{\rm ds1}$–$C_{{\rm d}sn}$ are charged by the current of $L_{\rm ep}$. At t_3, D_1–D_n are turned on and

$$V_{C_{\rm ds1}}(t_3) = V_{C_{\rm ds2}}(t_3) = \cdots = V_{C_{{\rm d}sn}}(t_3) = \frac{V_{\rm in} + V_{C_1}}{n}. \tag{2}$$

Mode 4 [see Fig. 3(d), $t_3 \le t < t_4$]: during $t_3 - t_4$, C_1 and $C_{\rm ds1}$–$C_{{\rm d}sn}$ are charged by the current of $L_{\rm ep}$. At t_4, the energy of $L_{\rm ep}$ is reduced to zero and D_1–D_n are turned off, while the current of L_s decreases linearly.

Mode 5 [see Fig. 3(e), $t_4 \le t < t_5$]: during $t_4 - t_5$, the current of L_s still decreases linearly, while C_1 is discharging through R_1. At t_5, the current of L_s is reduced to zero.

Mode 6 [see Fig. 3(f), $t_5 \le t \le t_6$]: the rectifier diodes D_{o1}–$D_{\rm on}$ are turned off and $C_{\rm out}$ provides power to the load, while C_1 is discharging through R_1. At t_6, the switches S_1–S_n are turned on again and the next switching period begins.

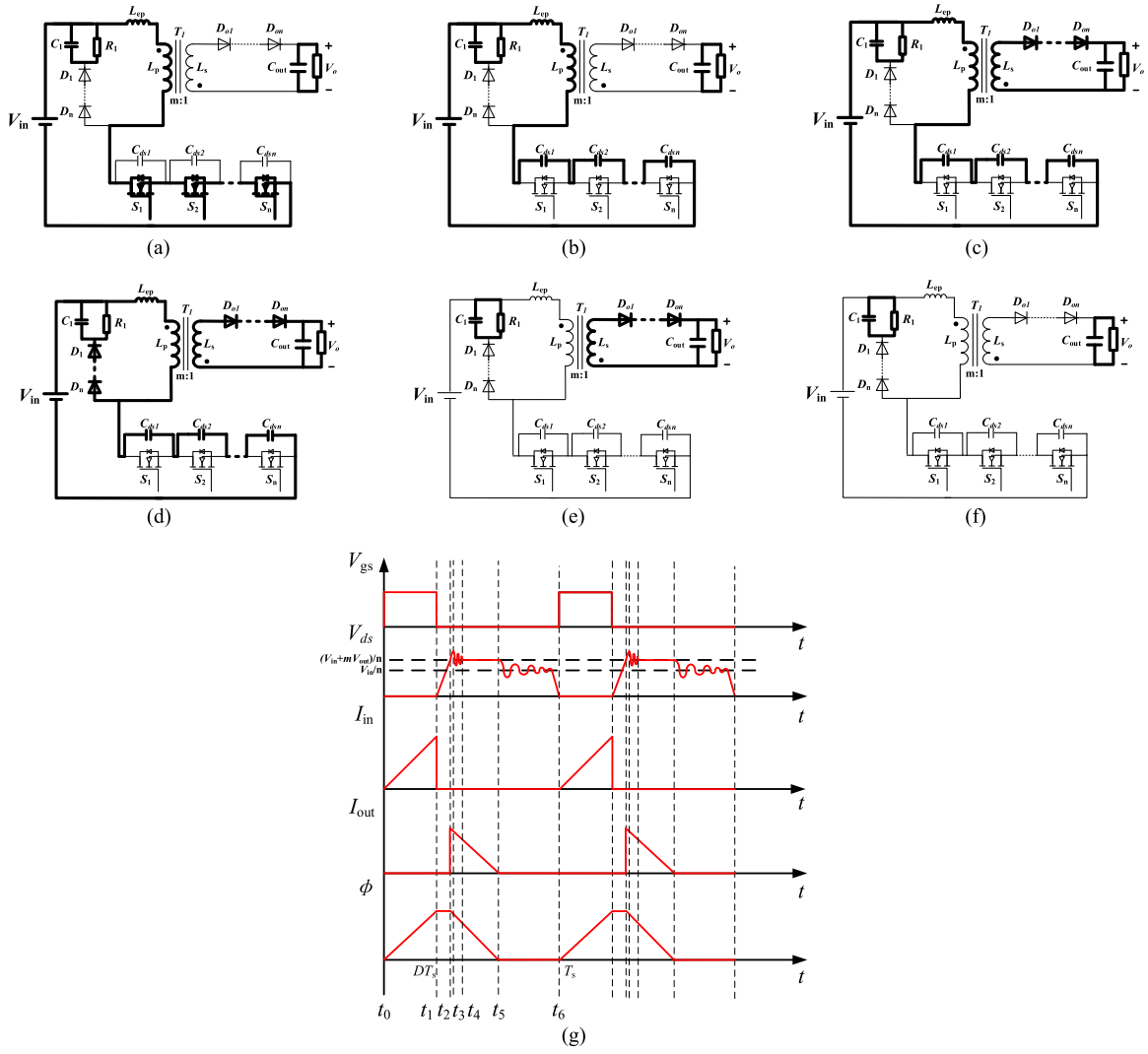

Fig. 3. Equivalent circuit of each stage. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Main waveforms under DCM.

III. CM Interference Mechanism and Multiswitch CM Noise Modeling

A. High-Frequency Equivalent Circuit of UHV-SMPS

The structure of the proposed UHV-SMPS with high-frequency parasitic circuit is shown in Fig. 4. Compared with Fig. 2, the distributed capacitance between the drain and the grounding heat sink of MOSFETs C_{s1}–C_{sn}, the stray capacitance between the primary side and the secondary side of the main transformer $C_{\rm ps}$, and the distributed capacitance of the primary winding C_p are added.

B. Analysis of Interference Sources

The voltage potential jump of MOSFET being turned on and off is the cause for the CM interference source. Thus, the $V_{\rm ds}$ voltage of MOSFET could be modeled by mathematical software Mathcad as follows.

When the flyback converter works under discontinuous conduction mode (DCM), there are two resonances (M1, M2) in the process of MOSFETs being turned on and off, which are

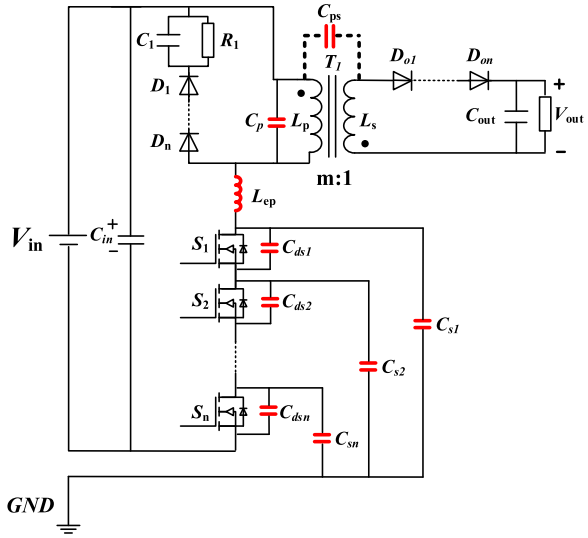

Fig. 4. Structure of the proposed UHV-SMPS with high-frequency parasitic circuit.

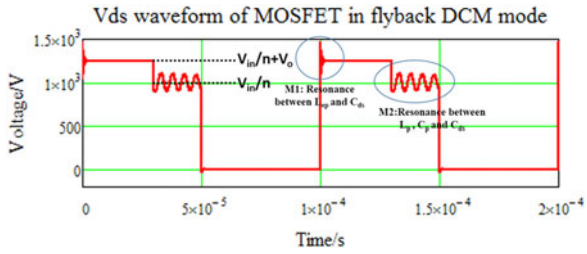

Fig. 5. MOSFET's switching waveform based on the flyback DCM mode.

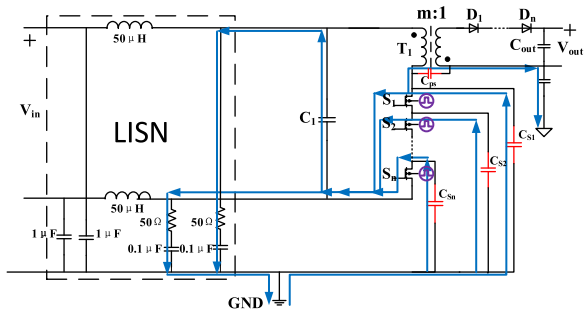

Fig. 6. CM interference conduction paths of UHV-SMPS.

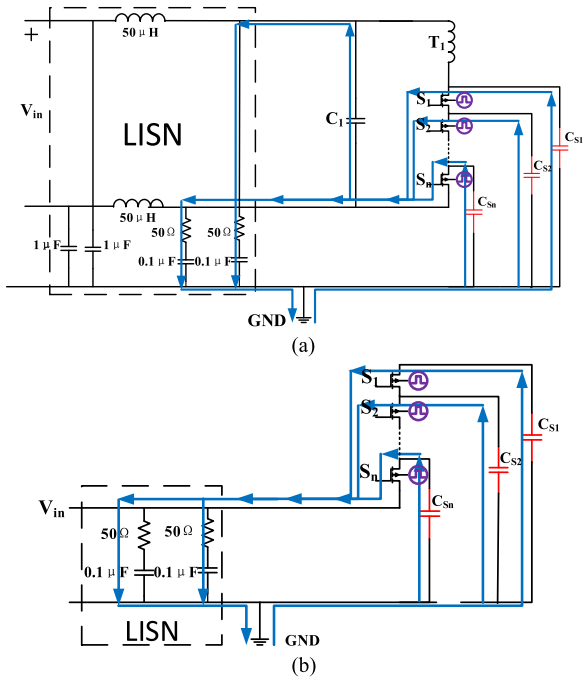

Fig. 7. Simplified derivation of the CM interference equivalent circuit. (a) Simplification 1. (b) Simplification 2.

shown in Fig. 5. Owing to a resonance between the primary-side leakage inductor $(L_{\rm ep})$ of transformer and the parasitic capacitance $(C_{\rm ds})$ of the MOSFETs, there is a high-frequency and high-voltage surge during the M1 period. Since the secondary current runs dry before the end of one switching period in the case of the DCM operation, there is a lower frequency resonance between the primary-side inductor L_p, distributed capacitance of the primary winding C_p, and $C_{\rm ds}$ of the MOSFETs, which are called the M2 resonance. The frequency of M1 and M2 resonance are calculated as follows:

$$f_{M1} = \frac{1}{2\pi\sqrt{L_{\rm ep}C_{\rm ds}}} \tag{3}$$

$$f_{M2} = \frac{1}{2\pi\sqrt{L_p\left(C_p + C_{\rm ds}\right)}}. \tag{4}$$

C. CM Interference Coupling Paths

The CM noise conduction paths of UHV-SMPS are shown in Fig. 6, and S_1–S_n are interference sources produced by the MOSFETs. On one hand, the CM noise loops by the primary-side input capacitance C_1, line impedance stabilization network (LISN), and stray capacitance C_{s1}–C_{sn} between MOSFETs' drain and ground. On the other hand, the CM noise conducts to the secondary side of transformer through secondary winding coupling capacitance $C_{\rm ps}$, then loops by the parasitic capacitance of the secondary side.

D. CM Noise Modeling of Switches' Serialization

The CM conduction paths of UHV-SMPS shown in Fig. 6 can be simplified as follows.

First, to reduce the interwinding capacitance $C_{\rm ps}$, the Faraday shield is used which can suppress the transfer of CM EMI between primary side and secondary side of the transformer. The Faraday shield is a circular metal shielding layer which is made up of a thin copper foil. One thing to note is that Faraday shield cannot be connected head-to-tail. And the Faraday shield is connected to the ground of the secondary side which cuts the conducting path to the primary side. Besides, the triple insulated wire is used as the transformer coil, which could largely (63%) reduce the stray capacitance between windings and Faraday shield. Thus, the circuit of secondary winding can be removed as presented in Fig. 7(a).

Next, in the high-frequency environment, the inductive impedance of primary winding is much larger than the capacitive impedance of input capacitance, because of the large values of the primary winding's inductor and input capacitance C_1. Therefore, the primary winding can be removed due to the CM noise not flowing through it, and the input capacitance can be also shorted out, as Fig. 7(b) shows.

Then, the derived results in Fig. 7(b) can be mathematically modeled as Fig. 8(a) shows. V_1–V_n are the interference sources' voltages of *n* MOSFETs; C_{s1}–C_{sn} are the parasitic capacitances of each MOSFET's drain to the ground. To simplify the model in Fig. 8(a) by the Thevenin–Norton equivalent network theorem, the equivalent CM interference source which has only one interference source *V* with its parasitic capacitance *C* to the ground shown in Fig. 8(b) is deduced by mathematical induction as follows.

1) If the series-connected number $N = 1$, we have (see Fig. 9)

$$V = V_1 \tag{5}$$

$$C = C_{s1}. \tag{6}$$

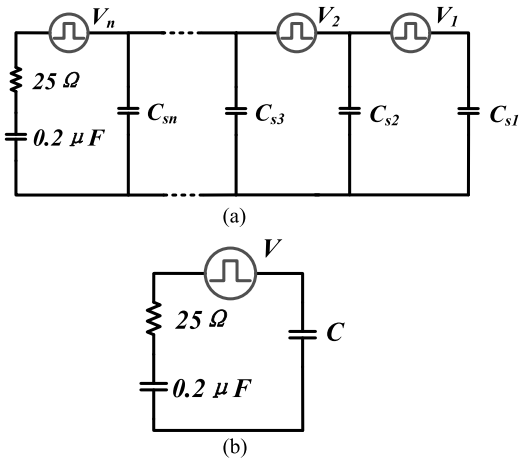

Fig. 8. Derivation of the CM interference mathematical model. (a) n MOSFETs in series. (b) Simplified equivalent model.

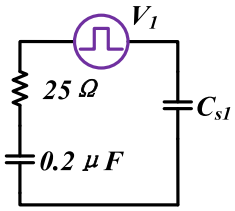

Fig. 9. Equivalent CM interference source and capacitance when $N = 1$.

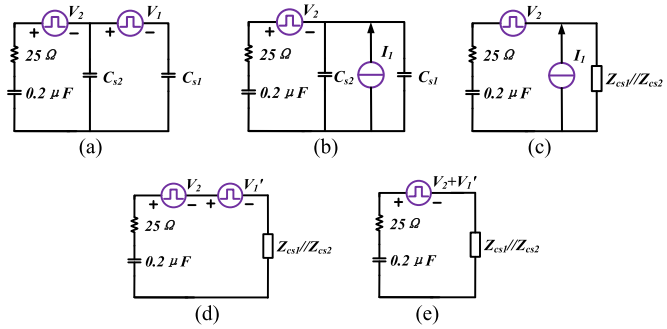

Fig. 10. Equivalent CM interference source and capacitance when $N = 2$. (a) Deduction 1. (b) Deduction 2. (c) Deduction 3. (d) Deduction 4. (e) Deduction 5.

2) If $N = 2$, see Fig. 10

$$I_1 = \frac{V_1}{Z_{CS1}} \tag{7}$$

$$V_1{}' = I_1 * (Z_{CS1}//Z_{CS2}) = \frac{V_1}{Z_{CS1}}(Z_{CS1}//Z_{CS2}) \tag{8}$$

$$V = V_2 + V_1{}' = V_2 + \frac{V_1}{Z_{CS1}}(Z_{CS1}//Z_{CS2}) = \left(\frac{V_2}{Z_{CS1}//Z_{CS2}} + \frac{V_1}{Z_{CS1}}\right)(Z_{CS1}//Z_{CS2}) \tag{9}$$

$$C = C_{s1}//C_{s2} = C_{s1} + C_{s2}. \tag{10}$$

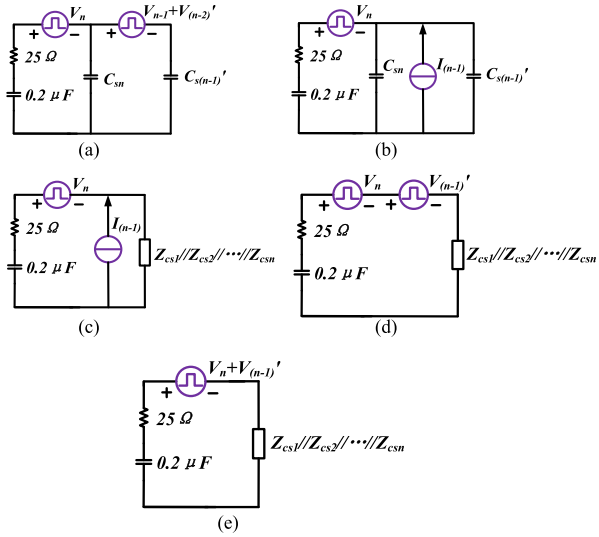

Fig. 11. Equivalent CM interference source and capacitance when $N = n$. (a) Deduction 1. (b) Deduction 2. (c) Deduction 3. (d) Deduction 4. (e) Deduction 5.

3) Assuming that when $N = n - 1$

$$V = V_{n-1} + V_{n-2}{}' = \left(\frac{V_{n-1}}{Z_{CS1}//Z_{CS2}//\cdots//Z_{CS(n-1)}} + \frac{V_{n-2}}{Z_{CS1}//\cdots//Z_{CS(n-2)}} + \frac{V_2}{Z_{CS1}//Z_{CS2}} + \frac{V_1}{Z_{CS1}}\right) * \left(Z_{CS1}//Z_{CS2}//\cdots//Z_{CS(n-1)}\right) \tag{11}$$

$$C = C_{s1}//C_{s2}//\cdots//C_{s(n-1)} = C_{s1} + C_{s2} + \cdots + C_{s(n-1)}. \tag{12}$$

4) If $N = n$, see Fig. 11.
From (11) and (12), we have

$$V_{n-1} + V_{n-2}{}' = \left(\frac{V_{n-1}}{Z_{CS1}//Z_{CS2}//\cdots//Z_{CS(n-1)}} + \frac{V_{n-2}}{Z_{CS1}//\cdots//Z_{CS(n-2)}} + \frac{V_2}{Z_{CS1}//Z_{CS2}} + \frac{V_1}{Z_{CS1}}\right) * \left(Z_{CS1}//Z_{CS2}//\cdots//Z_{CS(n-1)}\right) \tag{13}$$

$$C'_{s(n-1)} = C_{s1}//C_{s2}//\cdots//C_{s(n-1)}. \tag{14}$$

Thus, if $N = n$, then

$$I_{(n-1)} = \frac{V_{n-1} + V_{n-2}{}'}{Z'_{CS(n-1)}} = \frac{V_{n-1} + V_{n-2}}{Z_{CS1}//Z_{CS2}//\cdots//Z_{CS(n-1)}} = \frac{V_{n-1}}{Z_{CS1}//Z_{CS2}//\cdots//Z_{CS(n-1)}} + \frac{V_{n-2}}{Z_{CS1}//\cdots//Z_{CS(n-2)}} + \cdots + \frac{V_2}{Z_{CS1}//Z_{CS2}} + \frac{V_1}{Z_{CS1}} \tag{15}$$

$$V_{n-1}{}' = I_{n-1} * (Z_{CS1}//Z_{CS2}//\cdots//Z_{CSn}) = \left(\frac{V_{n-1}}{Z_{CS1}//Z_{CS2}//\cdots//Z_{CS(n-1)}} + \frac{V_{n-2}}{Z_{CS1}//\cdots//Z_{CS(n-2)}} + \frac{V_2}{Z_{CS1}//Z_{CS2}} + \frac{V_1}{Z_{CS1}}\right) * (Z_{CS1}//Z_{CS2}//\cdots//Z_{CSn}) \tag{16}$$

$$\begin{aligned} V = V_n + V_{n-1}{}' &= V_n + \left(\frac{V_{n-1}}{Z_{CS1}//Z_{CS2}//\cdots//Z_{CS(n-1)}} + \frac{V_{n-2}}{Z_{CS1}//\cdots//Z_{CS(n-2)}} + \frac{V_2}{Z_{CS1}//Z_{CS2}} + \frac{V_1}{Z_{CS1}}\right) * (Z_{CS1}//Z_{CS2}//\cdots//Z_{CSn}) \\ &= \left(\frac{V_n}{Z_{CS1}//Z_{CS2}//\cdots//Z_{CSn}} + \frac{V_{n-1}}{Z_{CS1}//Z_{CS2}//\cdots//Z_{CS(n-1)}} + \frac{V_{n-2}}{Z_{CS1}//\cdots//Z_{CS(n-2)}} + \frac{V_2}{Z_{CS1}//Z_{CS2}} + \frac{V_1}{Z_{CS1}}\right) * (Z_{CS1}//Z_{CS2}//\cdots//Z_{CSn}) \\ &= \sum_{m=1}^{n} \frac{V_m}{Z_{CS1}//\cdots//Z_{CSm}} * (Z_{CS1}//Z_{CS2}//\cdots//Z_{CSn}) \end{aligned} \tag{17}$$

$$C = C_{s1}//C_{s2}//\cdots//C_n = C_{s1} + C_{s2} + \cdots + C_n. \tag{18}$$

Next, we verify the initial value. If $n = 1$,$V = V_1$ and $C = C_{s1}$.

If $n = 2$,

$$V = \left(\frac{V_2}{Z_{CS1}//Z_{CS2}} + \frac{V_1}{Z_{CS1}}\right)(Z_{CS1}//Z_{CS2})$$

$$C = C_{s1}//C_{s2} = C_{s1} + C_{s2}.$$

Therefore, that is the end of the proof and the final equivalent voltage and capacitance are

$$V = \sum_{m=1}^{n} \frac{V_m}{Z_{CS1}//\cdots//Z_{CSm}} * (Z_{CS1}//Z_{CS2}//\cdots//Z_{CSn}) \tag{19}$$

$$C = C_{s1}//C_{s2}//\cdots//C_n = C_{s1} + C_{s2} + \cdots + C_{sn} \tag{20}$$

where Z_{cs1}–Z_{csn} are the impedance of C_{s1}–C_{sn}.

E. Quantitative Analysis for the Mathematical Model of the UHV-SMPS' CM EMI

Since the *n* MOSFETs are equally sharing the same voltage in the UHV-SMPS, it could be assumed that V_1 to V_n shown in Fig. 8(a) have the same value which is called V_s, and their parasitic capacitance between drain and ground is C_s. Thus, it is more easily for the discussion in quantitative analysis to the mathematical model below.

TABLE I
PARAMETERS OF SWITCH SERIES COMPONENTS EQUIVALENT INTERFERENCE SOURCE

Number of MOSFETs in series *n*	Voltage of equivalent interference source *V*	Equivalent parasitic capacitance *C*
1	Vs	Cs
2	1.5 Vs	2 Cs
3	2 Vs	3 Cs
.....	.....	.....
10	5.5 Vs	10 Cs

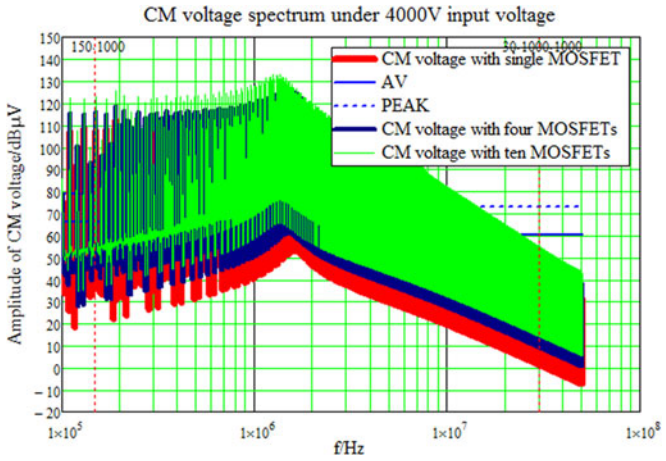

Fig. 12. Mathematical model of the switches' numbers and their CM interference spectrums.

By (19) and (20), MOSFETs serial number *n*, equivalent interference source voltage *V*, and the equivalent parasitic capacitance *C* between the drain and ground are shown in Table I.

From (19), (20), and Table I, it can be concluded that when MOSFETs are in series, the equivalent interference source voltage decreases compared with single MOSFET's interference source voltage (example: the equivalent interference source voltage is 2500 V when four MOSFETs in series to share 4000 V input voltage, which is smaller than the interference source voltage of 4000 V with single MOSFET to bear 4000 V input voltage); however, the parasitic capacitance of drain-to-ground increases, so both sides of the effect to the interference source voltage need to be comprehensively considered.

From the CM interference mathematical model in Fig. 8 and (19) and (20), using software Mathcad to the mathematical model, the serialization of MOSFETs, the number of MOSFETs in series, and the CM interference spectrum detected by LISN are shown in Fig. 12.

It can be seen that when the input voltage is 4000 V, the more MOSFETs connected in series, the more severe the CM interference. For example, in 190 kHz from Fig. 12, CM voltage of single switch is 112.36 dBμV, CM voltage of four switches in series is 118.55 dBμV, and ten is 125.42 dBμV.

F. Influence of mosfet dv/dt Slope

The analysis above is based on the assumption of ideal square waves of $V_{\rm ds}$. However, the slope of *dv/dt* is another key fact

in the CM EMI discussion decided by the $V_{\rm ds}$ voltage change according to the working of the converter. And the *dv/dt* could be reflected by the rising time T_r and falling time T_f of $V_{\rm ds}$. The T_r is defined as the period from the rising of $V_{\rm ds}$ to the beginning of oscillation M1, and the T_f is defined as the period after the end of oscillation M2 to zero. In the analysis below, what we concern is the influence of *dv/dt* on EMI in series-connected topology but not the difference between T_r and T_f. Thus, in order to simplify the further discussion, we assume that the slopes of rising time and falling time are the same for convenience of analysis. In this paper, due to the ultrahigh input voltage, the MOSFETs have to be connected in series. And all power switches connected in series should have the same *dv/dt* because of the $V_{\rm ds}$ voltage balance.

As for the comparison of single MOSFET *dv/dt* and multiple MOSFETs *dv/dt*, there are two representative types as shown in Fig. 13. One is the same *dv/dt* as shown in Fig. 13(a) with 1000 V 1 μs and 4000 V 4 μs. The other is the same T_r and T_f as shown in Fig. 13(b) with 1000 V 1 μs and 4000 V 1 μs. Then, by mathematically modeling the CM interference as Fig. 12 shown with the 4 kV input voltage including the *dv/dt* and stray capacitance C_s, the CM interference spectrums of two types *dv/dt* above are shown in Fig. 13(c). It can be seen that the slope of *dv/dt* influences more on the CM interference in the low- and medium-frequency domain (150 kHz–6 MHz). And the sequence of CM values from high to low is: four 1000 V 1 μs MOSFETs connected in series, single 4000 V 1 μs MOSFET, single 4000 V 4 μs MOSFET.

If the *dv/dt* of 4000 V MOSFET is increasing as shown in Fig. 13(d), the CM interference in the frequency domain 500 kHz–6 MHz would be greatly enlarged. The 4000 V 500 ns MOSFET has almost the same CM interference value with 1000 V 1 μs series-connected MOSFETs, which has eight times *dv/dt* difference. And CM interference value of 4000 V 100 ns MOSFET is 5–10 dBμV larger than 1000 V 1 μs series-connected MOSFETs, which has 40 times *dv/dt* difference.

Thus, during the design process, the *dv/dt* influence and serialization structure influence on EMI need to be overall considered.

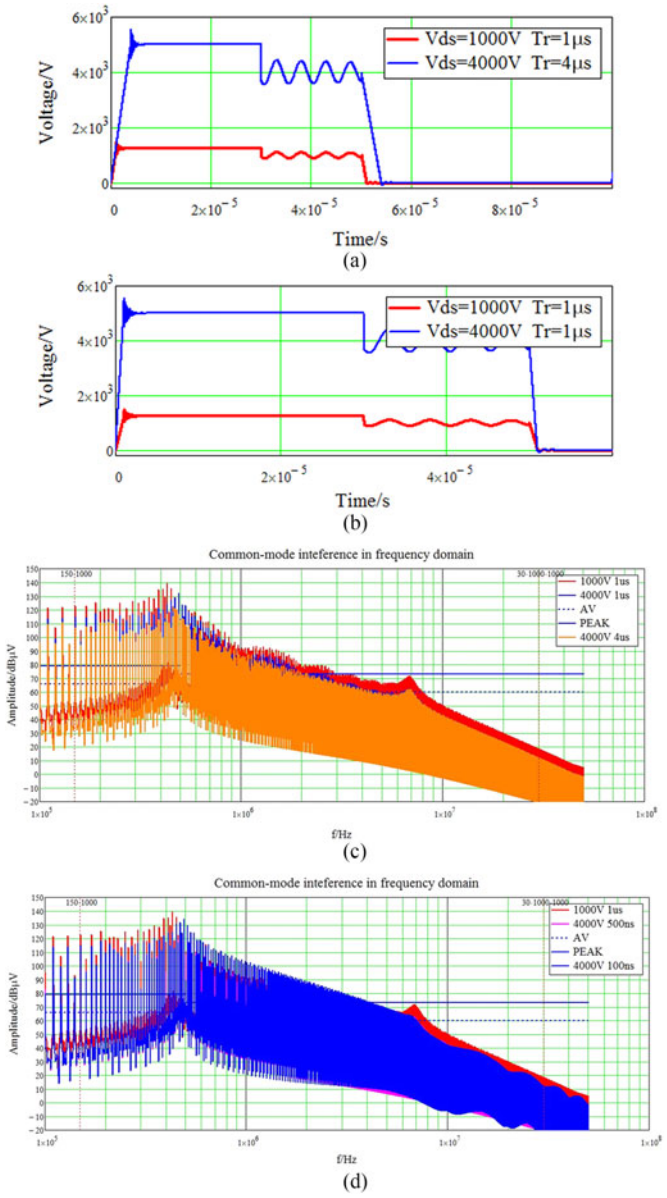

Fig. 13. Mathematical model of the EMI source. (a) $V_{\rm ds}$ waveform of MOSFET under same *dv/dt*. (b) $V_{\rm ds}$ waveform of MOSFET under the same T_r and T_f. (c) CM interference spectrums of $V_{\rm ds}$ waveforms. (d) CM interference spectrums of $V_{\rm ds}$ waveforms with increasing of *dv/dt*.

IV. Design Consideration

A. Analysis of Voltage Unbalance Causes and Solutions

For the series-connected MOSFETs, voltage balance is the most serious challenge. It includes static and dynamic balance. Static unbalance is mainly caused by different static characteristics of the MOSFET itself and can be solved by parallel resistance for each MOSFET. Usually, the static balance resistance $R_{\rm static}$ equals to $1/10R_{\rm OFF}$, where $R_{\rm OFF}$ is the leakage resistance of MOSFET. Dynamic unbalance is caused by the inconsistent operating time of each MOSFET in switching instants, including different dynamic characteristics and inconsistent delay time of driver. Because the switching process is very short, it is difficult to achieve the dynamic balance.

The causes for the voltage unbalance of series-connected MOSFETs can be generally divided into three parts. The most important cause is that the parasitic capacitances which influence the structure of the circuit, like the distributed capacitance (C_s) between the drain and the grounding heat sink of MOSFETs [15]. Then, the gate signals of the series-connected switches need to be strictly consistent. A large difference of $V_{\rm ds}$ will be caused when a tiny inconformity of the gate signals between the switches happened. Besides, the diversity and differentiation of the series-connected MOSFETs (like the difference of the parameter $R_{\rm ds(on)}$, $C_{\rm ds}$) will lead to the voltage unbalance.

Therefore, in the series-connected UHV-SMPS, it should be ensured that all switches have the same pattern and batch. So that the influence of switch itself can be reduced. Then, a new gate-driving solution needs to be proposed in order to solve the inconformity of the gate signals among the series-connected switches.

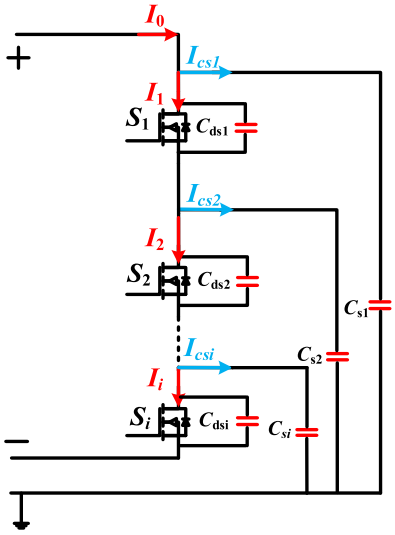

Fig. 14. Influence of parasitic capacitances on voltage unbalance.

However, the most important cause for voltage unbalance is the parasitic capacitances in power circuit. The parasitic capacitances will cause voltage unbalance even the drivers and MOSFETs are consistent.

During switching transients, the voltage $V_{\rm ds}$ of each MOSFET changes rapidly; thus, there are currents (I_{cs1} to I_{csi}) passing through the parasitic capacitances C_{s1}, C_{s2}, and C_{si} as shown in Fig. 14. Their magnitude can be expressed with

$$I_{csi} = C_{si} * \sum_{i=1}^{n} \frac{dV_{dsi}}{dt}. \tag{21}$$

Here, I_0, I_1, I_2, and I_i are, respectively, the currents going across the primary side of the transformer, MOSFET 1, MOSFET 2, and MOSFET i. It has

$$I_0 = I_1 + I_{cs1} \tag{22}$$

$$I_1 = I_2 + I_{cs2} \tag{23}$$

$$I_{i-1} = I_i + I_{csi}. \tag{24}$$

So

$$I_1 > I_2 > \cdots > I_i. \tag{25}$$

Additionally, a research [31] has shown an analytical formula which calculates the switching speed for MOSFET power device according to its current I_1

$$\frac{dV_{\rm ds}}{dt} = \frac{I_1 + g_m * (V_{\rm th} - U_t)}{C_{\rm GD} * (1 + R_G * g_m) + C_{\rm ds} + C_{\rm ds\_ext}}. \tag{26}$$

According to (26), the higher the current passing through the MOSFET, the higher the switching speed of the MOSFET

$$\frac{dV_{\rm ds1}}{dt} > \frac{dV_{\rm ds2}}{dt} > \cdots > \frac{dV_{\rm dsi}}{dt}. \tag{27}$$

Therefore, the voltage across MOSFET i at the end of the turn-off switching transition is higher than the one of MOSFET $i+1$ ($i = 1, 2, 3\ldots$), which will cause the breakdown of the MOSFET i.

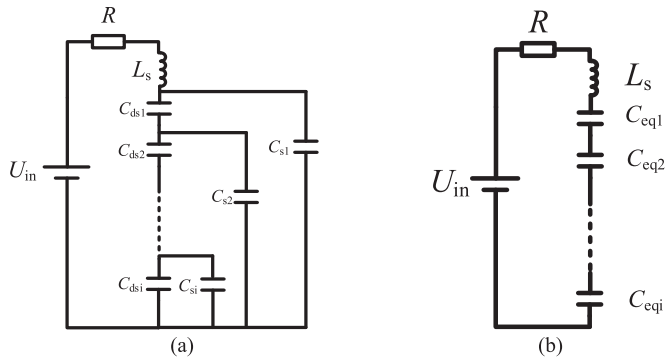

Fig. 15. Equivalent circuit when MOSFETs turn off. (a) Parasitic capacitances of *N* MOSFETs in series. (b) Equivalent circuit structure after simplification.

The parasitic capacitances of Fig. 14 can be simplified as equivalent circuit (see Fig. 15). *R* and L_S are the resistance and inductance of the power circuit, respectively. Because of the parasitic capacitances, equivalent capacitance between drain and source of each MOSFET is different. When the MOSFETs turn off, the equivalent capacitance is charged by input voltage, then each MOSFET will have different $dv_{\rm ds}/dt$ which lead to voltage unbalance. $C_{\rm eq1}$ to $C_{\rm eqi}$ ($i = 1, 2, 3\ldots$) are the equivalent capacitances between drain and source.

For example, five MOSFETs are connected in series and the value of $C_{\rm ds1} - C_{\rm ds5}$ equal to 100 pF, while the $C_{s1} - C_{s5}$ equal to 50 pF on the basis of following analysis.

$C_{\rm ds}$ is a parasitic capacitor between drain and source of MOSFET, which can be calculated as (28) according to datasheet

$$C_{\rm ds} = C_{\rm oss} - C_{\rm rss}. \tag{28}$$

Considering the size, cost, and reliability of the circuit, the high voltage level MOSFET is needed in order to decrease the number of MOSFETs connected in series. Some MOSFET models with high $V_{\rm ds}$ level and their $C_{\rm ds}$ are listed in Table II according to their datasheets. It can be seen that $C_{\rm ds}$ ranges from 10.7 to 245 pF. For purpose of intuitively and generally describing the modeling to voltage unbalance with series-connected MOSFETs, 100 pF is chosen for calculation convenience.

The parasitic capacitance C_s is important in the voltage balance analysis and the CM interference modeling. However, its value cannot be measured by experiment; thus, it needs to be obtained both by calculation and simulation.

On one hand, from datasheet of C2M1000170D, the drain area of MOSFET can be approximately calculated as follows:

$$S = D1 * E1 - \pi\left(\frac{\phi}{2}\right)^2 = 209.26\ \text{mm}^2. \tag{29}$$

The drain of MOSFET is connected to the heat sink and the heat sink is connected to the chassis of converter (ground). Between the drain of MOSFET and heat sink is the insulation spacer which could insulate the high voltage of MOSFET to ground. Al_2O_3 ceramic insulation spacer is selected because of its high heat conductivity, high dielectric strength. Al_2O_3 ceramic insulation spacer's relative dielectric constant is 9.77, thickness is 0.36 mm, and breakdown field strength is 65 kV/mm. Thus, C_s can be

TABLE II
$C_{\rm ds}$ OF HIGH-VOLTAGE MOSFET

Model	STP4N150	STF12N120K5	STW9N150	WPH40031E	C2M1000170D	SCT20N120
$V_{\rm ds}$ (V)	1500	1200	1500	1700	1700	1200
$C_{\rm oss}$ (pF)	120	110	280	90	12	65
$C_{\rm rss}$ (pF)	12	0.6	35	27	1.3	14
$C_{\rm ds}$ (pF)	108	109.4	245	63	10.7	51

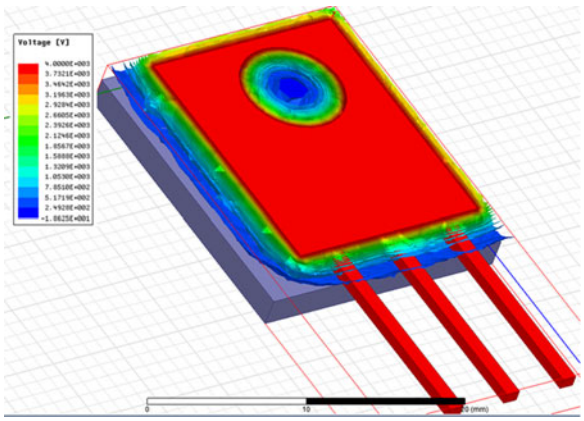

Fig. 16. Voltage filed of C2M1000170D simplified model in ANSYS Maxwell 3-D.

calculated as follows:

$$C_s = \frac{\varepsilon_0 \varepsilon_r S}{d} = \frac{9.77 * 8.85 * 10^{-12} * 209.26 * 10^{-6}}{0.36 * 10^{-3}} = 50.26 \text{ pF}. \quad (30)$$

On the other hand, based on the parameters above, the model of MOSFET is built in ANSYS Maxwell 3-D simulation software to verify the result. The voltage filed of Cree C2M1000170D simplified model is shown in Fig. 16. The MOSFET (red) is modeled according to the datasheet of C2M1000170D and its material is set as copper. The gray one is the heat sink which is set to aluminum. Between the MOSFET and heat sink is the Al_2O_3 ceramic insulation spacer, and its relative dielectric constant and thickness are 9.77 and 0.36 mm.

After electrostatic simulation, C_s is 52.831 pF which basically matches with the calculation result. The error is caused by the MOSFET boundary effect to the ground in ANSYS Maxwell 3-D simulation, which could be more accurate than calculation.

Therefore, with overall consideration of calculation and simulation results, C_s is chosen to be 50 pF for analysis convenience.

Then, $C_{\rm eq1}$ to $C_{\rm eq5}$ can be calculated as follows:

$$C_{\rm eq1} = \frac{1}{\frac{1}{C_{\rm eq5}} + \frac{1}{C_{\rm eq4}} + \frac{1}{C_{\rm eq3}} + \frac{1}{C_{\rm eq2}} + \frac{1}{C_{S1}}} + C_{\rm ds1} = 120.1 \text{ pF} \quad (31)$$

$$C_{\rm eq2} = \frac{1}{\frac{1}{C_{\rm eq5}} + \frac{1}{C_{\rm eq4}} + \frac{1}{C_{\rm eq3}} + \frac{1}{C_{S2}}} + C_{\rm ds2} = 124 \text{ pF} \quad (32)$$

$$C_{\rm eq3} = \frac{1}{\frac{1}{C_{\rm eq5}} + \frac{1}{C_{\rm eq4}} + \frac{1}{C_{S3}}} + C_{\rm ds3} = 129.5 \text{ pF} \quad (33)$$

$$C_{\rm eq4} = \frac{1}{\frac{1}{C_{\rm eq5}} + \frac{1}{C_{S4}}} + C_{\rm ds4} = 137.5 \text{ pF} \quad (34)$$

$$C_{\rm eq5} = C_{S5} + C_{\rm ds5} = 150 \text{ pF}. \quad (35)$$

According to (31)–(35), it can be seen that with the number of MOSFETs $i\,(i = 1, 2, 3\ldots)$ increasing, the equivalent capacitance corresponding with each MOSFET $C_{\rm eq}$ getting larger as (36) shows, which further reflects the result of (27)

$$C_{\rm eq1} < C_{\rm eq2} < \cdots < C_{\rm eq(i-1)} < C_{\rm eqi}. \quad (36)$$

By (36), the regulation to choose $C_{\rm com}$ can be designed as follows, assuming that $C_{\rm ds1} - C_{\rm dsi}$ equal to $C_{\rm ds1}$ and $C_{s1} - C_{si}$ equal to $C_s\,(i = 1, 2, 3\ldots)$, $C_{\rm com}$ of MOSFETs 1–*n* are defined as $\rm C_{com1} - C_{comn}$.

First, since $C_{\rm eq1} = C_{\rm eq2} = \ldots = C_{\rm eqi}$ is needed, the relationship of $C_{\rm com1}$ to $C_{\rm comi}$ can be expressed as follows:

$$C_{\rm com1} > C_{\rm com2} > \cdots > C_{\rm com(i-1)} > C_{\rm comi}. \quad (37)$$

Next, according to (31)–(35), the generalized formulas (38)–(41) are shown as follows:

$$C_{\rm eq1} = \frac{1}{\frac{1}{C_{\rm eqi}} + \frac{1}{C_{\rm eq(i-1)}} + \cdots + \frac{1}{C_{\rm eq2}} + \frac{1}{C_{S1}}} + C_{\rm ds1} \quad (38)$$

$$C_{\rm eq2} = \frac{1}{\frac{1}{C_{\rm eqi}} + \frac{1}{C_{\rm eq(i-1)}} + \cdots + \frac{1}{C_{\rm eq3}} + \frac{1}{C_{S2}}} + C_{\rm ds2} \quad (39)$$

$$C_{\rm eq(i-1)} = \frac{1}{\frac{1}{C_{\rm eqi}} + \frac{1}{C_{S(i-1)}}} + C_{\rm ds(i-1)} \quad (40)$$

$$C_{\rm eqi} = C_{\rm dsi} + C_{Si}. \quad (41)$$

Finally, $\rm C_{com1}$ to $\rm C_{comi}$ can be listed as (42)–(45), while $C_{\rm offset}$ is the benchmark compensation capacitance:

$$C_{\rm com1} = C_{\rm eqi} - C_{\rm eq1} + C_{\rm offset} = C_{\rm dsi} + C_{si} - \frac{1}{\frac{1}{C_{\rm eqi}} + \frac{1}{C_{\rm eq(i-1)}} + \cdots + \frac{1}{C_{\rm eq2}} + \frac{1}{C_{S1}}} - C_{\rm ds1} + C_{\rm offset} \quad (42)$$

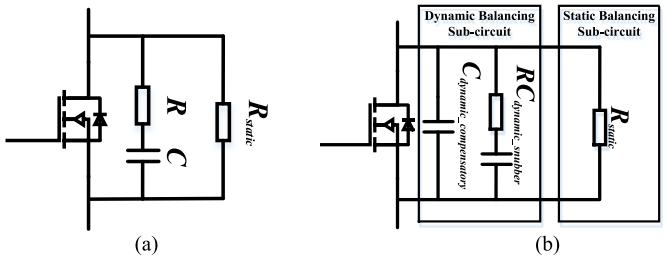

Fig. 17. Voltage balance circuit. (a) Traditional *RC* snubber. (b) Proposed *RC* snubber.

$$C_{\mathrm{com}2} = C_{\mathrm{eq}i} - C_{\mathrm{eq}2} + C_{\mathrm{offset}} = C_{\mathrm{ds}i} + C_{si} - \frac{1}{\frac{1}{C_{\mathrm{eq}i}} + \frac{1}{C_{\mathrm{eq}(i-1)}} + \cdots + \frac{1}{C_{\mathrm{eq}3}} + \frac{1}{C_{S2}}} - C_{\mathrm{ds}2} + C_{\mathrm{offset}} \tag{43}$$

$$\cdots\cdots$$

$$C_{\mathrm{com}(i-1)} = C_{\mathrm{eq}i} - C_{\mathrm{eq}(i-1)} + C_{\mathrm{offset}} = C_{\mathrm{ds}i} + C_{si} - \frac{1}{\frac{1}{C_{\mathrm{eq}i}} + \frac{1}{C_{S(i-1)}}} - C_{\mathrm{ds}(i-1)} + C_{\mathrm{offset}} \tag{44}$$

$$C_{\mathrm{com}i} = C_{\mathrm{offset}}. \tag{45}$$

Traditionally, the spike absorption of the MOSFET V_{ds} is achieved by the *RC* snubber which contains a resistor and a capacitance shown in Fig. 17(a) [32]. In the UHV-SMPS, due to the series-connected MOSFETs, the *RC* snubber not only achieves the spike absorption, but also accomplishes the mission of dynamic voltage balance of series-connected MOSFETs. Therefore, the two targets may not be realized very well synchronously.

In this paper, by adding compensatory capacitor to *RC* snubber circuit like Fig. 17(b) shows, the dynamic voltage balance could be realized first and then the *RC* snubber is used to suppress the spike of V_{ds} which can make a good realization of both dynamic balance and spike absorption. Fig. 17(b) shows the pattern of the passive snubber circuit which can be divided into two parts. C_{com}, $RC_{\mathrm{dynamic\_snubber}}$ are the dynamic balancing subcircuit and R_{static} is the static balancing subcircuit.

Then, the traditional *RC* snubber and the proposed *RC* snubber with compensatory are compared together through simulation based on the parameters from (31) to (35). If the five MOSFETs are connected in series and the input voltage is 4 kV, all parameters are listed in Table III.

1) Proposed RC Snubber With Compensatory Capacitance: From the equivalent capacitance in Table III, compensatory capacitances are added to all MOSFETs to make the equivalent capacitance all equal to 170 pF. The dynamic voltage waveforms before adding compensatory capacitances and after adding compensatory capacitances are shown in Fig. 18(a) and (b). It can be seen that the dynamic voltage balance could be achieved by adding compensatory capacitances; however, the spike of V_{ds} is still large. Then, the *RC* snubber with 10 kΩ and 100 pF is added to each MOSFET, and the V_{ds} waveforms are shown in Fig. 18(c) which shows a good consistency of five V_{ds} voltage

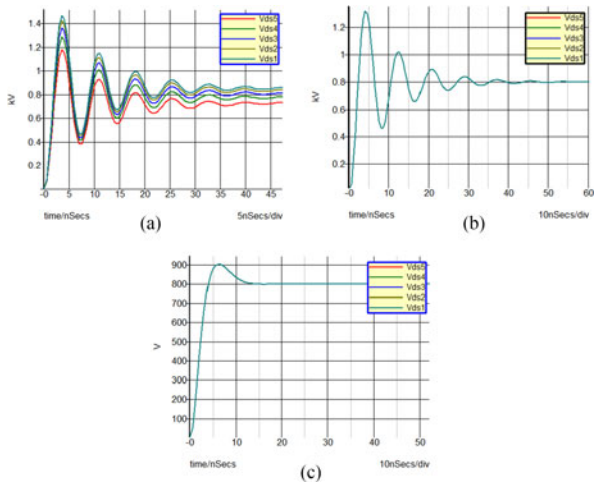

Fig. 18. Simulation of dynamic voltage balance with the proposed *RC* snubber. (a) Without any measures. (b) With compensatory capacitance. (c) Add extra *RC* snubber.

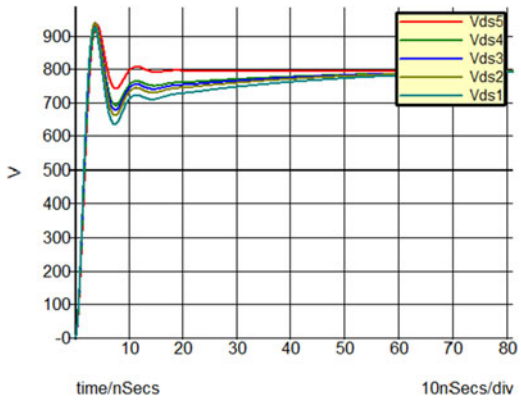

Fig. 19. Simulation of dynamic voltage balance with traditional *RC* snubber.

with peak value of 900 V and equalizing time of 13 ns. And the loss in the proposed *RC* snubber can be calculated as follows:

$$P_{RC\_\mathrm{com}} = \frac{1}{2}CU^2 * f * 5 = \frac{1}{2}(100 * 10^{-12}) * 900^2 * 10^4 * 5 = 2.025\ \mathrm{W}. \tag{46}$$

2) Traditional RC Snubber: By adding 551 pF 10 kΩ to MOS1, 545 pF 9 kΩ to MOS2, 500 pF 10 kΩ to MOS3, 492 pF 10 kΩ to MOS4, 481 pF 9 kΩ to MOS5, the waveforms of V_{ds} are shown in Fig. 19. It can be seen that the peak value of V_{ds} is 920 V, the equalizing time is nearly 70 ns, and the *RC* parameters are chosen by repeated attempts. And the loss in the traditional *RC* snubber can be calculated as (47), which is four times than the proposed *RC* snubber method

$$P_{RC} = \frac{1}{2}CU^2 * f * 5 = \frac{1}{2}(551 + 545 + 500 + 492 + 481) * 10^{-12} * 900^2 * 10^4 = 10.404\ \mathrm{W}. \tag{47}$$

TABLE III
PARAMETERS OF TRADITIONAL *RC* AND THE PROPOSED *RC* METHODS

Number	MOS 1	MOS 2	MOS 3	MOS 4	MOS 5
Equivalent capacitance	120.1 pF	124 pF	129.5 pF	137.5 pF	150 pF
Static resistor	500 kΩ	500 kΩ	500 kΩ	500 kΩ	500 kΩ
Traditional *R*	10 kΩ	9 kΩ	10 kΩ	11 kΩ	9 kΩ
Traditional *C*	551 pF	545 pF	500 pF	492 pF	481 pF
Proposed compensatory capacitance $C_{\rm com}$	49.9 pF	46 pF	40.5 pF	32.5 pF	20 pF
Proposed *R*	10 kΩ	10 kΩ	10 kΩ	10 kΩ	10 kΩ
Proposed *C*	100 pF	100 pF	100 pF	100 pF	100 pF

In conclusion, the proposed *RC* snubber with compensatory capacitance has more advantages than the traditional *RC* snubber which can be listed as follows:

1) more standardized parameters design method by separating the dynamic voltage balance process and the spike absorption process;
2) better consistency of $V_{\rm ds}$ waveforms;
3) faster voltage equalizing speed;
4) lower loss of *RC* snubber.

B. Driving Method

In order to guarantee the voltage balance, the driver must have a good consistency. For series-connected MOSFETs, the reference electric potential of driver is floating and the voltage between two adjacent switches is high. So between the power circuit and driver as well as each two driver require a high isolation voltage. Traditionally, some scholars use optocoupler in driver circuit to realize the high isolation voltage [18]. However, it costs too much and the driving signals may not in consistency, because each switch needs an optocoupler for its driver. Then, the usage of a pulse transformer can be easy to achieve higher level isolation voltage and has rapid response-speed, high reliability. Because the wide input voltage range is needed, the pulse transformer driving circuit has been selected, which has decoupling capacitors at both sides of the transformer in order to get a stable magnitude of the driving pulse. However, there are some new challenges to be solved, and the design consideration of the driving method has been focused on.

On one hand, the conventional driving circuit is that one MOSFET is driven by one pulse transformer. However, it would cost much and take up lots of space. Therefore, in this paper, an integrated pulse transformer is proposed and the topology is shown in Fig. 20. It has one primary winding and several secondary windings which have the same topology. It has a good consistency, simple structure, and high reliability owing to the special winding method. C_{q1}–C_{qn} are applied to raise the drive level under high duty cycle which are called "displacement capacitance." D_{11}, D_{12}–D_{n1}, D_{n2} are the Zener diodes for the purpose of SiC MOSFETs gate voltage being limited to –5 V to +18 V range.

On the other hand, the leakage inductor of each winding needs to be minimized, because it would affect the consistency of output signals. To do this, we use three measures. First, the toroidal core is applied to driving transformer. Because the window width of toroidal core is much wider than other core types, its leakage inductor is much smaller under the same number of turns. Second, we select VAC-W531 nanocrystal magnets core and set its turn number to only 11. This smaller number of turns leads to a reduced leakage inductance. Third, we wind the coils uniformly around the toroidal core. The relative position and interval between the primary winding and secondary winding are the two main causes of leakage inductance. Strikingly, these three methods have kept the leakage inductance of each winding to a minimum.

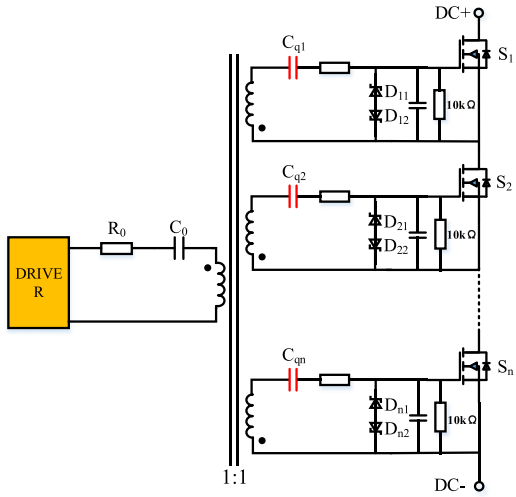

Fig. 20. Proposed integrated pulse transformer driver topology.

From Fig. 20, the drive circuit of MOSFET S_1 is chosen for analysis as follows:

$$U_{c0} = \frac{1}{T_s}\int_0^{T_s} U_{c0}dt = DU_{\rm DRV} \tag{48}$$

$$U_{c1} = \frac{1}{T_s}\int_0^{T_s} U_{c1}dt = DU_{\rm DRV} - U_D \tag{49}$$

$$V_{\rm gs} = U_{\rm DRV} - U_{C0} - U_{C1} = U_{\rm DRV} - U_D \tag{50}$$

$$U_D = \mathrm{U}_{D11} + \mathrm{U}_{D12}. \tag{51}$$

From (50), it can be seen that the driver output voltage $V_{\rm gs}$ is independent of the duty cycle *D*. Therefore, this proposed driver method is suitable to the duty cycle variation situation.

TABLE IV
AUXILIARY POWER SUPPLY DESIGN SPECIFICATIONS

Parameter	Specification
Input voltage	4000 V dc
Rated input voltage	2400 V dc
Output voltage/power	160/60 W
Line regulation	$<\pm 1\%$
Load regulation	$<\pm 1\%$
Stable voltage accuracy	$<\pm 1\%$
Ripple voltage	<0.5 V dc
Efficiency (rated voltage input)	$>80\%$
No-load loss	$<10 \pm 1$ W
Voltage withstand level	1) Input–output: AC5000V 2) Output–output: AC2500V

TABLE V
COMPONENTS AND PARAMETERS OF THE PROTOTYPE

Components	Parameters
Input voltage (V_{in})	300–4000 V dc
Output voltage (V_{out})	160 V dc
Maximum output power (P_o)	60 W
Switching frequency (f)	10 kHz
Turns ratio of transformer ($n_p : n_s$)	271:160
Primary winding inductance (L_p)	13 mH
Primary-side MOSFETs	C2M1000170D
Secondary-side diodes	DSA2-16A
Output capacitances (C_{o1}, C_{o2})	330 μF

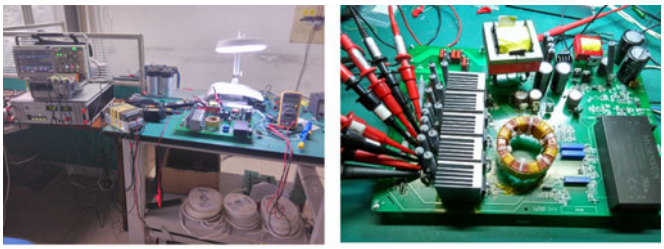

Fig. 21. Photograph of the prototype. (a) Experimental environment. (b) Prototype of the proposed UHV-SMPS.

V. EXPERIMENTAL ANALYSIS

A. Experimental Platform

In order to verify the accuracy of the above modeling and simulation, this paper sets up an UHV-SMPS based on series-connected SiC MOSFETs for MMC-HVDC auxiliary power supply, and the main design specifications are shown in Table IV, the circuit parameters are shown in Table V, and the prototype is shown in Fig. 21.

Some crucial components and parameters are designed according to the considerations below.

1) Switching Frequency: The maximum input voltage of UHV-SMPS is 4000 V. When 4000 V is used as input voltage, the duty cycle of MOSFET would be very low (almost 1%). According to the experimental test, if the switching frequency is high, the driver signals cannot generate correct voltage because of too small period during ON time. Therefore, 10 kHz is chosen as the switching frequency after many tests.

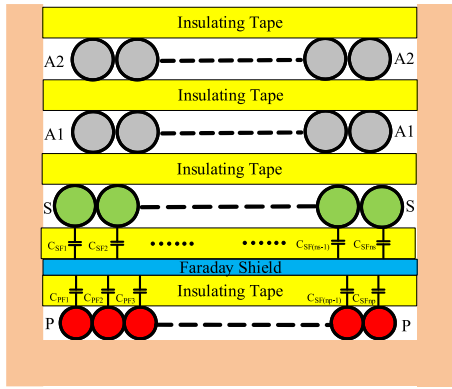

Fig. 22. Structure of main transformer.

2) MOSFET: As the rated operational voltage is 2400 V and maximum operational voltage is 4000 V, the loss is really considerable. SiC MOSFET has much lower loss than traditional Si MOSFET due to its small parasitic resistance like $R_{\text{ds(on)}}$. And because of the considerable loss, MOSFET would be really hot during operation. SiC MOSFET can work more stable in high-temperature environment than Si MOSFET. Therefore, SiC MOSFET is selected as main power switch. Then, considering the ultrahigh input voltage, SiC MOSFET C2M1000170D from Cree Corporation is chosen which could bear 1700 V voltage.

3) Main Transformer: The structure of main transformer is shown in Fig. 22 which contains one primary winding, one secondary winding, two auxiliary windings, and Faraday shield.

The main transformer is designed based on the AP method. The manganese zinc ferrite material TP4A with EE65 type is used as the magnets core and its working magnetization density is chosen to 200 mT. Primary winding inductor L_p and peak current can be calculated as follows:

$$L_p = \frac{(V_{\text{inmin}} D_{\max})^2}{2P_{\text{in}} f_s} = 13 \text{ mH} \tag{52}$$

$$I_{\text{dspeak}} = \frac{V_{\text{inmin}} D_{\max}}{L_p f_s} = 1.108 \text{ A}. \tag{53}$$

The number of turns of primary and secondary windings is calculated as follows:

$$N_p = \frac{L_p I_{\text{dspeak}}}{B_w A_e} = 135.6 \tag{54}$$

$$N_s = \frac{(V_o + V_D)(1 - D_{\max}) N_p}{V_{\text{inmin}} D_{\max}} = 80. \tag{55}$$

To avoid the skin effect of the conductor and reduce the difficulty of winding, the multistrand winding method is adopted. It can increase equivalent cross-sectional area of the winding, increase magnetic coupling, and reduce the leakage magnetic field. The triple insulated wire with conductor diameter 0.25 mm, external diameter 0.45 mm, and cross-sectional area 0.159 mm^2 is chosen. Two triple insulated coils are parallel winded. Thus, the turns of primary winding and secondary winding are doubled to $N_{\text{p}} = 271$ and $N_{\text{s}} = 160$.

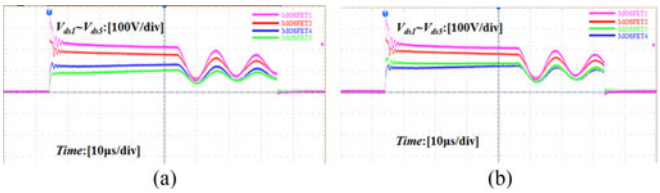

Fig. 23. $V_{\rm ds}$ waveforms under 500 V input voltage without any dynamic equalizing methods. (a) Waveforms of MOSFET 1, 2, 4, and 5. (b) Waveforms of MOSFET 1, 2, 3, and 4.

Five SiC MOSFETs in series are used in auxiliary power supply, which contains the *RCD* snubber circuit and MOSFET's passive snubber circuit between the drain and the source. The pulse transformer driver is used to drive five MOSFETs, which are controlled by a UC2844 chip.

To avoid the dangerous situation of short circuit due to the capacitance aging or breakdown of MOSFET, the following measures are adopted to protect the circuit. First, the high-voltage multilayered ceramics chip capacitances from AVX Corporation which has 2 kV voltage (only 900/2000 = 45% is used as maximum value) are used as the dynamic compensatory capacitance and *RC* snubber capacitance, which has low equivalent series resistance and high dc blocking voltage. Next, the high $V_{\rm ds}$ MOSFET C2M1000170D which could bear 1700 V voltage (only 900/1700 = 53% is used as maximum value) is used, which has abundant margin. Finally, the $V_{\rm ds}$ voltage protection circuit is adopted. If one MOSFET is brown down, the $V_{\rm ds}$ voltages of other MOSFETs would get larger. Then, the control chip UC3844 output would be clamped to zero, which means that the output of driving circuit is zero. Therefore, all MOSFETs in main circuit S_1 to S_5 would be turned off which are protected. The ERROR signal is delivered to the input of the UHV-SMPS and the converter would be powered off.

B. Experimental Results

Fig. 23 shows the voltage sharing of MOSFETs without any dynamic equalizing measures when the input is 500 V. By presenting the waveform 1234 at one time and the waveform 2345 at another time, the waveform 12 345 could be compared together. It can be seen that the experimental results agree with the theoretical analysis as (27) shows. $V_{{\rm ds}i}$ is larger than $V_{{\rm ds}(i+1)}$ $(i = 1, 2, 3, 4)$ because $C_{{\rm eq}i}$ is smaller than $C_{{\rm eq}(i+1)}$. Besides, the spikes of five MOSFETs are very large due to lacking of *RC* snubber circuit.

Then, the parallel compensatory capacitances $C_{\rm com1}$ to $C_{\rm com5}$ are added (65, 62, 57, 45, and 22 pF from the first to last) to MOSFETs according to (37)–(45). After dynamic compensation, all equivalent capacitances are approximated to 82 pF, and the compensatory capacitances values and their errors are shown in Table VI. It can be seen that all errors are smaller than 1%, which makes a good consistency of equivalent capacitances.

Because of the voltage spike, *RC* snubber circuit is added with the value of 5 kΩ and 47 pF. When the input voltage is 2400 and 4000 V, the maximum value of $V_{\rm ds}$ is 600 and 900 V

TABLE VI
COMPENSATORY CAPACITANCE VALUE AND ERROR

Number	C1/pF	C2/pF	C3/pF	C4/pF	C5/pF
Original value	16.5	19.8	25.8	37.3	60
Compensatory value	18 + 47	15 + 47	18 + 39	18 + 27	22
Final value	81.5	81.8	82.8	82.3	82
Error	0.61%	0.24%	0.98%	0.37%	0

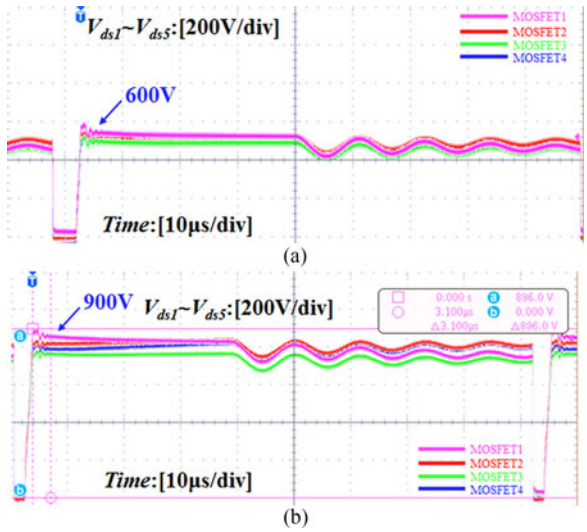

Fig. 24. $V_{\rm ds}$ waveforms with compensatory capacitance and *RC* snubber circuit. (a) Under 2400 V input voltage. (b) Under 4000 V input voltage.

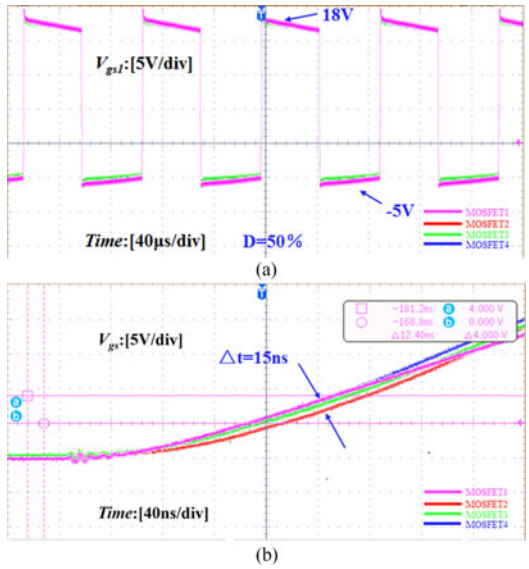

Fig. 25. $V_{\rm gs}$ waveforms of MOSFETs in series with the displacement capacitance. (a) Duty cycle = 50%. (b) Transient period.

(as shown in Fig. 24).The MOSFETs has a preferable purpose for voltage balancing.

Fig. 25 shows $V_{\rm gs}$ waveform of each MOSFET with the displacement capacitances $C_1 - C_5$ which value 1 μF. It can be seen from the waveforms in Fig. 25(a) that the driver output voltage $V_{\rm gs}$ is 16–18 V when the duty cycle equals to 50%. And

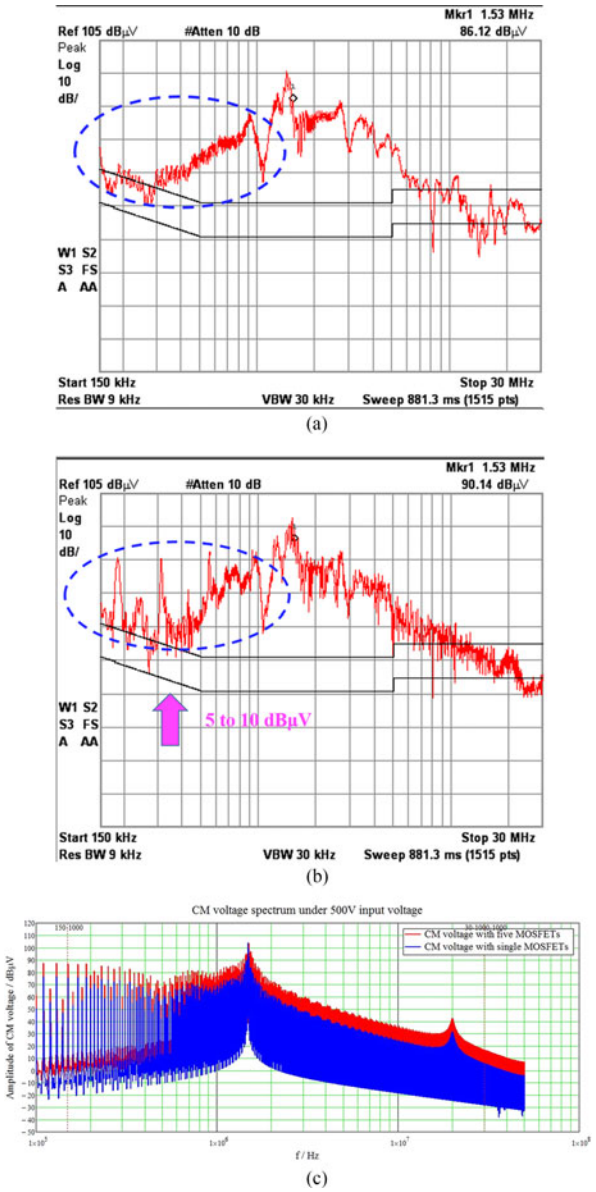

Fig. 26. CM voltage spectrum under 500 V input voltage. (a) Experimental spectrum with single MOSFET. (b) Experimental spectrum with five MOSFETs connected in series. (c) Theoretical spectrum with single MOSFET (blue) and five MOSFETs (red) connected in series.

from Fig. 25(b), the five MOSFETs have a good consistency with the delay only 15 ns.

The experimental results show that the method to guarantee the voltage sharing of MOSFETs connected in series as mentioned in Section IV is feasible, and the purposed UHV-SMPS can work stably and reliably.

C. CM Interference Experiment

The LISN is installed on the input side of the UHV-SMPS to detect CM voltage. Considering the maximum withstand voltage of LISN, the dc input voltage is limited to 500 V. Because the motivation of this paper is to study the EMI mechanism of switches with series-connected structure both in qualitative and quantitative analyses, EMI filter have not been designed yet. When using a single MOSFET, CM interference spectrum is shown in Fig. 26(a). When using the five MOSFETs in series, CM interference spectrum is shown in Fig. 26(b).

From Fig. 26(a) and (b), it can be see that in the frequency bands between 150 kHz and 1 MHz, the CMV of five MOSFETs is obviously higher than one MOSFET about 5–10 dBμV, which is consistent with the theoretical result shown in Fig. 26(c). Over 1 MHz, the CMV of five MOSFETs is only a little higher than one MOSFET, because of the high-frequency parasitic parameters impact, which is in accord with the quantitative analysis of mathematical modeling in Section III. The reduction of EMI would be considered in our next vision of UHV-SMPS. It is really hard to design an EMI filter for ultrahigh voltage (4 kV) application. And the experimental prototype is a product being developed for a company. The cost and size of the converter are really important. In the future, EMI of the converter may be suppressed by the printed circuit board layout or control method which does not need the EMI filter.

VI. Conclusion

In this paper, a 4000-V-ultrahigh-input-switched-mode power supply using series-connected MOSFETs is proposed and investigated. The challenges of the proposed scheme include the CM interference model of multiswitch and voltage balance of the switches. First, the CM interference of UHV-SMPS is evaluated by a high-frequency equivalent model of the proposed scheme. And a detailed multiswitch CM EMI mathematical model is derived and the interference quantity is calculated according to the coupling of series-connected switches. Second, a new design regulation for passive snubber circuit is proposed to realize input voltage balance. Through the regularity of the equivalent parasitic capacitances, the design of compensatory capacitance and voltage balance can easily be achieved. Third, a novel driving method based on the integrated pulse transformer is proposed. It can achieve both good consistency to the gate signals of MOSFETs and ultrahigh isolation voltage in the wide range input applications. Finally, the experimental results obtained from a 300–4000 V wide range input prototype verify the feasibility and validity of the proposed scheme and the theoretical analysis.

The proposed UHV-SMPS in this paper is the second vision. In this vision, the emphasis is put on the EMI analysis, realization of voltage balance and driving method. However, the converting efficiency of UHV-SMPS is not good and the loss of converter needs to be minimized. In the future, there are two objections for the next vision. One is the optimization of the loss and efficiency. The other is the design of the EMI suppressing method.

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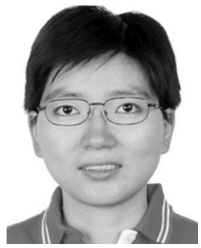

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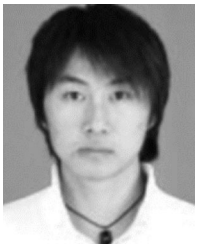

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