Optimized Switching Repetitive Control of CVCF PWM Inverters

Yongqiang Ye, *Senior Member, IEEE*, Guofeng Xu, Yuheng Wu, and Qiangsong Zhao

***Abstract*—In this paper, a novel optimized switching repetitive control (OSRC) scheme is developed and applied to a constant-voltage constant-frequency pulse width modulation inverter to enhance the stability and tracking performance with low sampling frequency. In OSRC, a switching integral phase lead compensator is applied to enlarge the stability margin, which is impaired by the phase lag of the inverter system. With the optimized switching strategy, the stable region can be much wider, which means that a larger robust filter Q can be applied to reduce the tracking error. The stability analysis and optimized design procedure are also given. Comparative experiments in different load situations are performed to demonstrate the validity of the proposed scheme.**

***Index Terms*—Constant-voltage constant-frequency (CVCF) pulse width modulation (PWM) inverter, optimization, repetitive control, switching phase lead compensation.**

I. Introduction

CONSTANT-VOLTAGE constant-frequency (CVCF) pulse width modulation (PWM) dc–ac converters or inverters are widely employed in ac power-conditioning systems, such as uninterruptible power supplies, grid-connected photovoltaic systems, and other industrial facilities. However, due to parameters uncertainties and nonlinear loads like rectifier loads, the output of inverters is often contaminated by harmonics. High-performance CVCF PWM converters should eliminate the harmonic distortion and output ac voltage with low total harmonic distortion (THD).

In order to improve the performance of CVCF PWM inverters, high-precision feedback control schemes, such as deadbeat or one-sampling-ahead-preview controller [1], [2], sliding-mode controller [3], and hysteresis controller [4], were proposed. However, all those feedback controllers cannot precisely track a periodic signal, or eliminate the harmonic distortions. Based on the internal model principle [5], repetitive control (RC) uses errors of pervious period(s) to exactly track periodic signals and eliminate harmonics. RC has been widely used in various aspects, such as optical storage [6], ball-screw-driven stages [7], and PWM converters [8]–[13]. And the periodic output of CVCF PWM inverters makes RC be an effective tool to reduce the THD and tracking error. However, the RC scheme requires large memory space to store the error date of previous period(s), and the computation burden of RC is also heavy, especially when the sampling frequency is high. Thus, high-performance microcontrollers (MCUs) and field programmable gate arrays are also required to satisfy the requirement of memory space and computation speed, which will increase the hardware cost. To reduce the hardware cost, low sampling rate RC [13] and multirate RC [14] were proposed, by reducing the sampling rate of the RC controller to decrease the memory space consumption and relieve the computation burden. Moreover, in high-power applications, the low switching frequency strategy is often used to reduce the switching losses. The sampling frequency is generally the same as or twice as high as the switching frequency [15], and therefore, the switching losses can also be decreased when a low sampling rate controller is applied.

However, when the sampling frequency is low, the conventional RC (CRC) scheme with integral linear phase lead compensation [11], which can compensate the phase lag of the plant, may easily cause overcompensation or undercompensation and result in degraded compensation performance [13]. And the tracking accuracy must compromise with stability, which will lead to higher THD and tracking error.

Thus, to increase the tracking performance with low hardware cost, this paper proposes a novel RC scheme called optimized switching RC (OSRC) for CVCF PWM inverters. In OSRC, the sampling frequency is low to reduce the memory space cost and relax the computation burden, and a switching integral phase lead compensator is applied to compensate the phase lag. The switching compensator, which is composed of two integral linear phase lead compensators, is running based on an optimized switching law to maximize the compensation performance. With the optimized switching strategy, the overcompensation or undercompensation phenomena in low sampling rate CRC can be overcame. Moreover, different from the fractional phase lead compensation RC (FPLC-RC) [13], in which the fractional phase lead compensator is approximated by a finite-impulse-response (FIR) filter, the approximation error in FPLC-RC does not exist in OSRC. Thus, OSRC can notably enlarge the stability margin, and thus, a larger robust

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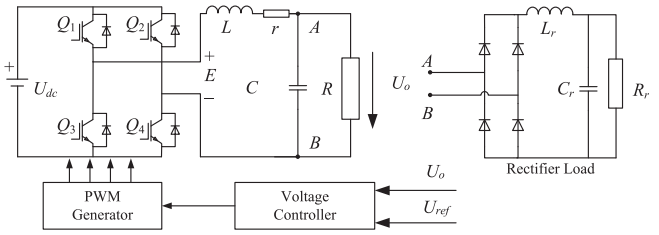

Fig. 1. CVCF PWM Inverter.

filter Q can be applied to achieve higher tracking accuracy and lower THD.

The remainder of this paper is organized as follows. Section II presents the model of a CVCF PWM inverter. Section III reviews the basics of linear phase lead compensation RC. The scheme of OSRC is given in Section IV with theoretical analysis and an optimized design procedure. The effectiveness of the proposed method is demonstrated through a series of comparative experiments in Section V. Finally, Section VI concludes this paper.

II. Modeling of CVCF PWM Inverter

Fig. 1 shows a single-phase CVCF PWM inverter, where $U_{\rm dc}$ is the bus voltage; Q_1–Q_4 are insulated gate bipolar transistors (IGBTs); L is the filter inductor; r is the equivalent series resistance (ESR) of the inductor L; C is the filter capacitor; R is the resistance load; L_r, C_r, and R_r are the rectifier loads; $U_{\rm ref}$ is the reference voltage; U_o is the output voltage; and E is the input PWM voltage, which is defined as follows:

$$E = \begin{cases} U_{\rm dc}, & \text{if } Q_1 \text{ and } Q_4 \text{ are on, } Q_2 \text{ and } Q_3 \text{ are off;} \\ -U_{\rm dc}, & \text{if } Q_1 \text{ and } Q_4 \text{ are off, } Q_2 \text{ and } Q_3 \text{ are on.} \end{cases}$$

The state-space model of the converter with resistance load R can be described as follows:

$$\begin{cases} \dot{x}(t) &= Ax(t) + Bu(t), \\ y(t) &= Cx(t) + Du(t) \end{cases} \tag{1}$$

where $x(t) = [U_o(t), \dot{U}_o(t)]^T$, $u(t) = E(t)$, $y(t) = U_o(t)$,

$$A = \begin{bmatrix} 0 & 1 \\ \dfrac{-(R+r)}{RLC} & \dfrac{-(L+CRr)}{RLC} \end{bmatrix}, B = \begin{bmatrix} 0 \\ \dfrac{1}{LC} \end{bmatrix},$$

$C = [1, 0]$, and $D = 0$.

The discrete form of (1) with a sampling period T_s can be written as

$$\begin{cases} x(k+1) &= Gx(k) + Hu(k), \\ y(k) &= Cx(k) + Du(k) \end{cases} \tag{2}$$

where $x(t) = [U_o(k), \dot{U}_o(t)]^T$, $u(k) = E(k)$, $y(k) = U_o(k)$, $G = e^{AT_s}$, and $H = \int_0^{T_s} e^{A\tau} B\, d\tau$.

The frequency responses of the inverter system in different load situations are shown in Fig. 2, where $L = 2.1$ mH, $C = 50\ \mu$F, and $r = 0.1\ \Omega$. The plot indicates that the inverter system has a resonance peak at the frequency $\omega = 1/\sqrt{LC}$. And under the no load condition ($R = \infty\ \Omega$), the system has the worst stability performance, which means the design of the voltage controller must be done under the no load condition to ensure the stability of the system with different loads.

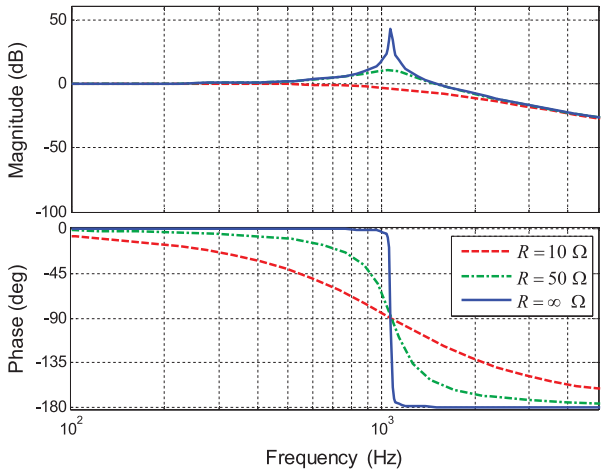

Fig. 2. Frequency responses of the inverter in different load situations.

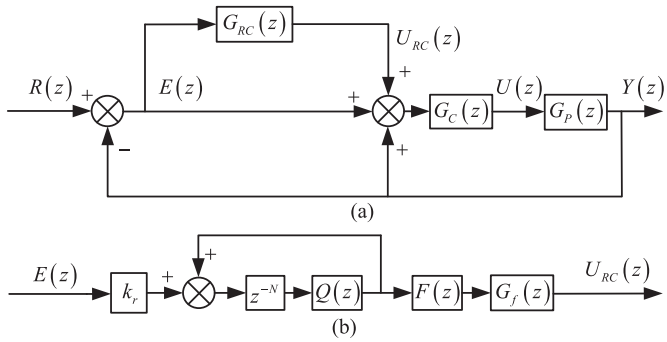

Fig. 3. General framework of an RC-controlled system. (a) An RC-controlled system. (b) Framework of $G_{\rm RC}(z)$.

III. Review of Linear Phase Lead Compensation RC

The general framework of an RC-controlled system is shown in Fig. 3(a), where $G_C(z)$ is the controller; $G_{\rm RC}(z)$ is the RC controller; $G_P(z)$ is the plant; $U_{\rm RC}(z)$ is the output of the RC controller; $U(z)$ is the output of the controller $G_C(z)$; and $E(z) = R(z) - Y(z)$ is the tracking error between the reference signal $R(z)$ and plant output $Y(z)$. Different from the ordinary plug-in type RC [11], in which the input of the controller $G_C(z)$ is $U_{\rm RC}(z) + E(z)$, the input of $G_C(z)$ in Fig. 3(a) is $U_{\rm RC}(z) + E(z) + Y(z) = U_{\rm RC}(z) + R(z)$. Due to the introduction of $Y(z)$, Fig. 3(a) can represent more control schemes, such as the direct RC control [16], which can be easily attained by letting $G_C(z) = 1$.

The transfer function of the RC controller $G_{\rm RC}(z)$ in Fig. 3(b) is given as

$$G_{\rm RC}(z) = k_r \frac{Q(z)F(z)G_f(z)z^{-N}}{1 - Q(z)z^{-N}} \tag{3}$$

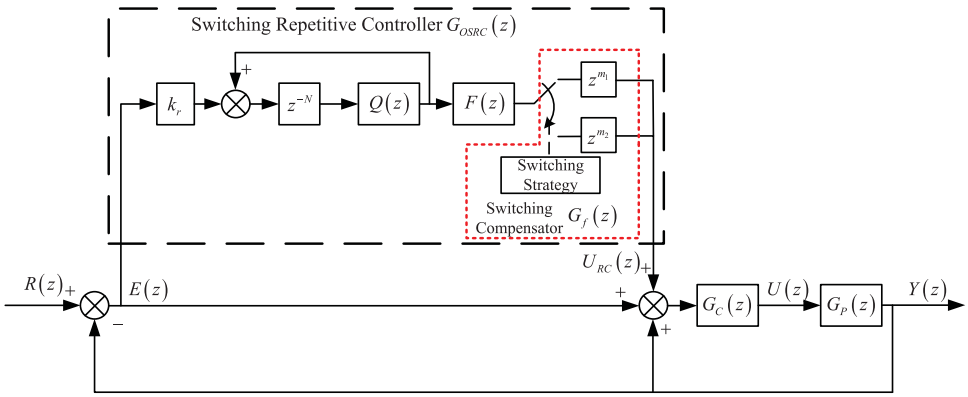

Fig. 4. Framework of an SRC-controlled system.

where k_r is the gain of the RC controller; $Q(z)$ is the robust filter [6], which is a constant less than 1 or a low-pass filter; $F(z)$ is a filter to attenuate the resonance peak of the plant and limit the bandwidth of the RC controller; $G_f(z)$ is a compensator that can improve the stability and dynamic performance of the system; and $N = T_{\text{ref}}/T_s$, where T_{ref} is the period of the reference signal and T_s is the sampling period of the controller.

The sensitivity function of the closed-loop system is given as

$$\begin{aligned} S(z) &= \frac{E(z)}{R(z)} \\ &= [1 - G_C(z)G_P(z)]\frac{1}{1 + G_{\text{RC}}(z)G_C(z)G_P(z)} \\ &= S_0(z)\frac{1}{1 + G_{\text{RC}}(z)G_C(z)G_P(z)} \end{aligned} \tag{4}$$

where $S_0(z) = 1 - G_C(z)G_P(z)$.

Based on the small gain theorem [17], (3) and (4), the sufficient conditions for the system stability are that $S_0(z)$ is stable and

$$\|Q(z)[1 - k_r G_f(z)P(z)]\|_\infty < 1 \tag{5}$$

where $P(z) = F(z)G_C(z)G_P(z)$ [11].

Based on the stability criteria (5), the smaller the value of $\|1 - k_r G_f(z)P(z)\|_\infty$ is, the wider the stable region is. Moreover, a wider stable region allows a larger $Q(z)$ to be applied to achieve higher tracking accuracy. In order to improve the stability and dynamic performance, the compensator $G_f(z)$ is often designed as the inverse of the plant, i.e., $G_f(z) = P(z)^{-1}$ [18]. However, due to the load variations and parameter uncertainties, the inverse is often unrealizable. In [11], Zhang proposed a simple linear phase lead compensation scheme to enhance the stability of the system. The compensator $G_f(z)$ is designed as an integral linear phase lead compensator z^m, which can provide a lead phase $\theta = m(\omega/\omega_N)180°$, where ω_N is the Nyquist frequency. By using an appropriate integral lead step m, the compensator $G_f(z) = z^m$ can effectively compensate the phase lag of the plant and improve the stability of the whole system.

However, the compensator $G_f(z) = z^m$ may easily result in overcompensation or undercompensation when the sampling frequency is low, which will further worsen the stability performance. In [13], Zhao and Ye proposed a fractional linear phase lead compensation scheme, i.e., $G_f(z) = z^{m+\gamma}$, where m is an integer and γ is a fraction. With the fractional linear phase lead compensation, the phase lag can be canceled more precisely under low sampling frequency. However, a fractional compensator is unrealizable in practice. In [13], the fractional compensator is approximated by an FIR filter based on Lagrange interpolation. A high-order FIR filter is needed to obtain an accurate approximation of the fractional compensator at the cost of computation complexity, otherwise the approximate error will worsen the stability.

IV. Optimized Switching Repetitive Control

The main aim of linear phase lead compensation in Section III is to enhance the stability of the system. As mentioned previously, the conventional integral phase lead compensation with low sampling frequency will deteriorate the stability of the system, and the FPLC must make a tradeoff between the computation complexity and stability. In this section, an OSRC scheme is proposed to achieve a wider stable region and higher tracking accuracy with low sampling frequency.

A. Scheme of Switching RC (SRC)

Although a simple integral linear phase lead compensation may easily cause overcompensation or undercompensation under low sampling frequency, a better compensation performance can be achieved by using a switching integral phase lead compensator, that is, the switching compensator switches between an overcompensation compensator and an undercompensation compensator. With an optimized switching strategy, SRC can notably improve the stability and tracking accuracy.

Fig. 4 shows the framework of an SRC-controlled system, which is similar to that in the CRC-controlled system, as shown in Fig. 3. However, the compensator $G_f(z)$ is a switching compensator, which can be written as follows:

$$G_f(z) = z^{f(j)} = \begin{cases} z^{m_1}, & (k-1)(\alpha+\beta) < j \le k\alpha; \\ z^{m_2}, & k\alpha < j \le k(\alpha+\beta) \end{cases} \tag{6}$$

where j is the index of the current reference signal cycle; $k = 1, 2, 3 \ldots$ is an integer; and α and β are the repeated use times for lead steps m_1 and m_2 every $\alpha + \beta$ cycles, respectively. And the switching action is executed based on the optimized switching strategy at the beginning of a certain cycle. The transfer function of the SRC controller $G_{\text{OSRC}}(z)$ is given as

$$G_{\text{OSRC}}(z) = k_r \frac{z^{f(j)} Q(z) F(z) z^{-N}}{1 - Q(z) z^{-N}}. \tag{7}$$

Remark 1: Similar to the linear phase lead compensator $G_f(z) = z^m$, the switch compensator (6) is a noncausal compensator, which cannot be directly implemented in the conventional discrete control systems. However, due to the special structure of RC, which has a pure delay line in the controller, the noncausal compensator (6) can be absorbed by the term z^{-N} in $G_{\text{OSRC}}(z)$. Thus, the noncausal compensator can be implemented in practice.

B. Stability Analysis

Theorem 1: Consider an SRC-controlled system depicted in Fig. 4. The closed-loop control system is stable if the following conditions are satisfied.

1) $S_0(z)$ is stable.
2)

$$\left\| Q^{\alpha+\beta}(z) \prod_{j=1}^{\alpha+\beta} G[f(j)] \right\|_\infty < 1 \tag{8}$$

where $G[f(i)] = 1 - k_r z^{f(j)} P(z)$.

Proof: In the SRC-controlled system, as Fig. 4 shows, the sensitivity function is derived as follows:

$$\begin{aligned} S_{\text{OSRC}}(z) &= \frac{E(z)}{R(z)} \\ &= [1 - G_C(z) G_P(z)] \frac{1}{1 + G_{\text{OSRC}}(z) G_C(z) G_P(z)} \\ &= S_0(z) \frac{1 - Q(z) z^{-N}}{1 - Q(z) z^{-N} [1 - k_r z^{f(j)} F(z) G_C(z) G_P(z)]} \\ &= \frac{M(z)}{1 - Q(z) z^{-N} G[f(j)]} \end{aligned} \tag{9}$$

where $M(z) = S_0(z)[1 - Q(z) z^{-N}]$.

Equation (9) contains a time-variant function $f(j)$, which increases the difficulty in analysis. In fact, $f(j)$ is a periodic function with a period of $(\alpha + \beta) T_{\text{ref}}$. Moreover, according to Longman [19], the period T_{ref} of the reference signal can be treated as long compared to the transient of the CVCF PWM inverters. Thus, (9) can be rewritten in the form of the frequency transfer function from one period to the next as follows:

$$\begin{aligned} E(z) &= z^{-N} Q(z) G[f(j)] E(z) + M(z) R(z) \\ &= z^{-N} Q(z) G[f(j)] \{ z^{-N} Q(z) G[f(j-1)] E(z) \\ &\quad + M(z) R(z) \} + M(z) R(z) \\ &\cdots \\ &= z^{-(\alpha+\beta)N} Q^{\alpha+\beta}(z) \prod_{i=1}^{\alpha+\beta} G[f(i)] E(z) \\ &\quad + M \left\{ 1 + \sum_{i=1}^{\alpha+\beta-1} \left\{ z^{-iN} Q^i(z) \prod_{j=1}^{i} G[f(j)] \right\} \right\} R(z). \end{aligned} \tag{10}$$

Based on (10), the sensitivity function $S_{\text{OSRC}}(z)$ can be rewritten as follows:

$$\begin{aligned} S_{\text{OSRC}}(z) &= \frac{M(z)}{1 - Q(z) z^{-N} G[f(j)]} \\ &= \frac{M \left\{ 1 + \sum_{i=1}^{\alpha+\beta-1} \left\{ z^{-iN} Q^i(z) \prod_{j=1}^{i} G[f(j)] \right\} \right\}}{1 - z^{-(\alpha+\beta)N} Q^{\alpha+\beta}(z) \prod_{i=1}^{\alpha+\beta} G[f(i)] E(z)}. \end{aligned} \tag{11}$$

Equation (9) shows that all the poles of $S_0(z)$ are the ones of the sensitivity function $S_{\text{OCRC}}(z)$, which means that $S_0(z)$ must be stable to stabilize the whole system. Moreover, based on the sensitivity function (11) and the small gain theorem [17], a sufficient condition for system stability is $\| Q^{\alpha+\beta}(z) \prod_{j=1}^{\alpha+\beta} G[f(j)] \|_\infty < 1$. ■

Remark 2: By comparing the stability criteria (8) with that of the conventional linear phase lead compensation RC (5), it can be seen that the condition $\| Q(z)[1 - k_r G_f(z) P(z)] \|_\infty < 1$ is a multiplicative term of (8), which means the violation of the inequality may be acceptable in SRC. That is, the integral lead compensator $G_f(z) = z^{m_1}$ or $G_f(z) = z^{m_2}$ in low sampling rate CRC may cause overcompensation or undercompensation, but the switching compensator (6) can have better compensation performance with appropriate switching strategy. In reality, the integral linear phase lead compensation RC is a special case of SRC, i.e., $m_1 = m_2$. Moreover, compared with FPLC-RC, SRC eliminates the byproduct of an approximate FIR filter, and the stability performance can be improved with lower computation complexity.

Remark 3: According to the sensitivity function (9), SRC can achieve zero steady-state error tracking with the assumption that $Q(z) = 1$, i.e., $\lim_{\omega \to \omega_r} \| E(z) \| = 0$, where ω_r satisfies $\omega_r = 2k\pi / T_{\text{ref}}$ ($k = 0, 1, 2, \ldots, N/2$ for an even N and $k = 0, 1, 2, \ldots, (N-1)/2$ for an odd N). However, $Q(z) = 1$ is unacceptable in practice, which will make the whole system unstable [18]. Thus, $Q(z)$ must be a low-pass filter or a constant less than 1, which can enhance the robustness and stability at the cost of tracking accuracy. Based on the stability criteria

(8), the smaller the value of $\|\prod_{j=1}^{\alpha+\beta} G[f(j)]\|_{\infty}^{\frac{1}{\alpha+\beta}}$ is, the larger the robust filter $Q(z)$ can be selected, which will improve the tracking accuracy.

Remark 4: The OSRC scheme can provide larger stability margin and improve the tracking performance. However, with increasing sampling frequency, the overcompensation or undercompensation phenomena in CRC can be relieved, at the cost of memory space consumption and computation burden, and the tracking performance also can be enhanced. Thus, the performance improvement of OSRC over CRC may be less notable with increased sampling frequency. Moreover, although the low sampling frequency RC can notably reduce hardware cost, the byproducts of low sampling rate are the low signal-to-noise ratio and limited bandwidth of controller. Compared with the low sampling frequency CRC, OSRC can effectively improve the tracking accuracy with the same sampling rate. However, due to the limited bandwidth, the tracking performance of OSRC with low sampling frequency cannot match that with higher sampling rate.

C. Optimized Design of SRC

As mentioned before, the smaller the value of $\left\|\prod_{j=1}^{\alpha+\beta} G[f(j)]\right\|_{\infty}^{\frac{1}{\alpha+\beta}}$ is, the better the stability and tracking accuracy can be achieved. Therefore, the aim of SRC design is to minimize the value of $\left\|\prod_{j=1}^{\alpha+\beta} G[f(j)]\right\|_{\infty}^{\frac{1}{\alpha+\beta}}$. Several items need to be designed: the filter $F(z)$, the switching compensator $G_f(z)$ (including m_1, m_2, α, and β), the RC gain k_r, and the robust filter $Q(z)$. To simplify the procedure of design, suppose $Q(z)$ is a constant and the controller $G_C(z) = 1$ as a direct RC-controlled system [16]. And the inverter parameters in the following design case are the sampling period $T_s = 2.5 \times 10^{-4}$ s, $L = 2.1$ mH, $C = 50$ μ F, $R = \infty$ Ω, and $r = 0.1$ Ω. The sampling frequency is noticeably low.

1) Design of Filter $F(z)$: As Fig. 2 shows, the high resonance peak in the CVCF PWM inverter will deteriorate the stability of the system. To enhance the stability performance, a notch filter can be designed to cancel out the resonant peak [13]. Moreover, the high gain of RC in high-frequency region may make the system unstable, thus, $F(z)$ must contain a low-pass filter. Therefore, the filter $F(z)$ can be designed as follows:

$$\begin{aligned} F(z) &= F_0(z)F_1(z) \\ &= \frac{z^r + 2 + z^{-r}}{4} F_1(z) \end{aligned} \tag{12}$$

where $F_0(z)$ is a zero-phase notch filter; r is the order of the notch filter and satisfies $r \approx \pi/\omega_r/T_s$, with ω_r being the notch frequency; and $F_1(z)$ is a low-pass filter that can be selected as a conventional Butterworth filter.

A design case of $F(z)$ is as follows:

$$F(z) = \frac{z^4 + 2 + z^{-4}}{4} \frac{0.2431z + 0.1294}{z^2 - 0.7793z + 0.1518} \tag{13}$$

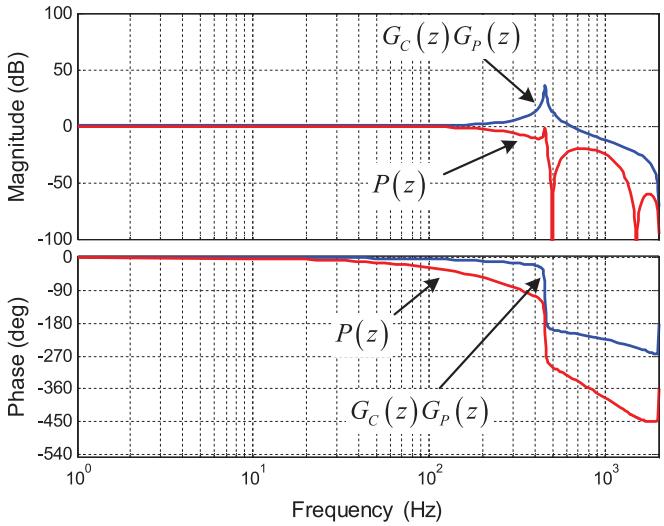

Fig. 5. Frequency response of $P(z)$ and $G_c(z)G_p(z)$.

where the notch frequency is $\omega_r = 3141$ rad/s, and the nature frequency and damping ratio of the low-pass filter are 3770 rad/s and 1.0, respectively.

The frequency response of $P(z)$ with filter (13) is shown in Fig. 5. Due to the approximate error of the notch filter order r, the notch filter $F_0(z)$ cannot precisely cancel out the resonant peak. A more complicated notch filter can be designed to improve the notch performance at the cost of computation complexity. However, due to the parameter variations and unmodeled dynamics, it is hard to achieve precise cancellation in practice. Therefore, the simple zero-phase notch filter $F_0(z) = (z^r + 2 + z^{-r})/4$ is adopted to attenuate the resonance in some degree. Fig. 5 also shows that the low-pass filter $F_1(z)$ aggravates the phase-lag problem, which must be compensated by the compensator $G_f(z)$.

2) Optimized Design of Switching Compensator $G_f(z)$: The design of switching compensator $G_f(z)$ includes the selection of lead steps m_1 and m_2, and the design of switching parameters α and β. And the optimization problem can be written as follows:

$$\min_{m_1, m_2, \alpha, \beta} \left\| \prod_{j=1}^{\alpha+\beta} G[f(j)] \right\|_{\infty}^{\frac{1}{\alpha+\beta}} \tag{14}$$

subject to

$$\begin{aligned} &0 \le \underline{m} \le m_1, m_2 \le \overline{m}; \\ &0 \le \underline{M} \le \alpha, \beta \le \overline{M} \end{aligned} \tag{15}$$

where $\overline{m}$ and $\underline{m}$ are the upper and lower bounds of lead steps m_1 and m_2, respectively, and $\overline{M}$ and $\underline{M}$ are the upper and lower bounds of switching parameters α and β, respectively,. Here, all the bounds are used to shape the feasible region. With those bounds, the optimization problem can be easily solved by the method of exhaustion offline, i.e., traverse all possible combinations of m_1, m_2, α, and β, and find the best combination that can minimize $\left\|\prod_{j=1}^{\alpha+\beta} G[f(j)]\right\|_{\infty}^{\frac{1}{\alpha+\beta}}$.

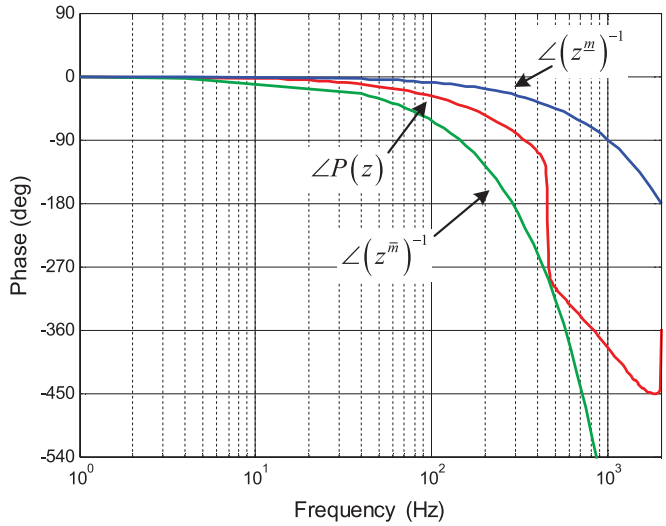

Fig. 6. Upper and lower bounds of lead step m.

The design aim of phase lead compensation is to compensate the phase lag of the plant $P(z)$. The overcompensation or undercompensation phenomenon will deteriorate the stability of the system. To nicely compensate the phase lag, the lead step m should satisfy $\angle z^m \approx \angle P^{-1}(z)$. Thus, the bounds $\overline{m}$ and $\underline{m}$ can be selected based on the following principles:

$$\begin{cases} \overline{m} &= \left\lceil \max \left| \frac{180 \angle P(j\omega)\omega_N}{\omega} \right| \right\rceil, \quad \forall \omega \in R; \\ \underline{m} &= \left\lfloor \min \left| \frac{180 \angle P(j\omega)\omega_N}{\omega} \right| \right\rfloor, \quad \forall \omega \in R. \end{cases} \tag{16}$$

A design case of $\overline{m}$ and $\underline{m}$ is shown in Fig. 6, which indicates that the phase lead compensation satisfies $\angle z^{\underline{m}} \le \angle P^{-1}(z) \le \angle z^{\overline{m}}$. Moreover, the bounds $\overline{M}$ and $\underline{M}$ also determine the size of the feasible region, and a larger value of $\overline{M} - \underline{M}$ can enlarge the feasible region, which means that better switching strategy may be attained at the cost of computation time. In fact, $\overline{M}$ is normally within 10 in practice.

Fig. 7 is the frequency responses of $|\prod_{j=1}^{\alpha+\beta} G[f(j)]|^{\frac{1}{\alpha+\beta}}$, $|1 - z^{m_1} P(z)|$, and $|1 - z^{m_2} P(z)|$, provided that $k_r = 1$, which indicates that OSRC can notably improve the stability of an inverter system. Notice that the curves of $|1 - z^{m_1} P(z)|$ and $|1 - z^{m_2} P(z)|$ show the compensation performance in CRC with lead steps m_1 and m_2, respectively. Although lead steps m_1 and m_2 cause overcompensation and undercompensation respectively, leading to the violation of (5) before and after 550 Hz if $Q = 1$, OSRC can enlarge the stable region by using the optimized switching compensation.

3) Design of k_r: It has been revealed in [16] that a larger RC gain k_r can improve the steady-state and dynamic performance. However, the magnitude of $Q(z)$ is much more important in determining the tracking accuracy. Moreover, a large k_r, which may result in overshoot and oscillation, will deteriorate the stability of the system, and a small $Q(z)$ must be adopted to ensure the stability, which will decrease the tracking performance. Table I presents the compensation performance of OSRC with different k_r. It can be seen that the optimized switching parameters are varying with different k_r, as well as the compensation performance.

4) Design of Q: The design of Q must satisfy the stability criteria (8), which can be rewritten as follows:

$$Q \le \frac{1}{\left\| \prod_{j=1}^{\alpha+\beta} G[f(j)] \right\|_\infty^{\frac{1}{\alpha+\beta}}}. \tag{17}$$

As mentioned before, a large value of $\|1 - P(z)G_f(z)\|_\infty$ in CRC requires a small Q to keep the stability of the system at the cost of tracking accuracy. Based on (17), with a wider stable region, the robust filter Q in OSRC can be much larger than that in CRC, which will notably decrease the tracking error.

V. Experiment Results

A. Experiment Setup

To validate the effectiveness of the proposed scheme, comparative experiments among the CRC controller, FPLC-RC controller, and OSRC controller are conducted under different loads. The experimental system consists of an inverter, a Data Acquisition board (Quanser QPIDe), and a PC with QuaRC and MATLAB/Simulink. And the inverter further comprises an IGBT inverter bridge, an *LC* filter, and a voltage sensor.

The parameters of the inverter system are listed in Table II, which are the same as those used in the design case previously. And the transfer function of the CVCF PWM inverter is given as

$$G_P(z) = \frac{0.2422z + 0.2413}{z^2 - 1.505z + 0.9887}. \tag{18}$$

The controller parameters in CRC, FPLC-RC, and OSRC are almost the same except the compensator $G_f(z)$ and the robust filter Q. In those controllers, the delay line is set as $N = 80$ and the filter $F(z)$ is the same as (13).

In the OSRC controller, the feasible region is shaped as $\overline{m} = 7$, $\underline{m} = 1$, $\overline{M} = 6$, and $\underline{M} = 1$. And the optimized switching parameters with different k_r are given in Table I, which suggests that a larger k_r will deteriorate the stability margin. However, as analyzed previously, a small k_r will result in longer convergence time. Thus $k_r = 1$ is adopted in the experiments to tradeoff between dynamic response and tracking accuracy. Moreover, the RC gain in CRC and FPLC-RC is also designed as $k_r = 1$. It can be seen from Fig. 7 that $\|1 - z^{m_1} P(z)\|_\infty = 1.08$, $\|1 - z^{m_2} P(z)\|_\infty = 1.21$, and $\|\prod_{j=1}^{\alpha+\beta} G[f(j)]\|_\infty^{\frac{1}{\alpha+\beta}} = 1.005$. Based on (17), the maximum value of Q in OSRC is $Q_{\max} = (1/1.005)^{1/2} = 0.99$. To ensure the robustness of the system, Q is selected as $Q = 0.95$. In the CRC controller, the compensator $G_f(z)$ is designed as $G_f = z^{m_1} = z^5$ and $G_f = z^{m_2} = z^4$ for comparison. The robust filter of CRC is selected as $Q = 0.87$ for lead step m_1 (the maximum robust filter for m_1 is $Q_{\max} = 0.92$) and $Q = 0.80$ for lead step m_2 (the maximum robust filter for m_2 is $Q_{\max} = 0.82$) to keep the robustness and stability. And in the FPLC-RC controller, the most efficient fractional compensator in the experiments is $G_f = 0.0117z^2 - 0.0977z^3 +$

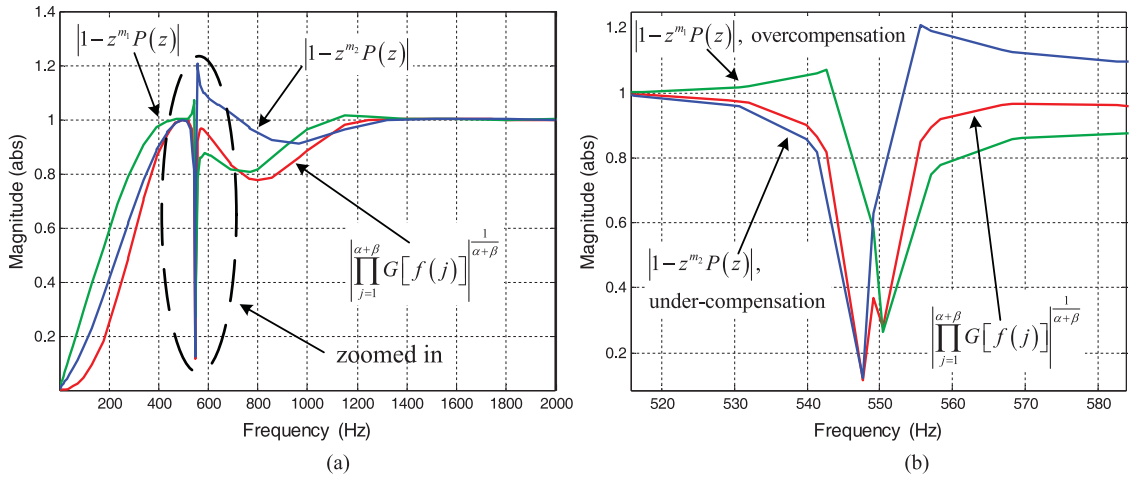

Fig. 7. Compensation performance of OSRC and CRC. (a) Original plot. (b) Zoomed-in plot.

TABLE I
COMPENSATION PERFORMANCE OF OSRC WITH DIFFERENT k_r

k_r	0.5	0.75	1.0	1.25	1.5
m_1	5	6	5	5	5
m_2	4	4	4	4	4
α	2	1	1	1	1
β	3	3	1	1	1
$\left\|\left\|\prod_{j=1}^{\alpha+\beta}G[f(j)]\right\|\right\|_\infty^{\frac{1}{\alpha+\beta}}$	1.002	1.003	1.005	1.013	1.029

TABLE II
PARAMETERS OF EXPERIMENT

Parameter	Value	Parameter	Value
DC bus voltage U_{dc}	100 V	Rectifier resistance R_r	100 Ω
Inductor L	2.1 mH	Rectifier capacitor C_r	4700 μF
Capacitor C	50 μF	PWM frequency f_c	4 kHz
Resistance R	100 Ω	Reference signal $r(t)$	$80\sin(100\pi t)$ V
Rectifier inductor L_r	2.5 mH	Sampling period T_s	2.5×10^{-4} s
Inductor ESR r	0.1 Ω		

$0.5859z^4+0.5859z^5-0.0977z^6+0.0117z^7\approx z^{4.5}$ [13], and the robust filter is tuned as $Q=0.92$. In the following experiment results, U_o is the output voltage, I_o is the output current, e is the tracking error, and the root-mean-square (rms) value of the tracking error e is marked as e(rms).

Moreover, in order to realize the OSRC scheme, besides the feedback signal $U_o(z)$, the only extra state that need to be measured is the reference signal cycle index j, which can be acquired by adopting a loop counter in the controller. The counting interval of the loop counter is T_{ref}, which is also the period of the reference signal. The output of the counter is the current cycle index j, and j satisfies $0\le j<\alpha+\beta$. When $0\le j<\alpha$, the compensator $G_f(z)=z^{m_1}$ is switched ON, and the compensator $G_f(z)=z^{m_2}$ is adopted when $\alpha\le j<\alpha+\beta$. And the

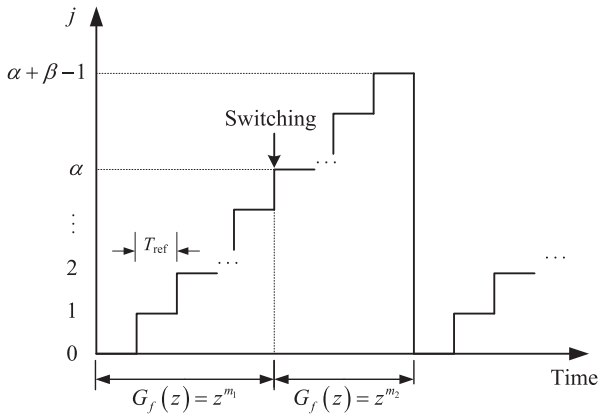

Fig. 8. Operation of the loop counter.

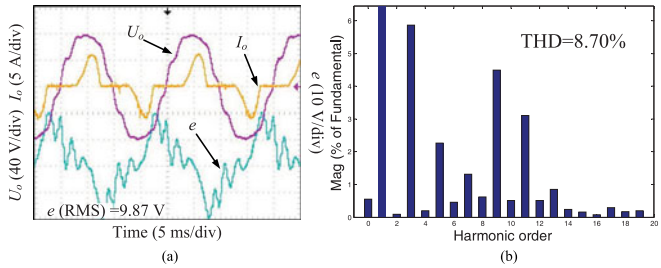

Fig. 9. Steady-state response without RC under rectifier load: (a) the output voltage; and (b) the spectrum of output voltage.

operation of the loop counter is illustrated in Fig. 8, where the X-axis is time and the Y-axis is the output of the counter.

B. Experiment Results

Generally speaking, OSRC can notably improve the tracking performance of the inverter system. Fig. 9(a) shows the output voltage of the system without any RC controller in the rectifier load situation. It can be seen from Fig. 9(a) that the tracking error is very large, and Fig. 9(b) suggests that the

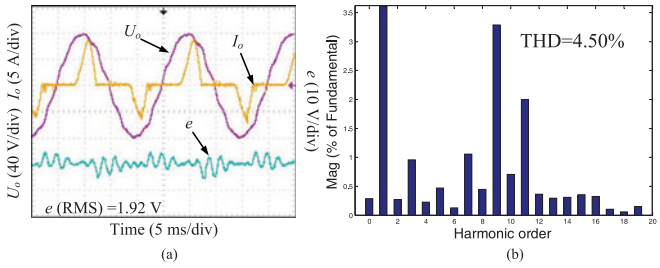

Fig. 10. Steady-state response with CRC ($G_f(z) = z^5$) under rectifier load: (a) the output voltage; and (b) the spectrum of output voltage.

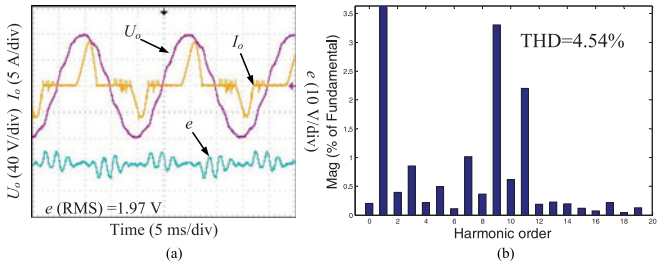

Fig. 11. Steady-state response with CRC ($G_f(z) = z^4$) under rectifier load: (a) the output voltage; and (b) the spectrum of output voltage.

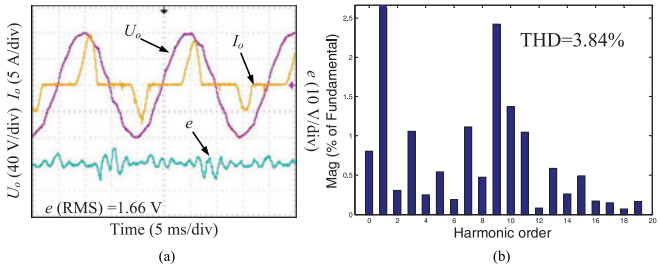

Fig. 12. Steady-state response with OSRC under rectifier load: (a) the output voltage; and (b) the spectrum of output voltage.

harmonic distortion is extremely serious, which is unacceptable in practice. Fig. 10(a) is the output voltage of the inverter controlled by the CRC controller with the compensator $G_f(z) = z^{m_1} = z^5$. Obviously, the CRC controller can significantly reduce the tracking error and attenuate harmonics. Similarly, Fig. 11, which is the steady-state response of the CRC controller with the compensator $G_f(z) = z^{m_2} = z^4$, also suggests that the CRC scheme can effectively improve the tracking performance. However, as mentioned before, the value of Q in the CRC controller must be small to ensure the stability of the system, which limits further improvement of the performance by adopting a larger Q. With the optimized switching compensator, OSRC can effectively enlarge the stability margin and thus a larger Q can be adopted to increase the tracking accuracy. Fig. 12, which is the response of the OSRC controller under the rectifier load, shows much smaller THD and tracking error than those of CRC. The experiment results of FPLC-RC are shown in Fig. 13, which are better than those of CRC. However, the approximation error in

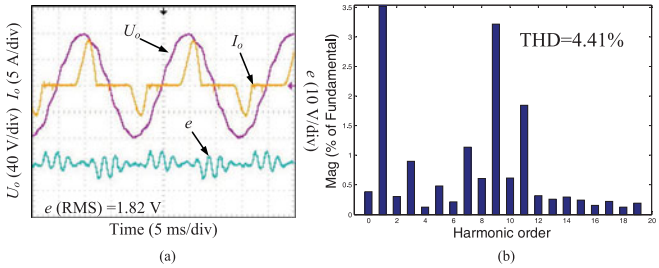

Fig. 13. Steady-state response with FPLC-RC under rectifier load: (a) the output voltage; and (b) the spectrum of output voltage.

TABLE III
EXPERIMENT RESULTS WITH DIFFERENT LOADS

Controller (Under No Load)	THD	e(rms)	Convergence Time
Without RC	5.68%	9.94	20 ms
CRC ($G_f(z) = z^{m_1} = z^5$)	2.83%	1.65	20 ms
CRC ($G_f(z) = z^{m_2} = z^4$)	2.93%	1.76	20 ms
OSRC	2.40%	1.45	20 ms
FPLC-RC	2.65%	1.57	20 ms
Controller (Under Resistance Load)	THD	e(rms)	Convergence Time
Without RC	4.77%	8.88	20 ms
CRC ($G_f(z) = z^{m_1} = z^5$)	2.63%	1.57	20 ms
CRC ($G_f(z) = z^{m_2} = z^4$)	2.70%	1.61	20 ms
OSRC	2.26%	1.29	20 ms
FPLC-RC	2.44%	1.51	20 ms

realizing the fractional lead compensator also limits the performance. The experiment results under no load and resistance load conditions are given in Table III. The steady-state performance, which is implied by THD and e(rms), similarly to the results under the rectifier load, also suggests that OSRC can significantly attenuate the harmonic distortion and improve the tracking accuracy.

To test the error convergence performance of the proposed method, the inverter first works without RC under rectifier situation. Then, RC is added to the control system when there is a trigger signal. Fig. 14 shows the error convergence responses with different controllers. It can be seen from Fig. 14(a)–(c) and (e) that the OSRC controller has the same convergence time as that of the CRC controller and FPLC-RC controller. Similarly, Table III also suggests that the OSRC controller can achieve the same convergence performance as other controllers under different load conditions. Moreover, Fig. 14 (d)–(f) demonstrates the previous analysis of k_r, i.e., a small k_r will lead to a longer convergence time, and a large k_r can result in overshoot and oscillation. Fig. 15 shows the responses of OSRC to sudden load change. It can be seen that the OSRC controller can recover from the sudden load change within about 20 ms, i.e., one cycle of the reference signal.

All those results demonstrate the effectiveness of the OSRC scheme. With the same computation complexity, OSRC can achieve much better stability and tracking performance than CRC. And the byproduct of FPLC-RC does not exist in OSRC. Thus, the OSRC controller is an ideal controller for CVCF PWM

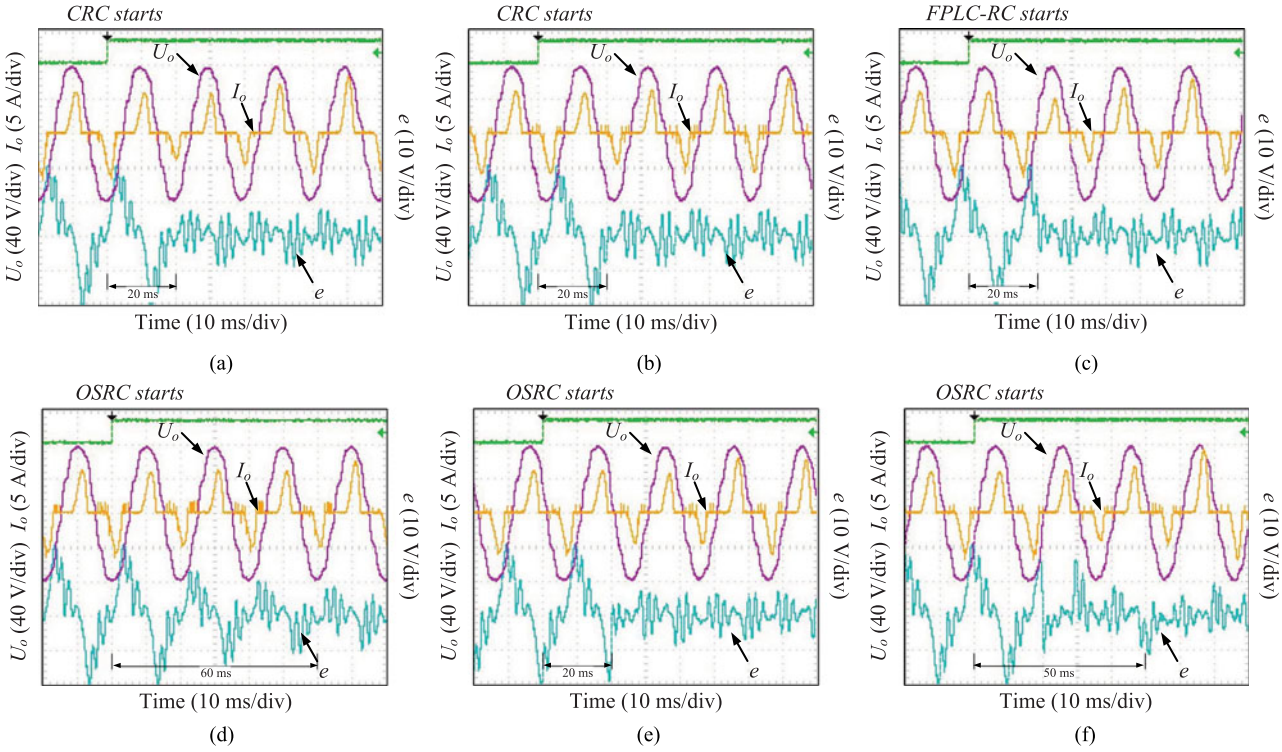

Fig. 14. Transient responses of system with different controllers: (a) CRC ($G_f = z^5$); (b) CRC ($G_f = z^4$); (c) FPLC-RC; and (d)–(f) OSRC with different k_r.

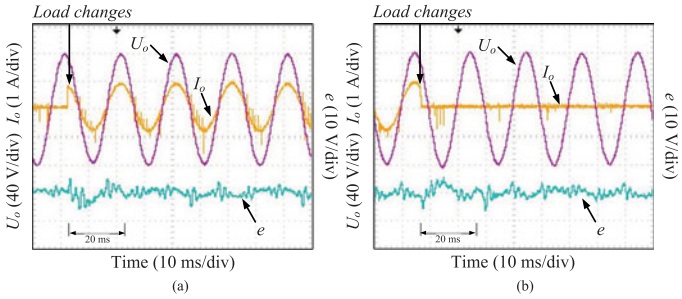

Fig. 15. Dynamic responses of OSRC to changed load: (a) $R = \infty\ \Omega \rightarrow R = 100\ \Omega$; and (b) $R = 100\ \Omega \rightarrow R = \infty\ \Omega$.

inverter systems to achieve high performance with low hardware cost and switching losses.

VI. Conclusion

Prior work has documented the effectiveness of RC in high-precision tracking systems, especially in CVCF PWM inverters. In order to reduce the hardware cost and switching losses, low sampling frequency RC can be applied at the cost of performance degradation. This paper proposes a low sampling rate OSRC scheme for CVCF PWM inverters to improve the stability and tracking precision. In OSRC, a novel switching integral phase lead compensator is applied to enlarge the stability margin, which is impaired by the phase lag. And with the optimized switching strategy, OSRC can maximize the stable region, which allows a better tradeoff between stability and tracking accuracy. Stability analysis and an optimized design procedure have been given. And some comparative experiments are performed to validate the efficacy of OSRC.

However, the design of the OSRC scheme is performed offline, which may hinder the performance as other model-based optimized controllers when the model is inaccurate. Future work should therefore include autotuning of the switching strategy. And this paper forms the basis of autotuning SRC for CVCF PWM dc–ac inverters.

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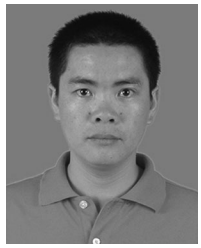

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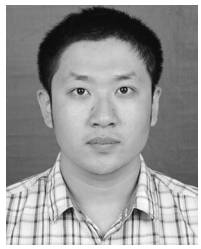

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