Optimized Control of the Modular Multilevel Converter Based on Space Vector Modulation

Yi Deng, *Member, IEEE*, Yebin Wang, *Senior Member, IEEE*, Koon Hoo Teo, *Member, IEEE*, Maryam Saeedifard, *Senior Member, IEEE*, and Ronald G. Harley, *Life Fellow, IEEE*

***Abstract*—This paper presents a general space vector modulation (SVM) method for the modular multilevel converter (MMC). Compared with earlier modulation methods, the proposed SVM method not only utilizes the maximum level number (i.e., $2n+1$, where n is the number of submodules in the upper or lower arm of each phase) of output phase voltages, but also leads to an optimized control performance in terms of capacitor voltage balancing, circulating current suppression, and common-mode voltage reduction. The maximum level number is achieved by introducing a new equivalent circuit of the MMC, and the optimized control is obtained by selecting the optimal redundant switching states. Since the computational burden of the SVM scheme is independent of the voltage level number, the proposed method is well suited to the MMC with any number of submodules. Simulation and experimental results are presented to validate the proposed method.**

***Index Terms*—Capacitor voltage balancing, circulating current suppression, common-mode voltage, modular multilevel converter (MMC), space vector modulation (SVM).**

I. Introduction

MULTILEVEL converters offer superior performance when compared to two-level converters, with advantages, such as reduced voltage stress on the power semiconductor devices, lower harmonics, lower instantaneous rate of voltage change (dv/dt), and lower common-mode voltages [1], [2]. As an emerging multilevel converter topology in the early 2000s [3], the modular multilevel converter (MMC) has recently attracted much research attention, because of its significant merits, such as modularity and scalability to meet high-voltage high-power requirements [4], [5]. For example, the first commercialized MMC-based high-voltage direct-current system, i.e., the "Trans Bay Cable Project," is reported to have achieved ±200 kV/400 MW using 216 submodules (SM) per arm [6].

It is imperative to regulate the SM capacitor voltages, for the sake of proper operation of the MMC. Furthermore, reducing the capacitor voltage ripples is always an important objective because it enables the adoption of smaller capacitors [7]. This eventually leads to a reduced cost of the MMC considering the large number of SM capacitors. At the same time, circulating currents have to be well controlled because of their significant influence on the ratings and power losses of the MMC. Since the SM capacitor voltages are mutually coupled with the circulating currents within the same phase leg of the MMC, the control of the MMC gets complicated. Viewed as the internal control of the MMC, the control of both capacitor voltages and circulating currents is typically achieved at the modulation stage. Another important control objective, i.e., the reduction of common-mode voltages, also usually relies on modulation methods [1], [2].

Low-frequency modulation methods, such as the selective harmonic elimination [8] and the nearest level control [9], [10], represent one control approach for the MMC. Compared with modulation methods at high switching frequencies, the low-frequency modulation methods cause lesser power losses. However, large SM capacitors are usually required by these low-frequency methods in order to reduce the capacitor voltage ripples. Some low-frequency methods [8] need computation of many switching angles, which results in extra complexity.

Several high-frequency pulse width modulation (PWM) methods have been applied to the MMC, and most of them can be classified into two categories: the carrier-based modulation (including the phase-shifted PWM [11]–[15] and the phase-disposition PWM [16], [17]) and the nearest level modulation (NLM) [18]–[23]. The phase-shifted PWM individually modifies the modulation signals for each SM. When the MMC consists of a large number of SMs, the computational burden and complexity of the phase-shifted PWM significantly increase. On the other hand, the NLM and phase-disposition PWM methods only require controllers for each entire arm of the MMC. This offers an advantageous feature for the MMC with a large number of SMs. Furthermore, the NLM is easier to implement than the

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Y. Deng was with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA. He is now with GalaTech, Inc., San Jose, CA 95131 USA (e-mail: ydeng35@gatech.edu).

Y. Wang and K. H. Teo are with Mitsubishi Electric Research Laboratories, Cambridge, MA 02139 USA (e-mail: yebinwang@ieee.org; teo@merl.com).

M. Saeedifard is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: maryam@ece.gatech.edu).

R. G. Harley is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA, and also with the School of Engineering, University of KwaZulu-Natal, Durban 4041, South Africa (e-mail: rharley@ece.gatech.edu).

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phase-disposition PWM, because no carrier waves or associated modifications are needed.

Compared with the aforementioned modulation methods, space vector modulation (SVM) techniques provide more flexibility to optimize the performance of multilevel converters, especially when the level number is large [24]–[26] (which is exactly the case for the MMC). However, few SVM strategies have been reported for the MMC at this time. In [27], a SVM method with control of capacitor voltages and circulating currents is presented for the MMC, but its implementation is complicated. A dual-SVM method for the MMC is introduced in [28]; however, the required two SVM schemes increase both computational burden and complexity. In addition, no control of capacitor voltages (except the sorting approach) or circulating currents is implemented in [28].

The obstacle for applying SVM to the MMC results from the following aspects: 1) the largely increased number of switching states that accompanies the larger number of levels; 2) the structure of the MMC (two arms in each phase) that is different from conventional multilevel converters; and 3) the integration of the SVM scheme with the control of the MMC. The SVM scheme in [29] is well suited to conventional multilevel converters, because it is independent of the converter level number and significantly simplifies the generation of switching sequences. However, it cannot be directly applied to the MMC, considering the different structure of the MMC and the integration of the control.

Based on the SVM scheme in [29], this paper proposes a generalized SVM method for the MMC, to overcome the aforementioned shortcomings of the earlier methods. Optimized control of capacitor voltages, circulating currents, and common-mode voltages by utilizing the redundant switching states is presented as well. Through a new equivalent circuit of the MMC, the proposed SVM method utilizes the maximum level number (i.e., $2n+1$, where n is the number of SMs in the upper or lower arm of each phase) of the output phase voltages, thus leading to the maximum number of redundant switching states for optimizing the control. The computational burden of the SVM scheme is independent of the voltage level number, so the proposed method is well suited to control the MMC with a large number of SMs.

The rest of this paper is organized as follows: Section II describes the equivalent circuit and basics of control of the MMC; Section III presents the proposed SVM method; Sections IV introduces the optimized control strategy; Sections V and VI demonstrate some typical simulation and experimental results, respectively; and Section VII concludes this paper.

II. Equivalent Circuit and Control of the MMC

A. Equivalent Circuit of the MMC

Fig. 1 shows the circuit diagram of one phase (phase a) of the MMC, which contains an upper arm and a lower arm. There are n SMs in each arm (i.e., SM_{aP1}–SM_{aPn} in the upper arm and SM_{aN1}–SM_{aNn} in the lower arm). A detailed half-bridge SM is shown in Fig. 1. The output voltage v_{SM} of a SM is v_C ("ON" state) when S_1 is switched ON and S_2 is switched OFF, and is zero ("OFF" state) when S_1 is switched OFF and S_2 is

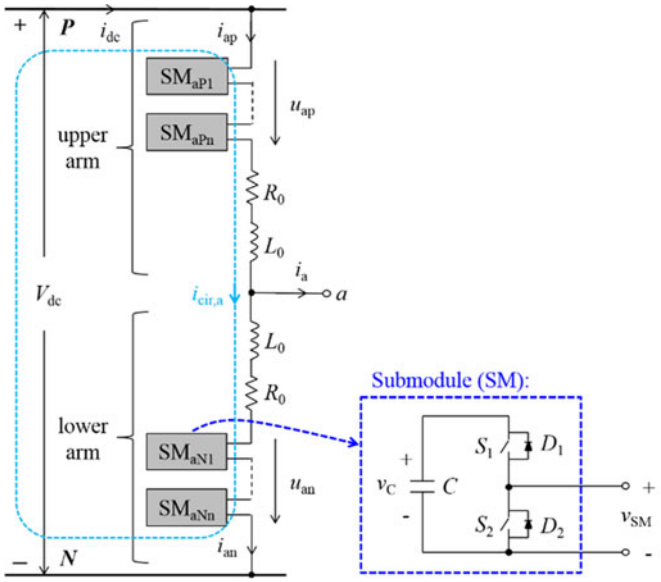

Fig. 1. Circuit diagram of one phase of the MMC.

switched ON. V_{dc} and i_{dc} are, respectively, the dc-link voltage and current; i_{ap} and i_{an} are the currents of the upper and lower arms, respectively; and i_a is the output current of phase a. The inductors (inductance is L_0) in the upper and lower arms are the buffer inductors; the parasitic ohmic losses in each arm are represented by a resistor R_0. Other phase legs are identical to phase a.

Based on Kirchhoff's voltage law, the output voltage v_{aN} of phase a relative to the negative terminal of the dc-link is, respectively, calculated for the upper and lower arms as follows:

$$v_{aN} = V_{dc} - u_{ap} - L_0 \cdot di_{ap}/dt - R_0 \cdot i_{ap} \tag{1a}$$

$$v_{aN} = u_{an} + L_0 \cdot di_{an}/dt + R_0 \cdot i_{an} \tag{1b}$$

where u_{ap} and u_{an} are the total output voltages of the SMs in the upper and lower arms of phase a, respectively. From (1) and according to Kirchhoff's current law, v_{aN} is obtained as follows:

$$v_{aN} = v_{a0} - L_0/2 \cdot di_a/dt - R_0/2 \cdot i_a \tag{2a}$$

$$v_{a0} = \left(V_{dc} - u_{ap} + u_{an}\right)/2. \tag{2b}$$

Based on (2), the equivalent circuit of a three-phase MMC for the load is depicted in Fig. 2(a), where v_{b0} and v_{c0} are the corresponding voltages of phases b and c similarly defined as in (2b). In this paper, v_{h0} ($h = a, b,$ or c) is called the "modulation voltage."

Meanwhile, the currents of the upper and lower arms of phase a are [11]

$$i_{ap} = i_{cir,a} + i_a/2 \tag{3a}$$

$$i_{an} = i_{cir,a} - i_a/2 \tag{3b}$$

where $i_{cir,a} = (i_{ap} + i_{an})/2$ is called the circulating current of phase a and is independent of the load. Based on Kirchhoff's voltage law, the circulating current is determined by [22]

$$L_0 \cdot \frac{di_{cir,a}}{dt} + R_0 \cdot i_{cir,a} = u_{diff,a} = \left(V_{dc} - u_{ap} - u_{an}\right)/2 \tag{4}$$

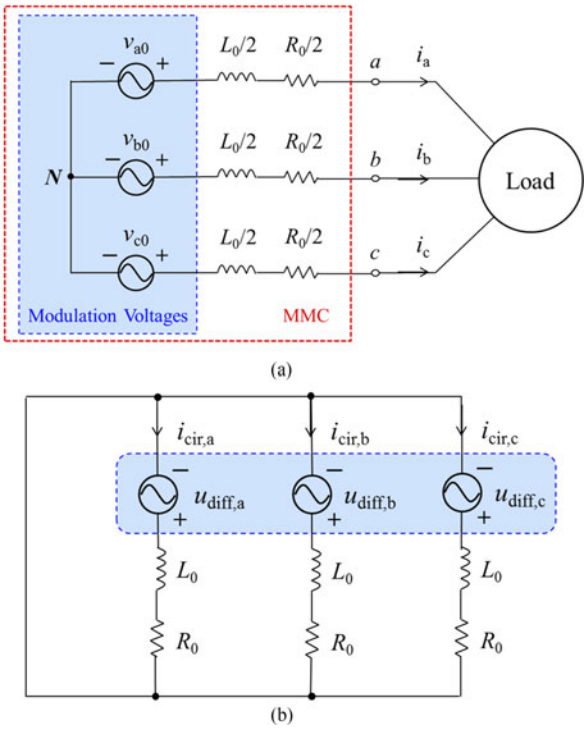

Fig. 2. Equivalent circuit of a three-phase MMC: (a) For the load; (b) for the circulating currents.

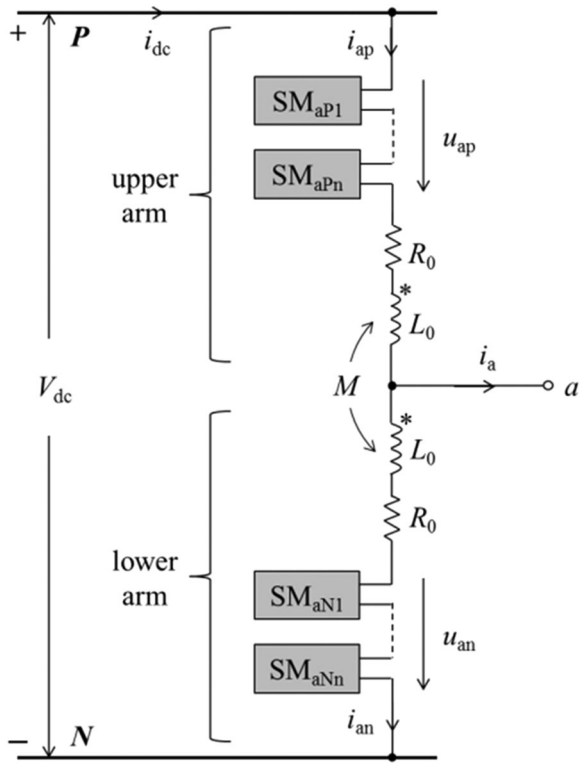

Fig. 3. Circuit diagram (one phase) of an MMC when coupled buffer inductors are used.

where $u_{\mathrm{diff},a}$ is called the "difference voltage" of phase a. Accordingly, the equivalent circuit of the three-phase MMC for the circulating currents is shown in Fig. 2(b), where $u_{\mathrm{diff},h}$ and $i_{\mathrm{cir},h}$ are, respectively, the difference voltage and circulating current of phase h similarly defined in (4).

Fig. 2 reveals that the MMC can be controlled by regulating the modulation voltage v_{h0} and the difference voltage $u_{\mathrm{diff},h}$. The reference value of v_{h0} is determined in accordance with the load and the applications of the MMC (i.e., external control), and can generally be obtained from a current regulator. On the other hand, the reference value of $u_{\mathrm{diff},h}$ is adjusted to control the circulating current, and, consequently, the SM capacitor voltages (i.e., internal control), which will be introduced in detail later.

When coupled buffer inductors are used as shown in Fig. 3, (1a) and (1b), respectively, become

$$v_{aN} = V_{\mathrm{dc}} - u_{ap} - L_0 \cdot di_{ap}/dt - R_0 \cdot i_{ap} - M \cdot di_{an}/dt \tag{5a}$$

$$v_{aN} = u_{an} + L_0 \cdot di_{an}/dt + R_0 \cdot i_{an} + M \cdot di_{ap}/dt. \tag{5b}$$

Consequently, (2a) turns into

$$v_{aN} = v_{a0} - (L_0 - M)/2 \cdot di_a/dt - R_0/2 \cdot i_a \tag{6}$$

where M is the mutual inductance. The equivalent circuit shown in Fig. 2(a) is still applicable in this condition, except that the series inductance is $(L_0 - M)/2$ rather than $L_0/2$. Accordingly, (4) becomes

$$(L_0 + M) \cdot di_{\mathrm{cir},a}/dt + R_0 \cdot i_{\mathrm{cir},a} = u_{\mathrm{diff},a} \tag{7}$$

which means that the equivalent circuit shown in Fig. 2(b) is also applicable, except that the inductance is $L_0 + M$ instead of L_0.

B. Control of Capacitor Voltages and Circulating Currents

The variations of SM capacitor voltages can be analyzed through the capacitor energies. According to Fig. 2, the energy stored in the capacitors of the upper arm (W_{ap}) and the lower arm (W_{an}) of phase a, respectively, deviate as follows:

$$dW_{ap}/dt = u_{ap} \cdot i_{ap} \tag{8a}$$

$$dW_{an}/dt = u_{an} \cdot i_{an}. \tag{8b}$$

By substituting (1)–(3) into the above equations, the derivatives of the total capacitor energy ($W_{ap} + W_{an}$) of phase a and the unbalanced energy ($W_{ap} - W_{an}$) between the upper and lower arms are obtained as

$$\frac{d(W_{ap} + W_{an})}{dt} = V_{\mathrm{dc}} \cdot \left(i_{\mathrm{cir},a} + \frac{i_a}{2}\right) - 2u_{\mathrm{diff},a} \cdot i_{\mathrm{cir},a} - v_{a0} \cdot i_a \tag{9a}$$

$$\frac{d(W_{ap} - W_{an})}{dt} = V_{\mathrm{dc}} \cdot \left(i_{\mathrm{cir},a} + \frac{i_a}{2}\right) - u_{\mathrm{diff},a} \cdot i_a - 2v_{a0} \cdot i_{\mathrm{cir},a} \tag{9b}$$

which show that the circulating current $i_{\mathrm{cir},a}$ plays a significant role in controlling the capacitor energies (i.e., the capacitor voltages in each arm).

More specifically, $i_{\text{cir},a}$ and $u_{\text{diff},a}$ can be expressed by their dc and harmonic components as follows:

$$i_{\text{cir},a} = I_{\text{cir},a} + \sum_{k=1}^{\infty} i_{\text{cir}(k)} \tag{10a}$$

$$u_{\text{diff},a} = U_{\text{diff},a} + \sum_{k=1}^{\infty} u_{\text{diff}(k)} \tag{10b}$$

where $I_{\text{cir},a}$ and $U_{\text{diff},a}$ are the dc components, and $i_{\text{cir}(k)}$ and $u_{\text{diff}(k)}$ are the kth order harmonics. Then, (9) is rewritten as

$$\frac{d\left(W_{ap}+W_{an}\right)}{dt} = \underline{V_{\text{dc}} \cdot I_{\text{cir},a} - 2u_{\text{diff},a} \cdot i_{\text{cir},a} - v_{a0} \cdot i_a} + V_{\text{dc}} \cdot \left(\sum_{k=1}^{\infty} i_{\text{cir}(k)} + \frac{i_a}{2}\right) \tag{11a}$$

$$\frac{d\left(W_{ap}-W_{an}\right)}{dt} = \underline{V_{\text{dc}} \cdot I_{\text{cir},a} - u_{\text{diff}(1)} \cdot i_a - 2v_{a0} \cdot \left(I_{\text{cir},a} + i_{\text{cir}(1)}\right)} + V_{\text{dc}} \cdot \left(\sum_{k=1}^{\infty} i_{\text{cir}(k)} + \frac{i_a}{2}\right) - \left(U_{\text{diff},a} + \sum_{k=2}^{\infty} u_{diff(k)}\right) \cdot i_a - 2v_{a0} \cdot \sum_{k=2}^{\infty} i_{\text{cir}(k)} \tag{11b}$$

where only the parts underlined contribute to dc components (v_{a0} is assumed to contain only dc and fundamental frequency components). The dc components should be zero in the steady state, in order to stabilize the total and unbalanced capacitor energies.

From (11a), the dc component of the circulating current can be regulated to maintain the total capacitor energy. The active power provided by the dc-link voltage then is delivered to the load and compensates for the power losses of the phase leg. On the other hand, (11b) indicates that the unbalanced capacitor energy between the upper and lower arms can be controlled by regulating the fundamental-frequency component of the difference voltage $u_{\text{diff},a}$ that is in phase with the output current i_a, or the fundamental-frequency component of the circulating current that is in phase with (the fundamental-frequency component of) the modulation voltage v_{a0}. Similar conclusions hold for the other phases. Based on (8)–(11), the steady-state capacitor voltages and arm currents can be estimated as in [19] to specify the SM capacitors and buffer inductors.

Fig. 4 shows a control diagram for capacitor voltages and circulating currents, taking phase a as an example. It consists of three control loops, i.e., the averaging control, the circulating current control, and the arm-balancing control; and finally, a reference value $u^*_{\text{diff},a}$ of the difference voltage is generated. Corresponding to (11a), the averaging control forces the average capacitor voltage $\bar{v}_{C,a}$ of the phase to follow its reference value

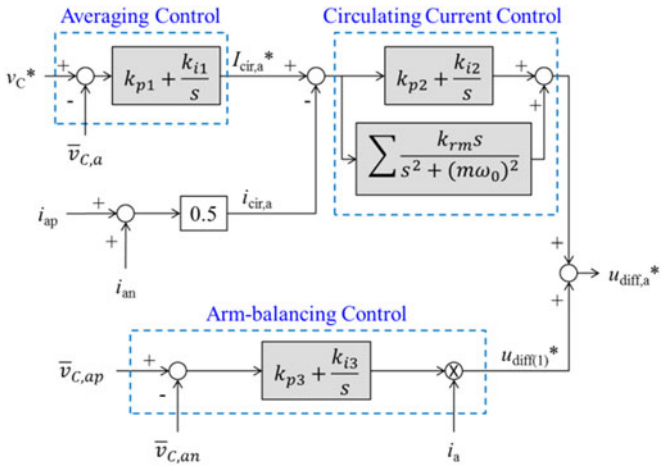

Fig. 4. Control of the capacitor voltages and circulating current for one phase (phase a as an example).

v_C^*, with

$$\bar{v}_{C,a} = \left(\bar{v}_{C,ap} + \bar{v}_{C,an}\right)/2 \tag{12a}$$

$$\bar{v}_{C,ap} = \left(\sum_{i=1}^{n} v_{C,api}\right)/n \tag{12b}$$

$$\bar{v}_{C,an} = \left(\sum_{i=1}^{n} v_{C,ani}\right)/n \tag{12c}$$

where $\bar{v}_{C,ap}$ and $\bar{v}_{C,an}$ are the average capacitor voltages of the upper and lower arms of phase a, respectively; $v_{C,api}$ is the capacitor voltage of the ith SM in the upper arm; and $v_{C,ani}$ is the capacitor voltage of the ith SM in the lower arm. The averaging control gives a reference value $I^*_{\text{cir},a}$ of the dc component of the circulating current. Based on (11b), the arm-balancing control loop generates a fundamental-frequency component $u_{\text{diff}(1)}{}^*$ of the difference voltage to cancel the capacitor voltage difference between the upper and lower arms.

The circulating current-control loop forces the circulating current to follow the reference dc component $I_{\text{cir,a}}{}^*$, as well as eliminates second-order (and higher order if needed) components of the circulating current. Similar to the averaging control and arm-balancing control, the circulating current-control loop applies a proportional-integral (PI) controller to track the reference dc component. A set of resonant controllers [23] expressed as follows:

$$G_r(s) = \sum \frac{k_{rm}s}{s^2 + (m\omega_0)^2} \tag{13}$$

where ω_0 is the fundamental angular frequency and k_{rm} is the coefficient for the mth-order resonant frequency, is utilized to eliminate the corresponding harmonics. If needed, using non-ideal resonant controllers can further increase the robustness of the control system against frequency deviation [30].

According to (4), the circulating current-control loop in fact regulates the dc and second-order (and higher order if the corresponding resonant controller is applied) components of the difference voltage. Finally, a reference value $u^*_{\text{diff},a}$ of the

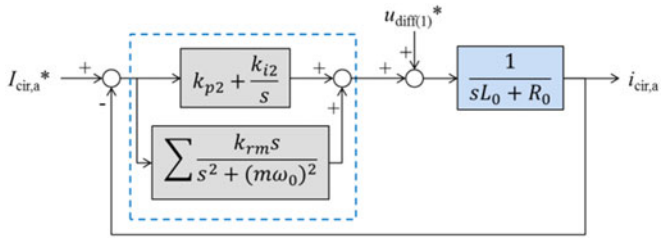

Fig. 5. Closed-loop diagram of the circulating current control.

difference voltage is generated to achieve the capacitor voltage and circulating current control.

Fig. 5 shows the closed-loop diagram of the circulating current control, taking (4) into account. The open-loop transfer function is

$$G_o(s)=\left(k_{p2}+\frac{k_{i2}}{s}+\sum\frac{k_{rm}s}{s^2+(m\omega_0)^2}\right)\cdot\frac{1}{sL_0+R_0}. \quad (14)$$

At the resonant frequency $m\omega_0$, the gain of $G_o(s)$ is infinite, so the mth-order harmonic of the circulating current is eliminated in the steady state. More detailed analysis of the circulating current control is presented in Section V.

Note that the control of capacitor voltages and circulating currents may also be implemented in other approaches. For example, it can be designed to force the circulating current to contain only the dc component [12], [23], which minimizes the power losses of the MMC but may increase the ripples of the capacitor voltages according to (11). Injecting specific circulating currents based on the steady state or instantaneous information of the MMC to reduce the capacitor voltage ripples is investigated in [19]. Based on the synchronous reference frame, PI controllers instead of resonant controllers can be adopted to eliminate specific harmonics of the circulating currents [15]. However, it is a common point of those methods that the control of capacitor voltages and circulating currents is achieved by regulating the reference difference voltage $u_{\mathrm{diff,h}}{}^*$ for each phase of the MMC.

III. Proposed SVM Method for the MMC

As explained in the previous section, the MMC can be controlled by regulating the modulation voltages (external control for the load) and the difference voltages (internal control for the SM capacitor voltages and circulating currents). Assume that now the reference values of the modulation and difference voltages have been obtained, then how to generate the gate signals (i.e., modulation strategy) according to those reference values? This section proposes a general SVM method for the MMC based on the SVM scheme introduced in [29].

A. Generating the Modulation Voltages for the Load

The general multilevel SVM scheme introduced in [29], as illustrated in Fig. 6 based on the space vector diagram of a five-level converter, is applied to generate the reference value v_{h0}^* of the modulation voltage v_{h0} required by the load. Accordingly,

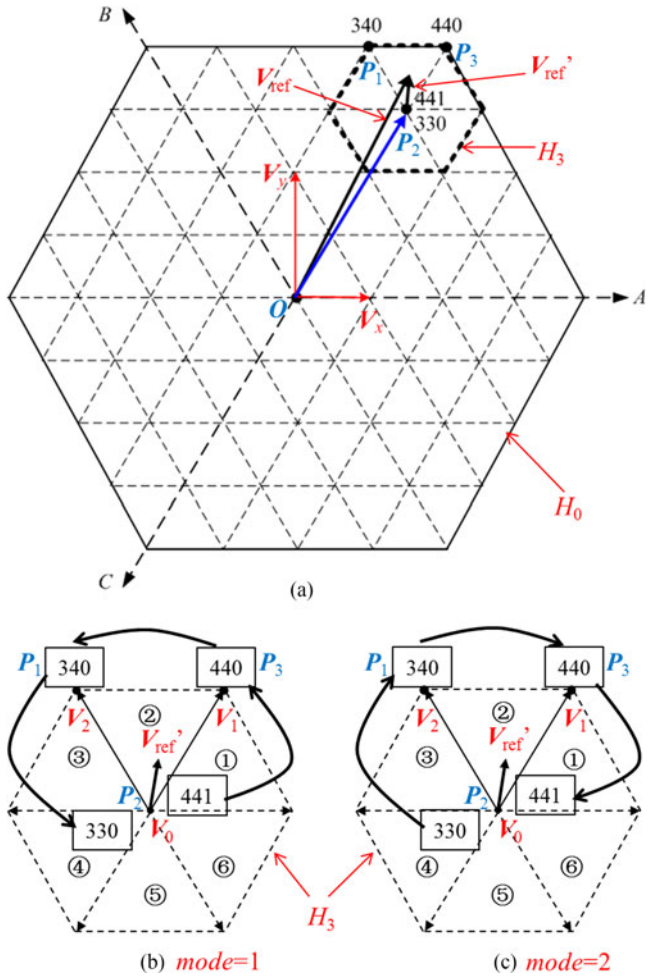

Fig. 6. General SVM scheme in [29]: (a) Detecting the modulation triangle; (b) and (c) two switching sequence modes.

the reference vector $\boldsymbol{V}_{\mathrm{ref}}$ is defined [24], [25], [29] as follows:

$$\begin{aligned}\boldsymbol{V}_{\mathrm{ref}}&=(N-1)\left(v_{a0}^*+v_{b0}^*\cdot e^{j\frac{2}{3}\pi}+v_{c0}^*\cdot e^{j\frac{4}{3}\pi}\right)\\&=(N-1)\left(M\cdot\frac{\sqrt{3}}{2}V_{\mathrm{dc}}\cdot e^{j\theta}\right)\end{aligned} \quad (15)$$

where N is the number of voltage levels; M $(=\hat{v}_{ab}/V_{\mathrm{dc}})$ is the modulation index, where $\hat{v}_{ab}$ is the peak value of the reference line-to-line voltage $(v_{a0}^*-v_{b0}^*)$; and θ is the phase angle of $\boldsymbol{V}_{\mathrm{ref}}$.

Two "orthogonal unit vectors" $\boldsymbol{V}_x$ and $\boldsymbol{V}_y$ shown in Fig. 6 decouple the three-phase components, thus essentially easing the detection of the reference vector's location. More specifically, $\boldsymbol{V}_x$ only contains the component of phase a, while $\boldsymbol{V}_y$ only contains the components of phases b and c. A candidate switching state $S_aS_bS_c$, for the vertex (i.e., P_2) of the modulation triangle $\Delta P_1P_2P_3$ (i.e., the nearest three vectors $\boldsymbol{O}P_1$, $\boldsymbol{O}P_2$, and $\boldsymbol{O}P_3$) closest to the origin, is consequently detected by the general SVM in a single step [29]

$$\begin{bmatrix}S_a\\S_b\\S_c\end{bmatrix}=\mathrm{int}\left(\begin{bmatrix}x-\min(x,y,-y)\\y-\min(x,y,-y)\\-y-\min(x,y,-y)\end{bmatrix}\right) \quad (16)$$

TABLE I
MAPPING OF DETERMINING SWITCHING SEQUENCES[①] [29]

reg	1	2	3	4	5	6
D_h	$D_a = 1 - d_{01}$ $D_b = 1 - d_{01} - d_1$ $D_c = 1 - d_{01} - d_1 - d_2$	$D_a = d_{01} + d_1$ $D_b = d_{01} + d_1 + d_2$ $D_c = d_{01}$	$D_a = 1 - d_{01} - d_1 - d_2$ $D_b = 1 - d_{01}$ $D_c = 1 - d_{01} - d_1$	$D_a = d_{01}$ $D_b = d_{01} + d_1$ $D_c = d_{01} + d_1 + d_2$	$D_a = 1 - d_{01} - d_1$ $D_b = 1 - d_{01} - d_1 - d_2$ $D_c = 1 - d_{01}$	$D_a = d_{01} + d_1 + d_2$ $D_b = d_{01}$ $D_c = d_{01} + d_1$

[①] D_h and $1 - D_h$ are the respective duty cycles of the two switching states $K_h + 1$ and K_h for phase h.

where $\min(x,\ y,\ -y)$ denotes the minimum value among x, y, and $-y$; $\text{int}(\gamma)$ stands for the corresponding integer parts of all the elements in an array γ; and

$$x = \frac{V_{\text{ref}(x)}}{V_{\text{dc}}},\ y = \frac{V_{\text{ref}(y)}}{\sqrt{3}V_{\text{dc}}} \tag{17}$$

are the coordinates of the reference vector with respect to the two orthogonal unit vectors, where $V_{\text{ref}(x)}$ and $V_{\text{ref}(y)}$ are, respectively, the real and imaginary components of the reference vector. The essence of (16) is that $\{x,\ y,\ -y\}$ represents a coordinate of the reference vector in the original ABC-frame, so equally subtracting $\min(x,\ y,\ -y)$ from the three components yields another coordinate of the reference vector.

After shifting the origin of the reference vector $\boldsymbol{V}_{\text{ref}}$ to the detected vertex (P_2), a so-called "remainder vector" $\boldsymbol{V}_{\text{ref}}{}'$ is yielded, which is inside a two-level hexagon H_3. Based on this remainder vector as shown in Fig. 6(b) and (c), the duty cycles of the nearest three vectors are determined in the same way as for a two-level SVM [29]

$$\begin{cases} d_1 = \frac{2}{\sqrt{3}}\left[V_{rx}\ \sin\left(\frac{reg}{3}\pi\right) - V_{ry}\cos\left(\frac{\text{reg}}{3}\pi\right)\right] \\ d_2 = -\frac{2}{\sqrt{3}}\left[V_{rx}\sin\left(\frac{reg-1}{3}\pi\right) - V_{ry}\cos\left(\frac{\text{reg}-1}{3}\pi\right)\right] \\ d_0 = 1 - d_1 - d_2 \end{cases} \tag{18}$$

where V_{rx} and V_{ry} represent the real and imaginary part of $\boldsymbol{V}'_{\text{ref}}/V_{\text{dc}}$, respectively; d_1 and d_2 are, respectively, the duty cycles of $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$; d_0 is the total duty cycle for the "zero vectors," i.e., the switching states at the detected vertex (e.g., 441 and 330 at P_2); reg is the region number (①–⑥) of the remainder vector $\boldsymbol{V}'_{\text{ref}}$ in the two-level hexagon H_3 and is given [29] by

$$\text{reg} = \text{int}\,(3\theta_{\text{rem}}/\pi) + 1 \tag{19}$$

where $\theta_{\text{rem}}\ (0 \le \theta_{\text{rem}} < 2\pi)$ is the angle of the remainder vector with respect to the real axis, and $\text{int}(3\theta_{\text{rem}}/\pi)$ represents the integer part of $3\theta_{\text{rem}}/\pi$. In this paper, each switching sequence (e.g., $441 \to 440 \to 340 \to 330$) contains two zero vectors, and the duty cycles d_{01} and d_{02} of the two zero vectors are set to be equal (i.e., $d_{01} = d_{02} = 0.5d_0$) for the objective of the optimal harmonic performance [31].

All the switching sequences are then generated as follows based on the switching state in (16) and the duty cycles in (18). It has been demonstrated in [24] and [29] that any optimized switching sequence (with the minimum number of switch transitions in every switching cycle) can be equivalently achieved by two successive switch states K_h and $K_h + 1$ for each phase, as long as the duty cycles of K_h and $K_h + 1$ (i.e., $1 - D_h$ and D_h, respectively) are the values summarized in Table I. As the two "zero vectors" in the switching sequence $K_aK_bK_c$ and $(K_a + 1)(K_b + 1)(K_c + 1)$ are redundant switching states of the vertex detected in (16). For example, 330 and 441 at P_2 are the two zero vectors for the switching sequence $330 \to 340 \to 440 \to 441$ shown in Fig. 6. The mapping in Table I makes the generation of switching sequences to be as simple as the NLM method.

Since each value of $K_aK_bK_c$ leads to a switching sequence, all the redundant switching states for the detected vertex can be generated [29] based on (16) as follows:

$$\begin{bmatrix} K_a \\ K_b \\ K_c \end{bmatrix} = \begin{bmatrix} S_a + N_0 \\ S_b + N_0 \\ S_c + N_0 \end{bmatrix},\ \text{where } N_0 \text{ is any integer} \in [0,\ N - 2 - \max(S_a, S_b, S_c)] \tag{20}$$

where $\max(S_a,\ S_b,\ S_c)$ is the maximum value among S_a, S_b, and S_c. The range of N_0, determined by the voltage level number N and the modulation index M, indicates the total number of redundancies. The maximum value of N_0 is $N-2 - \max(S_a,\ S_b,\ S_c)$ because otherwise $K_h + 1$ ($h = a$, b, or c) exceeds $N - 1$. Compared with other modulation methods, the SVM scheme provides the significant flexibility to optimize the performance of the MMC by selecting the optimal N_0.

Aforementioned is a brief review of the SVM scheme. For more details please refer to [29]. Note that this scheme is independent of the level number of the converter and the location of the reference vector, thus well suited to the MMC.

With the switching state K_h and duty cycle D_h, the actual modulation voltage applied to phase h of the MMC is [24]

$$\begin{aligned} v_{h0} &= (1 - D_h) \cdot \frac{K_h V_{\text{dc}}}{N - 1} + D_h \cdot \frac{(K_h + 1)\, V_{\text{dc}}}{N - 1} \\ &= (K_h + D_h)\, V_{\text{dc}}/(N - 1)\,. \end{aligned} \tag{21}$$

Assume that k_{hp} and $k_{hn}\ (0 \le k_{hp},\ k_{hn} \le n)$ SMs, respectively, in the upper and lower arms of phase h are in the "ON" state. If the capacitor voltages are assumed to be well balanced, i.e., $v_C = V_{\text{dc}}/n$ for any SM, then (2b) is rewritten as

$$v_{h0} = \left(V_{\text{dc}} - k_{hp} \cdot V_{dc}/n + k_{hn} \cdot V_{\text{dc}}/n\right)/2. \tag{22}$$

Combining (21) and (22) yields the following relationship:

$$n - k^*_{hp} + k^*_{hn} = 2n \cdot (K_h + D_h)/(N - 1) \tag{23}$$

where * represents the reference value. Since (23) offers some flexibility of selecting k_{hp} and k_{hn}, this flexibility is used to

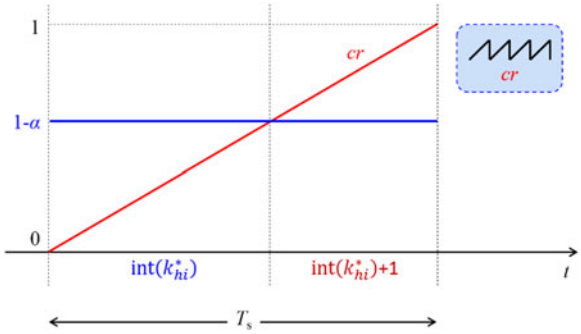

Fig. 7. Generation of k_{hi} ($h = a, b,$ or c; $i =$ p or n) during a switching cycle T_s.

control the circulating currents and capacitor voltages, as introduced later.

Note that as shown in (22), $0 \le v_{h0} \le V_{\rm dc}$ and the minimum voltage step for v_{h0} is $V_{\rm dc}/(2n)$, so theoretically the maximum level number is $N = 2n + 1$. In other words, because of the equivalent circuit in Fig. 2, the proposed SVM method naturally generates the maximum number of levels.

B. Applying the Reference Difference Voltage

In order to control the capacitor voltages and circulating currents, the reference difference voltage $u^*_{{\rm diff},h}$ obtained from Fig. 4 for phase h needs to be applied. Combining (4) and (23) then gives reference values for k_{hp} and k_{hn} as follows:

$$k^*_{hp} = n - \frac{n}{N-1} \cdot (K_h + D_h) - \frac{n}{V_{\rm dc}} \cdot u^*_{{\rm diff},h} \tag{24a}$$

$$k^*_{hn} = \frac{n}{N-1} \cdot (K_h + D_h) - \frac{n}{V_{\rm dc}} \cdot u^*_{{\rm diff},h}. \tag{24b}$$

Finally, a general solution for each k_{hi} ($i =$ p or n) during a switching cycle T_s is obtained as

1) If $k^*_{hi} \le 0$

$$k_{hi} = 0. \tag{25a}$$

2) If $k^*_{hi} \ge n$

$$k_{hi} = n. \tag{25b}$$

3) If $0 < k^*_{hi} < n$

$$k_{hi} = \begin{cases} \text{int}\left(k^*_{hi}\right), & \text{when } 0 < t \le (1-\alpha)\,T_s \\ \text{int}\left(k^*_{hi}\right) + 1, & \text{when } (1-\alpha)\,T_s < t \le T_s \end{cases} \tag{25c}$$

where int(k^*_{hi}) represents the integer part of k^*_{hi}, and

$$\alpha = k^*_{hi} - \text{int}\left(k^*_{hi}\right). \tag{26}$$

Fig. 7 illustrates the way to generate k_{hi} for each arm of the MMC during a switching cycle T_s, where cr is a carrier wave. The implementation of the proposed SVM method is as easy as the NLM method [18]–[22].

C. Selection of SMs

After k_{hp} and k_{hn} of phase h are obtained from (25), the capacitor voltages of the SMs in each arm are balanced by selecting the appropriate on-state SMs according to the direction of the arm current, known as the so-called "sorting method" [16], [20].

1) If the arm current is positive, the SMs with the lowest capacitor voltages are selected to be the on-state so that the capacitors of these SMs are charged.
2) If the arm current is negative, the SMs with the highest capacitor voltages are selected to be the on-state so that the capacitors of these SMs are discharged.

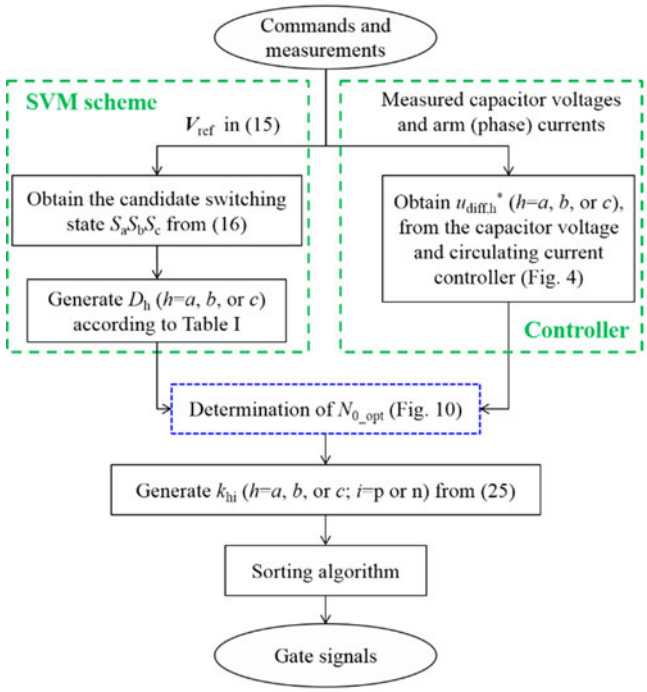

Fig. 8. Proposed SVM method for the MMC.

Fig. 8 illustrates the diagram of the proposed SVM method, which represents a general framework for implementing SVM-based control for the MMC. It can be conveniently extended for other control objectives, by replacing the capacitor voltage and circulating current control block with customized controllers. Note that though any redundant switching states determined by N_0 in (20) can be utilized to control the MMC, the control performances are not identical. The next section introduces a way to select the optimal N_0 (named N_{0_opt}) according to different control objectives.

IV. Optimized Control Strategy

For each redundant switching state $K_aK_bK_c$ generated in (20) by the SVM scheme, the number of on-state SMs for each arm of the MMC is given by (25). The MMC usually consists of a large number of SMs, so the number of redundant switching states is usually large, especially for small modulation indices [24], [25], [29]. This offers significant flexibility for optimizing the control performance. The objective is to find the optimal redundant switching state, i.e., the optimal N_0 in (20).

The capacitor voltages and circulating currents resulting from each redundant switching state are estimated first. Without the

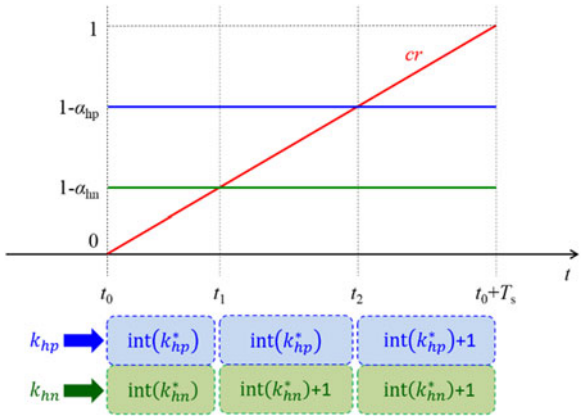

Fig. 9. Values of k_{hp} and k_{hn} during a switching cycle T_s.

loss of generality, Fig. 9 illustrates the values of k_{hp} and k_{hn} during a switching cycle when assuming $1-\alpha_{hp} > 1-\alpha_{hn}$, where α_{hp} and α_{hn} are obtained from (26) for k^*_{hp} and k^*_{hn}, respectively. The switching cycle is divided into three time intervals and during each interval, the values of k_{hp} and k_{hn} are constant. As an example, the estimation of the capacitor voltages and circulating currents is demonstrated for the first interval (from t_0 to t_1) as follows. The other two intervals can be analyzed in a similar way.

The capacitor voltages and circulating currents are sampled at the beginning (i.e., t_0) of each switching cycle. Based on (4), the circulating current of phase h at t_1 is estimated as

$$i_{\mathrm{cir},h}(t_1) = \left(\frac{V_{\mathrm{dc}} - u_{hp}(t_0) - u_{hn}(t_0)}{2} - R_0 \cdot i_{\mathrm{cir},h}(t_0)\right) \times \frac{\Delta t_0}{L_0} + i_{\mathrm{cir},h}(t_0) \tag{27a}$$

$$u_{hi}(t_0) = \sum_{k=1}^{n} \left(S_{hik}(t_0) \cdot v_{C,hik}(t_0)\right), \quad i = p \text{ or } n \tag{27b}$$

where $\Delta t_0 = t_1 - t_0 = (1-\alpha_{hn})T_s$; S_{hik} denotes the ON ($S_{hik}=1$) and OFF ($S_{hik}=0$) states of the kth SM in the upper (i = p) or lower arm (i = n) of phase h. Subsequently, the capacitor voltages of the kth SM in the upper and lower arms, respectively, of phase h at t_1 are estimated based on (3) as

$$v_{C,hpk}(t_1) = v_{C,hpk}(t_0) + S_{hpk}(t_0) \cdot \left(\frac{i_{\mathrm{cir},h}(t_0) + i_{\mathrm{cir},h}(t_1)}{2} + \frac{i_h}{2}\right)\frac{\Delta t_0}{C} \tag{28a}$$

$$v_{C,hnk}(t_1) = v_{C,hnk}(t_0) + S_{hnk}(t_0) \cdot \left(\frac{i_{\mathrm{cir},h}(t_0) + i_{\mathrm{cir},h}(t_1)}{2} - \frac{i_h}{2}\right)\frac{\Delta t_0}{C} \tag{28b}$$

where C is the capacitance of the SM capacitors; i_h is the output current of phase h sampled at t_0, and is considered as a constant during the switching cycle.

Repeating the process in (27) and (28) for the other two time intervals then gives the estimated capacitor voltages and circulating currents at the end (i.e., $t_0 + T_s$) of the switching cycle.

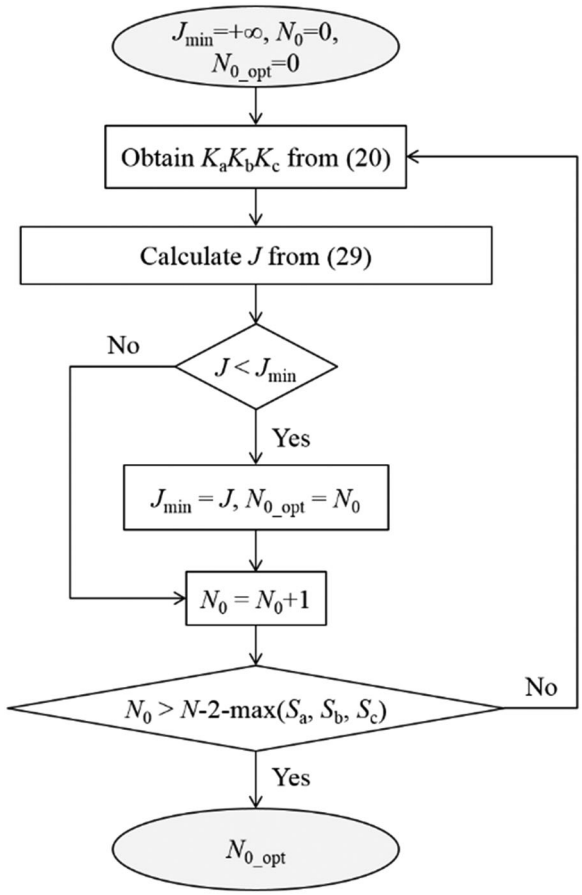

Fig. 10. Determination of N_{0_opt} (the optimal N_0).

To achieve the best capacitor voltage balancing, the optimal N_0 should minimize the following objective function:

$$J = \sum_{h=a,b,c} \left\{\left(v'_{C,hp} - V_{\mathrm{dc}}\right)^2 + \left(v'_{C,hn} - V_{\mathrm{dc}}\right)^2\right\} \tag{29a}$$

$$v'_{C,hp} = \sum_{k=1}^{n} v_{C,hpk}(t_0 + T_s) \tag{29b}$$

$$v'_{C,hn} = \sum_{k=1}^{n} v_{C,hnk}(t_0 + T_s) \tag{29c}$$

where $v'_{C,hp}$ and $v'_{C,hn}$ represent, respectively, the estimated total capacitor voltages in the upper and lower arms of phase h at $t_0 + T_s$. The optimal N_0 (i.e., N_{0_opt}) is, therefore, found by computing and comparing J for all the possible values of N_0, as shown in Fig. 10.

If the control objective is to optimally suppress the circulating currents, then an objective function can be defined as

$$J_2 = \sum_{h=a,b,c} \max\left(\left|i_{\mathrm{cir},h}(t_1) - I^*_{\mathrm{cir},h}\right|, \left|i_{\mathrm{cir},h}(t_2) - I^*_{\mathrm{cir},h}\right|, \left|i_{\mathrm{cir},h}(t_0 + T_s) - I^*_{\mathrm{cir},h}\right|\right) \tag{30}$$

where $\max(x, y, z)$ denotes the maximum value among x, y, and z; and $I^*_{\mathrm{cir},h}$ is the desired circulating current of phase h, typically defined according to the active power of the MMC

TABLE II
PARAMETERS OF THE MMC FOR THE SIMULATION

Parameter	Value
DC-link voltage ($V_{\rm dc}$)	12 kV
No. of SMs per arm (n)	4
SM capacitor reference voltage (v_C^*)	3 kV
SM capacitance (C)	1.41 mF
Arm inductance (L_0)	5 mH
Parasitic resistor in each arm (R_0)	13 mΩ
Carrier frequency (f_s)	5 kHz
Modulation index (M)	1.0 or 0.3
Voltage level number (N)	9
Load resistance (R_L) and inductance (L_L) per phase (Y-connected)	15 Ω + 10 mH
Fundamental frequency (f_0)	50 Hz
Simulation time step (Δt)	10 μs

TABLE III
CONTROL PARAMETERS FOR THE SIMULATION

Controller	Parameters
Averaging control	$k_{p1} = 100, k_{i1} = 10000$
Circulating current control	$k_{p2} = 20, k_{i2} = 400;$ $k_{r2} = 400;$ $k_{r4} = 300$
Arm-balancing control	$k_{p3} = 30, k_{i3} = 500$

[12], [23]. Applying J_2 to Fig. 10 generates the $N_{0\_\rm opt}$ for the optimal circulating current suppression.

Another typical control objective is to minimize common-mode voltages. Based on the estimated capacitor voltages, the instantaneous common-mode voltage can be calculated for any time instants and then evaluated similarly to (27)–(30). Alternatively, according to (21), the average common-mode voltage during a switching cycle is obtained as

$$V_{\rm com} = \frac{1}{3}\sum_{h=a,b,c}\left(\frac{(K_h + D_h)\,V_{\rm dc}}{N-1}\right). \tag{31}$$

Consequently, the $N_{0\_\rm opt}$ for an optimized common-mode voltage control is generated by applying the following objective function to Fig. 10:

$$J_3 = \left(V_{\rm com} - \frac{V_{\rm dc}}{2}\right)^2. \tag{32}$$

The rest of this paper focuses on optimizing the capacitor voltage balancing. Note that this paper only optimizes the selection of redundant switching states, for purposes of the optimal harmonic performance and simple implementation. If needed, the duty cycles d_{01} and d_{02} of the zero vectors can also be optimized to further improve the control performance [26].

V. SIMULATION RESULTS

Simulations are carried out to demonstrate the proposed SVM method, based on a three-phase MMC with the parameters shown in Table II. The control parameters (capacitor voltages are divided by the reference value before being sent to the controller) in Fig. 4 are presented in Table III.

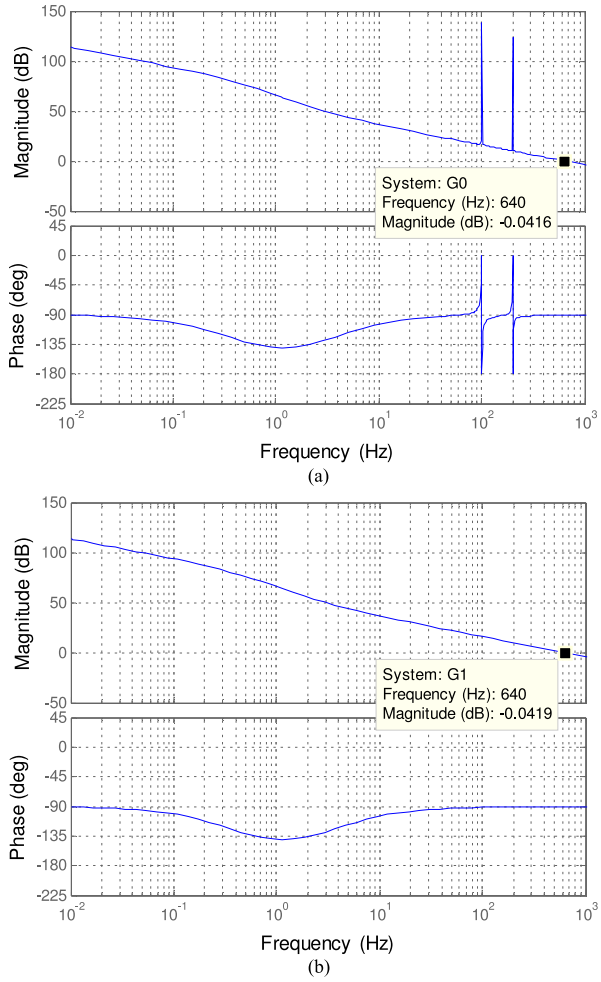

Fig. 11. Bode diagram of the circulating current controller for simulations: (a) With the resonant controllers; (b) without the resonant controllers.

Fig. 11(a) shows the Bode diagram of the open-loop transfer function in (14). The bandwidth of the controller is about 640 Hz, and the phase margin is around 90°. Fig. 11(b) shows the Bode diagram of the circulating current controller when the resonant controllers are unused (i.e., only applies the PI controller). It is observed that the resonant controllers have very narrow bandwidths. They only affect the harmonics around the resonant frequencies, as the two spikes shown in Fig. 11(a). Therefore, a general way to design the circulating current controller is selecting the PI control parameters first and then adding the resonant controllers.

A. Performance of the Capacitor Voltage Balancing and Circulating Current Suppression

For the sake of fair comparisons, the optimization of redundant switching states is not activated in this section, and

$$N_0 = \text{round}\left(\frac{N - 2 - \max(S_a, S_b, S_c)}{2}\right) \tag{33}$$

is adopted, where round(x) represents the nearest integer of x. The modulation index M is 1.0 in order to display all the voltage levels.

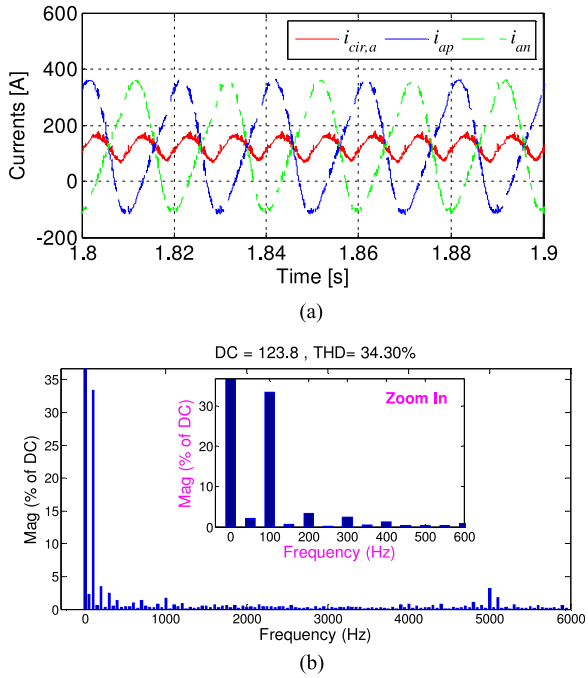

Fig. 12. Simulation results ($M = 1.0$) when the circulating current control only applies the PI controller: (a) Arm and circulating currents of phase a; (b) harmonic spectrum of the circulating current.

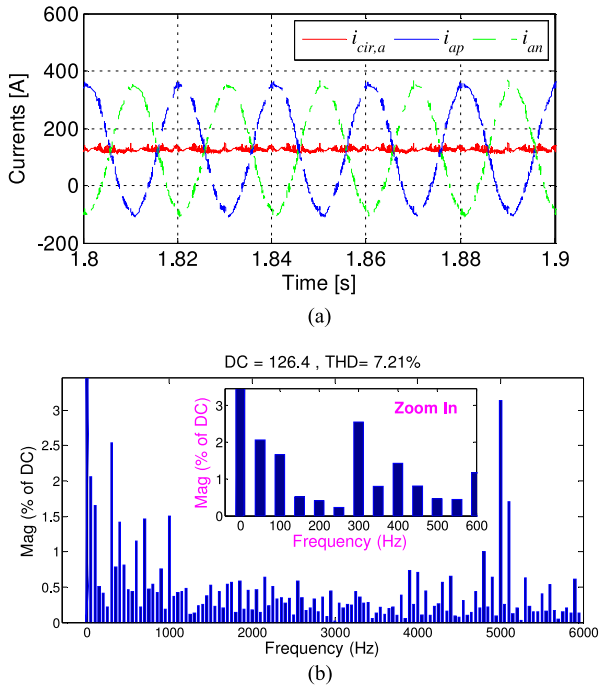

Fig. 13. Simulation results ($M = 1.0$) when the resonant controllers are added to the circulating current control: (a) Arm and circulating currents of phase a; (b) harmonic spectrum of the circulating current.

Theoretically, more resonant controllers lead to a better performance of the circulating current suppression, but increase the computational burden. This paper uses two resonant controllers ($k_{r2} = 400$ and $k_{r4} = 300$) for demonstration purposes. Fig. 12(a) shows the simulated arm and circulating currents of phase a, when the circulating current control in Fig. 4 only applies the PI controller. The harmonic spectrum of the circulating current appears in Fig. 12(b). It is observed that without the resonant controllers, the circulating current contains abundant harmonics, especially the second-order (100 Hz) harmonic component. When the resonant controllers are added, Fig. 13 shows the simulated arm and circulating currents of phase a, as well as the harmonic spectrum of the circulating current. Comparison with Fig. 12 demonstrates that the second- and fourth (200 Hz)-order harmonics of the circulating current are significantly suppressed. The total harmonic distortion of the circulating current is reduced from 34.3% to 7.21%. In the rest of this paper, the resonant controllers are always added.

Note that the circulating current contains a harmonic component at the carrier frequency (5 kHz), as shown in Figs. 12(b) and 13(b). This harmonic inherently results from the PWM operation and is determined by the buffer inductance. According to Fig. 9, the maximum variation of the circulating current during a switching cycle is estimated as follows:

$$\Delta\, i_{\mathrm{cir},h(\max)} = V_{\mathrm{dc}}\, T_s/(4nL_0) \tag{34}$$

which occurs when $\alpha_{hp} = \alpha_{hn} = 0.5$ in Fig. 9. This maximum variation of the circulating current should be taken into consideration when designing the buffer inductors.

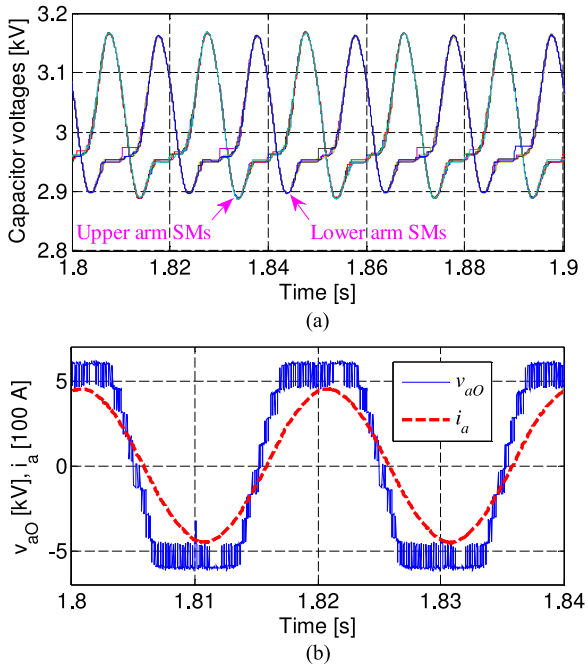

Fig. 14. Simulation results when $M = 1.0$: (a) SM capacitor voltages of phase a; (b) output voltage and current of phase a.

Fig. 14(a) illustrates the simulated SM capacitor voltages of phase a. All the capacitor voltages are regulated to the reference value. Fig. 14(b) shows the output voltage v_{aO} ($= v_{aN} - V_{\mathrm{dc}}/2$) and current of phase a, where the maximum level number ($N = 9$) of the output voltage is observed.

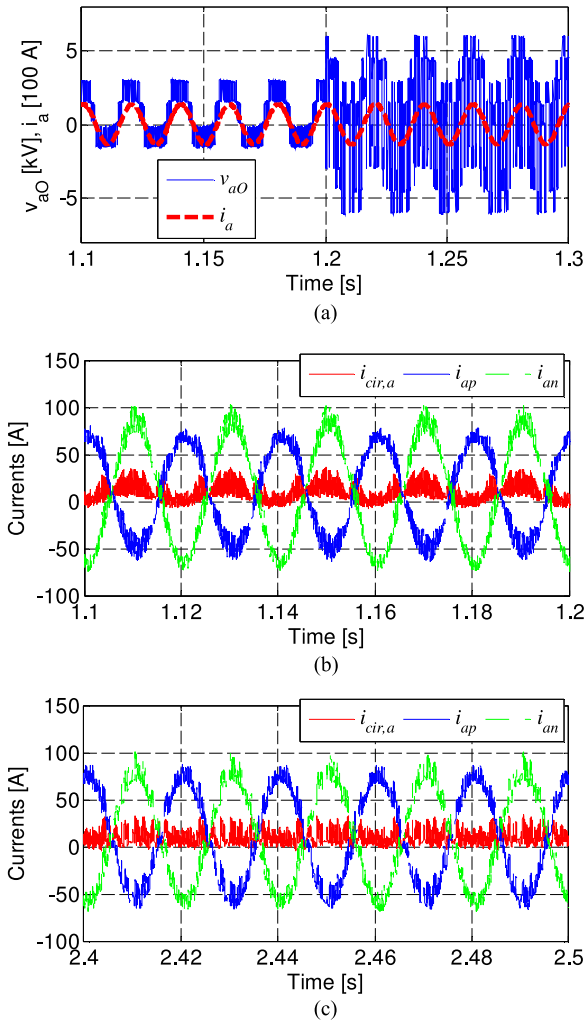

Fig. 15. Simulation results of phase a ($M = 0.3$) when the optimized control is activated at 1.2 s: (a) Output voltage and current; (b) arm and circulating currents without the optimized control; and (c) arm and circulating currents using the optimized control.

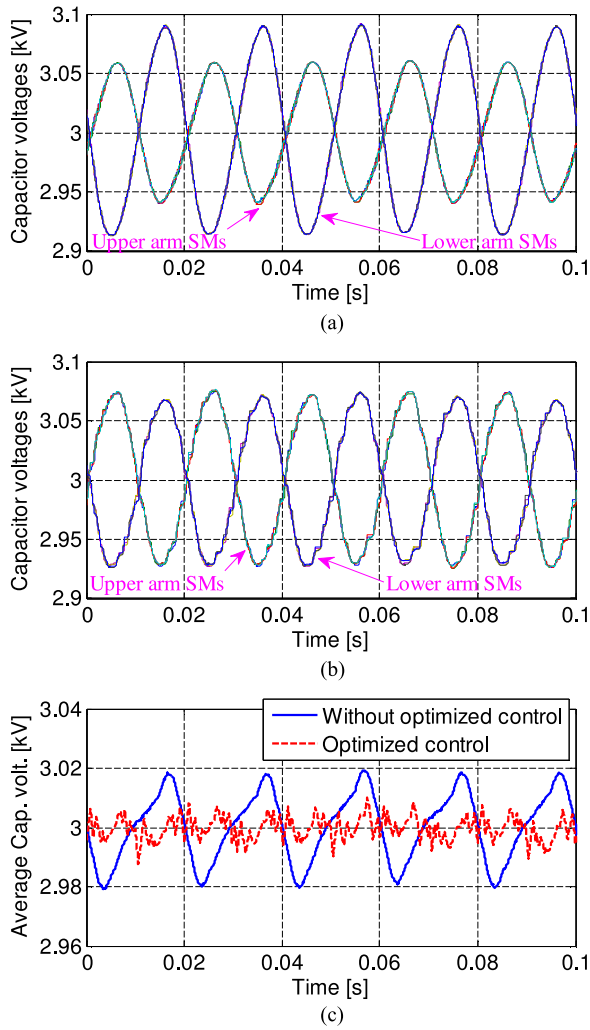

Fig. 16. Simulated capacitor voltages of phase a ($M = 0.3$) with and without the optimized control: (a) Without the optimized control; (b) using the optimized control; and (c) average capacitor voltages.

B. Optimized Capacitor Voltage Balancing

Fig. 15 presents the simulation results of phase a for a low modulation index ($M = 0.3$), where the N_0 in (33) is adopted before the optimized control is activated at 1.2 s. The output voltage in Fig. 15(a) shows that for a low modulation index, not all the available voltage levels are utilized if the redundant switching states are not optimally selected. The optimized control selects the optimal switching state among all the redundant ones, thus utilizing all the available voltage levels. Different redundant switching states generate identical line-to-line voltages, which are demonstrated by the output current in Fig. 15(a). Because for the low modulation index, the maximum variation (30 A) of the circulating current explained for (34) is comparable to the dc and fundamental-frequency components, distortion of the arm and circulating currents is observed in Fig. 15(b) and (c).

Accordingly, Fig. 16 shows the steady-state capacitor voltages of phase a, with and without the optimized control. The optimized control not only improves the capacitor voltage balancing between the upper and lower arms, but also forces the total capacitor energy of the entire phase to better follow its reference value.

Note that the optimized control inevitably adds computational burden because of searching for the optimal redundant switching states, though the maximum number of iterations required by Fig. 10 is only $N - 1$ (the lower the modulation index, the larger the number of redundant switching states). If computational resources are limited, then the optimized control can be deactivated and the following N_0 would be a good choice according to (32):

$$N_0 = \text{round}\left(\max\left(\frac{N-1}{2} - \frac{1}{3}\sum_{h=a,b,c}(S_h + D_h), 0\right)\right) \quad (35)$$

where $\max(x, y)$ represents the larger value between x and y. This N_0 leads to a good compromise among computational burden, common-mode voltage reduction, and capacitor voltage and circulating current control. In this case, the proposed

Fig. 17. Experimental setup.

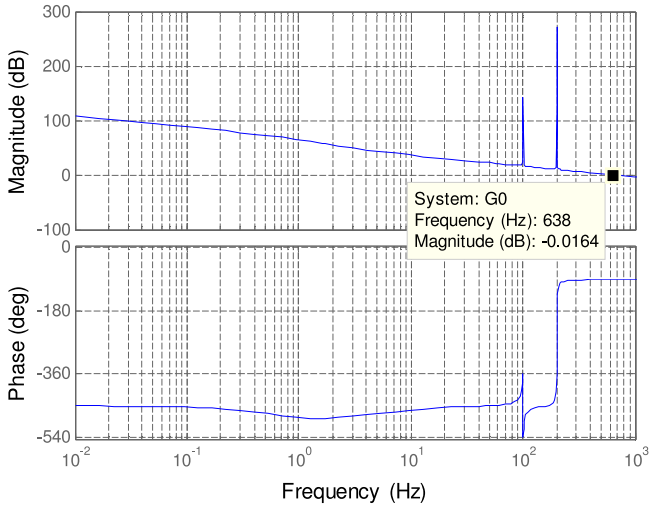

Fig. 18. Bode diagram of the circulating current controller for the experiment.

TABLE IV
PARAMETERS OF THE EXPERIMENTAL SETUP

Parameter	Value
DC-link voltage (V_{dc})	120 V
No. of SMs per arm (n)	4
SM capacitor reference voltage (v_C^*)	30 V
SM capacitance (C)	1.41 mF
Arm inductance (L_0)	2.5 mH
Parasitic resistor in each arm (R_0)	13 mΩ
Carrier frequency (f_s)	5 kHz
Modulation index (M)	0.4
Voltage level number (N)	9
Load resistance (R_L) and inductance (L_L) per phase (Y-connected)	15 Ω + 10 mH
Fundamental frequency (f_0)	50 Hz
OPAL-RT time step (Δt)	20 μs

TABLE V
CONTROL PARAMETERS FOR THE EXPERIMENT

Controller	Parameters
Averaging control	$k_{p1} = 10, k_{i1} = 120$
Circulating current control	$k_{p2} = 10, k_{i2} = 200;$ $k_{r2} = 400;$ $k_{r4} = 300$
Arm-balancing control	$k_{p3} = 30, k_{i3} = 500$

SVM-based control method is as computationally efficient as the NLM-based method.

VI. EXPERIMENTAL RESULTS

The proposed SVM method is also tested based on the experimental setup of a three-phase MMC shown in Fig. 17, according to the operating conditions summarized in Table IV and the control parameters presented in Table V. Fig. 18 depicts the corresponding Bode diagram of the circulating current controller. The bandwidth of the controller is about 640 Hz, and the phase margin is around 90°.

A dc power supply maintains a 120-V dc-link voltage for the MMC. A real-time simulator OPAL-RT [32] is used to implement the proposed SVM method in real time and to generate the gate signals for the MMC's power switches. The OPAL-RT interfaces (receives commands and sends real-time results) with a command station (laptop) via TCP/IP protocol. For the experimental results presented later, the SM capacitor voltages directly use the data sampled by the OPAL-RT (filtered by a second-order filter with a cutoff frequency of 1200 Hz and a quality factor of 0.707) from the voltage sensors, while the other measured results are recorded through an oscilloscope. The bandwidth of the oscilloscope probes is 40 kHz.

Fig. 19 shows the measured output voltage, arm currents, output current, and SM capacitor voltages of one phase (e.g., phase c), when the optimization of redundant switching states is not activated and (33) is adopted. As previously explained, the output voltage does not utilize all the available voltage levels, for the low modulation index ($M = 0.4$) test condition. The maximum ripple (peak-to-peak) of the SM capacitor voltages reaches 3 V (10% of the reference capacitor voltage).

The corresponding experimental results, when the optimized control is applied, are shown in Fig. 20. Significantly different from the voltage waveform in Fig. 19(a), now the output voltage contains all the available voltage levels. The maximum ripple of the SM capacitor voltages is reduced to 2.3 V (i.e., 23.3% of the original maximum ripple is further reduced) because of the optimized control. To more evidently compare the performance of the two control strategies, Fig. 21 illustrates the instantaneous maximum and minimum values among all the measured capacitor voltages in Figs. 19 and 20, respectively. It is also shown that the optimized control causes the capacitor voltages to better follow the reference value.

Comparing Figs. 19 and 20 also indicate that though the output phase currents are close, the optimized capacitor voltage control causes slightly more distortion of the arm currents. This is expected since in (29) the circulating currents are not taken into consideration. As a result, the generated optimal redundant switching states may lead to larger variations of the difference

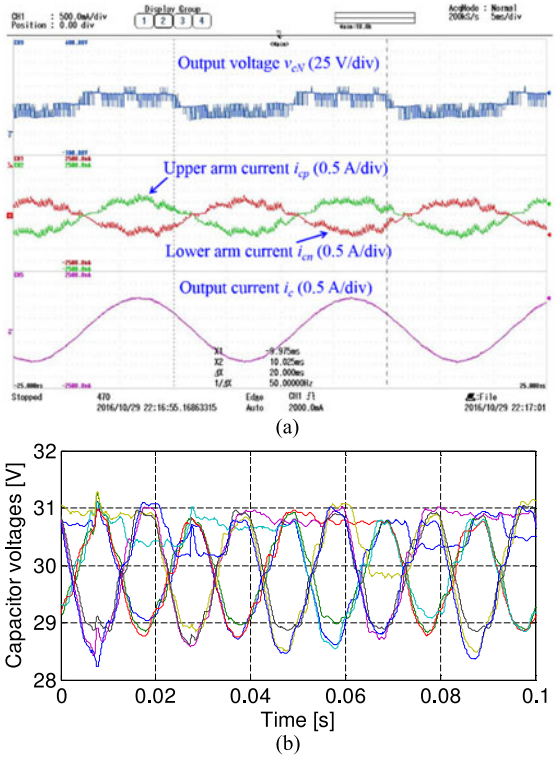

Fig. 19. Experimental results when the optimized control is not applied: (a) Output voltage, arm currents, and output current of phase c; (b) SM capacitor voltages of phase c.

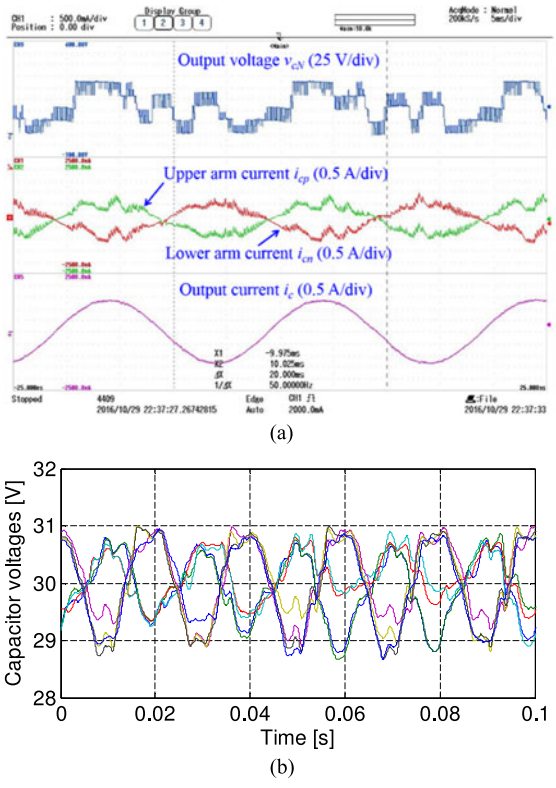

Fig. 20. Experimental results based on the optimized control: (a) Output voltage, arm currents, and output current of phase c; (b) SM capacitor voltages of phase c.

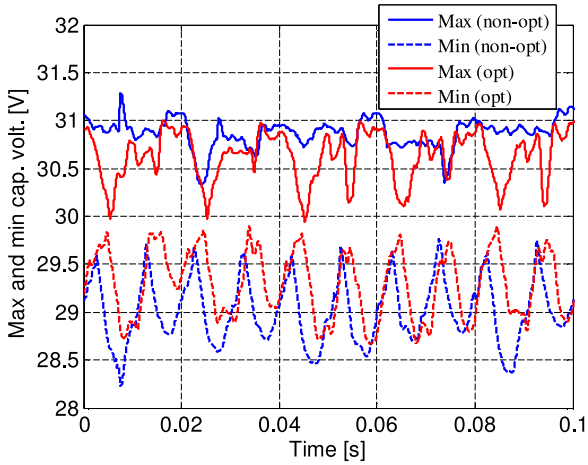

Fig. 21. Measured instantaneous maximum and minimum capacitor voltages among all the capacitors of phase c, with and without the optimized control.

voltages, and, consequently, that of the circulating currents and arm currents. A new objective function combining (29) and (30) can be adopted if the capacitor voltages and circulating currents need to be optimized at the same time.

VII. Conclusion

This paper proposes a general SVM method for the MMC. An optimized control strategy for capacitor voltage balancing, circulating current suppression, or common-mode voltage reduction is presented as well, by utilizing the redundant switching states offered by the SVM scheme. Compared with earlier modulation methods for the MMC, this proposed new SVM method generates the maximum level number (i.e., $2n + 1$, where n is the number of SMs in the upper or lower arm of each phase) of the output phase voltages, based on a new equivalent circuit of the MMC. Since the computational burden of the SVM scheme is independent of the voltage level number, the proposed new method is well suited to the MMC with a large number of SMs. Simulation and experimental results, for a three-phase MMC with four SMs in each arm, verify the proposed new method.

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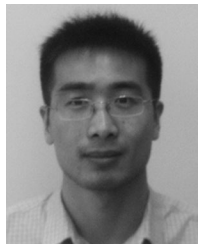

Yi Deng (S'12–M'16) received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2008 and 2010, respectively, and the Ph.D. degree in electrical engineering from Georgia Institute of Technology, Atlanta, GA, USA, in 2016.

He was with Mitsubishi Electric Research Laboratories, Cambridge, MA, USA, in 2012 and 2013, respectively. He was with ABB U.S. Corporate Research Center, Raleigh, NC, USA, in 2015–2017. He is currently with GalaTech Inc., San Jose, CA, USA. His research interests include power electronics (especially in medium-voltage and high-power areas), electric machines and their drive systems, electric vehicles, renewable energy grid integration, FACTS devices, and power system control and operation.

Yebin Wang (S'06–M'10–SM'16) received the B.Eng. degree in mechatronics engineering from Zhejiang University, Hangzhou, Zhejiang, China, in 1997, the M.Eng. degree in control theory and engineering from Tsinghua University, Beijing, China, in 2001, and the Ph.D. degree in electrical engineering from the University of Alberta, Edmonton, AB, Canada, in 2008.

From 2001 to 2003, he was a Software Engineer, Project Manager, and R&D Manager in industries, Beijing. Since 2009, he has been with Mitsubishi Electric Research Laboratories, Cambridge, MA, USA, where he is currently a Principal Member Research Staff. His research interests include nonlinear control and estimation, optimal control, adaptive systems, and their applications, including mechatronic systems.

Koon Hoo Teo (M'06) received the M.S. and Ph.D. degrees in electrical engineering from the University of Alberta, Edmonton, AB, Canada, in 1985 and 1990, respectively.

He was with Nortel Networks for about 15 years, where his main research focuses on wireless communication. He is currently with Mitsubishi Electric Research Labs, Cambridge, MA, USA. He is the author and coauthor of 60 papers, more than 110 granted patents and patent applications. His research interests include simulation and characterization of metamaterial, power amplifier, and power devices and their applications to the energy and communication space.

Dr. Teo received the Nortel Innovation Award.

Maryam Saeedifard (SM'11) received the B.S. and M.S. degrees in electrical engineering from Isfahan University of Technology, Isfahan, Iran, in 1998 and 2002, respectively, and the Ph.D. degree in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2008.

From 2007 to 2008, she was with ABB Corporate Research Center, Dattwil-Baden, Switzerland, working in the power electronic systems group. She joined Purdue University in January 2010, where she served as an Assistant Professor with the School of Electrical and Computer Engineering. Since January 2014, she has been with the ECE Faculty, Georgia Institute of Technology, Atlanta, GA, USA. Her main research interests include power electronics and applications of power electronics in power systems and transportation systems.

Dr. Saeedifard has served on the technical program committees of the IEEE Power Electronics Society, the *IEEE Applied Power Electronics Conference and Exposition*, and the *IEEE Industrial Electronics Conference*. She is an Editor for the IEEE TRANSACTIONS ON SUSTAINABLE ENERGY, the IEEE TRANSACTIONS ON POWER DELIVERY, and the IEEE TRANSACTIONS ON POWER ELECTRONICS.

Ronald G. Harley (M'77–SM'86–F'92–LF'09) received the M.Sc.Eng. degree (*cum laude*) in electrical engineering from the University of Pretoria, Pretoria, South Africa, in 1965, and the Ph.D. degree from the University of London, London, U.K., in 1969.

He is currently a Regents' Professor with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, USA, and also a Professor Emeritus with the School of Engineering, University of KwaZulu-Natal, Durban, South Africa. He has coauthored more than 500 papers in refereed journals and international conference proceedings and holds six patents. His research interests include dynamic behavior of electric machines, power systems and their components, and controlling them by the use of power electronics and intelligent control algorithms.

Dr. Harley received the Cyril Veinott Electromechanical Energy Conversion Award from the IEEE Power Engineering Society for "outstanding contributions to the field of electromechanical energy conversion" in 2005 and the IEEE Richard H. Kaufmann Field Award with the citation "for contributions to monitoring, control, and optimization of electrical processes including electrical machines and power networks" in 2009.