Imbalance Mechanism and Balanced Control of Capacitor Voltage for a Hybrid Modular Multilevel Converter

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***Abstract*—Due to different charging and discharging characteristics of full-bridge submodules and half-bridge submodules in hybrid modular multilevel converters (MMC), capacitor voltage imbalance will occur under boosted ac voltage or reduced dc voltage conditions. To address this issue, the mechanism of capacitor voltage imbalance is carefully studied, with three main factors—modulation index, power angle, and hybridization ratio—summarized and their effect on capacitor voltage imbalance analyzed. Further, a control strategy based on fundamental frequency reactive circulating current injection is proposed to keep the capacitor voltage balanced in the hybrid MMC. The amplitude and phase angle of the injected circulating current are calculated and their influence on the energy fluctuation in the submodules' capacitors and the semiconductors' current stress is explored. Experimental results under boosted ac voltage and reduced dc voltage conditions demonstrate the feasibility and validity of the proposed scheme.**

***Index Terms*—Capacitor voltage balance, fault ride-through, fundamental frequency reactive circulating current (FFRCC), hybrid modular multilevel converter (MMC), high voltage dc (HVDC).**

I. Introduction

MODULAR multilevel converters (MMC), first proposed in [1], are the most attractive topology for high-power, high-voltage applications [2], [3]. In a MMC-based high-voltage dc (HVDC) system, the capability to handle dc short-circuit faults is one of the main challenges, especially for overhead line transmissions. In terms of potential dc fault management schemes, using MMCs with dc short-circuit fault ride-through (DC-FRT) capability has become a promising method [4]–[10], because it can not only control ac grid-side reactive power during the fault period [11]–[13], but also maintain half-active power transmission capability under pole-to-ground (PTG) fault conditions [14], [15]. Among various topologies for MMC with DC-FRT capability [5]–[7], [9], [10], [16], [17], hybrid MMC containing half half-bridge submodules (HBSMs) and half full-bridge submodules (FBSMs) is a promising candidate in terms of cost, efficiency, and insulated-gate bipolar transistor (IGBT) series operation.

To further increase power device utilization, hybrid MMCs can also operate with a higher ac output voltage for a given dc voltage limit by increasing the number of FBSMs in a phase leg [10], [18]. In addition, hybrid MMC-based HVDC systems can operate at a reduced dc-link voltage to avoid flashovers under extreme atmospheric conditions. Thus, operation of hybrid MMCs can be divided into three scenarios: normal operations (i.e., HBSMs-based MMCs), boosted ac output voltage operations, and reduced dc-link voltage operations. For normal operation, the behavior of the FBSMs is identical to that of the HBSMs. For the other two operating scenarios, FBSMs are required to output a negative voltage; thus, the FBSMs and HBSMs in a hybrid MMC function differently during the charging and discharging periods, which may cause problems due to capacitor voltage imbalance. For example, the FBSMs can charge or discharge regardless of the direction of the arm current, while the HBSMs can only charge during the positive period of the arm current and discharge during the negative period. Under certain operational conditions, when the net energy flowing through the HBSMs is not zero in a fundamental frequency period, the capacitor voltage of the HBSMs will continue increasing (decreasing), while the capacitor voltage of the FBSMs will correspondingly continue decreasing (increasing) after the fundamental frequency period, creating an imbalance [10]. As a result, overcharging these capacitors may cause their failure or accelerated fatigue, with cascading effects on all the other components. Moreover, running the capacitors undercharged reduces the maximum voltage capability of the arm, leading to instability of the whole converter because of a loss in control of the arm currents.

A few studies have developed methods to address the issue of capacitor voltage imbalance, including injecting reactive power, increasing the number of FBSMs, and retrofitting the topology of the hybrid MMC. In [10], reactive power was used to generate a sufficient charging or discharging interval for the HBSMs, but decreased the power factor. Increasing the number of FBSMs

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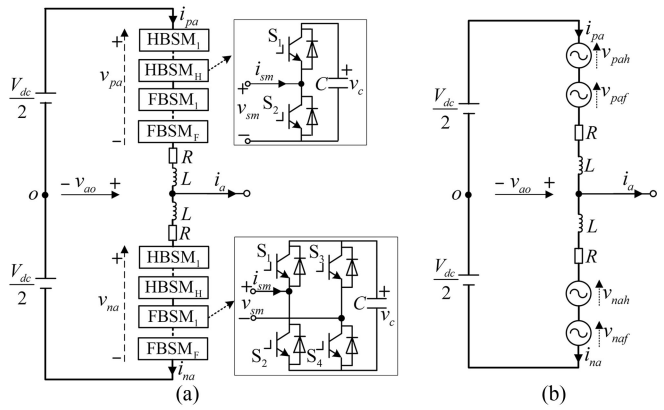

Fig. 1. Basic structure of one leg of the hybrid MMC: (a) physical circuit and (b) equivalent circuit.

in a phase leg was suggested to ensure that only the FBSMs were inserted to generate the required arm output voltage [18]. However, this approach increased the device cost and power loss of the converter. An asymmetric mixed MMC was proposed in [19], in which the upper arm consisted of HBSMs and the lower arm of FBSMs. Although the converter could maintain capacitor voltage balance during symmetric reduced dc-link voltages caused by a pole-to-pole dc fault, the topology could not handle asymmetric reduced dc-link voltages caused by a flexible PTG dc fault or a boosted ac output voltage (i.e., $m > 1$).

This paper analyzes the mechanism of capacitor voltage imbalance for a hybrid MMC, studying the effect of three factors (modulation index, power angle, and hybridization ratio). Based on these analyses, a circulating current injection based on an fundamental frequency reactive circulating current (FFRCC) is proposed to keep the capacitor voltage balanced. Compared with existing solutions, this method does not affect the performance of the hybrid MMC. The remainder of this paper is organized as follows. In Section II, the operating principle of a hybrid MMC is briefly introduced, while the mechanism and three main factors of capacitor voltage imbalance are analyzed and summarized in Section III. In Section IV, the principles of the FFRCC injection method are presented, and the relevant experimental results are provided in Section V. Finally, Section VI draws some conclusions.

II. Operating Principle of a Hybrid MMC

Fig. 1(a) depicts one leg of the symmetric hybrid MMC proposed in [9] and [10], where each arm consists of *N* submodules (SM), i.e., *H* HBSMs and *F* FBSMs. In the figure, $V_{\rm dc}$ is the rated dc-link voltage, *L* is the arm inductor, *C* and v_c are the capacitor and its voltage in each SM, respectively, $v_{\rm pa}$ and $v_{\rm na}$ are the total voltages generated by all the SMs in the upper and lower arms, respectively, $i_{\rm pa}$ and $i_{\rm na}$ are the arm currents in the upper and lower arms, respectively, and i_a is the output ac phase current. Fig. 1(b) shows the equivalent circuit of one leg of the hybrid MMC, where the HBSMs and FBSMs are modeled as two voltage sources.

Taking phase A as an example, arm currents $i_{\rm pa}$ and $i_{\rm na}$ can be expressed as follows:

$$\begin{cases} i_{\rm pa} = i_a/2 + i_{\rm cira} \\ i_{\rm na} = -i_a/2 + i_{\rm cira} \end{cases} \tag{1}$$

where $i_{\rm cira}$ is the circulating current flowing in phase A, and should be one third of the dc-side current at steady state for a three-phase system when the higher order (i.e., greater than 1) harmonic circulating currents are properly suppressed.

According to Kirchhoff's voltage law, the following equations can be derived from Fig. 1:

$$\begin{cases} v_{\rm pa} = V_{\rm dc}/2 - v_{\rm ao} - (L\, di_{\rm pa}/dt + Ri_{\rm pa}) \\ v_{\rm na} = V_{\rm dc}/2 + v_{\rm ao} - (L\, di_{\rm na}/dt + Ri_{\rm na})\,. \end{cases} \tag{2}$$

Combining (1) and (2) yields

$$\begin{cases} v_{\rm pa} = V_{\rm dc}/2 - e_a - (L\, di_{\rm cira}/dt + Ri_{\rm cira}) \\ v_{\rm na} = V_{\rm dc}/2 + e_a - (L\, di_{\rm cira}/dt + Ri_{\rm cira}) \end{cases} \tag{3}$$

where e_a is the differential mode component of the lower and upper arm output voltages of phase A, and can be expressed as follows:

$$e_a = v_{\rm ao} + Ldi_a/(2dt) + Ri_a/2. \tag{4}$$

Due to the negative voltage output capability of the FBSMs, each arm can output a negative arm voltage. Thus, the amplitude of e_a (i.e., E_m) can be larger than $V_{\rm dc}/2$, such that the hybrid MMC can provide boosted ac voltage operation or reduced dc-link voltage operation. To satisfy the arm output voltage requirement under these operating conditions, the number of FBSMs *F* and the number of HBSMs *H* should meet the following conditions [10], [18], [20]:

$$\begin{cases} (H+F)V_c \geq v_{\rm arm,max} \\ FV_c \geq |v_{\rm arm,min}| \end{cases} \tag{5}$$

where V_c is the rated SM capacitor voltage, and $v_{\rm arm,max}$ and $v_{\rm arm,min}$ are the maximum and minimum values of the required arm output voltage, respectively. The voltage $v_{\rm arm,max}$ primarily depends on the normal operation requirements, while $v_{\rm arm,min}$ mainly depends on the minimum required dc voltage. If the minimum required dc voltage is zero, $v_{\rm arm,max}$ and $v_{\rm arm,min}$ can be expressed as follows [10], [20]:

$$\begin{cases} v_{\rm arm,max} = (1+m)\, V_{\rm dc}/2 \\ v_{\rm arm,min} = -mV_{\rm dc}/2 \end{cases} \tag{6}$$

where *m* is the modulation index defined as $2E_m/V_{\rm dc}$.

III. Mechanism of Capacitor Voltage Imbalance

When hybrid MMCs operate under boosted ac voltage or reduced dc-link voltage conditions, the FBSMs are required to output a negative voltage. To maintain capacitor voltage balance, the HBSMs and the FBSMs must exchange energy when the required output voltage is positive. The interval for energy

exchange is determined by modified sorting and selection algorithms, where capacitor voltages of the FBSMs and HBSMs should be sorted and selected together when the arm output voltage is positive, and only FBSMs are inserted when the arm output voltage is negative [18]–[20]. However, due to the obviously different charging and discharging behaviors of FBSMs and HBSMs, only using the modified sorting and selection algorithms cannot guarantee the capacitor voltage balance. To analyze this potential issue, a detailed analysis of the charging and discharging of HBSM and FBSM capacitors in a fundamental frequency period will be conducted in this section, with the following four assumptions:

1) any redundant design for the SMs is neglected;
2) the aforementioned modified sorting and selection algorithm is adopted;
3) power losses on the SMs are neglected;
4) all HBSMs (FBSMs) are identical and assumed to be instantaneous voltage balancing; thus, analysis of all capacitor voltage balancing can be simplified to the analysis of the HBSMs and FBSMs.

Further, following the previous analysis, three main factors affecting capacitor voltage imbalance are summarized and analyzed quantitatively.

A. Charging and Discharging of FBSMs and HBSMs

Assuming the converter works as an inverter, the arm output voltage and arm current of the upper arm in phase A can be expressed as follows:

$$\begin{cases} v_{\mathrm{pa}} = (1 - m\,\sin\omega_1 t)\,V_{\mathrm{dc}}/2 \\ i_{\mathrm{pa}} = [m\,\cos\varphi/2 + \sin(\omega_1 t - \varphi)]\,I_m/2 \end{cases} \tag{7}$$

where m is the modulation index defined as $2E_m/V_{\mathrm{dc}}$ and φ is the difference between the phase angles of e_a and i_a. In an HBSM-based MMC, m should be less than 1.0, while in a hybrid- or FBSM-based MMC m can be larger than 1.0.

The instantaneous power flowing through the upper arm of phase A can be determined by

$$p_{\mathrm{pa}} = \frac{V_{\mathrm{dc}} I_m}{8}\left[2\,\sin(\omega_1 t - \varphi) - m^2\,\sin\omega_1 t\,\cos\varphi + m\,\cos(2\omega_1 t - \varphi)\right] \tag{8}$$

and the energy absorbed by all arm capacitors can be expressed as follows:

$$W_{\mathrm{pa}} = \frac{V_{\mathrm{dc}} I_m}{16\omega_1}\left[-4\,\cos(\omega_1 t - \varphi) + 2m^2\,\cos\omega_1 t\,\cos\varphi + m\,\sin(2\omega_1 t - \varphi)\right]. \tag{9}$$

Note that the net energy absorbed in one fundamental period is zero. For a HBSM-based MMC or FBSM-based MMC, the behavior of all SMs during charging and discharging are identical, so providing an even energy distribution into each SM can keep the capacitor voltage balanced. For a hybrid MMC, the FBSMs and HBSMs work with different charging and discharging intervals. Thus, merely ensuring the prerequisite of zero net energy absorbed in one fundamental period cannot keep the capacitor voltage balanced.

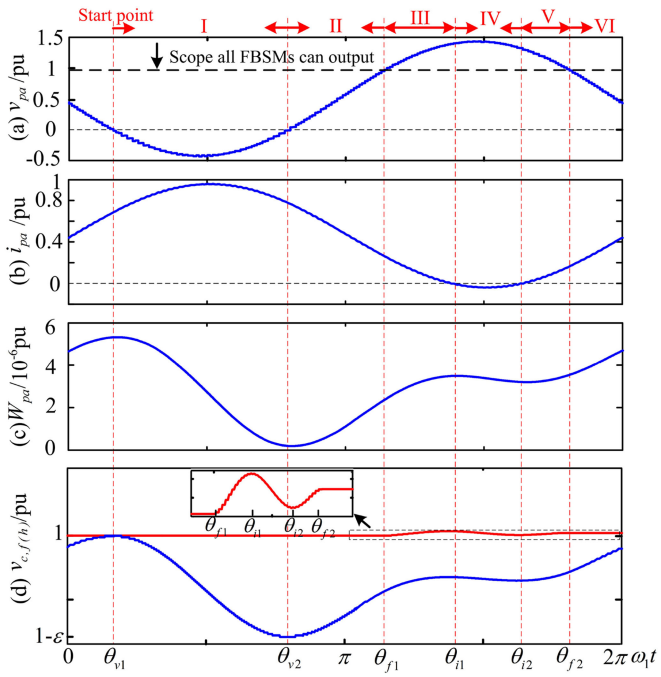

Fig. 2. Qualitative analysis of the capacitor voltage imbalance problem (in p.u.): (a) arm output voltage, (b) arm current, (c) energy absorbed by the capacitors, and (d) capacitor voltages.

Fig. 2 shows the normalized arm output voltage, arm current, transferred energy, and capacitor voltages of a hybrid MMC. In the figure, θ_{v1} and θ_{v2} are the zero crossings of the arm output voltage, θ_{i1} and θ_{i2} are the zero crossings of the arm current, and θ_{f1} and θ_{f2} are the points where the arm voltage equals the maximum voltage the FBSMs can generate. These values can be written as follows:

$$\begin{cases} \theta_{v1} = \arcsin(1/m); & m \geq 1 \\ \theta_{v2} = \pi - \arcsin(1/m); & m \geq 1 \\ \theta_{i1} = \pi + \arcsin(m\,\cos\varphi/2) + \varphi; & 1 \leq m \leq 2/\cos\varphi \\ \theta_{i2} = 2\pi - \arcsin(m\,\cos\varphi/2) + \varphi; & 1 \leq m \leq 2/\cos\varphi \\ \theta_{f1} = \pi + \arcsin[(2FV_c/V_{\mathrm{dc}} - 1)/m]; & m \geq 1 \\ \theta_{f2} = 2\pi - \arcsin[(2FV_c/V_{\mathrm{dc}} - 1)/m]; & m \geq 1. \end{cases} \tag{10}$$

As shown in Fig. 2, a fundamental period is divided into six stages. Taking θ_{v1} as the starting point and assuming the capacitor voltages of the HBSMs and FBSMs are identical at the point θ_{v1} yields

$$v_{c,f}(\theta_{v1}) = v_{c,h}(\theta_{v1}) = V_c \tag{11}$$

where $v_{c,f}$ and $v_{c,h}$ represent the capacitor voltages of the FBSMs and HBSMs, respectively.

The criterion for capacitor voltage balance is whether the capacitor voltages of the HBSMs and FBSMs are again identical

at the end of one fundamental period, expressed as follows:

$$v_{c,f}(2\pi+\theta_{v1}) = v_{c,h}(2\pi+\theta_{v1}). \tag{12}$$

1) Stage I ($\theta_{v1} \le \omega_1 t \le \theta_{v2}$): In stage I, the arm voltage $v_{\rm pa}$ is negative and the arm current $i_{\rm pa}$ is positive. The FBSMs are discharged and the HBSMs are bypassed, and the capacitor voltages can be expressed as follows:

$$\begin{cases} v_{c,f}(\theta_{v2}) = \sqrt{V_c^2 + 2\int_{\theta_{v1}}^{\theta_{v2}} p_{\rm pa} d\omega_1 t/FC} \\ v_{c,h}(\theta_{v2}) = V_c. \end{cases} \tag{13}$$

2) Stage II ($\theta_{v2} \le \omega_1 t \le \theta_{f1}$): In stage II, both the arm voltage $v_{\rm pa}$ and arm current $i_{\rm pa}$ are positive; thus, the inserted SM would be charged. Since the FBSMs were discharged in the previous stage, the FBSMs have priority to be charged. When the arm voltage reaches the maximum voltage that the FBSMs can generate (i.e., the point θ_{f1} shown in Fig. 2), the HBSMs will be inserted. The capacitor voltages can be deduced using

$$\begin{cases} v_{c,f}(\theta_{f1}) = \sqrt{V_c^2 + 2\int_{\theta_{v1}}^{\theta_{f1}} p_{\rm pa} d\omega_1 t/FC} \\ v_{c,h}(\theta_{f1}) = V_c. \end{cases} \tag{14}$$

3) Stage III ($\theta_{f1} \le \omega_1 t \le \theta_{i1}$): During this stage, the HBSMs to be charged are inserted, and $v_{c,f}$ and $v_{c,h}$ can be expressed as follows:

$$\begin{cases} v_{c,f}(\omega_1 t) = \sqrt{v_{c,f}^2(\theta_{f1}) + 2\int_{\theta_{f1}}^{\theta} n_f v_{c,f} i_{\rm pa} d\omega_1 t/FC} \\ v_{c,h}(\omega_1 t) = \sqrt{V_c^2 + 2\int_{\theta_{f1}}^{\theta} n_h v_{c,h} i_{\rm pa} d\omega_1 t/HC} \end{cases} \tag{15}$$

where n_f and n_h are the number of inserted FBSMs and HBSMs, respectively, and are related to $v_{c,f}$ and $v_{c,h}$. If $v_{c,f}$ is smaller than $v_{c,h}$, all FBSMs (i.e., *F* FBSMs) are inserted, and the number of inserted HBSMs is derived from the remaining arm voltage; on the other hand, if $v_{c,f}$ is equal to $v_{c,h}$, both FBSMs and HBSMs have an equal chance to be inserted, and n_f should be proportional to *F/N*. Thus, n_f and n_h can be expressed as follows:

$$\begin{cases} n_f = F \\ n_h = {\rm round}(v_{\rm pa}/V_c) - F \end{cases}; \quad v_{c,f} < v_{c,h} \tag{16.a}$$

$$\begin{cases} n_f = {\rm round}(Fv_{\rm pa}/NV_c) \\ n_h = {\rm round}(v_{\rm pa}/V_c) - n_f \end{cases}; \quad v_{c,f} = v_{c,h}. \tag{16.b}$$

Since the arm voltage is positive during $[\theta_{f1}, 2\pi + \theta_{v1}]$, the charging and discharging behaviors of the FBSMs and HBSMs are identical. Thus, capacitor voltage imbalance [i.e., $v_{c,f}\,(2\pi + \theta_{v1}) \ne v_{c,h}\,(2\pi + \theta_{v1})$] will not occur once $v_{c,h}\,(\theta_{i1})$ equals $v_{c,f}\,(\theta_{i1})$, and an imbalance may only occur if $v_{c,f}\,(\theta_{i1})$ and $v_{c,h}\,(\theta_{i1})$ satisfy

$$v_{c,f}(\theta_{i1}) < v_{c,h}(\theta_{i1}). \tag{17}$$

When (17) is satisfied, the voltage generated by the HBSMs can be expressed as $v_{\rm pa} - Fv_{c,f}$ according to (16.a), and the net energy stored in the HBSMs during stages I–III can be expressed as follows:

$$\Delta W_{h,{\rm increase1}} = \int_{\theta_{f1}}^{\theta_{i1}} (v_{\rm pa} - Fv_{c,f}) i_{\rm pa} d\omega_1 t. \tag{18}$$

4) Stage IV ($\theta_{i1} \le \omega_1 t \le \theta_{i2}$): In this stage, the arm voltage $v_{\rm pa}$ is positive and the arm current $i_{\rm pa}$ is negative, so the HBSMs can be discharged. The discharged energy from the HBSMs can be expressed as follows:

$$\Delta W_{h,{\rm decrease}} = -\int_{\theta_{i1}}^{\theta_{i2}} n_h v_{c,h} i_{\rm pa} d\omega_1 t \tag{19}$$

where n_h is the number of inserted HBSMs, $0 \le n_h \le H$.

Similar to the analysis in stage III, n_h can be expressed as follows:

$$\begin{cases} n_h = H; & v_{c,f} < v_{c,h} \\ n_h = {\rm round}(Hv_{\rm pa}/NV_c); & v_{c,f} = v_{c,h}. \end{cases} \tag{20}$$

Capacitor voltage imbalance will not occur once $v_{c,h}\,(\theta_{i2})$ equals $v_{c,f}\,(\theta_{i2})$, and an imbalance may only occur if $v_{c,f}\,(\theta_{i2})$ and $v_{c,h}(\theta_{i2})$ satisfy

$$v_{c,f}(\theta_{i2}) < v_{c,h}(\theta_{i2}). \tag{21}$$

Under this condition, $\Delta W_{h,{\rm decrease}}$ can be expressed as follows:

$$\Delta W_{h,{\rm decrease}} = -\int_{\theta_{i1}}^{\theta_{i2}} Hv_{c,h} i_{\rm pa} d\omega_1 t. \tag{22}$$

5) Stage V ($\theta_{i2} \le \omega_1 t \le \theta_{f2}$): In stage V, both the arm voltage $v_{\rm pa}$ and arm current $i_{\rm pa}$ are positive, and any inserted SMs will be charged.

When (21) is satisfied, FBSMs have charging priority. However, since the arm output voltage reference is larger than the maximum voltage that all the FBSMs can generate, HBSMs will be inserted. The energy charged by all of the inserted HBSMs can be expressed as follows:

$$\Delta W_{h,{\rm increase2}} = \int_{\theta_{i2}}^{\theta_{f2}} n_h v_{c,h} i_{\rm pa} d\omega_1 t. \tag{23}$$

Similar to the analyses in stages III and IV, a capacitor voltage imbalance will not occur once $v_{c,h}(\theta_{f2})$ equals $v_{c,f}\,(\theta_{f2})$, and an imbalance may only occur if $v_{c,f}\,(\theta_{f2})$ and $v_{c,h}(\theta_{f2})$ satisfy

$$v_{c,f}(\theta_{f2}) < v_{c,h}(\theta_{f2}). \tag{24}$$

Similar to stage III, when (24) is satisfied, the increased energy stored in the capacitors of the HBSMs can be expressed as follows:

$$\Delta W_{h,{\rm increase2}} = \int_{\theta_{i2}}^{\theta_{f2}} (v_{\rm pa} - Fv_{c,f}) i_{\rm pa} d\omega_1 t. \tag{25}$$

6) Stage VI ($\theta_{f2} \le \omega_1 t \le 2\pi + \theta_{v1}$): In this stage, both the arm voltage $v_{\rm pa}$ and arm current $i_{\rm pa}$ are positive, and the inserted SMs will be charged.

When (24) is satisfied, FBSMs have charging priority. An imbalance occurs once the capacitor voltages of the FBSMs and HBSMs satisfy

$$v_{c,f}(2\pi+\theta_{v1}) < v_{c,h}(2\pi+\theta_{v1}). \tag{26}$$

Since the FBSMs can generate the required arm output voltage, all of the HBSMs will be bypassed during this period.

Because the total net energy transferred in one fundamental period in each arm is zero [10], we can use (11) and (26) to deduce that the capacitor voltages of the HBSMs will increase while the capacitor voltages of the FBSMs will decrease. Thus

$$\Delta W_{h,\text{increase1}} + \Delta W_{h,\text{increase2}} > \Delta W_{h,\text{decrease}} \tag{27}$$

can be further taken as the criterion for the imbalance problem. Note that an imbalance of the capacitor voltage will occur in the hybrid MMC for the inverter when the maximum energy discharged by the HBSMs in an arm (i.e., $\Delta W_{h,\text{decrease}}$) is smaller than the minimum energy charged by the HBSMs (i.e., $\Delta W_{h,\text{increase1}} + \Delta W_{h,\text{increase2}}$), which can be written as follows:

$$\Delta W_h = \Delta W_{h,\text{increase1}} + \Delta W_{h,\text{increase2}} - \Delta W_{h,\text{decrease}} > 0 \tag{28}$$

where ΔW_h is the net energy absorbed by the HBSMs in a fundamental frequency period.

Substituting (7), (18), (22), and (25) into (28) yields

$$\begin{aligned}\Delta W_h = &\int_{\theta_{f1}}^{\theta_{i1}} \left[\frac{V_{\text{dc}}}{2}(1 - m\sin\omega_1 t) - F v_{c,f}\right] \\ &\times \frac{I_m}{2}\left[\frac{m\cos\varphi}{2} + \sin(\omega_1 t - \varphi)\right] d\,\omega_1 t \\ &+ \int_{\theta_{i2}}^{\theta_{f2}} \left[\frac{V_{\text{dc}}}{2}(1 - m\sin\omega_1 t) - F v_{c,f}\right] \\ &\times \frac{I_m}{2}\left[\frac{m\cos\varphi}{2} + \sin(\omega_1 t - \varphi)\right] d\,\omega_1 t \\ &+ \int_{\theta_{i1}}^{\theta_{i2}} H v_{c,h} \times \frac{I_m}{2} \times \left[\frac{m\cos\varphi}{2} + \sin(\omega_1 t - \varphi)\right] \\ &\qquad d\,\omega_1 t > 0. \end{aligned} \tag{29}$$

The previous analysis can also be applied to potential capacitor voltage imbalance when the converter operates as a rectifier. During this process, the arm output voltage and arm current of the upper arm in phase A can be expressed as follows:

$$\begin{cases} v_{\text{pa}} = (1 - m\sin\omega_1 t)V_{\text{dc}}/2 \\ i_{\text{pa}} = -\left[m\cos\varphi/2 + \sin(\omega_1 t - \varphi)\right] I_m/2 \end{cases};\ m \geq 1. \tag{30}$$

Comparing (7) and (30), we can see that the arm currents will be opposite. Thus, according to the previous analysis, the FBSMs will be charged during stage I and the HBSMs may be discharged during stages III and V and only charged during stage IV. Assuming the energy discharged by the HBSMs in stages III and V is $\Delta W_{h,\text{decrease1}}$ and $\Delta W_{h,\text{decrease2}}$ and the energy charged by the HBSMs during stage IV is $\Delta W_{h,\text{increase}}$, then $\Delta W_{h,\text{decrease1}}$ to $\Delta W_{h,\text{increase}}$ can be expressed as follows:

$$\begin{cases} \Delta W_{h,\text{decrease1}} = -\int_{\theta_{f1}}^{\theta_{i1}} (v_{\text{pa}} - F v_{c,f}) i_{\text{pa}} d\omega_1 t \\ \Delta W_{h,\text{decrease2}} = -\int_{\theta_{i2}}^{\theta_{f2}} (v_{\text{pa}} - F v_{c,f}) i_{\text{pa}} d\omega_1 t \\ \Delta W_{h,\text{increase}} = \int_{\theta_{i1}}^{\theta_{i2}} H v_{c,h} i_{\text{pa}} d\omega_1 t. \end{cases} \tag{31}$$

Similar to the previous analysis, we can see that a capacitor voltage imbalance will also occur in a hybrid MMC operating as a rectifier when $\Delta W_{h,\text{decrease1}}$ to $\Delta W_{h,\text{increase}}$ satisfy

$$\Delta W_h = \Delta W_{h,\text{increase}} - \Delta W_{h,\text{decrease1}} - \Delta W_{h,\text{decrease2}} < 0 \tag{32}$$

where ΔW_h is the net energy absorbed by the HBSMs in a fundamental frequency period.

Substituting (30) and (31) into (32) yields

$$\begin{aligned}\Delta W_h = &-\int_{\theta_{f1}}^{\theta_{i1}} \left[\frac{V_{\text{dc}}}{2}(1 - m\sin\omega_1 t) - F v_{c,f}\right] \\ &\times \frac{I_m}{2}\left[\frac{m\cos\varphi}{2} + \sin(\omega_1 t - \varphi)\right] d\omega_1 t \\ &- \int_{\theta_{i2}}^{\theta_{f2}} \left[\frac{V_{\text{dc}}}{2}(1 - m\sin\omega_1 t) - F v_{c,f}\right] \\ &\times \frac{I_m}{2}\left[\frac{m\cos\varphi}{2} + \sin(\omega_1 t - \varphi)\right] d\omega_1 t \\ &- \int_{\theta_{i1}}^{\theta_{i2}} H v_{c,h} \times \frac{I_m}{2} \times \left[\frac{m\cos\varphi}{2} + \sin(\omega_1 t - \varphi)\right] \\ &\qquad d\omega_1 t < 0. \end{aligned} \tag{33}$$

Comparing (29) and (33), it is clear that a capacitor voltage imbalance will occur when ΔW_h is positive for the inverter, and will occur when ΔW_h is negative for the rectifier.

Furthermore, ΔW_h is mainly determined by the modulation index *m*, power angle φ, the number of FBSMs *F*, the number of HBSMs *H*, and θ_{f1} to θ_{f2} for a specific V_{dc}, I_m, and V_c. A close look at (10) reveals that the values of θ_{f1} to θ_{f2} are determined by three factors: *m*, φ, and the hybridization ratio *F/N*.

Based on the previous analyses, some conclusions concerning the capacitor voltage imbalance issue can be summarized.

1) Due to the different charge and discharge behaviors of a hybrid MMC, merely ensuring that zero net energy is absorbed in one fundamental period cannot keep the capacitor voltage balanced. An additional prerequisite of zero net energy absorbed in the HBSMs in one fundamental period should also be considered.
2) The capacitor voltage imbalance problem is mainly determined by the modulation index *m*, power angle φ, and the hybridization ratio *F/N*.

B. Effects of Primary Factors on Capacitor Voltage Imbalance

1) Modulation Index and Power Angle: For this scenario, the hybridization ratio *F/N* is set to a constant value of 2/3. Fig. 3(a) shows the analysis results to illustrate effect of the modulation index and power angle on capacitor voltage balance in a hybrid MMC operating as an inverter under a boosted ac voltage. The base value is $V_{\text{dc}} I_m/\omega_1$, and the main parameters of the converter are given in Table I.

The following two points can be determined:

1) the possibility of capacitor voltage imbalance (i.e., $\Delta W_h > 0$) increases as the modulation index increases;
2) the maximum value of ΔW_h with a fixed modulation index occurs at a power factor of unity.

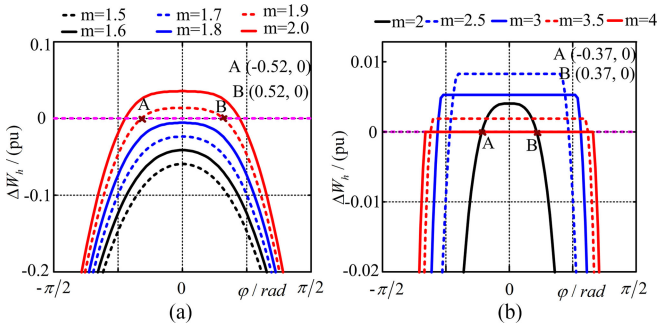

Fig. 3. Analysis results demonstrating the effect of modulation index and power angle on capacitor voltage imbalance for a hybrid MMC working as an inverter with $F/N = 2/3$: (a) boosted ac voltage and (b) reduced dc-link voltage.

TABLE I
SIMULATION PARAMETERS

Items	Values
Rated power	200 MVA
DC-link voltage	320 kV
Numbers of SMs per arm	300
Arm inductance	314 mH
SM capacitance	5 mF
Rated capacitor voltage	1.6 kV

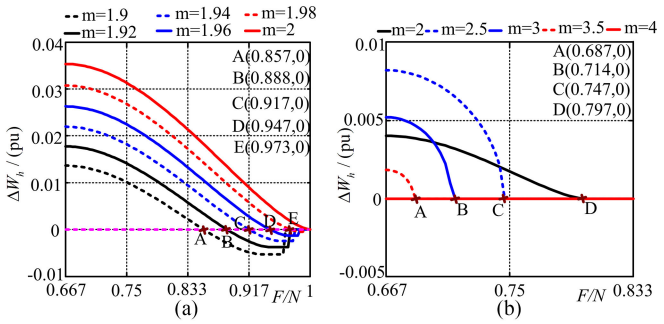

Fig. 4. Analysis demonstrating the effects of modulation index and hybridization ratio on a hybrid MMC operating as an inverter with unity power factor: (a) boosted ac voltage and (b) reduced dc-link voltage.

Fig. 3(b) shows the analysis results to illustrate how the modulation index and power angle in a hybrid MMC operating under a reduced dc-link voltage condition affects voltage imbalance. During normal operation, the hybrid MMC is assumed to operate with $m = 1.6$ and $\varphi = 0$. The base value is $E_m I_{\rm dc}/\omega_1$. As the dc-link voltage decreases, the modulation index m increases and the number of inserted SMs decreases. When m reaches 4 (i.e., $V_{\rm dc,red} = 1.6/4\ V_{\rm dc} = 0.4\,V_{\rm dc}$), the FBSMs in the hybrid MMC can generate the required arm output voltage and all HBSMs are bypassed, so ΔW_h is set to zero and no capacitor voltage imbalance occurs. Note that the power factor will also decrease following the reduction in dc-link voltage when $m \le 4$ so as to keep the capacitor voltage balanced.

2) Modulation Index and the Hybridization Ratio: In this scenario, the power factor is set to a constant of 1.0. Fig. 4(a) shows the analysis results that illustrate the effects of the modulation index m and hybridization ratio F/N on a hybrid MMC operating under boosted ac voltage. The base value is $V_{\rm dc} I_m/\omega_1$, with the main parameters of the converter given in Table I. From the figure, we can see that the required hybridization ratio increases along with increasing modulation index, and that the hybrid MMC cannot operate with a modulation index of 2.0 unless the hybridization ratio F/N reaches 1 (i.e., operates as an FBSM-based MMC).

Fig. 4(b) shows the analysis of ΔW_h for changes in the modulation index m and the hybridization ratio F/N in a hybrid MMC operating under reduced dc-link voltage. During normal operation, hybrid MMC is assumed to operate with $m = 1.6$ and $\varphi = 0$. The base value is $E_m I_{\rm dc}/\omega_1$ and ΔW_h is set to be zero when the FBSMs can output the required arm output voltage (i.e., $m \ge 4$). Observe that the required hybridization ratio F/N decreases along with a decreasing dc-link voltage to ensure the capacitor voltage remains balanced. When modulation index m equals 2 (i.e., $V_{\rm dc,red} = 0.8V_{\rm dc}$), the required hybridization ratio is 0.797 to maintain a balanced capacitor voltage.

IV. ANALYSIS OF FFRCC INJECTION

Using the previous analysis, we have determined that capacitor voltage imbalance is highly related to three main factors: modulation index m, power angle φ, and hybridization ratio F/N. Some published research efforts have attempted to solve this issue by decreasing the power factor [10] or by increasing the hybridization ratio [18]. However, both of these methods have a detrimental influence on the performance of a hybrid MMC. To enhance this performance, a new method based on circulating current injection is proposed in this section.

A. Principle and Control Strategy

Given that the converter operates as an inverter, the arm currents without an FFRCC injection for phase A can be expressed as follows:

$$\begin{cases} i_{\rm pa} = [m\cos\varphi/2 + \sin(\omega_1 t - \varphi)]I_m/2 \\ i_{\rm na} = [m\cos\varphi/2 - \sin(\omega_1 t - \varphi)]I_m/2 \end{cases}; \quad m \ge 1\,. \tag{34}$$

We can assume the injected FFRCC is

$$i_{\rm FFRCC} = I_{m,\rm rec}\sin(\omega_1 t \pm \pi/2) \tag{35}$$

where $I_{m,\rm rec}$ is the current amplitude.

Thus, the arm currents with an FFRCC injection can be written as follows:

$$\begin{cases} i_{\rm pa,FFRCC} = \frac{I_m}{2}\left[\frac{m\cos\varphi}{2} + \sin(\omega_1 t - \varphi)\right] \\ \qquad\qquad + I_{m,\rm rec}\sin(\omega_1 t \pm \pi/2) \\ i_{\rm na,FFRCC} = \frac{I_m}{2}\left[\frac{m\cos\varphi}{2} - \sin(\omega_1 t - \varphi)\right] \\ \qquad\qquad + I_{m,\rm rec}\sin(\omega_1 t \pm \pi/2) \end{cases}; \quad m \ge 1\,. \tag{36}$$

Assuming the phase angle of the injected FFRCC is known (i.e., $\pi/2$ or $-\pi/2$), (36) can be rewritten as follows:

$$\begin{cases} i_{\mathrm{pa,FFRCC,lead}} = mI_m\ \cos\varphi/4 \\ \qquad\qquad + I_{m,p,\mathrm{lead}}\ \sin(\omega_1 t + \varphi_{p,\mathrm{lead}}) \\ i_{\mathrm{na,FFRCC,lead}} = mI_m\ \cos\varphi/4 \\ \qquad\qquad + I_{m,n,\mathrm{lead}}\ \sin(\omega_1 t + \varphi_{n,\mathrm{lead}}) \end{cases};\quad m \geq 1 \tag{37}$$

$$\begin{cases} i_{\mathrm{pa,FFRCC,lag}} = mI_m\ \cos\varphi/4 \\ \qquad\qquad + I_{m,p,\mathrm{lag}}\ \sin(\omega_1 t + \varphi_{p,\mathrm{lag}}) \\ i_{\mathrm{na,FFRCC,lag}} = mI_m\ \cos\varphi/4 \\ \qquad\qquad + I_{m,n,\mathrm{lag}}\ \sin(\omega_1 t + \varphi_{n,\mathrm{lag}}) \end{cases};\quad m \geq 1 \tag{38}$$

where $I_{m,p,\mathrm{lead}}$, $I_{m,n,\mathrm{lead}}$, $I_{m,p,\mathrm{lag}}$, $I_{m,n,\mathrm{lag}}$, and $\varphi_{p,\mathrm{lead}}$, $\varphi_{n,\mathrm{lead}}$, $\varphi_{p,\mathrm{lag}}$, $\varphi_{n,\mathrm{lag}}$ can be expressed as follows:

$$\begin{cases} I_{m,p,\mathrm{lead}} = \sqrt{(I_m\ \cos\varphi/2)^2 + (I_{m,\mathrm{rec}} - I_m\ \sin\varphi/2)^2} \\ I_{m,n,\mathrm{lead}} = \sqrt{(I_m\ \cos\varphi/2)^2 + (I_{m,\mathrm{rec}} + I_m\ \sin\varphi/2)^2} \\ I_{m,p,\mathrm{lag}} = \sqrt{(I_m\ \cos\varphi/2)^2 + (I_{m,\mathrm{rec}} + I_m\ \sin\varphi/2)^2} \\ I_{m,n,\mathrm{lag}} = \sqrt{(I_m\ \cos\varphi/2)^2 + (I_{m,\mathrm{rec}} - I_m\ \sin\varphi/2)^2} \end{cases} \tag{39}$$

$$\begin{cases} \varphi_{p,\mathrm{lead}} = \arctan\left[(2I_{m,\mathrm{rec}} - I_m\ \sin\varphi)/\left(I_m\ \cos\varphi\right)\right] \\ \varphi_{n,\mathrm{lead}} = \pi - \arctan\left[(2I_{m,\mathrm{rec}} + I_m\ \sin\varphi)/\left(I_m\ \cos\varphi\right)\right] \\ \varphi_{p,\mathrm{lag}} = -\arctan\left[(2I_{m,\mathrm{rec}} + I_m\ \sin\varphi)/\left(I_m\ \cos\varphi\right)\right] \\ \varphi_{n,\mathrm{lag}} = \pi + \arctan\left[(2I_{m,\mathrm{rec}} - I_m\ \sin\varphi)/\left(I_m\ \cos\varphi\right)\right]. \end{cases} \tag{40}$$

Note that both the leading and lagging reactive currents can improve capacitor voltage balance, as shown in the previous analysis in Fig. 3. Comparing (39) and (40), observe that $I_{m,p,\mathrm{lead}}$ ($I_{m,n,\mathrm{lead}}$) is equal to $I_{m,n,\mathrm{lag}}$ ($I_{m,p,\mathrm{lag}}$), and $|\sin(\varphi_{p,\mathrm{lead}})|$ ($|\sin(\varphi_{n,\mathrm{lead}})|$) is equal to $|\sin(\varphi_{n,\mathrm{lag}})|$ ($|\sin(\varphi_{p,\mathrm{lag}})|$). Thus, leading and lagging reactive current injections have a similar influence on the operation of a hybrid MMC.

The amplitude of the injected FFRCC should ensure that ΔW_h after the injection is no more than zero. Ignoring the voltage drops on the arm inductors, and taking the leading FFRCC as an example, the amplitude $I_{m,\mathrm{rec}}$ should meet

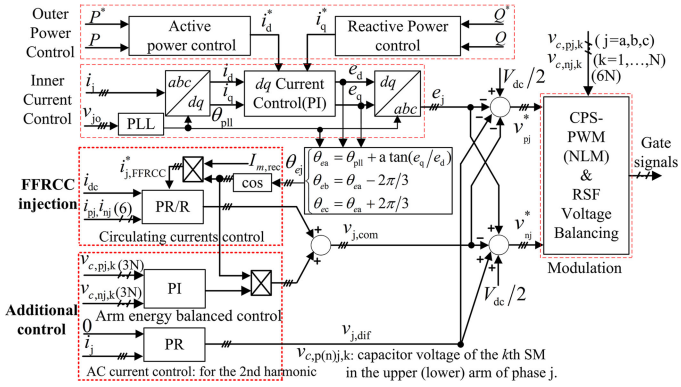

Fig. 5. Schematic diagram of the control strategy with FFRCC injection for a hybrid MMC-based HVDC system.

$$\begin{aligned} \Delta W_{h,\mathrm{FFRCC}} = &\int_{\theta_{f1,\mathrm{FFRCC}}}^{\theta_{i1,\mathrm{FFRCC}}} (v_{\mathrm{pa}} - Fv_{c,f}) i_{\mathrm{pa,FFRCC}} d\omega_1 t \\ &+ \int_{\theta_{i2,\mathrm{FFRCC}}}^{\theta_{f2,\mathrm{FFRCC}}} (v_{\mathrm{pa}} - Fv_{c,f}) i_{\mathrm{pa,FFRCC}} d\omega_1 t \\ &+ \int_{\theta_{i1,\mathrm{FFRCC}}}^{\theta_{i2,\mathrm{FFRCC}}} Hv_{c,h} i_{\mathrm{pa,FFRCC}} d\omega_1 t \leq 0 \end{aligned} \tag{41}$$

where the four angles $\theta_{f1,\mathrm{FFRCC}}$ to $\theta_{f2,\mathrm{FFRCC}}$ can be expressed as (42) shown at the bottom of this page.

Since the upper and lower arms operate differently after FFRCC injection as shown in (37)–(40), the required amplitude of FFRCC for the upper and lower arms to achieve a negative $\Delta W_{h,\mathrm{FFRCC}}$ may be different. To avoid capacitor voltage imbalance, the amplitude of the injected FFRCC should be larger than the required amplitudes of the FFRCCs for both the upper and lower arms.

The required FFRCC can be injected with a proportional resonant (PR) control using either direct modulation [21]–[23] or indirect modulation-based control [24], [25]. The former method is simple, but suffers from circular interactions among various electrical quantities: arm current, capacitor voltage ripple, and the ripple voltage across the phase leg [22], [23]. On the other hand, the latter features good decoupling performance between electrical parameters inside (e.g., capacitor voltage ripples) and outside the converter (e.g., ac and dc output current) [25]. However, considering that direct modulation-based control has been widely adopted in existing systems, FFRCC injection with direct modulation-based control is given here.

$$\begin{cases} \theta_{i1,\mathrm{FFRCC}} = \pi + \arcsin[mI_m \cos\varphi/(4I_{m,p,\mathrm{lead}})] - \varphi_{p,\mathrm{lead}}; & mI_m\ \cos\varphi \leq 4I_{m,p,\mathrm{lead}} \\ \theta_{i2,\mathrm{FFRCC}} = 2\pi - \arcsin[mI_m\ \cos\varphi/(4I_{m,p,\mathrm{lead}})] - \varphi_{p,\mathrm{lead}}; & mI_m\ \cos\varphi \leq 4I_{m,p,\mathrm{lead}} \\ \theta_{f1,\mathrm{FFRCC}} = \pi + \arcsin[(2FV_c/V_{dc} - 1)/m]; & m \geq 1 \\ \theta_{f2,\mathrm{FFRCC}} = 2\pi - \arcsin[(2FV_c/V_{dc} - 1)/m]; & m \geq 1 \end{cases} \tag{42}$$

Fig. 5 shows a detailed control scheme for a hybrid MMC-based HVDC system, where the outer loop is an active/reactive power control and the inner loop consists of current control. For the sake of brevity, no further details concerning the vector control are given here. The FFRCC injection is implemented using PR control, where θ_{ej} is the phase angle of the differential mode component of the lower and upper arm output voltages [e.g., e_a in (4)].

To present the proposed FFRCC injection clearly, four important points are noted.

1) To insure the injected FFRCCs do not flow into the ac and dc sides, the FFRCCs are injected in the three phases simultaneously. Their amplitudes are equal, and their phases are positive sequence.
2) Due to the aforementioned circular interaction of parameters resulting from direct modulation-based control, any asymmetrical ac component of the arm currents after FFRCC injection shown in (37) will pollute the ac output current with even-order harmonics where the second-order harmonic is dominant; thus, additional PR control is added to suppress the second-order harmonic, as shown in the additional control in Fig. 5.
3) Considering the naturally existing circulating currents of the even-order harmonics—particularly the second-order harmonic—in a direct modulated converter, the second-order harmonic is also suppressed by the PR control, shown in the FFRCC injection control in Fig. 5. In addition, additional resonant (R) control against the three-order harmonic should also be added to avoid the influence of FFRCC injection on the dc-side current.
4) Considering the voltage drop on the arm inductors, FFRCC injection will affect capacitor energy balance between the upper and lower arms. To mitigate this influence, balanced control of the arm energy [24] is added, as shown in the additional control in Fig. 5.

B. Influence and Performance Evaluation

1) Energy Fluctuation in Arm Capacitors: Ignoring the voltage drops on the arm inductors, $v_{\rm pa}$ and $v_{\rm na}$ can be expressed as follows:

$$\begin{cases} v_{\rm pa} = (1 - m\sin\omega_1 t)V_{\rm dc}/2 \\ v_{\rm na} = (1 + m\sin\omega_1 t)V_{\rm dc}/2 \end{cases}; \quad m \geq 1\,. \tag{43}$$

With the leading FFRCC, the change of instantaneous power flowing in each arm can be expressed as follows:

$$\begin{cases} \Delta p_{\rm pa} = (1 - m\sin\omega_1 t)V_{\rm dc}/2 \times I_{m,\rm rec}\cos\omega_1 t \\ \Delta p_{\rm na} = (1 + m\sin\omega_1 t)V_{\rm dc}/2 \times I_{m,\rm rec}\cos\omega_1 t \end{cases}; \quad m \geq 1\,. \tag{44}$$

The change in energy stored in the arm capacitors can be expressed as follows:

$$\begin{cases} \Delta W_{\rm pa} = \int \Delta p_{\rm pa}dt = \frac{V_{\rm dc}I_{m,\rm rec}\sin\omega_1 t}{2\omega_1} \\ \qquad\qquad + \frac{mV_{\rm dc}I_{m,\rm rec}\cos 2\omega_1 t}{8\omega_1} \\ \Delta W_{\rm na} = \int \Delta p_{\rm na}dt = \frac{V_{\rm dc}I_{m,\rm rec}\sin\omega_1 t}{2\omega_1} \\ \qquad\qquad - \frac{mV_{\rm dc}I_{m,\rm rec}\cos 2\omega_1 t}{8\omega_1} \end{cases}; \quad m \geq 1. \tag{45}$$

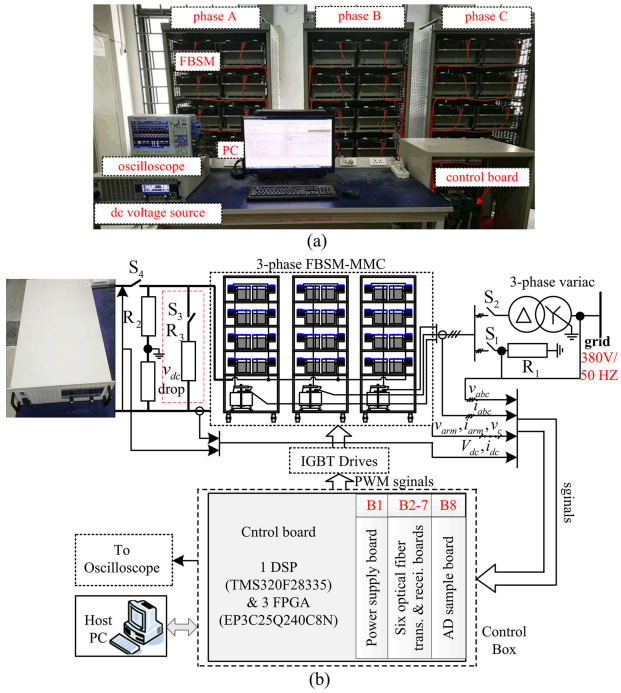

Fig. 6. Photograph and schematic diagram of the experimental setup: (a) photograph and (b) schematic diagram.

Note that an FFRCC injection causes a fundamental frequency energy ripple and a double frequency energy ripple in a hybrid MMC, which benefits the energy exchange between FBSMs and HBSMs and ensures the capacitor voltage remains balanced.

2) Current Stress of the Semiconductors: If the transmitted power is kept constant, the ac-side current correspondingly decreases under boosted ac-side voltage conditions. Thus, the FFRCC injection has only a slight influence on any increase in the current stress of the semiconductors. Similarly, under reduced dc-link voltage conditions, the transmitted power will correspondingly decrease, resulting in a decrease of the maximum arm current. Taking a hybrid MMC operating with $m = 1.6$ and $\varphi = 0$ as an example, if we assume E_m is increased to $0.95\,V_{\rm dc}$ $(m = 1.9)$, then the ac-side current will decrease to 0.84 p.u. Thus, the maximum allowed FFRCC injection is 0.27 times that of the amplitude of the ac-side current under normal operation without an increase in semiconductor current stress. Similarly, under reduced dc voltage conditions with a 0.2 p.u. dc-link voltage drop, the transmitted power decreases to 0.8 p.u. Thus, the maximum allowed FFRCC injection is 0.3 times that of the amplitude of the ac-side current under normal operation without further increasing semiconductor current stress. Since it is more important to ensure capacitor voltage balance, the transmitted power could be relatively reduced if the required FFRCC injection is larger than the maximum allowed value considering the allowed current stress of the semiconductors in the SMs.

V. Experimental Results

To verify the previous analysis and the proposed FFRCC injection, a three-phase FBSM-based MMC experimental setup is implemented, shown in Fig. 6. Each arm includes eight

TABLE II
PARAMETERS OF THE EXPERIMENTAL SETUP

Items	Values
Rated power	4 kW
DC-link voltage	200 V
Numbers of SMs per arm	3
Rated capacitor voltages	100 V
Transformer inductance L_T	6 mH
Arm inductance L	8 mH
SM capacitance	3.8 mF
Resistance R_1	13.3 Ω
Resistance R_2	16 (100) Ω
Resistance R_3	100 Ω
Discharging resistance	12.8 kΩ
Sampling frequency	10 kHz
Switching frequency	5 kHz (PD-PWM)

FBSMs. The control system consists of one TMS320F28335 DSP and three EP3C25Q240C8N field-programmable gate array (FPGAs). The DSP realizes station control (i.e., vector control), while the sorting algorithm for the SM capacitor voltages for each phase is performed in each FPGA. For each SM, there is one IGBT module (SEMIKRON/SK100 GH12T4T) and two driving modules (SEMIKRON/SKYPE R 32 PRO R). In addition, each FBSM is configured with four control signals (two gate-driving signals, the SM voltage signal, and the error signal) to interact with the upper controller (i.e., the EP3C25Q240C8N FPGA). To avoid electromagnetic interference when delivering the measured capacitor voltage and the driving signals, all signals are received and transmitted by optical fiber.

The detected capacitor voltage is converted to a pulse signal whose frequency is proportional to the value of the detected voltage. An AD652 is used to implement the analog-to-digital conversion for the capacitor voltage. Using an input clock frequency for the AD652 of 2 MHz, and a sampling frequency for the capacitor voltage of 10 kHz resulted in a quantization error of less than 0.8 V for the analog-to-digital conversion.

In this paper, three FBSMs are adopted for each arm, with one FBSM operating as a HBSM, i.e., a hybridization ratio *F/N* of 2/3. The main circuit parameters for the experiments are shown in Table II, where R_2 is 100 Ω for the boosted ac output voltage experiment and 16 Ω for the reduced dc voltage experiment.

Fig. 7 shows the experimental results for the three-phase hybrid MMC working as an inverter with a resistance load. In this case, switches S_1 and S_4 are closed while S_2 and S_3 are open. Considering the symmetry of the three phases, and to make the waveforms more clear, Fig. 7(A) shows the dynamic performance of the ac-side current, arm currents, circulating current, and capacitor voltages (lower arm) for phase A, where the modulation index increases from 1.8 to 1.9 and the transmitted active power increases from 3.6 to 4.0 kW. Due to inductance in the arm, the converter supplies a set amount of reactive power, so that I_m and φ are 14.22 A and 0.094 $(\mathrm{atan}(\omega_1 L/2R_1))$, calculated from (7). Since $|\varphi|$ is smaller than the critical value [i.e., 0.52 shown in Fig. 3(a)], ΔW_h is larger than zero. According to the previous analysis, a capacitor voltage imbalance occurs, verified by the results in Fig. 7(A)-d. Furthermore, $v_{c,h}$ continues increasing until it reaches the protection value (120 V), at which point the system shuts down. Fig. 7(B) shows the results

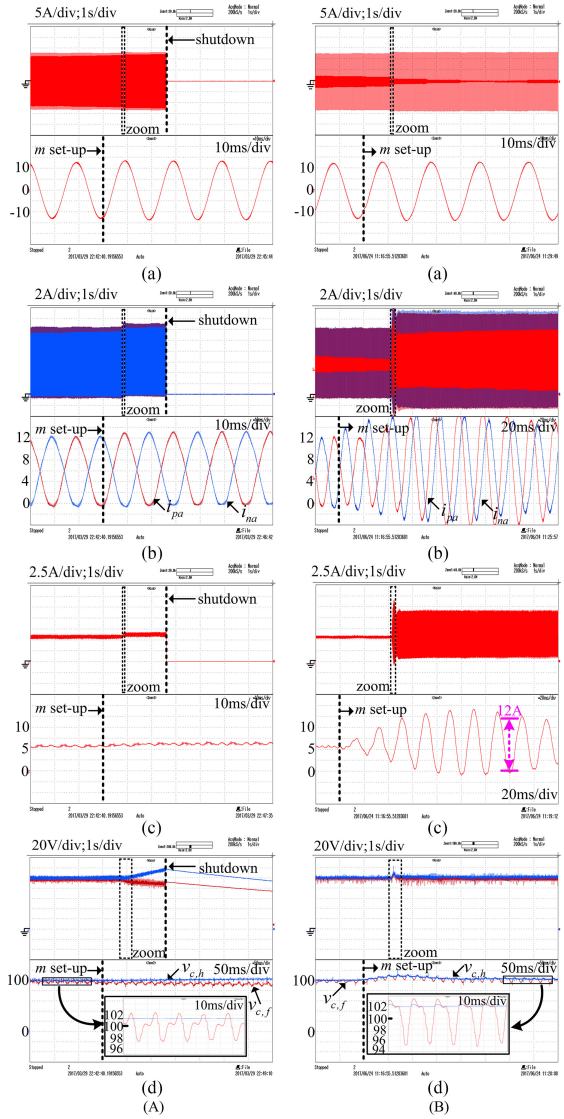

Fig. 7. Experimental results for a hybrid MMC working as an inverter (A) without and (B) with fundamental reactive circulating current injection, where the power factor on the load side is unity and m increases from 1.8 to 1.9: (a) ac-side current, (b) arm currents, (c) circulating current, and (d) capacitor voltages.

with the proposed FFRCC scheme. When the modulation index increases, three leading FFRCCs of 6A are is injected. From the results, we can see that no capacitor voltage imbalance occurs.

Fig. 8 shows the experimental results for the three-phase hybrid MMC working as a grid-connected inverter with a unity power factor (ac grid side) under reduced dc-link voltage conditions. In this case, switches S_2 and S_4 are closed while S_1 is open, and S_3 is closed to emulate the dc voltage drop. Under normal operating conditions, the ac terminal voltage of the transformer with no load is 160 V, and the transmitted active power is 2.4 kW. When the reduced dc-link voltage is applied to the system, I_m and φ become 8 A and 0.156 $(\mathrm{atan}[\omega_1(L/2 + L_T)/(160/8)])$, respectively. According to the previous analysis, $|\varphi|$ is smaller than the critical value [i.e., 0.37 shown in Fig. 3(b)] and ΔW_h is larger than zero, which means that a capacitor voltage imbalance occurs. The results in Fig. 8(A)-e demonstrate this conclusion, where $v_{c,h}$

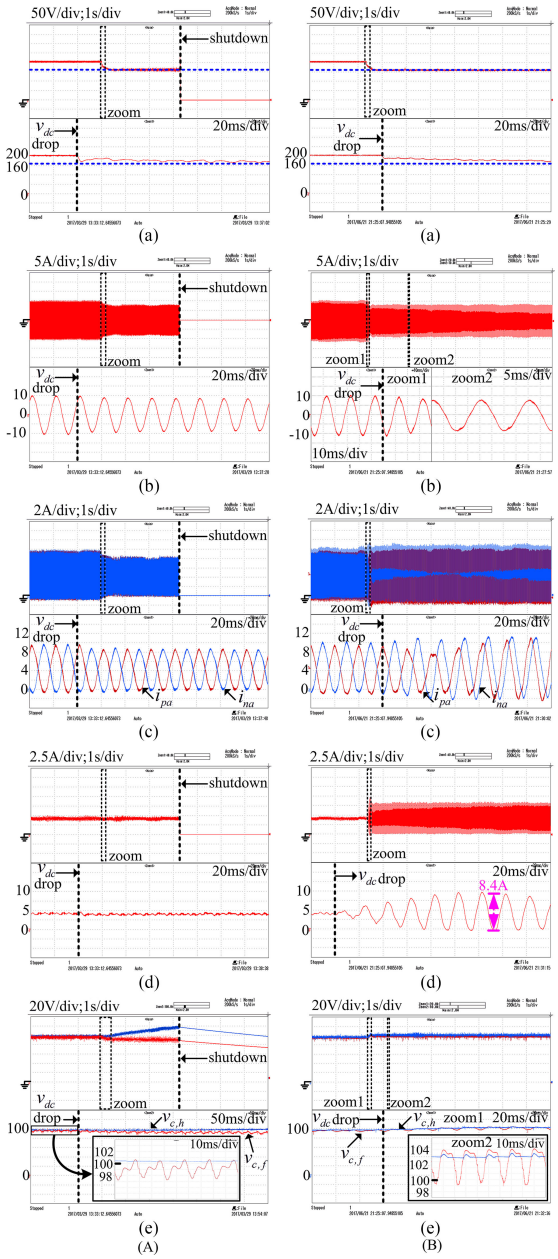

Fig. 8. Experimental results for a hybrid MMC working as an inverter (A) without and (B) with fundamental reactive circulating current injection, where $m = 1.6$, the power factor on the ac grid side is unity and the dc-link voltage drops to 0.8 p.u.: (a) dc-link voltage, (b) ac-side current, (c) arm currents, (d) circulating current, and (e) capacitor voltages.

continues increasing until it reaches the protection value and the system shuts down. Fig. 8(B) shows the results with the proposed FFRCC scheme. Three leading FFRCCs of 4.2A are injected, which suppresses any potential capacitor voltage imbalance.

VI. Conclusion

In this paper, the mechanism underlying capacitor voltage imbalance in a hybrid MMC is analyzed in depth. Based on this analysis, the three main factors of modulation index, power angle, and hybridization ratio are summarized, and the effects of these three factors on capacitor voltage imbalance are analyzed. According to the theoretical findings, an improved control strategy based on FFRCC injection is proposed to ensure capacitor voltage balance in a hybrid MMC. In this approach, the amplitude and phase angle of the injected circulating current are given, and their influence on the energy fluctuation in the SMs' capacitors and the semiconductors' current stress is explored. Compared with conventional solutions, this method does not increase the required number of FBSMs, reduce the power factor, or change the symmetric structure of the hybrid MMC. The experimental results demonstrate the validity of the proposed scheme, showing that the capacitor voltage is kept balanced by injecting the proposed circulating current under both boosted ac voltage conditions and the reduced dc voltage conditions when using a hybrid MMC.

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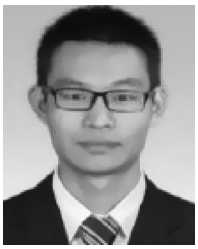

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