High-Efficiency High Step-Up DC–DC Converter With Dual Coupled Inductors for Grid-Connected Photovoltaic Systems

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***Abstract*—This paper introduces a non-isolated high step-up dc–dc converter with dual coupled inductors suitable for distributed generation applications. By implementing an input parallel connection, the proposed dc–dc structure inherits shared input current with low ripple, which also requires small capacitive filter at its input. Moreover, this topology can reach high voltage gain by using dual coupled inductors in series connection at the output stage. The proposed converter uses active clamp circuits with a shared clamp capacitor for the main switches. In addition to the active clamp circuit, the leakage energy is recycled to the output by using an integrated regenerative snubber. Indeed, these circuits allow soft-switching conditions, i.e., zero voltage switching and zero current switching for active and passive switching devices, respectively. The mentioned features along with a common ground connection of the input and output make the proposed topology a proper candidate for transformer-less grid-connected photovoltaic systems. The operating performance, analysis and mathematical derivations of the proposed dc–dc converter have been demonstrated in the paper. Moreover, the main features of the proposed converter have been verified through experimental results of a 1-kW laboratory prototype.**

***Index Terms*—Dual-coupled inductors, grid-connected photovoltaic (PV) system, high-efficiency, high step-up dc–dc converter, high voltage gain, nonisolated, zero voltage switching (ZVS), zero current switching (ZCS).**

I. Introduction

POWER electronics converters play a significant role in power conversion of distributed generation (DG) systems. Distributed systems as such produces dc or ac voltage and current, which must be converted to voltage and current that are compatible to the load or to the grid requirements. Therefore, new infrastructures based on different power converters must be implemented for various power management of these sources [1], [2]. Rapid depletion of fossil fuels along with the environmental pollution problems have led to a great interest in investigating the power generation from alternative clean energy resources. Renewable energy sources including wind, hydro, geothermal, solar, marine, and biomass energies are becoming increasingly important in DG systems. Among a variety of renewable energy sources, photovoltaic (PV) systems have the advantage of unlimited and freely available resource, i.e., solar beams that radiates almost anywhere throughout the globe. Since there is no moving part in the structure of a PV module, it inherits a quiet and clean energy production with minimum maintenance requirement and long-life characteristic. In recent years, PV systems got the largest growth in both investigations and installations among other renewable energy sources [3]–[6].

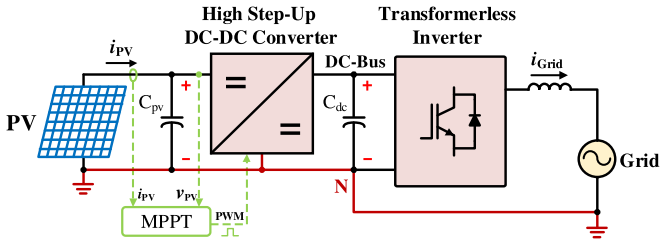

Fig. 1. General layout of a transformer-less grid-connected PV system.

Most of the growth in the installed PV systems has been allocated to the grid-connected PV market compared to the off-grid market. Moreover, compared to the PV systems with either line frequency or high-frequency transformers, the transformer-less PV system has typically a higher efficiency and reliability, as well as lower complexity and manufacturing cost. Besides, the PV module must be grounded in most standards in order to eliminate common mode current. One convenient way to reach this goal is to implement a common grounded transformer-less inverter [3]–[6]. Such grid–connected PV system is illustrated in Fig. 1. Since the output voltage of a PV module is usually low (about 20–50 V), a front-end high step-up dc–dc converter is required to boost and regulate the PV voltage to the voltage level of the dc-bus (400 or 800 V). In order to eliminate common mode current in grounded PV systems, the step-up converter should allow a shared ground between the PV ground and the grid neutral line. On the other hand, if the PV current has too much

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ripple in such low-voltage systems, the maximum power point tracker (MPPT) algorithm cannot extract most power from the panel. Hence, in order to increase system overall efficiency and reliability, a front-end dc–dc converter should draw a continuous low ripple current and maximize the power capture [7], [8].

Theoretically, the conventional boost converter can reach high-voltage gain by using a large duty cycle close to 1, which normally results in high conduction losses. The shortcomings of the conventional boost converter are remarkable especially in high-voltage applications, where the switch must endure high voltage stresses and severe reverse-recovery loss in the output diode. Various voltage boosting techniques have been implemented in step-up dc–dc converters, including multistage/multilevel, switched-capacitor (charge pump), voltage multiplier, switched inductor, and voltage lift topology. Indeed, each voltage boosting techniques can provide voltage step-up with its own pros and cons [9]. As it is said, these converters can provide higher voltage gain compared to the conventional boost converter, but in the case of a very large voltage gain application, these converters need an increased number of components with multistage/level solutions. This, of course, causes an increased complexity, cost, and decreases also the efficiency and power density.

Another promising voltage boosting technique to step-up the voltage level of dc–dc converters is employing coupled magnetics (i.e., transformer and coupled inductors). High-frequency transformers can be employed to level up the input voltage with the benefit of providing electrical isolation. However, when electrical isolation is not required, using coupled inductors can be a simpler and more flexible solution to boost the voltage level of step-up converters [9]. In 2003, a family of high efficient, high step-up dc–dc converters with coupled inductors has been introduced [10]. These converters use passive clamping to recycle the leakage energy of coupled inductors that also reduces the reverse-recovery of the output diode. In [11], a high step-up converter with coupled inductor and passive snubber has been introduced. By reducing the resonance between the leakage inductance and the parasitic capacitance of semiconductors, this converter can reduce the maximum voltage blocking requirements.

Different design considerations with voltage boosting techniques have been considered to reach higher voltage gain and efficiency, and lower component rating, and manufacturing cost [12]–[16]. Despite of many advantages including higher voltage gain at minimum component stress, the input current ripple of these converters are large and discontinuous, which may degrade the life time of input source, e.g., PV and fuel cell. The current-fed solution with integrated transformer structure is an effective solution for high-voltage gain applications. This concept combined with soft switching has been used in a single switch structure to fulfill a high voltage gain, high efficiency, and low ripple input current characteristics [18]–[21]. As in high-power applications the single switch dc–dc converters must endure high current stresses; hence they are not perfect candidates for high power applications. Some step-up dc–dc converters based on an active coupled inductor network have been proposed in [22], [23], which employed an *X* shape switched coupled inductor at the input. Though, the mentioned converters benefit from shared current stress, the current drawn from the input source has a considerable ripple.

Parallel input layouts like the well-known interleaved structures can effectively reduce the ripple current of the input source and allow an increased power level for the circuit by sharing a high input current of step-up dc–dc converters. Hence, the current stress of semiconductor devices and the magnetic component size of the input side can be reduced [24]–[32]. The implementation of built-in transformer in interleaved dc–dc converters is a promising solution for voltage boosting of high step-up applications [27]–[29]. One shortcoming related to these circuits is their large number of components that can increase the cost and size of the converter. The dual coupled inductors concept that comprises of series secondary side coupled inductors are another voltage boosting technique that have shown a great potential for high step-up applications with high power density [30]–[32]. An asymmetrical interleaved high step-up converter with a voltage multiplier module has been introduced in [30]. This structure integrates a flyback-boost converter and an interleaved boost converter with dual coupled inductors. An input parallel output series dc–dc converter is introduced in [31], which employs an improved interleaved boost converter and voltage multiplier module. Different from both mentioned converters, the converter in [32] employs active clamping to achieve zero voltage switching (ZVS), and hence the switching loss can be reduced significantly. Indeed the mentioned converters are interesting solutions for voltage step-up and high-power applications. Although their components count/rating may not be as efficient as they could be. Furthermore, most of the mentioned dc–dc converters have floating output and are not common grounded, which may limit their implementation for transformer-less grid-connected PV applications.

Considering the above aspects and shortcomings of high-voltage boost dc–dc converters, a novel soft-switched parallel high step-up dc–dc converter suitable for high power conversion with minimal component count is proposed in this paper. In the proposed converter, an integrated regenerative snubber effectively recycles the leakage energy to the output and the voltage spike of the main switches is absorbed due to the active clamp circuits of each phase. Furthermore, the active clamp brings soft-switching conditions to all semiconductors as well. The circuit derivation of the proposed converter can be found in Fig. 2. The proposed converter is made out of two major coupled inductor based dc–dc converters in the way that it shares the primary sides of coupled inductors and integrates the secondary sides of coupled inductors in a dual coupled structure. Moreover, the proposed converter uses only one clamp capacitor for both main switches. Though two switches are used to reach the active clamp feature, there is not much difficulty in generating gate signals for controlling the additional switches since the main and clamp switches operate complementary. Also all active switches are implemented at the low voltage side, meaning low $r_{ds(\mathrm{on})}$ switches can be used for active switching devices, which along with ZVS condition of all switches and zero current switching (ZCS) of all didoes lead to a high operating efficiency. In addition to the clamp circuit, the stored leakage energy of the

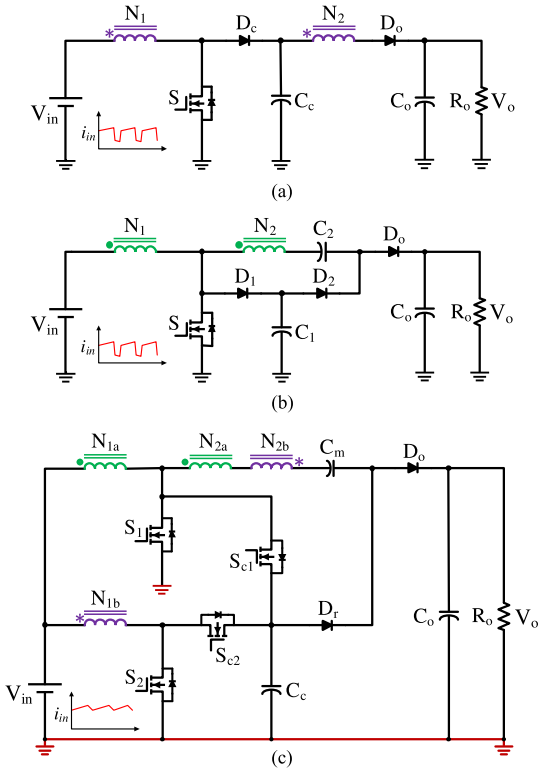

Fig. 2. Topology derivation of the proposed converter, (a) clamp mode coupled inductor boost converter [10], (b) coupled inductor boost converter with regenerative passive snubber [11], and (c) the proposed dc–dc converter.

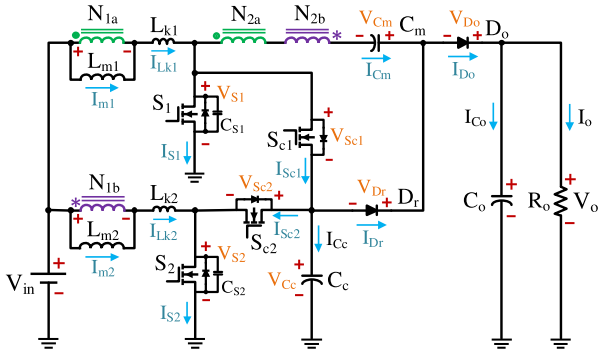

Fig. 3. Equivalent circuit of the proposed input parallel dc–dc converter.

coupled inductors can be recycled to the load with a regenerative passive snubber. Besides, due to its parallel input structure the proposed converter draws a low ripple input current. All features along with a high-voltage gain can be fulfilled with low quantity and reduced voltage stress components. Added to the mentioned advantageous features, the proposed converter allows a common ground connection between the input and output, which is a crucial characteristic when operating with transformer-less grid-connected PV systems.

The paper is organized as follows, Section II describes the principle of operation and analysis of the proposed converter, and Section III provides design considerations and experimental results of a laboratory prototype followed by a conclusion in Section IV.

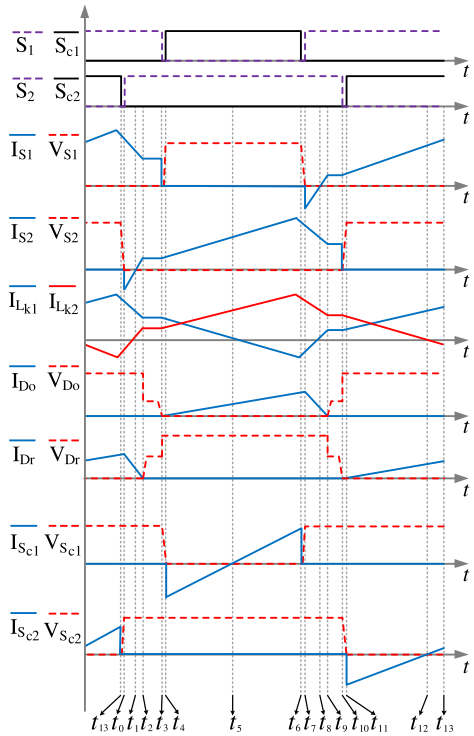

Fig. 4. Key waveforms and operating states of the proposed converter.

II. Principles of Operation and Analysis

Fig. 3 shows the equivalent circuit of the proposed converter, where the assumed voltage polarities and current directions are also given. In the following subsections, the principles of operation and a comprehensive analysis of the proposed dc–dc converter is described.

A. Operating States

The proposed converter has 14 states of operation during one switching cycle, as shown in Fig. 4. Since, the coupled inductors in this converter do not store energy (unlike Flyback transformer) and due to the multiplier capacitor connected in series with the secondary side of both coupled inductors that acts as a dc-blocking capacitor, the proposed dc–dc converter operates in continuous conduction mode. In order to perform the steady-state analysis, several assumptions are made as follows:

1) the coupled inductors are modeled ideally with a magnetizing inductor (L_m), a leakage inductor (L_k), and an ideal transformer, with a turns ratio of $n = \frac{N_{2a}}{N_1 a} = \frac{N_{2b}}{N_{1b}}$;
2) all the semiconductors are considered ideal;
3) all the capacitors are large enough to consider their voltage constant during one switching cycle.

Fig. 5 illustrates the operating states of the proposed converter at one switching cycle. The principle of operation of the proposed converter is written in the following.

State 1 $[t_0 - t_1]$*:* The main switch S_1 is in the ON state and the clamp switches (S_{c1} and S_{c2}) are in OFF state. The input voltage source transfers energy to the magnetizing inductor L_{m1} and leakage inductor L_{k1}. Additionally, at $t = t_0$ the antiparallel diode of the main switch S_2 begins to conduct and the

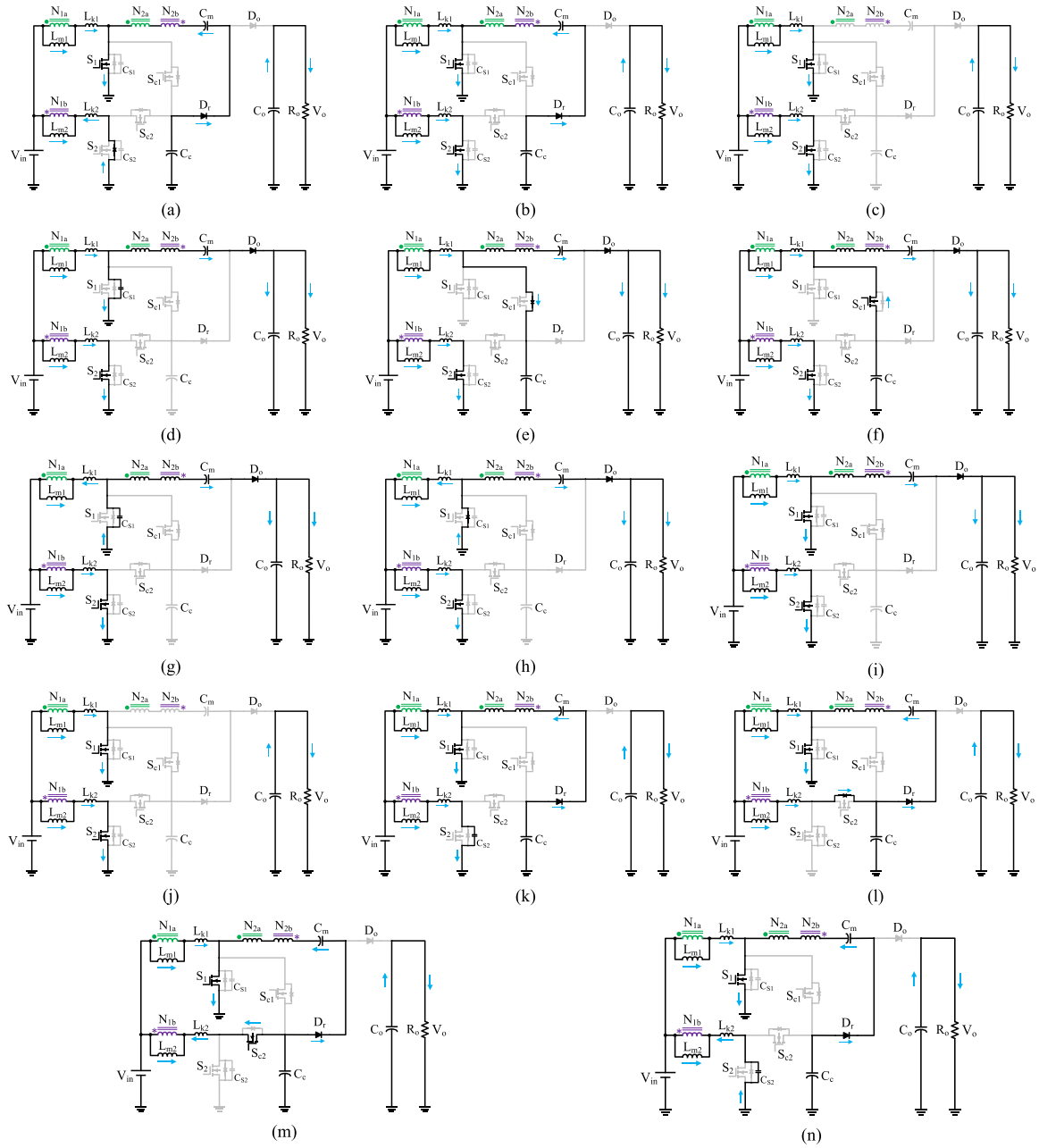

Fig. 5. Operation states of the proposed converter in one switching cycle, (a) state 1 $[t_0 - t_1]$, (b) state 2 $[t_1 - t_2]$, (c) state3 $[t_2 - t_3]$, (d) state 4 $[t_3 - t_4]$, (e) state 5 $[t_4 - t_5]$, (f) state 6 $[t_5 - t_6]$, (g) state 7 $[t_6 - t_7]$, (h) state 8 $[t_7 - t_8]$, (i) state 9 $[t_8 - t_9]$, (j) state 10 $[t_9 - t_{10}]$, (k) state 11 $[t_{10} - t_{11}]$, (l) state 12 $[t_{11} - t_{12}]$, (m) state 13 $[t_{12} - t_{13}]$, and (n) state14 $[t_{13} - t_0]$.

magnetizing inductor L_{m2} is discharging. The clamp capacitor C_c transfers its energy to the multiplier capacitor C_m through the regenerative diode D_r and the secondary windings of the coupled inductors. The output capacitor C_o supplies the load at this state. The following equations can be written in this state of operation:

$$i_{Lm1}(t) = I_{Lm1}(t_0) + \frac{V_{\text{in}}}{L_{m1}}(t - t_0) \tag{1}$$

$$i_{Lk1}(t) = I_{Lk1}(t_0) + \frac{V_{Cc} - V_{Cm}}{nL_{k1}}(t - t_0). \tag{2}$$

State 2 $[t_1 - t_2]$*:* At $t = t_1$ the turn ON signal is applied to the main switch S_2 when its antiparallel diode is conducting, so the ZVS turn ON condition is achieved for the main switch S_2. Furthermore, the magnetizing inductor L_{m2} and leakage inductor L_{k2} are charging in this state. The other circuit conditions are the same as in the last time interval

$$V_{Sc1} = V_{Sc2} = V_{Cc} \tag{3}$$

$$i_{Lm2}(t) = I_{Lm2}(t_1) + \frac{V_{\text{in}}}{L_{m2}}(t - t_1) \tag{4}$$

$$i_{Lk2}(t) = I_{Lk2}(t_1) + \frac{V_{Cm} - V_{Cc}}{nL_{k2}}(t - t_1). \tag{5}$$

State 3 $[t_2 - t_3]$*:* At $t = t_2$ the regenerative diode D_r is turned OFF at ZCS condition, which effectively alleviate the reverse-recovery loss. At the end of this state the main switch S_1 is turned OFF. Other circuit conditions are the same as in the last time interval.

State 4 $[t_3 - t_4]$*:* At the beginning of this state the main switch S_1 is turned OFF, then the parallel capacitor C_{s1} and the leakage inductance L_{k1} starts to resonate. Due to the small size of the switch parallel capacitor, the leakage inductor discharges linearly, and hence the voltage across the main switch S_1 increases from zero with a constant slope, which allows ZVS operation reducing turn OFF loss. Furthermore, the output diode D_o is turned ON with ZCS condition at $t = t_3$, which alleviates the turn ON losses. The multiplier capacitor C_m and secondary windings of the coupled inductors discharge through the output diode D_o to charge the output capacitor and supply the load. The other circuit conditions are the same as in the last time interval.

State 5 $[t_4 - t_5]$*:* At $t = t_4$, the voltage of C_{s1} reaches to the voltage of C_c, thus, the antiparallel diode of the clamp switch S_{c1} starts to conduct and the magnetizing inductor L_{m1} and leakage inductor L_{k1} give their energy to charge the clamp capacitor C_c. As a result, the clamp voltage of the switch S_1 clamped effectively without ringing and spike problems. The other circuit conditions are the same as in the last time interval. The following equations can be written in this state:

$$i_{Lm1}(t) = I_{Lm1}(t_4) + \frac{V_{\text{in}} - V_{Cc}}{L_{m2}}(t - t_4) \tag{6}$$

$$i_{Lk1}(t) = I_{Lk1}(t_4) + \frac{V_o - V_{Cm} - (n\ +\ 1)V_{Cc}}{nL_{k1}}(t - t_4) \tag{7}$$

$$i_{Lk2}(t) = I_{Lk2}(t_4) + \frac{V_{Cm} + (n\ +\ 1)V_{Cc} - V_o}{nL_{k2}}(t - t_4). \tag{8}$$

State 6 $[t_5 - t_6]$*:* At $t = t_5$ when the antiparallel diode of the clamp switch S_{C1} is conducting the turn ON signal is applied to the clamp switch S_{c1}, thus, ZVS turn ON can be achieved for the clamp switch. Other circuit conditions are the same as the last time interval. The voltage stress across the main switch can be written as

$$V_{S1} = V_{Cc}. \tag{9}$$

State 7: $[t_6 - t_7]$*:* The clamp switch S_{C1} is turned OFF at $t = t_6$. After that, the leakage inductor L_{k1} and parallel capacitor C_{S1} starts to resonate. Because of the small size of the parallel capacitor, current changes almost linearly in the leakage inductance, and as it is said in state 4, the voltage across the main switch S_1 decreases to zero with a constant slope and the voltage across the clamp switch increases with a constant slope from zero. As a result, the ZVS condition is achieved and the turn OFF loss of the clamp switch decreases. In addition, the leakage inductance L_{k1} change its current direction in this state. The other circuit conditions are the same as in the last time interval.

State 8 $[t_7 - t_8]$*:* When the voltage across the parallel capacitor C_{S1} reaches zero the antiparallel diode of the main switch S_1 starts to conduct. Moreover, the stored energy in leakage inductor (L_{k1}) is discharged linearly by the coupled inductor primary voltage, which also controls the current falling rate of the output diode D_o. The other circuit conditions are the same as in the last time interval.

State 9 $[t_8 - t_9]$*:* At $t = t_8$ the turn ON signal is applied to the main power switch S_1 when its antiparallel diode is conducting, thus, ZVS is achieved for the main switch S_1. The leakage inductor L_{k1} changes its direction and the input voltage source V_{in} charges the magnetizing inductor L_{m1} and leakage inductor L_{k1}. Other circuit conditions are the same as in the last time interval.

State 10 $[t_9 - t_{10}]$*:* At $t = t_9$ the output diode D_o is turned OFF at ZCS condition, which alleviates reverse-recovery problem. At this state, the proposed converter operates like in State 3.

State 11 $[t_{10} - t_{11}]$*:* At $t = t_{10}$ the main switch S_2 is turned OFF, then the parallel capacitor C_{s2} and leakage inductance L_{k2} starts to resonate. Because the leakage inductance is larger than the parallel capacitor the voltage across the main switch S_2 increases from zero with a constant slope, which allows ZVS operation and reduces the turn OFF loss. Furthermore, the regenerative diode D_r is turned ON at ZCS condition and the clamp capacitor C_c transfers its energy to the multiplier capacitor C_m. The other circuit conditions are the same as in the last time interval.

State 12 $[t_{11} - t_{12}]$*:* At $t = t_{11}$, the voltage of the C_{s2} reaches to the voltage of C_c, thus, the antiparallel diode of the clamp switch S_{c2} is conducting and the magnetizing inductor L_{m2} and leakage inductor L_{k2} give their energy to charge the clamp capacitor C_c. As a result, the voltage of S_2 clamped and the leakage inductor energy is recycled, which not only mitigate the voltage stresses across the main switch, but also increases the efficiency. The other circuit conditions are the same as in the last time interval.

State 13 $[t_{12} - t_{13}]$*:* At $t = t_{12}$, the antiparallel diode of the clamp switch S_{C2} is conducting from the previous stage, then the turn ON signal is applied to the clamp switch, thus, ZVS turn ON can be achieved for the clamp switch. Other circuit conditions are the same as in the last time interval. Following equations can be written for this state of operation:

$$V_{S2} = V_{Cc} \tag{10}$$

$$i_{Lm2}(t) = I_{Lm2}(t_{12}) + \frac{V_{\text{in}} - V_{Cc}}{L_{m2}}(t - t_{12}) \tag{11}$$

$$i_{Lk2}(t) = I_{Lk2}(t_{12}) + \frac{V_{Cm} - (n\ +\ 1)V_{Cc}}{nL_{k2}}(t - t_{12}). \tag{12}$$

State 14 $[t_{13} - t_0]$*:* The clamp switch S_{C2} is turned OFF at $t = t_{13}$. After that the leakage inductor L_{k2} and parallel capacitor C_{S2} start to resonate again. Because of the larger size of the leakage inductor L_{k2} compared to the parallel capacitor C_{S2}, the voltage across the main switch S_2 decreases to zero with a constant slope and voltage across the clamp switch increases with a constant slope from zero. Thus, the turn OFF losses of the clamp switch decreases. At the end of this time interval the

voltage across the parallel capacitor C_{S2} reaches zero and the antiparallel diode of the main switch S_2 starts to conduct and the proposed converter begins a new switching cycle.

B. Voltage Gain Derivation

In order to simplify the voltage gain derivation, the effects of the leakage inductance and parallel capacitor of the main switches have been neglected. By applying volt–second balance to the magnetizing inductor L_{m2} during the turn ON and OFF states of S_2, the voltage across the clamp capacitor can be achieved as (13), which is identical to the output capacitor of a boost converter

$$V_{Cc} = \frac{V_{\text{in}}}{1 - D}. \tag{13}$$

In (13), D is the duty cycle of the main switches. By applying Kirchhoff's Voltage Law (KVL) in State 12 and considering (13) the voltage stress across the multiplier capacitor C_m can be derived as

$$V_{Cm} = V_{Cc} + nV_{\text{in}} + n\left(V_{Cc} - V_{\text{in}}\right) = \frac{(n + 1)V_{\text{in}}}{1 - D}. \tag{14}$$

By applying KVL in State 6, and considering (13) and (14), it can be found that the voltage across the multiplier capacitor is half of the output voltage ($V_{Cm} = V_o/2$), and hence the ideal voltage gain can be written as

$$M = \frac{V_o}{V_{\text{in}}} = \frac{2(n + 1)}{1 - D}. \tag{15}$$

In order to consider the leakage inductance effect into the voltage gain, the rising and falling slope of the current of the output diode D_o can be used to derive the voltage gain including the leakage inductance effect. Considering m_r as the rising slope and m_f as the falling slope of the output diode current the following equations can be written:

$$\frac{di_{Do}}{dt} = m_r = \frac{V_o - (n + 1)V_{Cc} - V_{Cm}}{L_{Lk}} \tag{16}$$

$$\frac{di_{Do}}{dt} = m_f = \frac{V_o - V_{Cm}}{L_{Lk}} \tag{17}$$

where $L_{Lk} = n^2(L_{k1} + L_{k2})$.

From the steady-state analysis and (16) the peak current of the output diode can be written as

$$I_{Do(\text{peak})} = m_r t_r = \left[\frac{V_o - (n + 1)V_{Cc} - V_{Cm}}{L_{Lk}}\right](1 - D)T_s \tag{18}$$

where T_S and t_r are switching period and rise time, respectively.

Furthermore, the fall time t_f of the output current from (17) and (18) can be written as

$$t_f = \left[\frac{V_o - (n + 1)V_{Cc} - V_{Cm}}{V_{Cm} - V_o}\right]. \tag{19}$$

From the current stress analysis and considering the output current diode as a triangle the following equation can be written as

$$I_{Do(\text{avg})} = I_o = \frac{1}{2}\frac{t_r + t_f}{T_s} I_{Do(\text{peak})}. \tag{20}$$

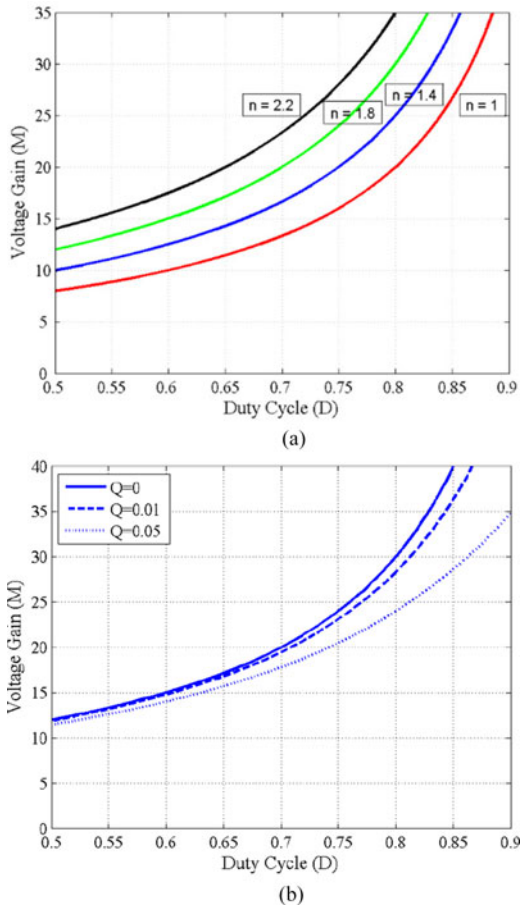

Fig. 6. Voltage gain of the proposed converter versus duty cycle, (a) under various turns ratio and (b) with n = 2 including nonidealities and different Q factors.

From (16) to (20), the voltage gain of the proposed converter with the leakage inductance effect can be written as

$$M = \frac{V_o}{V_{\text{in}}} = \frac{4(n + 1)}{1 - D + \sqrt{(1 - D)^2 + \frac{16n^2(L_{k1} + L_{k2})}{T_S R_o}}} \tag{21}$$

where R_o is the load of the proposed converter.

When the leakage inductances are neglected the voltage gain is the same as given in (15). From (21) it can be derived that the voltage gain is affected not only by the turns ratio and duty cycle, but also by the leakage inductance, output load, and switching frequency. By assuming an equal leakage inductance for both coupled inductors ($L_{k1} = L_{k2} = L_k$), (21) can be rewritten as

$$M = \frac{V_o}{V_{\text{in}}} = \frac{4(n + 1)}{1 - D + \sqrt{(1 - D)^2 + Q}}. \tag{22}$$

In (22), $Q = 32\, n^2 L_k / T_s R$ is the factor that represents the effect of leakage inductance. Fig. 6(a) illustrates the ideal voltage gain plot with several turns ratio. It can be inferred that the turns ratio has a significant impact on increasing the voltage gain of the proposed converter. Moreover, a high step-up voltage gain can be realized without any extreme duty cycle or high turns ratio. Fig. 6(b) illustrates the voltage gain versus duty

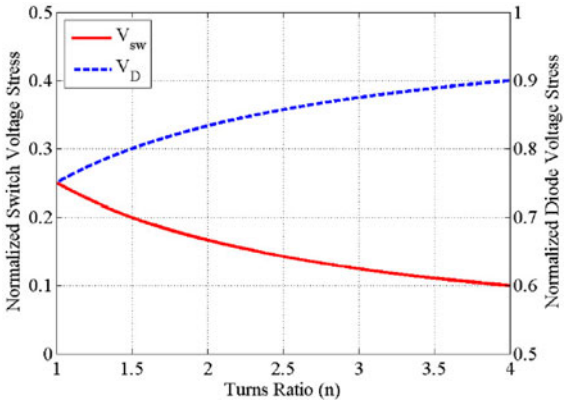

Fig. 7. Normalized voltage stresses for all switches and diodes versus turns ratio.

cycle plot for turns ratio of $n = 2$ and considering the effect of nonidealities such as leakage inductance and load by means deviations in Q factor. In order to simplify the voltage and current analysis in the following subsections, ideal coupling with zero leakage inductance has been considered for coupled inductors.

C. Voltage Stress Across the Semiconductors

From the steady-state analysis it can be seen that the voltage across all the power switches during their turn OFF period is equal to the voltage of the clamp capacitor, thus, from (3), (9)–(10), and (13) it is found that the maximum voltage across all active switches are identical ($V_{\rm SW}$) and they can be derived as

$$V_{\rm SW} = \frac{V_{\rm in}}{1 - D} = \frac{V_o}{2\,(n + 1)}. \tag{23}$$

From (23), it can be seen that the voltage stress across the active switches is much lower than the output voltage, and hence low $r_{DS(\rm on)}$ switches can be used for the active switching devices. From (13) and (15), the maximum voltage across the diodes can be written as

$$V_{Dr} = V_{Do} = \frac{(2n + 1)\,V_{\rm in}}{1 - D} = \frac{(2n + 1)}{(2n + 2)}V_o. \tag{24}$$

A comparison of the voltage stress for all switches and diodes is shown in Fig. 7. It can be seen that the voltage stresses of all switches are much lower than the output voltage. Moreover, the voltage stresses of the diodes are lower than the output voltage. Since the voltage stress of all switches are much lower than the output voltage, low ON-state resistance switches can be used that reduce the conduction loss and help to improve the efficiency.

D. Current Stress Analysis

From the steady-state analysis in the previous section, the average current, which flows through the diodes, is equal to output current I_o and peak current of the diodes can be expressed as

$$I_{Dr(\rm peak)} = I_{Do(\rm peak)} = \frac{2I_o}{1 - D}. \tag{25}$$

Therefore, the current stresses of the diodes increase as the duty cycle of the main switches increases.

From the equivalent circuit of the proposed converter, the secondary side of both coupled inductors are in series with the multiplier capacitor, hence the following equations can be written by applying ampere–second balance for multiplier capacitor

$$I_{Cm(\rm avg)} = 0 \rightarrow I_{\rm sec} = I_{N2b(\rm avg)} = I_{N2a(\rm avg)} = 0. \tag{26}$$

It should be noted that the secondary current of both coupled inductors that are equal are indicated by $I_{\rm sec}$ in the following of this paper. Considering the relationship between the primary and secondary currents in coupled inductors the following equation can be written as

$$I_{N1a(\rm avg)} = I_{N1b(\rm avg)} = nI_{Cm(\rm avg)} = 0. \tag{27}$$

By considering the input parallel structure of the proposed converter and neglecting the power losses, the average current through the magnetizing inductors can be written as

$$I_{Lm1(\rm avg)} = I_{Lm2(\rm avg)} = 0.5I_{\rm in(avg)} = \frac{(n + 1)\,I_o}{1 - D}. \tag{28}$$

From steady-state analysis, the current stresses on the main switches can be derived as

$$I_{S1(\rm peak)} = 0.5I_{\rm in(avg)} + nI_{Dr(\rm peak)} + I_{Dr(\rm peak)} = \frac{(n + 1)\,I_o}{1 - D} + \frac{2nI_o}{1 - D} + \frac{2I_o}{1 - D} = \frac{3I_o\,(n + 1)}{1 - D} \tag{29}$$

$$I_{S2(\rm peak)} = 0.5I_{\rm in(avg)} + nI_{Do(\rm peak)} = \frac{(n + 1)\,I_o}{1 - D} + \frac{2nI_o}{1 - D} = \frac{I_o\,(3n + 1)}{1 - D}. \tag{30}$$

For the clamp switches the current stresses can be derived as

$$I_{Sc1(\rm peak)} = I_{Sc2(\rm peak)} = 0.5I_{\rm in(avg)} = \frac{(n + 1)\,I_o}{1 - D}. \tag{31}$$

Moreover, the rms current of the main switches and active clamp switches can be derived by

$$I_{S1(\rm RMS)} = (n + 1)\,I_o\sqrt{\frac{(2D - 1)}{(1 - D)^2} + \frac{13}{3\,(1 - D)}} \tag{32}$$

$$I_{S2(\rm RMS)} = I_o\sqrt{\left(\frac{n + 1}{1 - D}\right)^2(2D - 1) + \frac{10n^2 + 9n + 3}{3\,(1 - D)}} \tag{33}$$

$$I_{SC1(\rm RMS)} = \frac{I_o\,(n + 1)}{\sqrt{3\,(1 - D)}} \tag{34}$$

$$I_{SC2(\rm RMS)} = I_o\sqrt{\frac{3(n + 1)^2 + (2n + 1 - D)^2 - 3\,(n + 1)\,(2n + 1 - D)}{3\,(1 - D)}}. \tag{35}$$

A comparison of the RMS current stress of main and clamp switches is shown in Fig. 8. It can be seen that for a given voltage gain, switches rms current increase by increasing in the turns ratio of the coupled inductor. This means that a higher duty cycle is beneficial for reducing conduction loss of the switches.

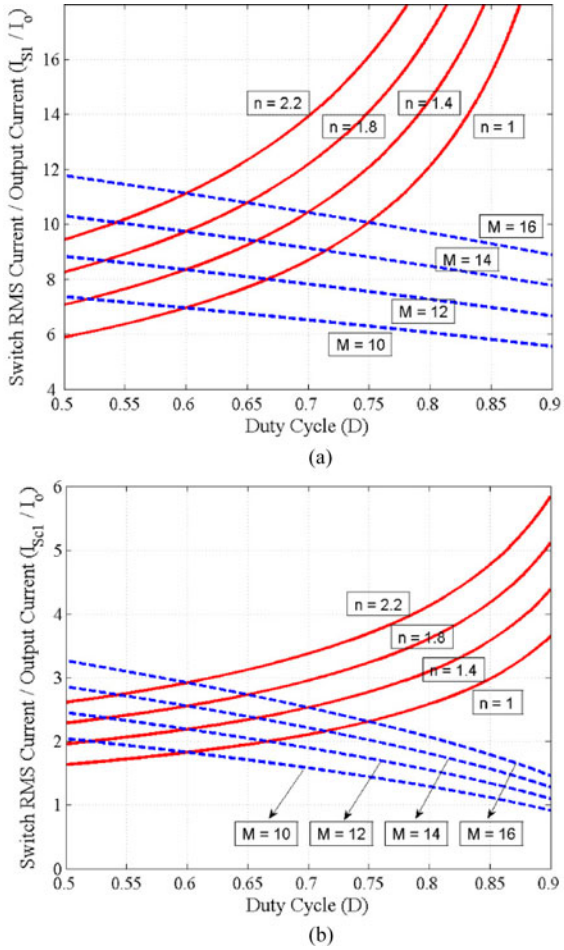

Fig. 8. Normalized rms current versus duty cycle plot of (a) main switch S_1 and (b) clamp switch S_{C1}.

By rearranging the voltage gain equation for n and substituting in (29) and (30), it can be seen that for a given voltage gain the variation in duty cycle has almost no effect on the switch current stress. Considering Fig. 8, it is clear that for given voltage gain a turns ratio between 1 and 1.4 can be beneficial for reducing switch rms current stress and their power loss.

E. Soft-Switching Performance

One of the advantages of the proposed converter is that it allows soft switching for all the semiconductors, which reduces the power losses in the switching devices and, thus, improves the conversion efficiency. The ZVS turn ON for the clamp switches can be realized by applying the turn-on signal gate when their antiparallel diodes are in the ON state during State 5 and State 12 for the clamp switches S_{C1} and S_{C2}, respectively. To achieve ZVS turn ON for the main switches, the stored energy in the leakage inductances in State 7 and State 14 should be more than that of the parallel capacitor for the main switches S_1 and S_2, respectively. The ZVS turn ON condition for the main switches by neglecting the power losses in the proposed converter can be written in the following equation as:

$$\frac{1}{2}L_{ki}I^2_{\text{in(avg)}} \geq \frac{1}{2}\,C_{Si}V^2_{CS1} \quad for \;\; i = 1.2. \tag{36}$$

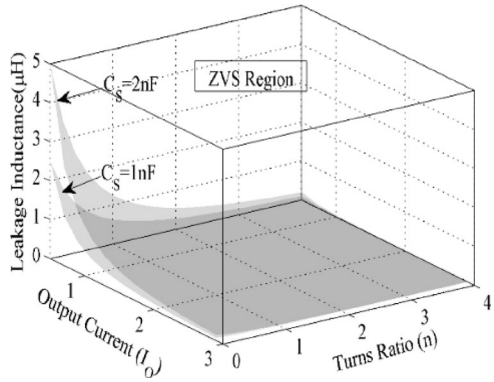

Fig. 9. A 3D plot for ZVS region in the proposed converter with $V_{in} = 50$ V, $C_S = 1\ nF$ and $C_S = 2\ nF$.

Considering (15) and a lossless condition for the converter ($P_{\text{in}} = P_{\text{out}}$), (36) can be rewritten as

$$4L_{ki}I_o^2(n\ +\ 1)^2 \geq C_{Si}V^2_{\text{in}} \;\; for \;\; i = 1.2. \tag{37}$$

From (37), the ZVS region of the proposed converter can be derived based on output current and input voltage. The leakage inductance versus output current (I_o) and turns ratio (n) with $V_{\text{in}} = 50$ V, $C_S = 1$ nF and $C_S = 2$ nF is shown in Fig. 9. It can be seen that as the turns ratio and the output current increases, the soft switching region extends. Another way to enlarge the ZVS region is to increase the leakage inductance. This is important because we have ZVS condition only if the inductive stored energy in the leakage inductance were equal or larger than the capacitive stored energy in the parasitic capacitor of the switch. On the other hand, increasing the leakage inductance has detrimental effect on the voltage conversion performance. Hence, in practice a tradeoff should be considered to fulfill the required voltage ratio, while maintaining a high conversion efficiency.

The diodes D_r and D_o current falling rate are controlled by the leakage inductances of the both coupled inductors, which alleviates the diodes reverse-recovery problem, reduces the electromagnetic interference noise and improves the circuit efficiency. From a steady-state analysis, the output diode D_o turn-off current falling rate can be expressed as

$$\frac{di_{Do}}{dt} = \frac{-V_o}{4n^2L_k}. \tag{38}$$

From a similar derivation the current falling rate of the regenerative diode D_r is given by

$$\frac{di_{Dr}}{dt} = \frac{-V_o}{4n\,(n\ +\ 1)\,L_k}. \tag{39}$$

From (38) and (39), it can be seen that the reverse-recovery problem can be alleviated effectively by employing a small leakage inductance as the turns ratio increases. To alleviate the reverse-recovery on the diode effectively, di/dt should be less than 100 A/μs [33]. From (38) and (39), the minimum leakage inductances that guarantee a di/dt below 100 A/μs are derived as 167 and 250 nH for diodes D_r and D_o, respectively.

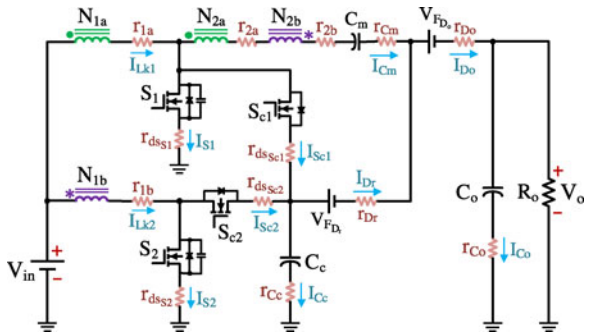

Fig. 10. Equivalent circuit including power losses of the proposed converter.

F. Efficiency Analysis

Practically, there are conduction losses caused by parasitic resistance of the circuit elements. Therefore, the conduction losses affect the voltage gain and efficiency. The equivalent circuit of the proposed converter including the parasitic resistances is shown in Fig. 10, where r_{ds_Sx} is the power switches ON-state resistance, V_{F_Dx} is the diode forward voltage, r_{Dx} is the diode resistance, r_{1x} and r_{2x} are series resistance of the coupled inductors, and r_{Cx} is the (equivalent series resistance) ESR of the capacitors. It should be noted that in all the mentioned subscripts, the respective components would be substituted with the term x. In order to evaluate the impact of these parasitic parameters, the leakage inductances of both coupled inductors are assumed to be zero.

Power losses of the proposed dc–dc converter include loss related to switches, diodes, capacitors, and magnetic components. Switch losses comprises switching ($P_{\mathrm{ON-OFF}}$) and conduction losses (P_{rS}). Hence, the total power loss in the power switch can be written as

$$P_{\mathrm{SW}} = P_{rS} + P_{\mathrm{ON-OFF}}. \tag{40}$$

The conduction loss in a power switch (MOSFET) is due to the resistance of the switch during conduction time, which can be expressed as

$$P_{rS} = r_{ds(\mathrm{on})} \times I^2_{\mathrm{SW(RMS)}} \tag{41}$$

where $r_{ds(\mathrm{on})}$ is the resistance of switch during turn ON period.

The switching power loss during turn ON and OFF time of the switching devices is another part of the switch loss. Due to ZVS operation of the main and clamp switches and ZCS operation of both diodes, the switching losses are neglected in the efficiency calculation.

The diodes power loss comprises of a small resistive conduction loss and the loss related to the forward voltage. The diode currents in one switching cycle can approximately be written as

$$i_D = i_{Do} = i_{Dr} = \begin{cases} 0 & 0 < t \le DT \\ \frac{2I_o}{(1-D)^2}t & DT < t \le T \end{cases}. \tag{42}$$

Moreover, its rms value can be derived as

$$I_{D(\mathrm{RMS})} = I_{Dr(\mathrm{RMS})} = I_{Do(\mathrm{RMS})} = \frac{2I_o}{\sqrt{3\,(1\,-\,D)}}. \tag{43}$$

Hence, the conduction resistive loss and the loss related to the forward voltage can be written as given in following equations:

$$P_{rF} = r_D \times I^2_{D(\mathrm{RMS})} \tag{44}$$

$$P_{VF} = V_F \times I_{D(\mathrm{avg})}. \tag{45}$$

Thus, the total diode conduction loss can be written as

$$P_D = P_{VF} + P_{rF}. \tag{46}$$

The current through capacitor C_o is approximately given by

$$i_{Co} = \begin{cases} -I_o & 0 < t \le DT \\ \frac{2I_o}{(1-D)^2}t - I_o & DT < t \le T \end{cases}. \tag{47}$$

Moreover, the rms current of the output capacitor can be derived by

$$I_{Co(\mathrm{RMS})} = I_o\sqrt{\frac{4}{3\,(1\,-\,D)} + D}. \tag{48}$$

The current of the other capacitors can be written similar to (47), and hence their rms current can be derived by

$$I_{Cc(\mathrm{RMS})} = (n\,+\,1)\,I_o\sqrt{\frac{2}{3\,(1\,-\,D)}} \tag{49}$$

$$I_{Cm(\mathrm{RMS})} = 2I_o\sqrt{\frac{2}{3\,(1\,-\,D)}}. \tag{50}$$

Thus, the power losses due to ESR of the capacitors can be derived as

$$P_{rC} = \mathrm{ESR} \times I^2_{C(\mathrm{RMS})}. \tag{51}$$

The current, which passes through the primary and secondary windings of the coupled inductors, causes power losses due to the winding parasitic resistances. To obtain the primary side power losses, the leakage inductances current in one switching cycle can be written like (42) and (47) and its rms value can be expressed as (52) as shown at the bottom of the next page.

The total power losses in the primary and secondary windings can be written as

$$P_{\mathrm{wire}} = (r_{1a} + r_{1b}) \times I^2_{Lk(\mathrm{RMS})} + (r_{2a} + r_{2b}) \times I^2_{Cm(\mathrm{RMS})}. \tag{53}$$

In addition, there are some power losses in the cores of coupled inductor, which depend on the core volume and core type. Thus, the total power losses of the coupled inductors can be written as

$$P_{rL} = P_{\mathrm{wire}} + P_{\mathrm{Core}}. \tag{54}$$

The total power loss of the proposed converter can be expressed as

$$P_{\mathrm{Loss}} = P_{\mathrm{SW}} + P_D + P_{rC} + P_{rL}. \tag{55}$$

Hence, the efficiency of the proposed converter can be calculated from

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{out}} + P_{\mathrm{Loss}}} \tag{56}$$

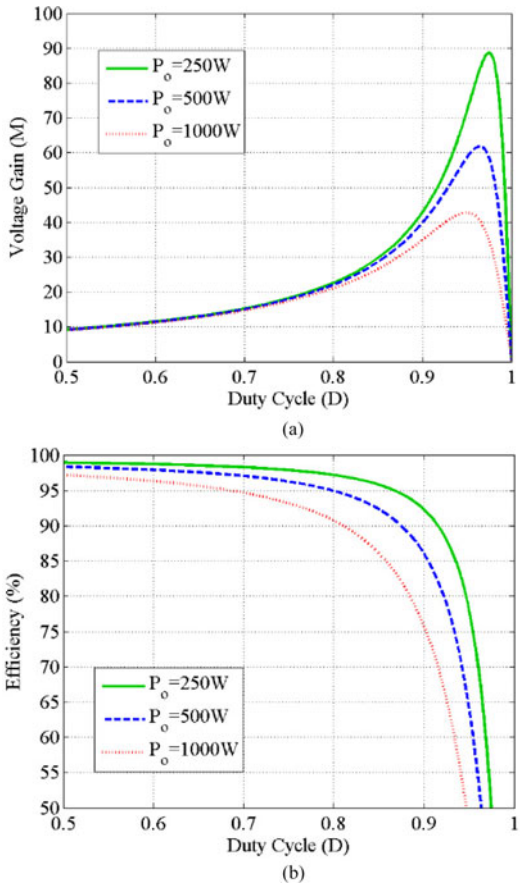

Fig. 11. Theoretical calculations of the proposed converter at various output powers, (a) voltage gain versus duty cycle and (b) efficiency versus duty cycle.

and the voltage conversion ratio of the converter including the conduction losses can be calculated from

$$M = \eta \times \frac{2\,(n\ +\ 1)}{1\ -\ D}. \tag{57}$$

The voltage gain and efficiency plots of the proposed converter versus duty cycle at different output powers have been shown in Fig. 11. The specifications of the proposed converter used in these figures have been assumed to be $V_{\rm in} = 40$, $V_o = 400$ V, $n = 1.33$, $r_{1a} = r_{1b} = 30$ mΩ, $r_{2a} = r_{2b} = n \times r_{1a}$, $r_{dS1} = r_{dS2} = r_{dsSc1} = r_{dsSc2} = 7.6$ mΩ, $r_{Dr} = r_{Do} = 16.5$ mΩ, $V_{FDo} = V_{FDr} = 0.84$ V, $r_{Cc} = r_{Cm} = 22$ mΩ, r_{Co}= 260 mΩ.

G. Performance Comparison

Table I provides a comprehensive summary of the main circuit features of the proposed converter and the most related and recent studies from the literature. These converters are mainly interleaved or other having input parallel structures of dc–dc converters, where their main features such as voltage gain, switch and diode voltage stresses, total number of components, input current ripple, switching condition, and common ground connection between the input and output of the converter have been compared.

From Table I, it can be seen that the voltage gain and main switch voltage stress of similar converters in [27], [28], [30]–[32] are identical to the voltage gain of the proposed converter, which indeed is advantageous to the converter in [23], [25], and [29]. Regarding the input current ripple it should be noted that their input current have been compared in case of assuming identical input inductance (as a single or a magnetizing of coupled inductors), switching frequency, output voltage, and power. Moreover, only the converters with an active clamp circuit have the feature of ZVS, which can significantly reduce the switching loss and heat sink requirement in which the overall can improve the power density and reliability of the proposed converter. The proposed dc–dc converter has a step up capability as high as of similar topologies with minimum total number of components and common ground connection between the input and output, which is a critical factor for front-end step-up dc–dc modules of grid tied transformer-less inverters. The mentioned features allow an efficient low-cost, low volume, and high power density implementation of step-up dc–dc converters for grid-connected PV applications.

III. Design Consideration and Experimental Results

Many factors affect the optimal design of a dc–dc converter such as cost, size/volume, efficiency, and power density. Once the specifications of a practical system is determined, the proposed converter can be designed based on the given requirements, such as output voltage, input voltage variation, input current ripple, and power level/density. The design considerations provided in this section are based on the analysis presented in the previous section, which include coupled inductor and capacitor designs followed by a selection guide of semiconductors. Moreover, the experimental results of a laboratory prototype have been provided to validate the performance and mentioned features of the proposed dc–dc converter.

A. Coupled Inductors Design

1) Turns Ratio of the Coupled Inductors: Considering the demanded voltage gain and allowable operating range, the duty cycle of the proposed converter can be defined according to the design criteria. From the aforementioned steady-state analysis of the proposed converter, the duty cycle of main switches has a minimum limitation and should exceed 0.5. Once the proper duty cycle range has been selected, the turns ratio can be calculated from (58) that determines its maximum permissible value

$$n < \frac{1}{4}\frac{V_{\rm out}}{V_{\rm in}} - 1. \tag{58}$$

$$I_{Lk(\rm RMS)} = I_o\sqrt{\left(\frac{n\ +\ 1}{1\ -\ D}\right)^2 (2D\ -\ 1) + \frac{11n^2 + n\,(10\ -\ D) + 3\,(1\ +\ D) + (1\ -\ D)^2}{3\,(1\ -\ D)}} \tag{52}$$

TABLE I
PERFORMANCE COMPARISON BETWEEN MOST REFERRED CONVERTER AND THE PROPOSED CONVERTER

Converters	Voltage Gain (V_o/V_{in})	Voltage Stress of Main Switches	Voltage Stress of Output Diode(s)	No. of Components			No. of Inductor Cores		Input Current Ripple	Switching Condition	Common Grounded
				S*	D*	C*	Single	Coupled			
Ref. [23]	$\frac{D(2n+1)+1}{1-D}$	$\frac{V_o}{D(2n+1)+1}$	$\frac{2nV_o}{D(2n+1)+1}$	2	3	3	0	2	Small	Hard switching	No
Ref. [25]	$\frac{2}{1-D}+nD$	$\frac{V_o}{2+nD(1-D)}$	$\frac{2V_o}{2+nD(1-D)}$	2	4	3	2	1	Small	Hard switching	Yes
Ref. [27]	$\frac{2(n+1)}{1-D}$	$\frac{V_o}{2(n+1)}$	V_o	4	4	5	2	1	Small	Soft switching (ZVS)	Yes
Ref. [28]	$\frac{2(n+1)}{1-D}$	$\frac{V_o}{2(n+1)}$	$\frac{2n+1}{2(n+1)}V_o$	2	6	5	2	1	Small	Soft switching (ZCS)	Yes
Ref. [29]	$\frac{2+n}{1-D}$	$\frac{V_o}{2+n}$	V_o	2	4	3	2	1	Small	Hard switching	Yes
Ref. [30]	$\frac{2(n+1)}{1-D}$	$\frac{V_o}{2(n+1)}$	$\frac{n}{n+1}V_o$	2	4	4	0	2	Very small	Hard switching	Yes
Ref. [31]	$\frac{2(n+1)}{1-D}$	$\frac{V_o}{2(n+1)}$	$\frac{n}{n+1}V_o$	2	4	4	0	2	Very small	Soft switching (ZCS)	No
Ref. [32]	$\frac{2(n+1)}{1-D}$	$\frac{V_o}{2(n+1)}$	V_o	4	2	4	0	2	Very small	Soft switching (ZVS)	No
Proposed converter	$\frac{2(n+1)}{1-D}$	$\frac{V_o}{2(n+1)}$	$\frac{2n+1}{2(n+1)}V_o$	4	2	3	0	2	Very small	Soft switching (ZVS)	Yes

S – switch; *D* – diode; *C* – capacitor.

Furthermore, the turns ratio of the coupled inductors is a dominant factor that determines the voltage and current stress of the semiconductors. Hence, a compromise should be considered in designing the turns ratio and duty cycle of the proposed converter.

2) Magnetizing Inductance: The input current ripple of the proposed converter can be determined by a proper selection of magnetizing inductances of the coupled inductors. Considering (28) and knowing that the frequency of the input current is twice the switching frequency (f_s), the current ripple of $x\%$ on each magnetizing inductor ($\Delta I_{Lm} = x\% \times I_{Lm}$) results in $(x/4)\%$ current ripple at the input. The minimum magnetizing inductance to guarantee 15% input current ripple can be derived as

$$L_m = L_{m1} = L_{m2} = \frac{V_{\text{in}} D}{x\% I_{Lm} f_s} = \frac{2V_{\text{in}} D}{x\% I_{\text{in}} f_s} = \frac{V_{\text{in}} D\,(1\ -\ D)}{x\%\,(n\ +\ 1)\, I_o f_s} \ \rightarrow\ L_m > \frac{5V_{\text{in}} D\,(1\ -\ D)}{3\,(n\ +\ 1)\, I_o f_s}. \tag{59}$$

3) Leakage Inductance: As mentioned before, the leakage inductance of the coupled inductors determine the soft switching region of the switching devices as shown in Fig. 9 calculated from (36) and (37). Moreover, the current falling rate of the diodes during the turn OFF time can be controlled by (38) and (39). In practice, a tradeoff should be conducted to guarantee sufficient ZVS region and current fall rate of the didoes.

B. Capacitors Design

The voltage ripple suppression on capacitors is the main consideration for the capacitor design. Considering an acceptable voltage ripple of $x\%$ on a capacitor ($\Delta V_C = x\% \times V_C$), the circuit capacitances can be estimated based on the output power, switching frequency, and converter parameters such as duty cycle and coupled inductor turns ratio

$$C_c = \frac{(1\ -\ D)\, I_o}{x\% V_{\text{in}} f_s} \tag{60}$$

$$C_m = \frac{(1\ -\ D)\, I_o}{x\%\,(n\ +\ 1)\, V_{\text{in}} f_s} \tag{61}$$

$$C_o = \frac{(1\ -\ D)\, I_o}{x\%\,(n\ +\ 1)\, 2V_{\text{in}} f_s}. \tag{62}$$

It should be noted that the value of clamp and multiplier capacitors should be selected large enough to prevent forming a resonant tank circuit with the leakage inductance of the coupled inductors in switching intervals, and hence their resonant frequency should be well higher than the switching frequency

TABLE II
POROTYPE PARAMETERS AND COMPONENTS

Parameter	Value/Description
Input voltage (V_{in})	30–40 V
Output voltage (V_o)	400 V
Maximum output power (P_o)	1 kW
Switching frequency (f_s)	50 kHz
Switches (S_1, S_2, S_{c1}, and S_{c2})	IPP076N15N5 (150 V, 112 A, $r_{ds}=$ 7.6 mΩ)
Diodes (D_r and D_o)	DPG15I400 (400 V, 15 A, $V_F = 0.84$ V $r_D = 16.5$ mΩ)
Coupled inductor turns ratio ($N_1 : N_2$)	12:16 - ETD59 ferrite core, N97 material
Magnetizing inductance (L_m)	41 μH
Leakage inductance (L_k)	3.7 μH
Capacitor C_c	3 × 4.7 μF - Film capacitor, ESR = 22 mΩ
Capacitor C_m	5 × 4.7 μF - Film capacitor, ESR = 22 mΩ
Output capacitor (C_o)	2 × 47 μF - Electrolytic capacitor, ESR = 260 mΩ

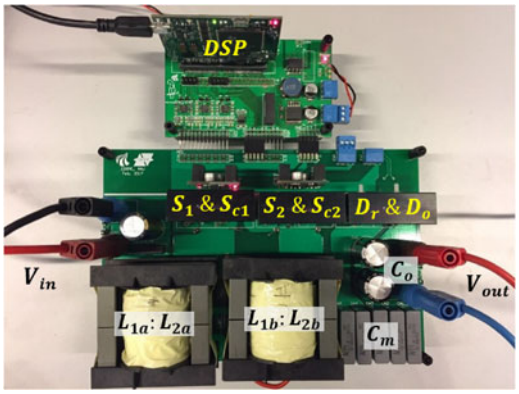

Fig. 12. Photo of the laboratory prototype.

($f_r \gg f_s$). Moreover, a large capacitor can reduce voltage ripple and give low power loss due to its low ESR. Once the capacitance of capacitors are determined, to reduce the power loss in ESRs, a proper solution is to parallel several capacitors to lower their ESR and its associated losses. Unfortunately, a large capacitor results in high cost and volume. Therefore, a compromise should be made between the aforementioned constraints.

C. Selection of Semiconductors

Active and passive semiconductors as switch and diode can be selected based on their voltage and current stresses. The voltage stress across the main and clamp switches and all diodes of the proposed converter can be calculated from (23) and (24), respectively. As mentioned before the average current through all diodes is equal to the output current, and their peak current can be calculated from (25). Furthermore, the current stress of both main and clamp switches can be calculated from (29)–(35). Indeed, a compromise should be considered between the duty cycle and turns ratio of coupled inductors to balance the semiconductors stresses.

D. Experimental Results

A 1-kW laboratory prototype has been built and tested with the specifications defined in Table II. A TMS320F28334 digital signal processor (DSP) was used for implementing modulation and control schemes. Fig. 12 illustrates the experimental setup of the proposed dc–dc converter. The PWM gate pulses for all active switching devices that are generated by the DSP are illustrated in Fig. 13. Implementation of the switching pulses for the first and second legs of the converter is based on two 180° phase shifted timers and the required dead-band for the complementary pulses in each phase was achieved by using the active high complementary function of the DSP [34]. A typical PV power system is shown in Fig. 14, in which the proposed dc–dc converter is used for extracting the maximum power of the PV array or the dc-bus voltage regulation purpose. In practice, two separate tests were conducted in order to verify the feasibility of MPPT operation, and output voltage regulation and steady-state validation of the proposed converter.

1) MPPT Implementation: One of the most important factors related to a PV system is to extract the maximum power

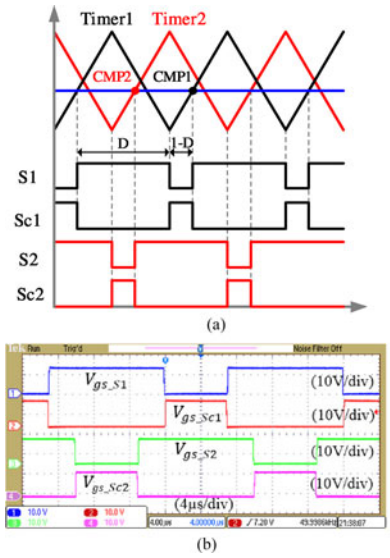

Fig. 13. Gate pulse implementation for active switches, (a) DSP modulation scheme and (b) experimentally obtained gate pulses.

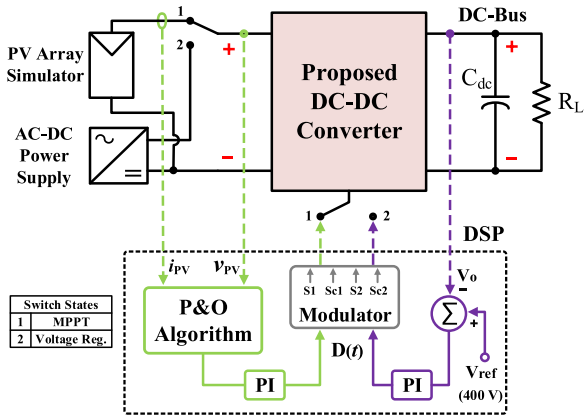

Fig. 14. Illustration of the PV power system and its control diagram.

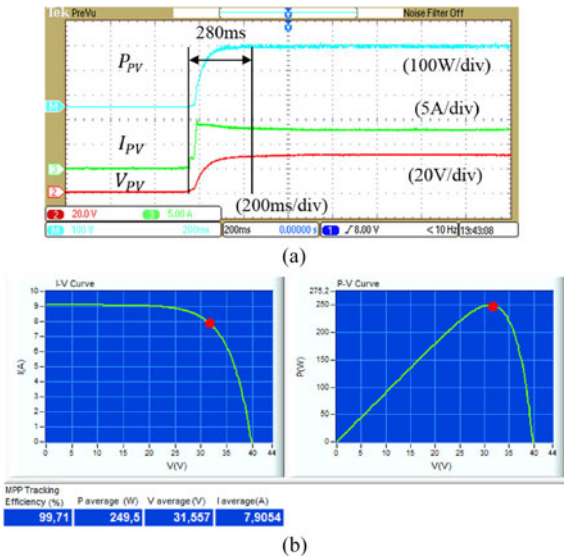

Fig. 15. MPPT test results, (a) dynamic response of the power, current, and voltage of the PV simulator and (b) MPP curves obtained from the PV simulator.

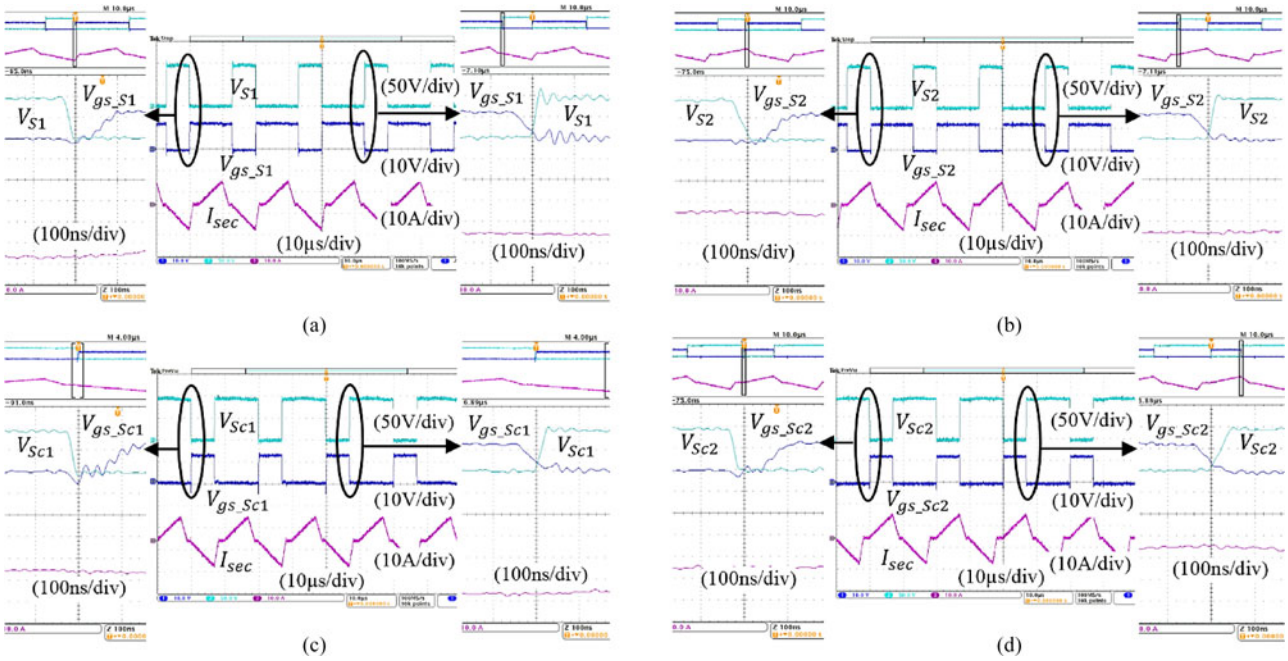

Fig. 16. Experimental soft-switching performance of active switches, (a) drain-source voltage (V_{S1}) and gate-source voltage ($V_{\mathrm{gs\_}S1}$) of S_1, (b) drain-source voltage (V_{S2}) and gate-source voltage ($V_{\mathrm{gs\_}S2}$) of S_2, (c) drain-source voltage (V_{Sc1}) and gate-source voltage ($V_{\mathrm{gs\_}Sc1}$) of S_{c1}, (d) drain-source voltage (V_{Sc2}) and gate-source voltage ($V_{\mathrm{gs\_}Sc2}$) of S_{c2}—the third row in all above subfigures is the coupled inductor secondary current (I_{sec}).

from the PV array. Many MPPT algorithms and techniques investigated before. Among them Perturb and Observe (P&O) technique is a simple and effective method for MPPT implementation with good tracking factor [35]. As indicated in Fig. 14, the MPPT is realized by sensing the current and voltage of PV and implementing P&O algorithm. Moreover, the duty cycle for all switching devices is generated through a proportional-integral (PI) compensator. In the experimental setup, a 62150H-1000S PV simulator is used as the input source and a HAS-50 current sensor is used for measuring the PV current. Due to the current limitation of the PV simulator, this test was conducted using a 250-W resistive load. From Fig. 15(a), it is evident that the MPPT time of the system is about 280 ms for power change from 0 to 250 W. The MPP tracking of the system is illustrated in Fig. 15(b) using the *I–V* and *P–V* curves obtained from the PV simulator. It is clear that the MPP of the PV system is occurred with 31.5 V of PV voltage.

2) Voltage Regulation and Steady-State Verification: In order to verify the steady-state performance of the proposed converter an ac–dc power supply was used as the input source. As indicated in table, the input voltage changes from 30 to 40 V and the output voltage is regulated to be 400 V. Most experimental results are recorded in full load (1 kW) with a 33 V input voltage and 12.12× voltage gain unless otherwise noted. The soft switching performance of all active switches (ZVS) is illustrated in Fig. 16. As it can be seen that the drain-source voltage of main (S_1 and S_2) and clamp (S_{c1} and S_{c2}) switches decrease to zero before they are turned ON. Moreover, it is clear that the drain-source voltage of all switches start to increase only after their gate-source voltage reduces to below the threshold voltage of the switch. Hence, all the active switching devices are turned ON and OFF in ZVS.

The voltage and current of all active and passive switching devices are shown in Fig. 17. The maximum voltage of all active switches is below 100 V, which is in accordance with the calculations from (23). Since the drain-source voltage of all active switches is far below the output voltage, switches with low drain-source ON-state resistance ($r_{ds(\mathrm{on})}$) can be used to reduce the conduction loss of the switching devices. As it can be seen from Fig. 17(a) and (b) the current of the main switches dips before start to increase, which clearly shows the ZVS operation of switching devices. It should be noted that the current of the clamp switches are measured from source to drain of the MOSFETs. Furthermore, the turn OFF losses are also eliminated due to the parallel capacitors of MOSFETs that result in almost no oscillations and no voltage spike problem, which normally exist on the switch in a coupled inductor dc–dc converter. As it can be seen from Fig. 17(c), both diodes turn ON and OFF with slow slopes leading to a ZCS condition that reduces the switching loss and reverse-recovery problem of them. Furthermore, the maximum voltage across both diodes is equal and around 330 V, which is in accordance with the calculations from (24).

The current through the primary and secondary windings of coupled inductors and the input current of the proposed dc–dc converter are shown in Fig. 18(a). It is clear that the input current has a low ripple despite of a small magnetizing inductance (∼40 μH), which is due to the shared input current in a magnetically coupled structure of the proposed converter. As a result, it is obvious that the frequency of input current is twice the switching frequency. The input current ripple is equal to 5 A, which is in accordance with the calculation from (59). Fig. 18(b) illustrates the input and output voltages along with the voltage across clamp and multiplier capacitor. It is clear that the voltage across capacitors C_c and C_m and the output volt-

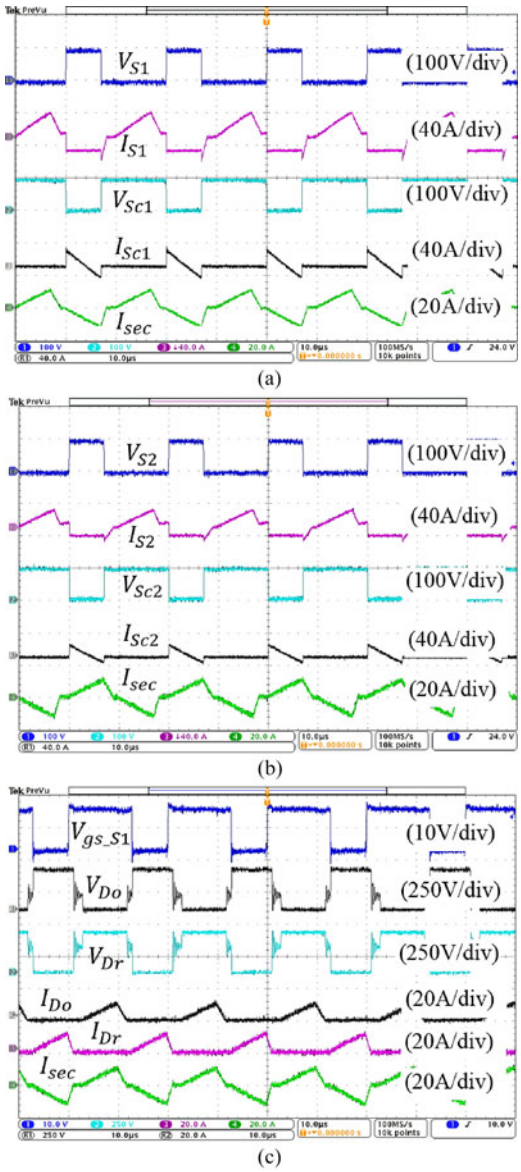

Fig. 17. Experimental voltage and current waveforms of the proposed dc–dc converter, (a) drain-source voltage (V_{S1}) and current (I_{S1}) of S_1, and drain-source voltage (V_{Sc1}) and current (I_{Sc1}) of S_{c1}, (b) drain-source voltage (V_{S2}) and current (I_{S2}) of S_2, and drain-source voltage (V_{Sc2}) and current (I_{Sc2}) of S_{c2}, and (c) gate-source voltage of S_1 ($V_{\mathrm{gs\_}S1}$), voltage across output diode (V_{Do}) and regenerative diode (V_{Dr}), current through output diode (I_{Do}) and regenerative diode (I_{Dr}) and coupled inductor secondary current (I_{sec}).

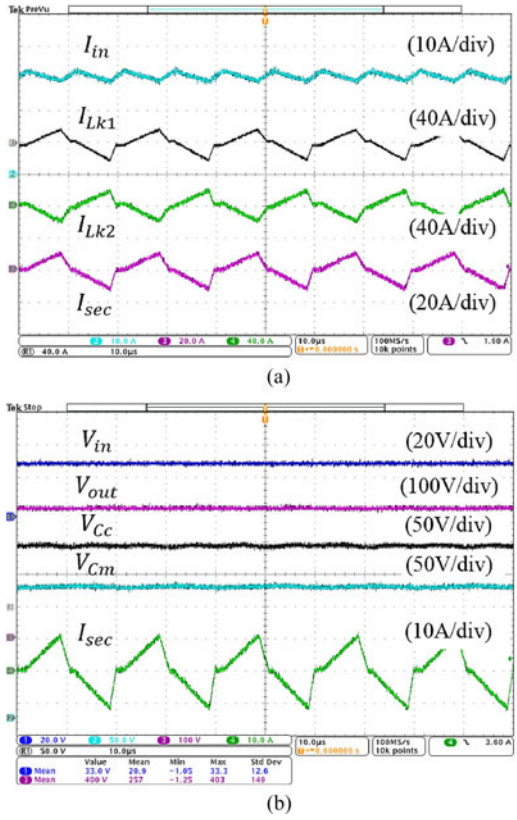

Fig. 18. Experimental voltage and current waveforms of the proposed dc–dc converter, (a) input current (I_{in}), current through L_{k1} (I_{k1}), current through L_{k2} (I_{k2}) and coupled inductor secondary current (I_{sec}), and (b) input voltage (V_{in}), output voltage (V_{out}), voltage across clamp capacitor (V_{Cc}) voltage across multiplier capacitor (V_{Cm}), and coupled inductor secondary current (I_{sec}).

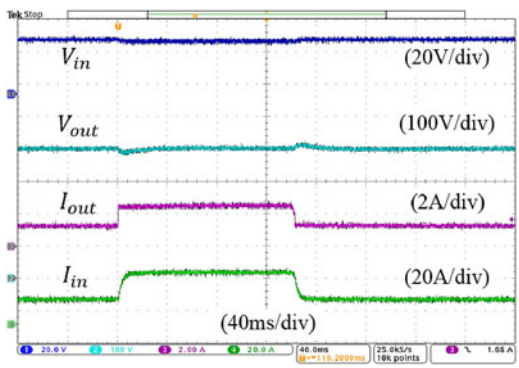

Fig. 19. Dynamic response of the proposed dc–dc converter under step load variation between half load (500 W) and full load (1 kW).

age are around 100, 200, and 400 V, respectively, which are in accordance with the calculations from (13) to (15). Obviously, all experimentally obtained voltage and current measurements illustrated in Figs. 17 and 18 are in accordance with the analysis and calculations available in previous sections.

In order to evaluate the dynamic response of the proposed converter, a load variation from half to full load has been performed. Fig. 19 illustrates the input and output voltages, and input and output currents of the proposed converter within the load variation. It is obvious that the proposed converter performs a fast dynamic response and excellent load regulation in a PI closed-loop control, which shows robustness of the system to a large load variation from 500 W to 1 kW and vice versa.

A high precision power analyzer (PPA5530) is used for efficiency measurements of the proposed converter. Fig. 20 illustrates the measured efficiency curves for two different input voltages. The maximum full load efficiency at 10× voltage gain (40 to 400 V) is 95.2% and the maximum full load efficiency at 13.33× voltage again (30 V to 400 V) is 93.6%. Using (40) to (56) and Table II, and considering 30-mΩ resistance for the primary winding and 3-W core loss for each coupled inductor, the mathematically calculated efficiencies at full load for 10× and 13.33× voltage gains are 96.1% and 94.6%, respectively, which are close to the experimentally measured values.

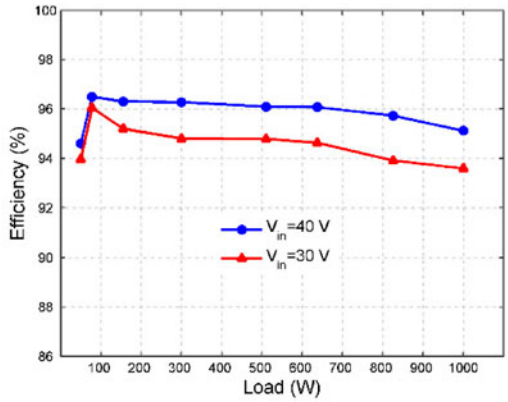

Fig. 20. Power conversion efficiency of the proposed converter for two input voltages under different output powers.

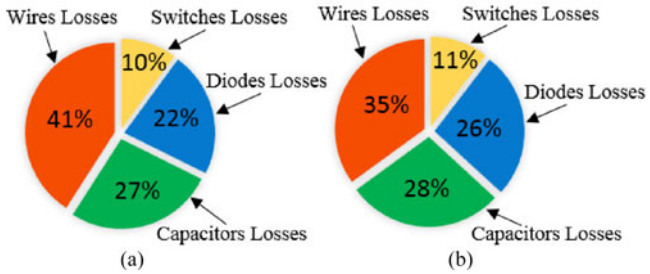

Fig. 21. Pie graph of loss breakdown at full load, (a) $V_{\rm in} = 30$ V and (b) $V_{\rm in} = 40$ V.

Obviously, from Fig. 20 the average conversion efficiency is more than 94%, and its maximum efficiency is 96.6%. Fig. 21 shows loss breakdown of the proposed converter at full load with $V_{\rm in} = 30$ V and $V_{\rm in} = 40$ V. It is clear that dominant power losses in the proposed converter are conduction losses occur in the coupled inductor wires and the capacitors. It should be noted that winding conduction loss gets dominant in high voltage gains and high output powers, which is due to its corresponding high current flow. Therefore, better-graded wires for coupled inductors and higher value capacitors (with lower ESR) can be used to further enhance the conversion efficiency of the proposed converter.

IV. Conclusion

A soft-switching high step-up dc–dc converter has been presented for DG applications. From the detailed operational analysis, mathematical derivations and experimental results of a 1-kW laboratory prototype, the proposed dc–dc converter has the following merits:

1) high-voltage step-up gain and high-power ability due to dual coupled inductor and shared input current structures;
2) low ripple current at the input realized with small magnetizing inductors for the coupled inductors;
3) low ON-state resistance switch implementation for all active switches, due to the reduced voltage stress that is comparatively lower than the output voltage;
4) minimized switching loss due to ZVS operation of the switches and ZCS operation of the diodes;
5) elimination of the turn OFF voltage spike and damaging ringing on the switches that normally exist due to the effect of leakage inductance, which is due to the integrated regenerative snubber and clamp circuits.

Experimental results reveal that the average conversion efficiency of the proposed converter was measured to be higher than 93%, and the maximum efficiency was measured to be 96.6%. It can be concluded that the proposed converter is a suitable candidate for the power conversion of low-voltage renewable energy sources such as in a grid-connected PV system.

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