Distributed Nonlinear Control With Event-Triggered Communication to Achieve Current-Sharing and Voltage Regulation in DC Microgrids

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***Abstract*—A distributed nonlinear controller is presented to achieve both accurate current-sharing and voltage regulation simultaneously in dc microgrids (MGs) considering different line impedances effects among converters. Then, an improved event-triggered principle for the controller is introduced through combining the state-dependent tolerance with a nonnegative offset. In order to design the event-triggered principle and guarantee the global stability, a generalized dc MG model is proposed and proven to be positive definite, based on which Lyapunov-based approach is applied. Furthermore, considering the effects from constant power loads, the damping performance of proposed controller is further improved which is comparative with the traditional V–I droop controller. The proposed event-triggered-based communication strategy can considerably reduce the communication traffic and significantly relax the requirement for precise real-time information transmission, without sacrificing system performance. Experimental results obtained from a dc MG setup show the robustness of the new proposal under normal, communication failure and communication delay operation conditions. Finally, communication traffic under different communication strategies is compared, showing a drastic traffic reduction when using the proposed approach.**

***Index Terms*—Current sharing, distributed nonlinear control, event-triggered communication, generalized dc microgrid (MG) model.**

I. Introduction

With the increasing penetration of renewable energy sources into modern electric grid, the concept of microgrid (MG) is identified as an effective method for future energy systems [1], [2]. Power converter is the key component applied in both ac and dc MGs to interface different sorts of energy resources and loads into the system. Controllability is thus largely enhanced through enabling the application of advanced management strategies. Under the paradigm of distributed generation and consumption, a robust and flexible control scheme is always preferred, while the challenges still exist on distributed information sharing, global stable and system coordination. In dc MGs, since there is no reactive power [3], transformer inrush current, or harmonics, higher power quality and system efficiency can be obtained comparing to ac MGs [4], [5]. Naturally, it is a more efficient method to connect the sources and loads directly to form a dc MG by using dc–dc converters without ac–dc or dc–ac transformations. Categorically, controllers for dc–dc converters in dc MGs shall satisfy two main control objectives: voltage regulation and proportional current sharing [6]–[14], [16].

Voltage–current (V–I) droop control by imposing virtual impedance is widely adopted to achieve communication-less current sharing among converters, but voltage deviations and current sharing errors still exist due to different line resistances [8], [9]. To achieve voltage restoration and accurate current sharing, the centralized secondary controller is applied to achieve voltage regulation and improve current sharing in dc MGs based on the hierarchical control structure [10]. However, loss of any communication link in such centralized communication networks can lead to the failure of the corresponding units, and potentially lead to system-level instability and cascaded failures [11]. Thus, the distributed control algorithm has emerged as an attractive alternative and if designed properly it can offer improved reliability, simplified communication network, reduced communication traffic, and enhanced scalability. In [12], a decentralized control is proposed to achieve the per-unit current sharing through low-bandwidth communication. Then, an improved droop control presented in [13] by using averaged voltage and current values are proposed to improve the current sharing and restore the dc bus voltages, which are developed for a two-converter system and its extension to a multiconverter system is not straightforward. For the methods mentioned above, the broadcast communication strategy as the centralized communication method is used to collect all the information from all the controllers. To decrease the communication traffic, a distributed voltage observer [14] is proposed to generate a voltage correction term adjusting the voltage reference by estimating the averaged voltage value, meanwhile a distributed current regulator provides a virtual impedance correction term based on the consensus-based communication [15]. Furthermore, a noise-resilient distributed voltage observer combined with consensus-based voltage/current regulator is proposed to achieve more resiliency control in dc MGs [16]. The traditional distributed communication strategy among distributed controllers is time-scheduled periodic sampling, which means measurements are

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taken periodically based on a constant sampling period and the controllers are updated synchronously. However, in industrial applications, the communication traffic should be decreased as much as possible due to the limited communication network bandwidth; thus, an efficient use of underlying communication infrastructure is very important from the perspective of system scaling and reliability [17]. In addition, the frequency of updating controllers to change the control values should be also decreased to extend the lifespan of actuators.

Recently, an aperiodic data exchanged communication strategy is proposed which provides the advantage of reduced communication traffic while guaranteeing the requirement performance simultaneously. The aperiodic data exchange can be realized using either event-triggered [18]–[19] or self-triggered approaches [23]. For event-triggered communication, the continuous monitoring of the state variables is required, but the good aspect is that it is unnecessary to send the information periodically. For self-triggered communication, it follows a proactive approach which evaluates the next information exchange instance ahead of schedule. By comparison, the continuous monitoring of the states in event-triggered controller allows it to respond quickly in case of larger disturbances and the self-triggered controller cannot respond immediately to disturbances. To be specific, the principle for the event-triggered communication mechanism is that a sampling execution is triggered when a state measurement error exceeds a given threshold which can be fixed, time-varying [24], or state-dependent tolerance determined by the performance [25]. With the fixed threshold, the controller is more conservative than that with state-dependent tolerance threshold. However, with state-dependent tolerance threshold, the frequency of triggered event is not further decreased under the steady-state stage compared with that under the transient stage. Thus, an improved event-triggered principle should be proposed to achieve less conservative under transient stage and less communication traffic especially under steady-state stage.

In case of ac power system applications, an event-triggered conception combined with the state estimation techniques for the energy management system to achieve power scheduling, while reducing the computational time, was presented [19]. In [20], an event-triggered conception combined with load frequency control model is introduced to properly schedule power generations. Beyond that, in [21], an event-triggered-based optimization algorithm is proposed to achieve optimal power flow. Meanwhile, in [22], a priority-based event-driven communication mechanism is outlined to achieve balance between demand and supply. Considering the applications for ac MGs, the self-triggered communication strategy is applied in [23] to achieve power scheduling.

However, abovementioned proposals use event-triggered-based control for power management purpose on the system-level, so there is no serious dynamic or stability issues in those applications. In addition, although above-mentioned studies achieve basic operation with event-triggered method, they need to be improved in terms of communication traffic reduction and robustness. Besides, for event-triggered-based applications, a detailed analysis of dynamic performance and stability features on the power-electronic level considering the influence from both communication sides and control aspects is still missing in existing literature, while this paper tends to provide both theoretical and experimental evaluation for this purpose. Furthermore, since dc MG is becoming a promising solution for future distribution systems, it is necessary to apply this conception in dc systems in order to evaluate the possibility and performance. Meanwhile, power flow in ac MGs depends on both the voltage phase angles difference and voltage magnitudes difference across the distribution lines, which is totally different from the power flow model in dc MGs. A separate study about event-triggered-based controller for dc MGs is required to achieve the suitable current sharing control and voltage regulation.

In addition, considering stability analysis for dc MGs, linearized system models derived by small signal approximation are analysed in [7] and [12], meanwhile, [14], [16] mainly focus on steady-state stage analysis. Thus, the large signal model for dc MGs should be proposed and analysed under both the transient-state and steady-state stage.

The main technical contributions of this paper are summarized as follows:

1) Considering different line impedances effects among converters, a novel distributed nonlinear controller is proposed to achieve accurate current sharing and voltage regulation simultaneously.
2) Theoretically, the generalized dc model carrying all the details of a dc MG is established and proven to be global definite positive. Combined with the proposed dc MG model, the global stability and convergence for the proposed controller is proven providing a guideline for controller design and system analysis.
3) A novel event-triggered principle, that combines the state-dependent tolerance with nonnegative offset, is proposed to reduce the communication traffic considerably while maintaining the desired control performance. The parameters designed for the event-triggered principle is not related to the system configuration.
4) Considering the effects from constant power loads (CPLs), the damping performance of the proposed controller is improved and compared with the traditional V–I droop controller.
5) Considering practical issues, experimental results are shown to verify the effectiveness of the proposed controller, including control performance comparison, robust performance under communication links failure and communication delay conditions, and communication traffic comparison.

The paper is organized as follows. In Section II, a generalized dc MG model is established. In Section III, a distributed nonlinear current controller is proposed and its stability analysis is provided. In Section IV, combined with the proposed controller, the event-triggered-based communication strategy is designed. In Section V, based on the extended model, the damping performance of proposed controller is improved. And the control coefficients design procedures are also provided. In Section VI, experimental results are presented to prove the

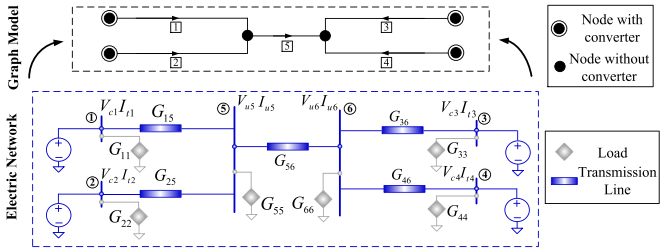


Fig. 1. Schematic representation of the adopted dc MG model.

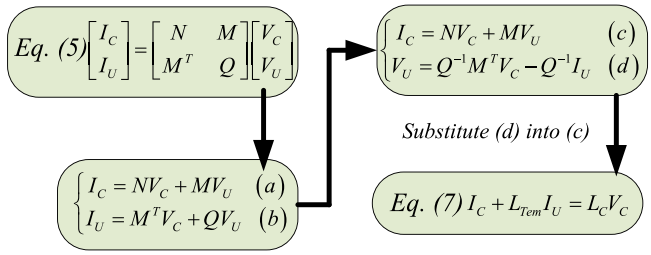


Fig. 2. Kron reduction process (5) to (7).

effectiveness of proposed controller. Finally, the paper is concluded in Section VII.

II. Generalized DC MG Model and Preliminaries

A. Generalized Electrical Network Model for a DC MG

The schematic representation of the adopted dc MG is shown in Fig. 1. In the lower panel of Fig. 1, a circuit representation for a dc MG is given including converters, local, and public loads. In Fig. 1, the conductance branches of distribution lines are represented by G_{15}, G_{25}, G_{36}, G_{46}, G_{56}, the conductance branches of local loads are represented by G_{11}, G_{22}, G_{33}, G_{44}, the conductance branches of public loads are represented by G_{55}, G_{66}, and the numbers in the circles in the lower panel of Fig. 1 represent the number of bus nodes. The upper panel illustrates the adopted graph representation for the same dc MG, based on which the weighted matrix L_W can be written. The numbers in the square box in the upper panel of Fig. 1 represent the number of distribution lines. Meanwhile, the dc MG model neglects the dynamic effects from inductances and capacitances of line impedances and only the resistive effect is considered.

The electrical network of the dc MG can be considered as a weighted graph $G_e = (\nu_e, \varepsilon_e, W)$ with the set of nodes $v_e = \{1, \ldots m, \ldots, n\}$ being m converters and $(n-m)$ uncontrollable nodes in the dc MG, the set of edges $\varepsilon_e \subset \nu_e \times \nu_e$ and the diagonal matrix $W \in R^{|\varepsilon_e| \times |\varepsilon_e|}$ on its diagonal the weights w_{ii} associated to electrical branch $e_i \in \varepsilon_e$ being the conductance of the branch. Without loss of generality, the load branches are not included in the set of edges ε_e.

Given the electrical branch $e_i \in \varepsilon_e$, $\gamma(e_i)$ denote its source node and $\tau(e_i)$ denote its terminal node. Introducing the incidence matrix $B \in R^{|\varepsilon_e| \times |\nu_e|}$, defining via its elements as

$$[B]_{ev} = \begin{cases} -1 & \text{if } v = \gamma(e) \\ 1 & \text{if } v = \tau(e) \\ 0 & \text{otherwise.} \end{cases} \tag{1}$$

The electric topology and the power line parameters are therefore fully carried by the weighted $L_W \in R^{n \times n}$ as

$$L_W = B^T W B. \tag{2}$$

And, based on the direction power flow shown in the upper part of Fig. 1, the matrix B and matrix W can be written in detail as an example which is shown in Fig. 26 in Appendix.

Notice that the direction of the power flow can be in both sides.

Furthermore, denote $V_N \in R^{|v_e|}$ as the voltage vector for converter nodes (controllable nodes) and uncontrollable nodes, the $BV_N \in R^{|\varepsilon|}$ is the vector which can express the component $V_{ni} - V_{nj}$, with $\{i, j\} \in \varepsilon_e$. The current vector $I_B \in R^{|\varepsilon_e|}$ on the branches can be represented as

$$I_B = WBV_N \tag{3}$$

where $V_N = [V_C^T, V_U^T]^T$ in which $V_C = [V_{c1}, \ldots, V_{cm}]^T$ represents the capacitor voltage of converter nodes and $V_U = [V_{u(m+1)}, \ldots, V_{un}]^T$ represents the voltage of uncontrollable nodes, and $I_B = [I_{b1}, \ldots, I_{b|\varepsilon_e|}]^T$ represents the current of all the branches. The current from all the nodes including converter nodes and uncontrollable nodes $I_N = [I_C^T, I_U^T]^T \in R^{|v_e|}$ can be represented as

$$I_N = B^T I_B = B^T W B V_N = L_W V_N \tag{4}$$

where $I_C = [I_{c1}, \ldots, I_{cm}]^T$ represents the output currents of converter nodes for line impedances, in which the currents of converters for both public and local loads are not included; and $I_U = [I_{u(m+1)}, \ldots, I_{un}]^T$ represents the currents of uncontrolled nodes for the public loads branches. The matrix L_W can be divided into block matrix formation as

$$L_W = \begin{bmatrix} N & M \\ M^T & Q \end{bmatrix} \tag{5}$$

where the dimensions of matrix N, M, and Q are $m \times m$, $m \times (n-m)$, and $(n-m) \times (n-m)$, respectively.

For the sake of clarity, take the case shown in Fig. 1 as an example. According to the matrix B and W shown in Fig. 26 in Appendix, the block matrices in L_W can be written as

$$N = \begin{bmatrix} G_{15} & 0 & 0 & 0 \\ 0 & G_{25} & 0 & 0 \\ 0 & 0 & G_{36} & 0 \\ 0 & 0 & 0 & G_{46} \end{bmatrix}, Q = \begin{bmatrix} G_{t1} & -G_{56} \\ -G_{56} & G_{t2} \end{bmatrix},$$
$$M = \begin{bmatrix} -G_{15} & -G_{25} & 0 & 0 \\ 0 & 0 & -G_{36} & -G_{46} \end{bmatrix}^T \tag{6}$$

where $G_{t1} = G_{15} + G_{25} + G_{56}$,$G_{t2} = G_{36} + G_{46} + G_{56}$.

In this sense, the main Kron reduction process [26] from (5) to (7) is shown in Fig. 2.

Based on the Kron reduction theory and the process shown in Fig. 2, considering the effects from public loads, the

transformation results can be divided into two categories as

$$\begin{cases} I_C + L_{\mathrm{Tem}} I_U = L_C V_C & \text{with public load (7.1)} \\ I_C = L_C V_C & \text{without public load (7.2)} \end{cases} \tag{7}$$

where $L_{\mathrm{Tem}} = -MQ^{-1}$, $L_C = N - MQ^{-1}M^T$ being L_{C} a symmetric matrix satisfying $L_C 1_m = 0$, in which the main diagonal elements are positive and off-diagonal elements are negative.

When public loads are connected to the system, by using the transformation matrix L_{Tem}, their currents I_{U} can be redistributed to the converter nodes. Then, the left part of (7.1) is the total currents for both line impedances and public loads. In order to apply this transformation, the current I_U is needed instead of the conductance value of public loads. When there are no public loads in the system, the current I_U is equal to zero, and then (7.1)) is changed to (7.2)). Comparing these two equations, whether public loads are connected or not, matrix L_C is not changed. To be specific, matrix L_C only carries the information of line impedances and their topology, which means the load information is not included. Thus, whether loads are connected or not, the matrix L_C is not changed. In other words, when the load connections are changed, the voltage distributions are changed accordingly based on the circuit theory and L_{C} is not changed because the topology of line impedances in the system is not changed.

According to the definition of the Laplacian matrix, L_C can be considered as a weighted Laplacian matrix for the electrical graph model G_e. Thus, L_C is positive semidefinite.

Furthermore, defining the matrix L_L as $L_L = diag(G_{11}, \ldots, G_{mm})$ with $G_{ii} > 0$ being the local load or shunt conductance at converter node *i*, thus the matrix L_L is positive definite. The conductance of branch is from the distribution lines and also called shunt conductance branch. The load branch is for the load in the system. The local load current from converters can be expressed as

$$I_L = L_L V_C \tag{8}$$

where $I_L = [I_{l1}, \ldots, I_{lm}]^T$ in which I_{li} represents the output current for local loads from converter node i. The total current I_T from the converter nodes can be expressed as

$$I_T = I_C + I_L + L_{\mathrm{Tem}} I_U = L_T V_C \tag{9}$$

where $I_T = [I_{t1}, \ldots, I_{tm}]^T$ in which I_{ti} represents the total output current from converter node i and $L_T = L_C + L_L$. Because the matrix L_C is positive semidefinite and the matrix L_L is positive definite, it is proven that the matrix L_T is positive definite.

To be mentioned, if not all the source nodes have the local loads or shunt conductance branches, at least one diagonal element of L_L is equals to zero which means matrix L_L is not positive definite any more. It is also proven in [27] that L_T can still be positive definite when at least one diagonal element of L_L is positive.

B. Communication Model

The communication network among controllers can be represented by an undirected communication graph $G_c = (v_c, \varepsilon_c)$ with the set of nodes $v_c = \{1, \ldots, m\}$ being the m distributed controllers for m converters, the set of communication edges $\varepsilon_c \subset \nu_c \times \nu_c$. If two controllers i and j can receive information between each other, then there is a communication link between the two nodes, denoted by $(i, j) \in \varepsilon_c$, and nodes i and j are called communication neighbors. All of the communication neighbors of node i constitute its communication neighbor set as $N_i^c = \{j \in v_c | (i, j) \in \varepsilon_c\}$. The adjacency matrix for graph G_c is defined as $A = (a_{ij})_{M \times M}$ with elements

$$a_{ij} = \begin{cases} 1, \text{if } j \in N_i^c \\ 0, \text{otherwise.} \end{cases} \tag{10}$$

Meanwhile, it is assumed that there does not exist self-edge in the graph for each node. The degree of node i is defined as $d_i = \sum_{j \in N_i^c} a_{ij}$. The degree matrix is the defined as $D = diag(d_1, \ldots, d_m)$. Then the Laplacian matrix of graph G_c is defined as $L = D - A$. For the matrix L, all the eigenvalues are nonnegative real numbers which can be ordered as ascending order as $0 = \lambda_1 \leq \cdots \leq \lambda_m$.

C. Conventional V–I Droop Control

One of the main control objectives for a dc MG is to achieve the output current sharing. Let $I_{si} > 0$ represent the maximum output current capability of the converter i. Then two converters i and j share their output currents proportionally according to the capability if

$$I_{ti}/I_{si} = I_{tj}/I_{sj}. \tag{11}$$

To be mentioned, considering the effects from real-time electricity prices and intermittent power profiles of renewable energy sources, the maximum output current capability I_{si} can be regulated by the higher control level according to economic optimization results and then the power sharing profile can be changed. Conventional V–I droop control for the dc–dc converters has the following form:

$$V_i = V_i^{\mathrm{ref}} - R_{di} I_{ti} \tag{12}$$

where V_i^{ref} is the nominal voltage value, R_{di} is the virtual impedance which can be designed according to the I_{si}, and V_i is the voltage reference for inner control loop.

However, voltage deviations inevitably appear when droop control is applied. Also, the load current cannot be accurately shared due to the differences on distribution lines. To achieve proportional current sharing, the voltage compensation strategy is usually designed using a secondary controller with communication among different converters.

In the next section, the novel distributed nonlinear current controller is proposed to achieve current sharing and voltage regulation with improved event-triggered communication strategy instead of the V–I droop control and the secondary controller.

III. Distributed Nonlinear Current Controller and Its Stability Analysis

A. Distributed Nonlinear Current Controller

Being different from the conventional V–I droop control, a distributed nonlinear current controller is proposed to achieve current sharing and voltage regulation based on converters states communication. The voltage reference for converter i is expressed as

$$V_i = V_i^{\text{nom}} - \int_0^t u_i(\tau)d\tau \tag{13}$$

where V_i^{nom} is the nominal voltage, and $u_i(t)$ is the voltage control input for converter i and will be determined by the following proposed nonlinear distributed controller. By differentiating V_i with respect to t, the dynamics for node i is expressed as

$$\dot{V}_i = -u_i. \tag{14}$$

Because the output voltage value V_{ci} can follow the voltage reference V_i quickly by the inner PI control loop, it is reasonable to assume that $V_{ci} = V_i$ in the following expression.

Assume that each controller for converters can measure its output voltage V_i and current I_{ti} which can be transmitted to all its communication neighbors via the communication network. The proposed distributed nonlinear controller for current sharing and voltage regulation is expressed as

$$u_i = \left(\frac{\sigma}{I_{si}}\right) V_i \sum\nolimits_{j\in N_i^c} \left(\frac{I_{ti}}{I_{si}} - \frac{I_{tj}}{I_{sj}}\right) \tag{15}$$

where $\sigma > 0$ is the integral coefficient.

Note that by following the idea from [12], the linear part of (15) is derived and in order to guarantee the globe stable of the controller, the linear part is multiplied by the local voltage feedback. The stability will be proven in Section III.B.

The proposed controller (15) apply the product of the output voltage and the output current as a nonlinear feedback formation, by which no linearization around the operating point is involved, thus global convergence analysis of the system can be conducted. For the close-loop dynamics of the system with the proposed controller, the equilibrium point of the entire system is analyzed first and then the stability analysis is provided. The close-loop dynamics of the dc MG is expressed as

$$\dot{V} = -\sigma S\widehat{V}LSI_T \tag{16}$$

where $V = col(V_i)$,$S = \text{diag}(1/I_{s1},\ldots,1/I_{sm})$,$\widehat{V} = \text{diag}(V_1,\ldots,V_m)$.

B. Analysis of Equilibria

The existence of the equilibrium point or the dynamic system (9) and (16) should be analyzed at the steady-state stage.

Define V^s and I_T^s as the voltage and current vector from converters in the dc MG at the steady state, respectively. Setting $\dot{V} = 0$ yields the steady-state (16) of the system as

$$-SV^sLSI_T^s = 0. \tag{17}$$

From (8), we can get

$$I_T^s = L_TV^s. \tag{18}$$

Since the voltages are positive, the equation $LSL_TV^s = 0$ is derived at the steady state. For (17), two cases should be considered. The first one is $L_TV^s = 0$. The second one is $L_TV^s \neq 0$, $LSL_TV^s = 0$. Because the matrix L_T is positive definite, output currents L_TV^s cannot be zero and always positive, the first case does not exist. The second case should be used to find the equilibrium point for the system.

Because it is assumed that the communication graph G_c is connected, the null space of the Laplacian matrix L is $span\{\mathbf{1}_N\}$ [15]. Thus $LSL_TV^s = 0$ implies that $SL_TV^s = \alpha\mathbf{1}_M$, where α is a nonzero real number and $\mathbf{1}_M$ is an M-order vector of all ones. Because matrix S and matrix L_T is full ranking and invertible, the equilibrium of the closed-loop system V^s is expressed as

$$V^s = \alpha {L_T}^{-1}S^{-1}\mathbf{1}_M. \tag{19}$$

Thus, the equilibrium point of the closed-loop system is uniquely existed.

C. Convergence Analysis

By using a nonlinear state feedback of signals V_i and I_{ti} at the same time, the current can be shared asymptotically which will be proven as follows. Since matrix L_T is positive definite, the Lyapunov functional candidate Z can be chosen as

$$Z = (1/2)\,V^TL_TV > 0. \tag{20}$$

Computing the time derivative of the Lyapunov function (20) yields

$$\begin{aligned}\dot{Z} &= V^TL_T\dot{V} = V^TL_Tu = V^TL_T\left(-\sigma S\widehat{V}LSI_T\right)\\ &= -\sigma(SL_TV)^T\widehat{V}LSL_TV = -\sigma\tilde{I}_T^T\tilde{L}\tilde{I}_T \le 0\end{aligned} \tag{21}$$

where $\tilde{I}_T = SL_TV$ is the weighted current, and $\tilde{L} = \widehat{V}L$ in which $\widehat{V}$ is approximately seen as the constant proportion for matrix L.

Since the communication graph G_c is connected, matrix L is positive semidefinite and then matrix $\tilde{L}$ is also positive semidefinite. Thus, the derivative of Lyapunov function is negative, which can guarantee the global stability of the system. Furthermore, by LaSalle's invariance principle,$\lim_{t\to\infty}\tilde{L}\tilde{I}_T = 0$. It has an eigenvalue *0* with eigenvector being the vector of all ones, it yields

$$\begin{aligned}&\lim_{t\to\infty}\left(\tilde{I}_{ti}(t) - \tilde{I}_{tj}(t)\right) = 0\\ &\Rightarrow \lim_{t\to\infty}\left(I_{ti}(t)/I_{si} - I_{tj}(t)/I_{sj}\right) = 0\end{aligned} \tag{22}$$

which means for any converters i and j, the current will achieve proportional sharing asymptotically. One theorem is proposed as follow to design the proposed nonlinear distributed controller.

Theorem 1: For system (9) and (14), if the electrical graph G_e and the communication graph G_c are connected, the current

sharing proportional is achieved asymptotically by the nonlinear distributed controller (15).

To be mentioned, the deviations among output voltages are necessary to control the power flow and guarantee the accurate current sharing. Compared with the droop controller, the proposed controller can keep the output voltages around the nominal value, no matter when the load is increased or decreased.

IV. Development of the Distributed Controller With Event-Triggered Communication

A. Conception and Structure of Event-Triggered-Based Controller

For the proposed nonlinear distributed controller (15), each local controller need to monitor the current information $I_{ti}(t)$ and output voltage $V_i(t)$ of itself and its neighbors current to generate the control input $u_i(t)$ at each sample time. A practical way to achieve this communication is that each local controller adopts a fixed sampling period and sends the sampled current state to its neighboring nodes synchronously. To achieve current sharing and voltage regulation, many samplings in a periodic sampling scheme are redundant, especially under steady-state stage. Thus, in order to decrease the communication traffic and the frequency of updating controller outputs, the event-triggered communication strategy should be applied by a proper design of the sampling strategy while guaranteeing the performance of the current sharing and voltage regulation.

In the following, it is assumed that each controller only sends its information at some prescribed time instants, denoted by

$$t_0^i = 0 < t_1^i \cdots < t_k^i, k \in N. \tag{23}$$

These time instants are determined by a special set of inequalities called event-triggered principles. When the time-dependent event-triggered principles are satisfied, a prescribed event occurs. The time instants t_k^i when events occur are called event time instant.

B. Design of Event-Triggered Communication Strategy

Let $I_{ti}(t_k^i)$ be the transmitted measurement of $I_{ti}(t)$ at the event time instant t_k^i. Defining the measurement error of converter i at time t as

$$e_i(t) = I_{ti}\left(t_k^i\right) - I_{ti}(t), \ \ t \in \left[t_k^i, t_{k+1}^i\right). \tag{24}$$

The error $e_i(t)$ is the difference between the sampled and the real-time state. When an event is triggered, the sampled state is replaced by the real-time state and the error is decreased to zero. Following the proposed distributed controller (15), an event-triggered-based distributed nonlinear controller can be expressed as

$$u_i(t) = -\left(\frac{\sigma}{I_{si}}\right) V_i(t) \sum_{j \in N_i^c} \left(\frac{I_{ti}\left(t_{k_i(t)}^i\right)}{I_{si}} - \frac{I_{tj}\left(t_{k_j(t)}^j\right)}{I_{sj}}\right), \quad t \in \left[t_k^i, t_{k+1}^i\right) \tag{25}$$

where $k_i(t) = \arg\max_{k \in N}\{t_k^i | t_k^i \le t\}$ means the subscript of the latest event time instant to the current time t, $I_{ti}(t_{ki(t)}^i)$ is the sampled state of $I_{ti}(t)$.

The event time instants should be properly chosen to guarantee the stability operation of a dc MG and its control performance. Thus, well-designed event-triggered principles should be established to generate these proper event time instants. For convenience, denote $\breve{I}_{ti}(t) = I_{ti}(t_k^i), \ t \in [t_k^i, t_{k+1}^i)$ and $\breve{I}_T(t) = col(\breve{I}_{ti}(t))$. Then the matrix form of controller (25) is expressed as

$$u = -\sigma \widehat{SV} L S \breve{I}_T. \tag{26}$$

Consider the same Lyapunov function in (20), the derivative of the function with even-triggered distributed controller (26) yields

$$\dot{Z} = V^T L_T \dot{V} = V^T L_T \left(-\sigma \widehat{SV} L S \breve{I}_T\right) = -\sigma I_T^T S \tilde{L} S \breve{I}_T. \tag{27}$$

Due to the definition (24), its vector form can be rewritten as $I_T = \breve{I}_T - e$. Then

$$\dot{Z} = -\sigma\left(\breve{I}_T - e\right)^T S \tilde{L} S \breve{I}_T = -\sigma \breve{I}_T^T S \tilde{L} S \breve{I}_T + \sigma e^T S \tilde{L} S \breve{I}_T. \tag{28}$$

By using the following inequality: for any vectors $x, y \in R^N$, the inequality $x^T y \le (1/2a)x^T x + (a/2)y^T y$ exists for a positive a [18]. Then

$$\begin{aligned} \dot{Z} &= -\sigma \breve{I}_T^T S \tilde{L} S \breve{I}_T + \sigma (Se)^T \left(\tilde{L} S \breve{I}_T\right) \\ &\le -\sigma \breve{I}_T^T S \tilde{L} S \breve{I}_T + \sigma \left(\frac{1}{2a}\|Se\|^2 + \frac{a}{2}\left\|\tilde{L} S \breve{I}_T\right\|^2\right). \end{aligned} \tag{29}$$

Based on the condition $\|Se\| < \rho \|\tilde{L} S \breve{I}_T\|$, then we can acquire

$$\dot{Z} \le -\sigma \breve{I}_T^T S \tilde{L} S \breve{I}_T + \sigma\left(\rho^2/2a + a/2\right)\left\|\tilde{L} S \breve{I}_T\right\|^2. \tag{30}$$

Let λ_M represent the largest eigenvalue of the matrix $\tilde{L}$, then

$$\left\|\tilde{L} S \breve{I}_T\right\|^2 = \breve{I}_T^T S \tilde{L} \tilde{L} S \breve{I}_T < \lambda_M \breve{I}_T^T S \tilde{L} S \breve{I}_T. \tag{31}$$

Then, combining (30) with (31), we have

$$\dot{Z} \le -\sigma\left(1 - \lambda_M\left(\rho^2/2a + q/2\right)\right) \breve{I}_T^T S \tilde{L} S \breve{I}_T. \tag{32}$$

Because $\sigma > 0$, $\dot{Z} < 0$ if a and ρ are reasonable chosen, as

$$1 - \lambda_M\left(\rho^2/2a + a/2\right) > 0 \tag{33}$$

which is equivalent to $a + \rho^2/a < 2/\lambda_M$. Since ρ^2/a is positive constant, the inequality (33) can be divided into two conditions as

$$a < 2/\lambda_M \tag{34}$$

$$\rho^2 < -a^2 + 2a/\lambda_M = -(a - 1/\lambda_M)^2 + 1/\lambda_M^2. \tag{35}$$

Thus if $\|Se\| < \rho \|\tilde{L} S \breve{I}_T\|$ holds and the conditions for a and ρ are as: $a < 2/\lambda_M$ and $0 < \rho < 1/\lambda_M$, $\dot{Z} < 0$ can be satisfied.

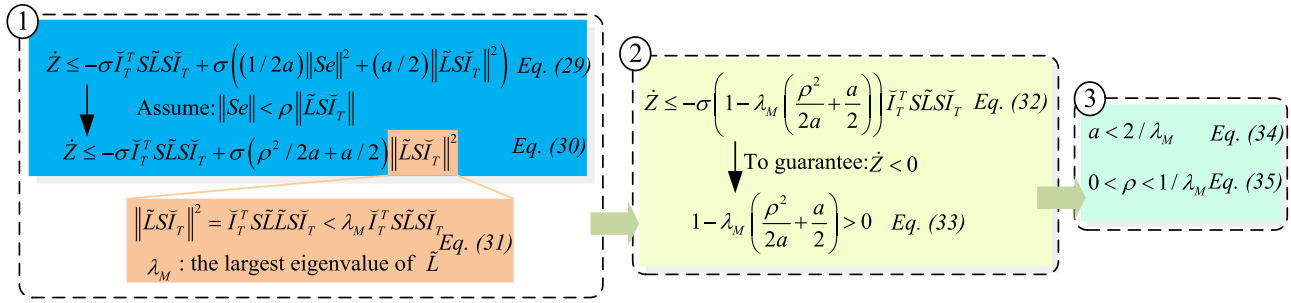


Fig. 3. Deduction process of the event-triggered-based communication design.

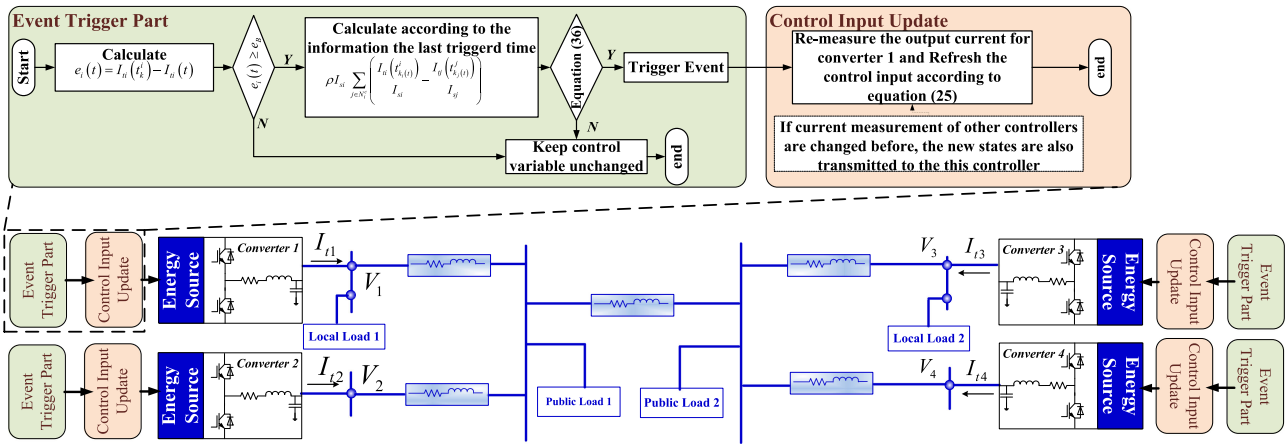


Fig. 4. Flow chart of the distributed event-triggered-based controller combined with the electrical topology.

The deduction process above is illustrated in Fig. 3 to make the process more clearly.

Furthermore, for each local controller, it is necessary to update the measurement of current $I_{ti}(t^i_{k_i(t)})$, when the condition $\|Se\| < \rho\|\tilde{L}S\check{I}_T\|$ is unsatisfied. When the condition $\|Se\| < \rho\|\tilde{L}S\check{I}_T\|$ is violated, it can be transformed as

$$|e_i(t)| \ge \rho I_{si}\left|\sum_{j\in N_i^c}\left(\frac{I_{ti}\left(t^i_{k_i(t)}\right)}{I_{si}} - \frac{I_{tj}\left(t^j_{k_j(t)}\right)}{I_{sj}}\right)\right|,$$
$$t \in \left[t_k^i, t_{k+1}^i\right), k_i(t) = \arg\max_{k\in N}\left\{t_k^i \,\middle|\, t_k^i \le t\right\}, \quad k_j(t)$$
$$= \arg\max_{k\in N}\left\{t_k^j \,\middle|\, t_k^j \le t\right\}. \tag{36}$$

Then, an event is triggered, the local controller i update its measurement of current $I_{ti}(t^i_{k_i(t)})$ as $I_{ti}(t)$.

Thus, (36) is the event-triggered principle for the proposed distributed controller which is totally distributed without using a centralized controller. However, for principle in (36), with the decreasing error between the output currents (the right part of inequality), the system will become more and more sensitive and conservative which means the controllers are triggered more frequent. Thus, even though the system is at steady-state stage, the frequency of triggered times is still not decreased which can cause more communication traffic. To further decrease the frequency of triggered times and communication traffic, a non-negative offset e_B is proposed and set for $|e_i(t)|$ which means before judging the event-triggered principle (36), the condition below should be judged first

$$|e_i(t)| \ge e_B \tag{37}$$

when inequality is satisfied, then to judge the inequality (36) being satisfied or not. By this method, the communication traffic can be decreased furthermore. The flow chart combined with the electrical network is illustrated in Fig. 4.

C. Design Guideline

Based on the proposed nonlinear controller shown in (15), the fundamental principle to design the triggered principle shown in (36) is to guarantee the global stability of the whole system. According to the Lyapunov stability theory, the design process can be divided into following steps:

1) In Section II-A, matrix L_T is proven to be positive definite which represents the electrical network of the system. Thus, L_T is chosen to establish Lyapunov functional candidate Z shown as (20). The derivative of Lyapunov functional candidate Z is derived according to step 2.
2) Due to the features of event-triggered principle, the proposed controller should be modified from (15) to (25) by using sampled current feedback instead of the real-time current feedback. The error $e_i(t)$ is defined as the difference between the sampled and the real-time state. Considering the error $e_i(t)$ variable, the time derivative of Lyapunov functional candidate Z can be derived as (28).

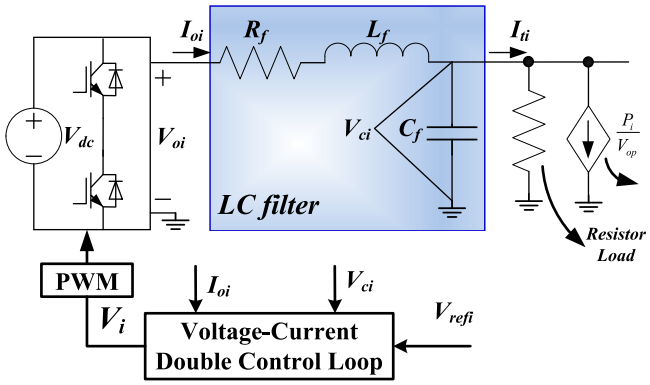


Fig. 5. Electrical structure of a buck converter system.

3) Based on the inequality $x^T y \leq (1/2a)x^T x + (a/2)y^T y$ from basic mathematical theory [18], the scaling transformation for the time derivative of Lyapunov candidate is derived as (29).
4) Based on the assumption $\|Se\| < \rho\|\tilde{L}S\breve{I}_T\|$, the readers can follow the next steps shown in Fig. 3 from (29) to (35). To satisfy the derivative of the Lyapunov candidate being negative definite, two requirements should be satisfied for the controller coefficients design which are $\sigma > 0$ and $0 < \rho < 1/\lambda_M$.

Finally, if the assumption $\|Se\| < \rho\|\tilde{L}S\breve{I}_T\|$ is violated, the controller should be triggered. Thus, from the violated condition, the triggered principle is derived as in (36).

V. Model Extension, Damping Improvement and Control Coefficients Design

In a typical dc MG, CPLs need to be carefully considered, which can undermine the stability and damping of the system. Traditionally, V–I droop controller can provide active damping of the oscillations [5], [28] by the virtual resistance. However, the proposed controller replaces V–I droop controller. Thus, it is necessary to compare the damping performance between the proposed controller and V–I droop controller. To study the damping performance of the proposed controller convincingly, the model in (16) is extended by considering the effects of output LC filter and inner *V–I* control loop in detail. To improve the damping performance of proposed controller, an extra proportional feedback is added based on the analysis results.

A. Model Extension

The electrical structure of one converter including LC filter, the constant resistive load and CPL is shown in Fig. 5.

The electrical structure is modeled as follows:

$$\frac{dI_{oi}}{dt} = \frac{1}{L_f}V_{oi} - \frac{R_f}{L_f}I_{oi} - \frac{1}{L_f}V_{ci} \tag{38}$$

$$\frac{dV_{ci}}{dt} = \frac{1}{C_f}I_{oi} - \frac{1}{C_f}I_{ti} \tag{39}$$

where L_{fi} is the filter inductor, R_{fi} is the equivalent resistance of the inductor, C_{fi} is the filter capacitor, I_{oi} is the inductor current, V_{oi} is the converter output voltage, V_{ci} has been defined in Section II. In addition, the inner *V–I* control loop is shown in Fig. 6.

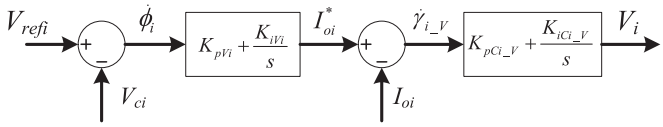


Fig. 6. Inner *V-I* control loop.

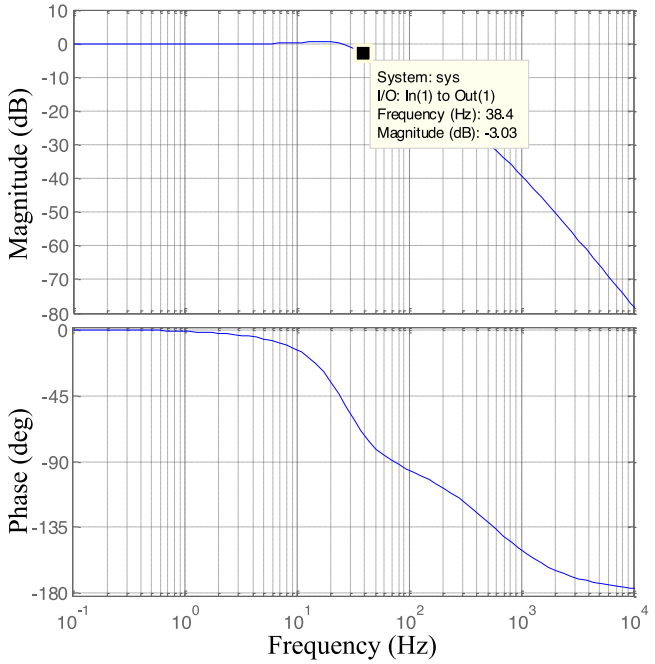


Fig. 7. Closed loop bode diagram from $V_{\mathrm{ref}i}$ to V_{oi}.

The model for the inner *V–I* control loop can be derived as

$$\dot{\phi}_i = V_{\mathrm{ref}i} - V_{ci} \tag{40}$$

$$I^*_{oi} = K_{iVi}\phi_i + K_{pVi}\left(V_{\mathrm{ref}i} - V_{ci}\right) \tag{41}$$

$$\dot{\gamma}_{i\_V} = I^*_{oi} - I_{oi} \tag{42}$$

$$V_i = V_{oi} = K_{iCi\_V}\gamma_{i\_V} + K_{pCi\_V}\left(I^*_{oi} - I_{oi}\right). \tag{43}$$

Models in literature [7], [8], [14], [16], [29] prove that it is reasonable to neglect the converter itself dynamics, thus $V_i = V_{oi}$. Based on (38)–(43), the complete converter system model is derived and the closed-loop bode diagram from $V_{\mathrm{ref}i}$ to V_{oi} is shown in Fig. 7.

In Fig. 7, it is illustrated that if the LC filter and inner control loop parameters are well designed, the converter system (with inner control loop and output filter) can be simplified as a low pass filter with 38.4 Hz cutoff frequency. Thus, for convenience, it is reasonable to model the closed-loop relationship from $V_{\mathrm{ref}i}$ to V_{oi} as

$$V_{oi} = \frac{\omega_c}{s+\omega_c}V_{\mathrm{ref}i} \Rightarrow \dot{V}_{oi} = \omega_c V_{\mathrm{ref}i} - \omega_c V_{oi} \tag{44}$$

where $\omega_c = 2\pi f = 241$ rad/s.

Then, for the modeling of CPL part, it is common practice to linearize it at the voltage operating point V_{op} [30] given as

$$I_{\mathrm{CPL}i}(v) \approx \underbrace{I_{\mathrm{Consti}}}_{a} + \underbrace{\left(-P_i/V_{op}^2\right)}_{b} v \tag{45}$$

where P_i is the constant power value, $I_{\mathrm{Consti}} = 2P_i/V_{op}$ is the equivalent constant current load. In (45), part (a) is as the constant current load which cannot affect the stability of the system, part (b) is the negative resistance part which can undermine stability of the system. Thus, the CPL currents from converters can be expressed as

$$I_{\mathrm{CPL}} = L_{\mathrm{CPL}} V_C + I_{\mathrm{Const}} \tag{46}$$

where $I_{\mathrm{Const}} = [I_{\mathrm{Const1}}, \ldots, I_{\mathrm{Const}m}]^T$, $I_{\mathrm{CPL}} = [I_{\mathrm{CPL1}}, \ldots, I_{\mathrm{CPL}m}]^T$ in which $I_{\mathrm{CPL}i}$ represents the CPL current of converter node i and $L_{\mathrm{CPL}} = \mathrm{diag}(-P_1/V_{op}^2, \ldots, -P_m/V_{op}^2)$.

Thus, considering the negative resistance effects from CPLs, the model in (9) representing the relationship between capacitor voltages and output currents should be changed as

$$I_T = I_C + I_L + L_{\mathrm{Tem}} I_U + I_{\mathrm{CPL}} = L_T' V_C + I_{\mathrm{Const}} \tag{47}$$

where $L_T' = L_T + L_{\mathrm{CPL}}$, I_C and I_L have been defined in Section II.

There is no general mathematical tool to test the damping performance for nonlinear controllers, thus the proposed controller in (16) is linearized by keeping the voltage feedback constant at the operating point. By this linearization, (16) is modified as

$$\dot{V}_{\mathrm{ref}} = -\sigma S \widehat{V}_{op} L S I_O \tag{48}$$

where $\widehat{V}_{op} = diag(V_{op}, \ldots, V_{op})$, in addition, because the LC filter effect is considered in the following analysis, the current feedback I_T (output current) should be replaced by I_O (inductor current) and the V (in the left part of (16)) should be replaced by V_{ref} due to the effect from inner control loop.

According to (38), (39), (44), (47), and (48), the extended model considering the electrical part and inner control loop is derived as

$$\begin{bmatrix} \dot{V}_{\mathrm{ref}} \\ \dot{V}_O \\ \dot{I}_O \\ \dot{V}_C \end{bmatrix} = \begin{bmatrix} 0_M & 0_M & -\sigma S \widehat{V}_{op} L S & 0_M \\ \omega_c I_M & -\omega_c I_M & 0_M & 0_M \\ 0_M & \frac{1}{L_f} I_M & -\frac{R_f}{L_f} I_M & -\frac{1}{L_f} I_M \\ 0_M & 0_M & \frac{1}{C_f} I_M & -\frac{1}{C_f} L_T' \end{bmatrix} \begin{bmatrix} V_{\mathrm{ref}} \\ V_O \\ I_O \\ V_C \end{bmatrix} + \begin{bmatrix} 0_M \\ 0_M \\ 0_M \\ -\frac{1}{C_f} I_M \end{bmatrix} I_{\mathrm{Const}} \tag{49}$$

where $V_{\mathrm{ref}} = col(V_{\mathrm{ref}i})$, $V_o = col(V_{oi})$, $I_o = col(I_{oi})$, $V_c = col(V_{ci})$, 0_M is the M-*dimension* zero matrix, and I_M is the M-*dimension* unit matrix.

Then, as shown in (13)–(15), only the integrator is considered in the controller. To improve the damping performance of the proposed controller, an extra proportional item is added in the controller and then the controller in (13) can be written as

$$V_{\mathrm{ref}i} = V_i^{\mathrm{nom}} - \int_0^t u_i(\tau) d\tau - \frac{\varsigma}{\sigma} u_i(t) \tag{50}$$

where ς is as the proportional coefficients. By computing the time derivative of (50), (48) is changed as

$$\dot{V}_{\mathrm{ref}} = -\sigma S \widehat{V}_{op} L S I_O - \varsigma S \widehat{V}_{op} L S \dot{I}_O. \tag{51}$$

Then substituting (38) in (51), it can be rewritten as

$$\begin{aligned} \dot{V}_{\mathrm{ref}} &= -\sigma S \widehat{V}_{op} L S I_O - \varsigma S \widehat{V}_{op} L S \left(\frac{1}{L_f} V_O - \frac{R_f}{L_f} I_O - \frac{1}{L_f} V_C \right) \\ &= \left(-\sigma + \varsigma \frac{R_f}{L_f} \right) S \widehat{V}_{op} L S I_O - \varsigma \frac{1}{L_f} S \widehat{V}_{op} L S V_O \\ &\quad + \varsigma \frac{1}{L_f} S \widehat{V}_{op} L S V_C. \end{aligned} \tag{52}$$

Thus, based on (52), the model (49) can be changed as (53) which is shown at the bottom of next page.

Based on the established two models (49) and (53), the damping performance and the maximum CPL power capability are studied in the following section.

TABLE I
ELECTRICAL SETUP AND CONTROL COEFFICIENTS

Category	Parameters	Value
Electrical Setup Parameters	Filter Inductor	1.8 mH
	DC Bus Capacitance	2200 μF
	Line impedance for Converter 1	0.13 Ω + 1.7 mH
	Line impedance for Converter 2	0.7 Ω + 1.2 mH
	Line impedance for Converter 3	0.4 Ω + 1.2 mH
	Line impedance for Converter 4	1.3 Ω + 1.7 mH
	Line impedance between public loads	1.7 Ω + 2.5 mH
Inner Voltage Loop Controller	Current proportional coefficient	0.5
	Current integral coefficient	2
Inner Current Loop Controller	Current proportional coefficient	0.009
	Current integral coefficient	0.09
Event-Triggered Controller	Proportional coefficient ς	0.05
	Integral coefficient σ	10
	ρ	0.2

B. Damping Comparison and Improvement

To analyze the model quantitatively, a dc MG including four paralleled converters, different line impedances, resistive loads, and CPLs is considered. The electrical information about the dc MG is shown in Table I.

Based on the model (49) in which only integral item is considered, the root locus in Fig. 8 shows the dynamic behavior of the system by changing the integral coefficient σ from 1 to 20. It can be observed from the zoom in part of Fig. 8 that one pair of poles is moving towards the imaginary axis indicating reduced system damping. Then, three pairs of poles on the real axis are moving toward each other implying enhanced response speed, and then moving away from the real axis showing reduced damping.

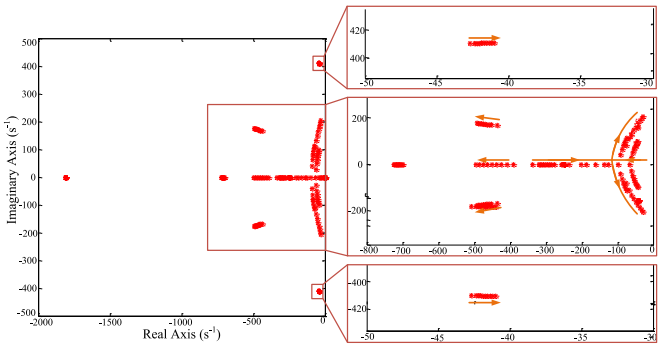


Fig. 8. Root locus plot by changing the integral coefficient σ from 1 to 20.

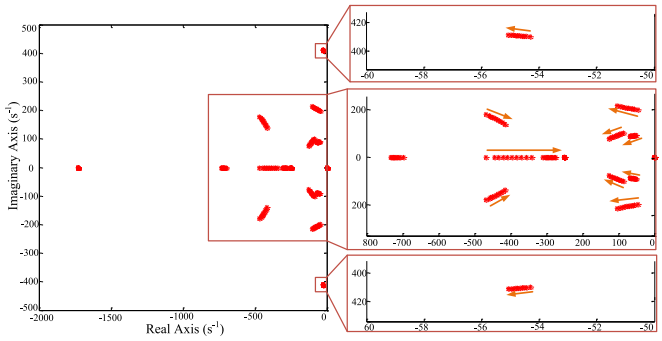


Fig. 9. Root locus plot by changing the proportional coefficient ς from 0.01 to 0.05.

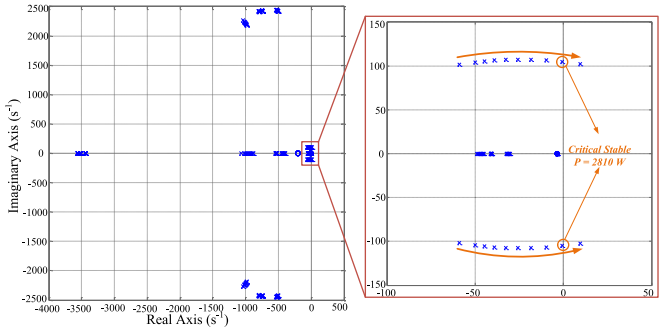


Fig. 10. Root locus plot by changing the Power of CPL from 200 to 3100 W for dc MG with *V–I* droop controller.

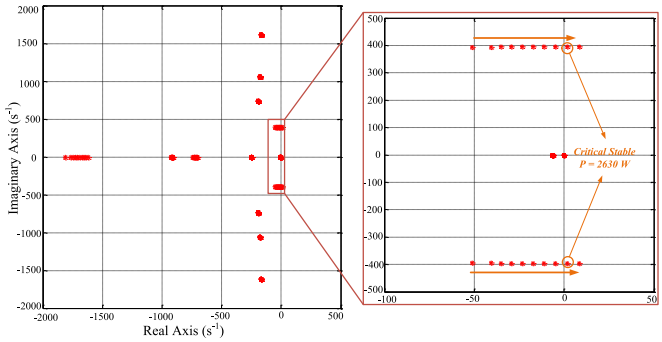


Fig. 11. Root locus plot by changing the Power of CPL from 200 to 2900 W for dc MG with the proposed controller.

Based on the model (53) in which both proportional and integral items are considered, the root locus in Fig. 9 shows the dynamic behavior of the system by changing the proportional coefficient ς from 0.01 to 0.05. From the zoom in part of Fig. 9, it is shown that four pairs of the poles are moving away from the imaginary axis and toward the real axis which can improve the damping of the proposed controller. Thus, considering the added proportional item in the proposed controller, the damping of the system can be improved by tuning the proportional coefficients.

Then, the damping performance and the maximum allowed CPL power are compared between the proposed controller and the *V–I* droop controller. To be mentioned, based on the electrical model and inner control loop in (38)–(43), the model of *V–I* droop controller can also be derived. The comparison results are shown in Figs. 10 and 11.

In Fig. 10, a dc MG with the *V–I* droop controller is studied with its CPL power changed from 200 to 3100 W. It is shown that the maximum allowed CPL power is around 2810 W when one pair of poles goes across the imaginary axis to the right half plane (RHP). In Fig. 11, a dc MG with the proposed controller is studied by changing its CPL power from 200 to 2900 W. It is shown that the maximum allowed power is around 2630 W when one pair of poles goes across the imaginary axis to the RHP. In comparison, the maximum allowed CPL power levels of the two controllers are comparable. In addition, the location of poles shown in Fig. 10 and 11 is similar indicating that the damping performances are also similar between two types of controllers. Thus, even though the *V–I* droop controller is replaced by the proposed controller, the damping performance can be preserved.

In addition, *V–I* droop controller inevitably causes voltage deviation which also increases the equivalent negative resistance of the CPL, resulting in reduced stability margin. In comparison, the proposed method can effectively maintain the voltage level, thus the stability range can be guaranteed to a certain degree.

Remark 1: The analysis shown in Figs. 8 and 9 is based on the complete system information including the line impedance values which are difficult to know in a real MG system. The root locus plot by changing the line impedance values in the system is shown in Fig. 12. It is shown that changing the line impedance values can only affect the poles which are far

$$\begin{bmatrix} \dot{V}_{\rm ref} \\ \dot{V}_O \\ \dot{I}_O \\ \dot{V}_C \end{bmatrix} = \begin{bmatrix} 0_M & -\varsigma\frac{1}{L_f}S\widehat{V}_{op}LS & \left(-\sigma+\varsigma\frac{R_f}{L_f}\right)S\widehat{V}_{op}LS & \varsigma\frac{1}{L_f}S\widehat{V}_{op}LS \\ \omega_c I_M & -\omega_c I_M & 0_M & 0_M \\ 0_M & \frac{1}{L_f}I_M & -\frac{R_f}{L_f}I_M & -\frac{1}{L_f}I_M \\ 0_M & 0_M & \frac{1}{C_f}I_M & -\frac{1}{C_f}L'_T \end{bmatrix} \begin{bmatrix} V_{\rm ref} \\ V_O \\ I_O \\ V_C \end{bmatrix} + \begin{bmatrix} 0_M \\ 0_M \\ 0_M \\ -\frac{1}{C_f}I_M \end{bmatrix} I_{\rm Const}. \quad (53)$$

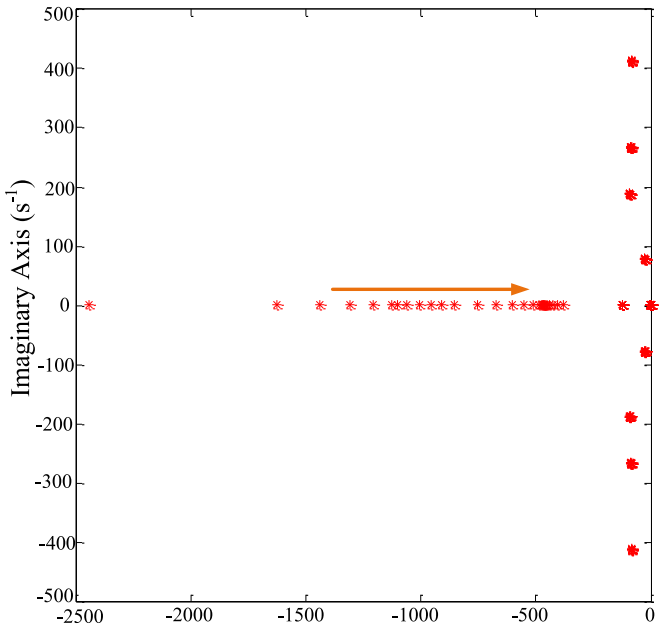


Fig. 12. Root locus plot by changing all line impedance values shown in Table I from 0.1 times to 5 times of that values.

away from imaginary axis and cannot affect the dynamic and steady-state performance of the controller. Thus, the coefficient design guideline can be used for real dc MG systems.

C. Design Procedure for Control Coefficients

To guarantee stability of the whole system synthesized with the proposed controller, three parameters should be considered as follows:

1) ρ is designed based on the communication network. ρ should satisfy $0 < \rho < 1/\lambda_M$ according to the analysis results shown in (35), where λ_M is the largest eigenvalue of the Laplacian matrix $\tilde{L}$ which represents the communication network shown in upper right of Fig. 13 as

$$\tilde{L} = V^{\text{nom}} L = 48^* \begin{bmatrix} 2 & -1 & 0 & -1 \\ -1 & 2 & -1 & 0 \\ 0 & -1 & 2 & -1 \\ -1 & 0 & -1 & 2 \end{bmatrix}. \quad (54)$$

2) As shown in (15) and (21), it is proven that σ should be positive to guaranteeing the stability of the system. Furthermore, as shown in Fig. 8, larger σ can decrease the damping performance of the proposed controller and σ should be less than 12 before the poles on the real axis go into the complex plane. In this paper, it is chosen as 10.
3) As the analysis given in Section V-B, to improve the damping performance of the proposed controller, a proportional feedback is added in the proposed controller. As shown in Fig. 9, both the damping and dynamic response performance can be improved by increasing the proportional coefficient ς. In this paper, it is chosen as 0.05.

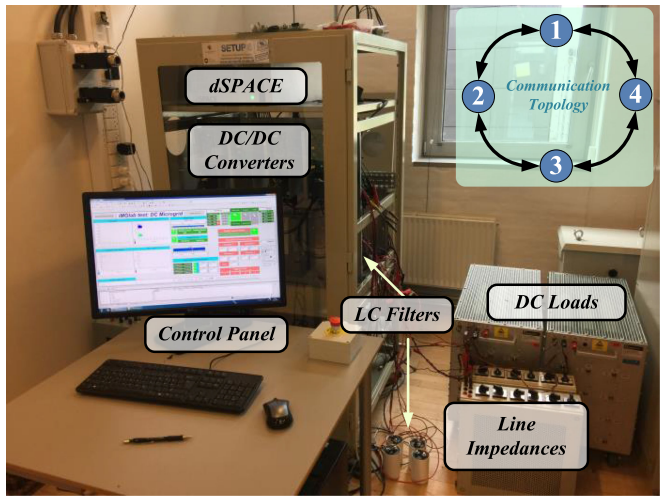


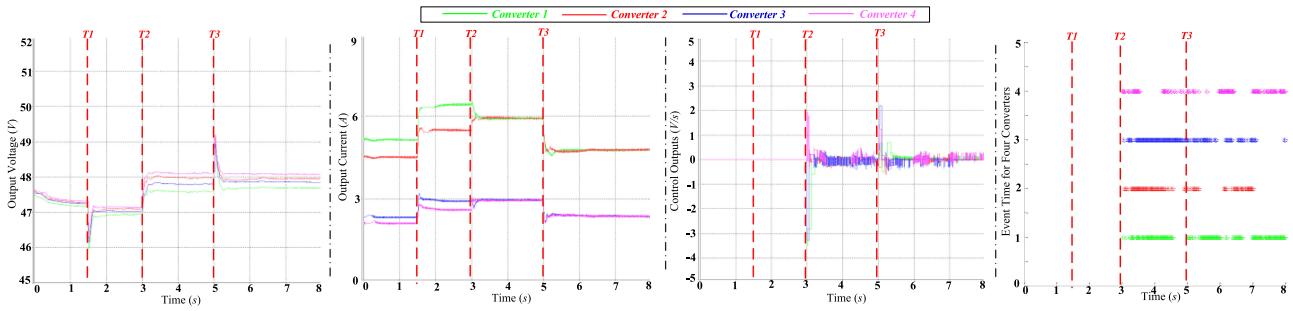
Fig. 13. Experimental setup in AAU-Microgrid research laboratory.

VI. Experimental Tests and Performance Evaluation

The proposed controller is tested in the experimental dc MG setup shown in Fig. 13. The setup consists of four parallel-connected dc–dc buck converters, dSPACE controller and monitoring platform, LC filters, four different line impedances, and loads. All the converters use the same LC filter parameters. Communication links for cases 1, 3, and 4 are built only between neighboring units shown in the top-right corner of Fig. 13. For case 2 which studies the communication failure tolerance, two different communication networks are considered as shown in Figs. 15 and 18. The ratio for four converter rated capacities is 2: 2: 1: 1 from converter 1 to 4. The nominal voltage for the dc MG is *48 V*. The electrical setup information and control coefficients are shown in Table I. The local loads 1 and 2 are connected to converter 1 and 3, respectively. The MG topology, local and public load connections are same as shown in Fig. 4.

A. Case 1: Performance Comparison Between the Proposed Controller and V–I Droop Controller

At the beginning, local loads 1, 2, and public load 2 are connected. Fig. 14 shows the performance comparison for proposed controller and droop controller. The droop controller is used before $t = T2$. As shown in Fig. 14(a) and (b), the voltage deviations from the nominal value are obvious and the output currents cannot be shared in proportion to the rated ratios among four converters. When the public load 1 is connected at $t = T1$, the voltages are deviated from the nominal value furthermore. At $t = T2$, the droop control is disabled and the proposed controller is activated. In addition, at $t = T3$, the public load 1 is disconnected. In a clear-cut contrast, the performance of output voltages independently from load changes achieves a stable distribution around the nominal value when the load is changed. Meanwhile, the accurate output current sharing is achieved very well after enabling the proposed controller under both transient- and steady-state stages, as shown in Fig. 14(b). To be mentioned, in order to achieve accurate current sharing through necessary



(a). Performance of Output Voltage (b). Performance of Output Current (c). Voltage Control Outputs (d). Event Time Instants

Fig. 14. Performance comparison for Case 1.

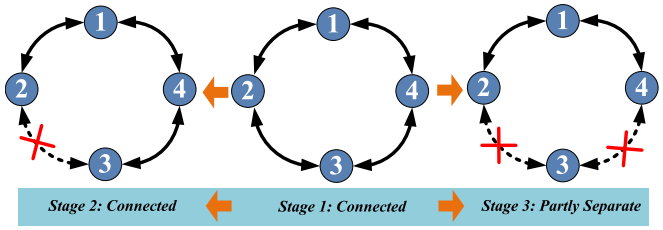


Fig. 15. Ring communication network and its failure process.

power flow among converters, it is reasonable to control the output voltage around nominal value allowing necessary deviations between each other.

Fig. 14(c) shows the controller outputs for the converters under the event-triggered communication strategy. It can be observed that each output is changed to a new control value only when an event occurs, which means that the control value updating for each converter is event-triggered and the frequency of changing control values is much decreased. Fig. 14(d) shows the event time instants of each converter. When the load is changed at $t = T3$, the events are generated more frequent which means the proposed event-triggered controller can adapt the change of the system quickly. Even though both the droop controller and the event-triggered controller can achieve stable operation, the proposed controller can achieve both better voltage regulation and accurate current sharing simultaneously.

B. Case 2: Communication Failure Tolerance

To test the communication failure tolerance for the proposed controller, two communication networks are considered in this case including ring communication network and cross-communication network.

The ring communication network and its failure process shown in Fig. 15 includes three stages: Stage 1: the ring communication network is intact, which is connected; stage 2: the communication link between converter 2 and 3 is failed down but the communication network is still a connected graph; stage 3: all the communication links of converter 3 are failed simultaneously causing that converter 3 is separated from the communication network. Figs. 16 and 17 show the experimental results under a ring communication network.

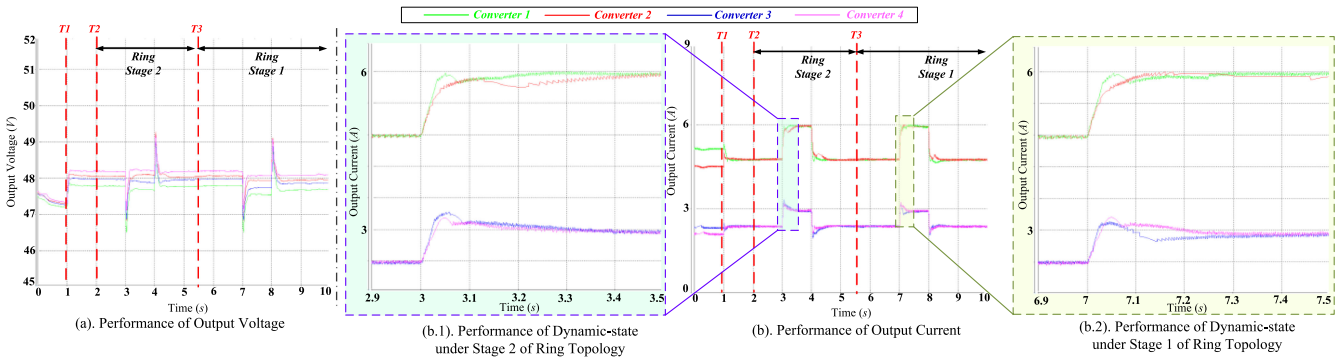
Fig. 16 compares the system performance between stages 1 and 2. At $t = T1$, the proposed controller is activated. At $t = T2$, the communication links between converter 2 and 3 are disabled. At $t = T3$, the communications link between converter 2 and 3 are recovered. During both the periods, the public load 1 in the system is connected and disconnected. Comparing the performance between *T2–T3* with that after *T3* shown in Fig. 16(a) and (b), it is seen that under both stages 1 and 2, the steady-state performance cannot be affected which means the output voltages are controlled around the nominal value and the current sharing is achieved accurately. Because communication networks under both stages 1 and 2 are connected graphs, the control performance can be guaranteed. However, comparing the transient-state performances under the stage 2 shown in Fig. 16(b.1) and that under the stage 1 shown in Fig. 16(b.2), the dynamic response in Fig. 16(b.2) is a little more quickly than the other shown in Fig. 16(b.1). Thus, the complete ring communication network can enhance the system response more quickly than that under stage 2.

Furthermore, Fig. 17 compares the system performance under stage 1 and stage 3. During stage 3, the public load 1 is also connected and disconnected respectively. Since the communication network under stage 3 is not a connected graph, the global current sharing performance cannot be guaranteed.

To be specific, as shown in Fig. 17(b), the current of converters 1, 2, and 4 are still well shared because the communication network among these three converters is still a connected graph, and the converter 3 current has deviation. For converter 3, when it detects its communication failure and is separated from the communication network, it disables its distributed control loop which means $u_i(t) = 0$, thus the voltage reference is kept at 48 V according to (13) and (15). As shown in Fig. 17(a), the output voltage from converter 3 (blue line) is controlled at 48 V after stage 3. Meanwhile, as shown in Fig. 17(b), converter 3 is still operating by injecting current for system even though the current sharing performance is not good.

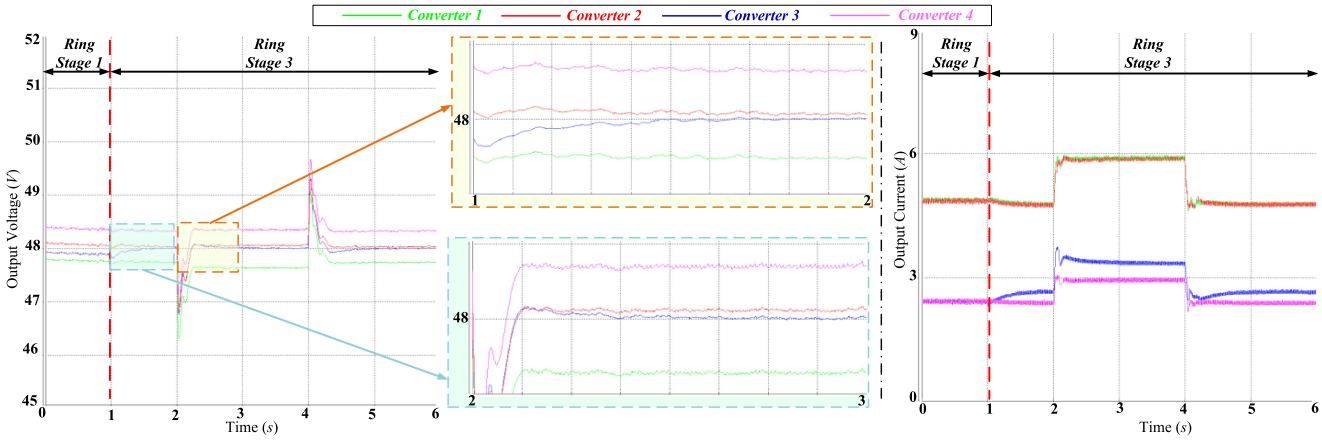
Furthermore, the cross-communication network and its failure process are shown in Fig. 18 from intact graph (Stage 1) to completely separate graph (Stage 6).

Fig. 19 shows the system performance of the whole changing process including the performance of output voltage regulation and output current sharing. At the beginning of this case, two local loads and public load 2 are connected in MG. During stage 2, public load 1 is connected and during stage 3, local load 1 is disconnected. During stage 6, local load 1 is connected and disconnected. In order to make the current sharing



(a). Performance of Output Voltage (b.1). Performance of Dynamic-state under Stage 2 of Ring Topology (b). Performance of Output Current (b.2). Performance of Dynamic-state under Stage 1 of Ring Topology

Fig. 16. Performance under ring communication network changed between stage 1 and 2.



(a). Performance of Output Voltage (b). Performance of Output Current

Fig. 17. Performance under ring communication network changed between stage 1 and 3.

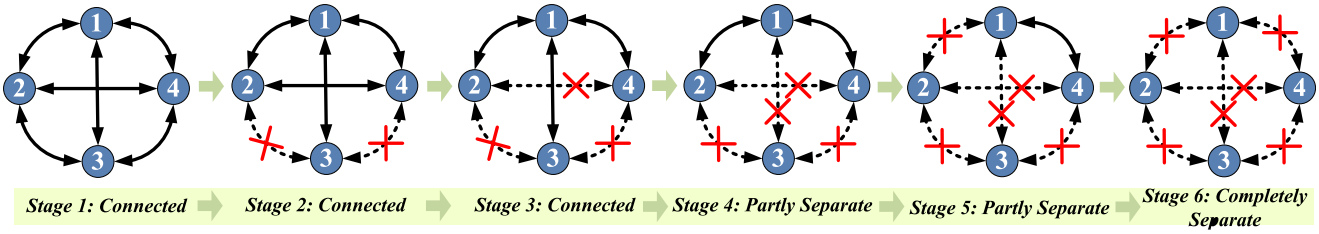
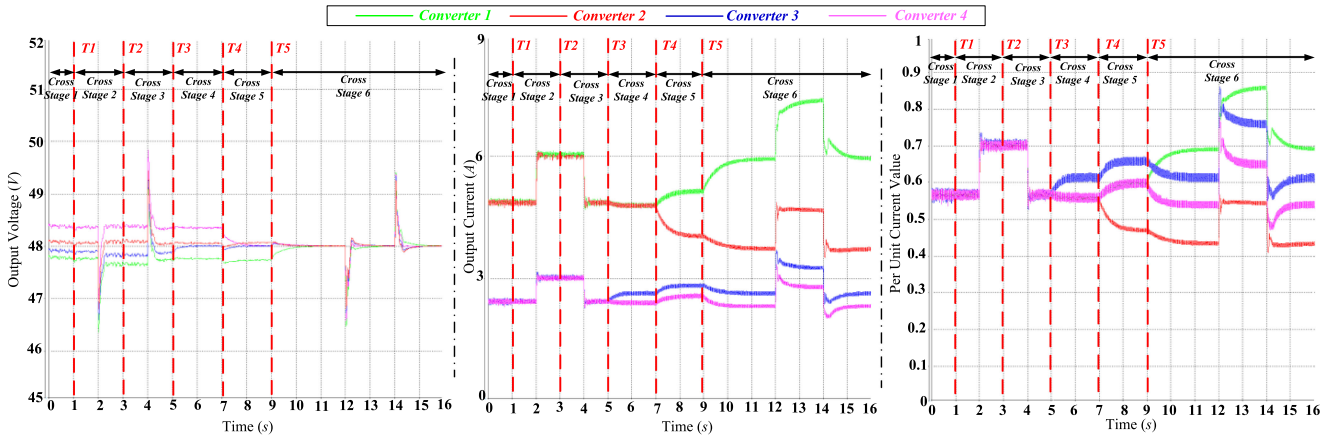
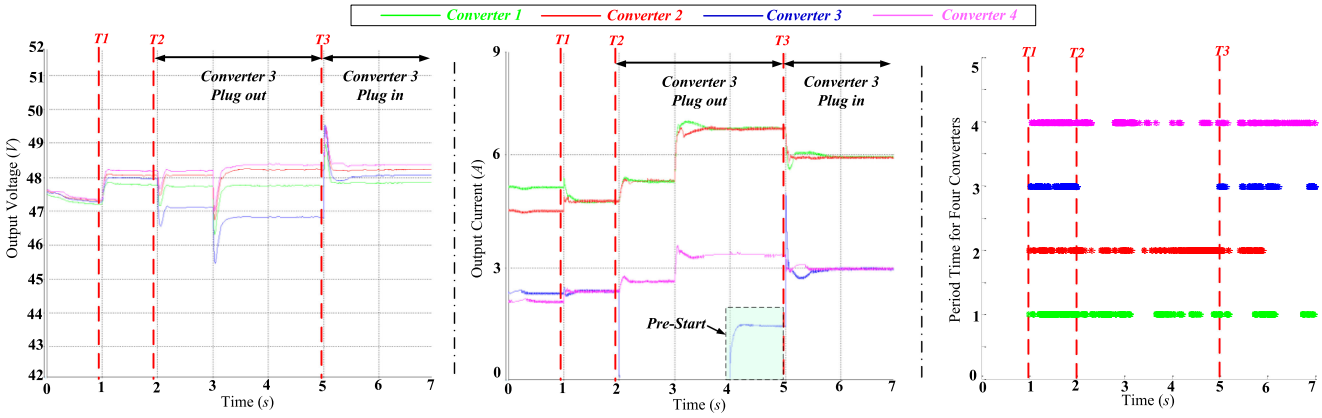


Fig. 18. Cross communication network.



(a). Performance of Output Voltage (b). Performance of Output Current (c). Perforance of Per Unit Current Value

Fig. 19. Performance under cross-communication network changed from stage 1 to stage 6.



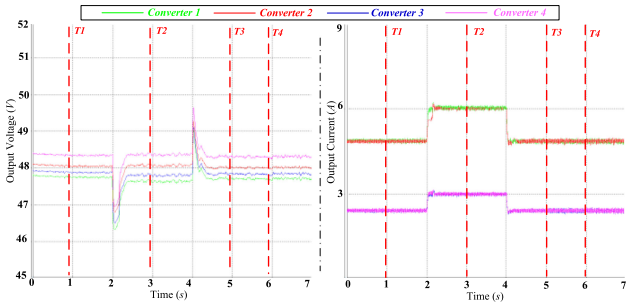
(a). Performance of Output Voltage (b). Performance of Output Current (c). Event Time Instants

Fig. 20. Performance for plug-and-play study.

performance more clearly during the failure process, Fig. 19 (c) presents the per-unit current value. From stage 1 to stage 3 before $t = T3$, even though three communication links are failed, the communication network is still a connected graph, thus the current sharing performance among four converters are guaranteed. Under stage 4 between $t = T3$ and $T4$, the communication network among converters 1, 2, and 4 is connected, thus the current sharing among these converters is accurate. Meanwhile, because the controller for converter 3 is separated from others, its output voltage is controlled at 48 V as discussed above. Then, under stage 5 between $t = T4$ and $T5$, the communication link between converter 1 and 4 is connected, thus the current sharing among these two converters is accurate as shown in Fig. 19(b) and (c). The communication links of converter 2 and 3 all failed, thus the output voltages from converters 2 and 3 are controlled at *48 V*. Finally, under stage 6 after $t = T5$, the communication in the system are completely separated, thus the proposed controller is disabled. All the converters are controlled only by the inner control loop which means the output current cannot be shared accurately and all the output voltage are controlled at *48 V*. In addition, comparing the performance shown in Fig. 19 after $t = T5$ (all the communication links are failed down) with the performance shown in Fig. 14 before $t = T2$ (the system is under V–I droop control), the current sharing performance from V–I droop controller is better. However, it also means that when all the communication links fail, the system can still be operated by controlling the voltage at the same value to avoid circular current in the system. Another choice is that, when the system detects that all the communication links fail, the droop control can be activated at the most serious condition temporarily. Thus, it is concluded that the tolerance of proposed event-triggered controller under communication failure condition can be preserved.

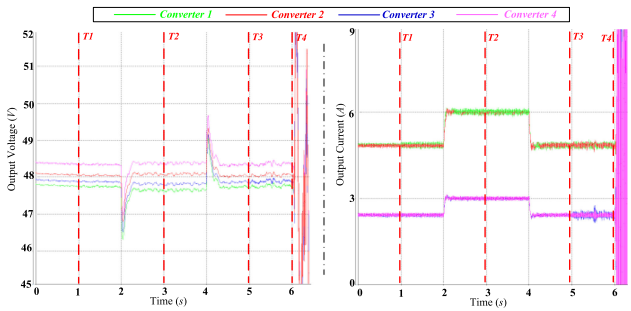
C. Case 3: Plug-and-Play Study

The performance about plug-and-play study is shown in Fig. 20. The local loads 1, 2 and public load 1 are connected to the system. The proposed controller is activated at $t = T1$. The converter 3 is plugged out at $t = T2$, then the voltage at the third bus is no longer available. Meanwhile, the failure of converter



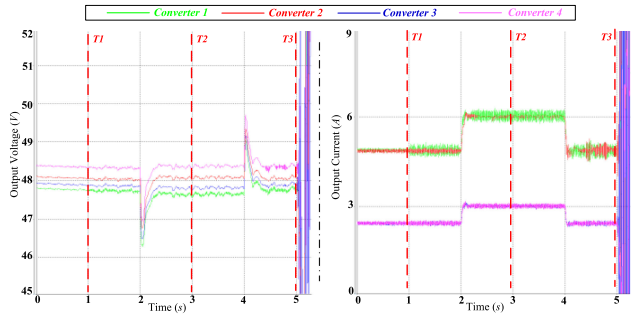
(a). Performance of Output Voltage (b). Performance of Output Current

Fig. 21. Control performance under 100 μs communication delay.



(a). Performance of Output Voltage (b). Performance of Output Current

Fig. 22. Control performance under 300 μs communication delay.



(a). Performance of Output Voltage (b). Performance of Output Current

Fig. 23. Control performance under 1000 μs communication delay.

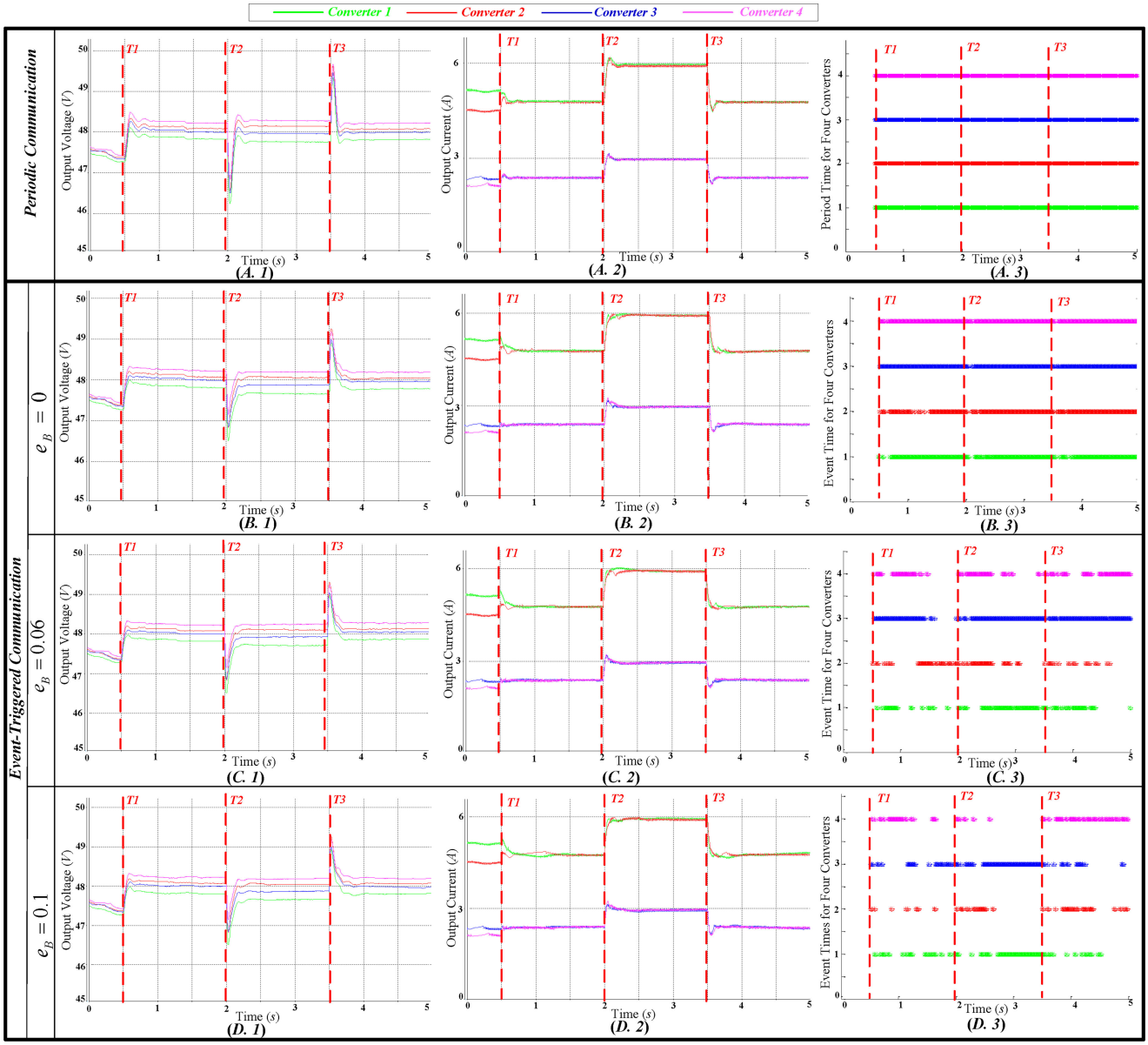


Fig. 24. Performance and communication traffic comparison among different communication strategies.

3 also means the communication links between converter 3 and 2, converter 3 and 4 are disabled simultaneously. Through the remaining communication links which still form a connected communication structure, the controllers regulate the remaining three output voltages around the nominal value and achieve the current sharing among the three converters.

Before plugging back the converter 3, the inter loop of converter 3 is activated first. At $t = T3$, the converter 3 is plugged back and the communication links and proposed controller for converter 3 are all activated. In Fig. 20(a) and (b), it is shown that during the period of plugging out, the public load 2 is connected in the system and the remained three converters can share the load proportionally and the output voltages can be controlled around the nominal value. After converter 3 is plugged in, the controller has properly updated the current sharing and voltage regulation normally. Fig. 20(c) shows the event time instants of each converter, from which it is seen that during the plugging out period, the controller for converter 3 is not triggered.

D. Case 4: Communication Delay Study

In this case, the communication delay effects for the proposed controller are studied. For the following three tests, local loads 1, 2 and public load 1 are connected in the system. After that, public load 2 is connected and disconnected from the system.

Fig. 21 shows the results of the system operating for 100 μs communication delay. The experimental process is as follows: at $t = T1$, $T2$, $T3$ and $T4$, 100 μs communication delay is added in the communication link for converter 1, converter 2, converter 3, and converter 4, respectively. At 2 and 4 s, the load is changed in the system. As shown in Fig. 21, the control performance can

be guaranteed even if all the communication links have 100 μs communication delay. It means that all the communication links exist in time delay simultaneously, the proposed controller can withstand 100 μs time delay or less.

Furthermore, as shown in Fig. 22, at $t = T1,\ T2,\ T3$ and $T4$, a 300 μs communication delay is added in the communication links for converter 1, converter 2, converter 3, and converter 4, respectively. It is shown that before $t = T4$, the system performance is kept well. After adding 300 μs communication delay for converter 4 at $t = T4$, the system become unstable. It means that if three-fourth of the communication links exist in time delay simultaneously, the proposed controller can withstand 300 μs time delay or less.

Fig. 23 shows the system performance with 1000 μs communication delay. At $t = T1,\ T2$, and $T3$, 1000 μs communication delay is added in the communication links for converter 1, converter 2, and converter 3, respectively. It is shown that before $t = T3$, the system performance can be kept well, and after adding 1000 μs communication delay to converter 3 at $t = T3$, the system becomes unstable. It means that if half of the communication links exist in time delay simultaneously, the proposed controller can withstand 1000 μs time delay or less.

To be mentioned, it is the normal case that the time delay does not exist in all the communication links simultaneously, thus the proposed controller is resilient to the time delay to certain degree. In addition, the communication delay has decisive effect on stability and performance. To alleviate this issue, the coefficient ρ can be chosen smaller to compensate the communication delay effects by increasing the frequency of triggering controller.

E. Case 4: Communication Traffic Comparison

The control performance and communication traffic comparison under four different communication strategies are studied. At the beginning of the test, the local loads 1, 2 and public load 2 are connected. Then at $t = T2$ and $T3$, the public load 1 is connected and disconnected, respectively.

The four strategies are as follows: periodic communication shown in Fig. 24(A.1)–(A.3), event-triggered communication without offset e_B in triggered principle shown in Fig. 24(B.1)–(B.3), event-triggered communication with offset $e_B = 0.06$ and $e_B = 0.1$ shown in Fig. 24(C.1)–(C.3) and (D.1)–(D.3), respectively. The experimental process under four conditions is same as: at $t = T1$, the proposed nonlinear controller is activated. It can be seen from Fig. 24(A.1), (B.1), (C.1), (D.1) and (A.2), (B.2), (C.2), (D.2), the steady-state performance about voltage regulation and current sharing are same. For transient-state performance, the overshoot under period communication is a little larger than that under event-triggered communication. In addition, comparing the event time instant between Fig. 24(A.3) and (B.3), a little different can be seen intuitively. However, the communication traffic differences between these two communication strategies are very large as shown in Fig. 25 quantitatively. The communication traffic under periodic communication is almost two times higher than that under event-triggered communication.

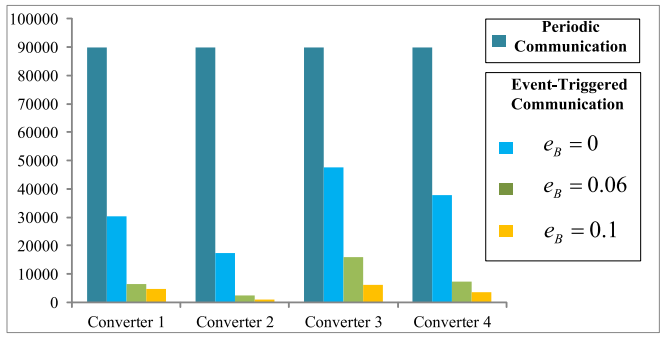


Fig. 25. Communication traffic comparison.

To be further discussed, under event-triggered communication with different offsets e_B, the control performances are almost same. But the as shown in Fig. 24(B.3), (C.3), and (D.3), the communication traffics are totally different. When there is no offset in the controller, even though the system is at the steady-state condition, the frequency of triggered events is not decreased as shown in Fig. 24(B.3). When the offset is set, the frequency of triggered event is decreased at both the transient-state and steady-state stage. The larger the offset is, the less the communication traffic is. But, if the offset is too large, the system will be unstable. To be more clearly, the total communication traffic comparison under four different communication strategies is shown quantitatively in Fig. 25. It is obvious that compared with the periodic communication condition, the communication traffic can be tremendously decreased. Meanwhile, with the offset in the triggered principle, the communication traffic can be decreased furthermore.

VII. Conclusion

A generalized dc MG model carrying all the details of a dc MG is proposed and proven to be positive definite. Considering different line impedances effects, a distributed nonlinear control scheme is proposed to achieve both precise current sharing and reasonable voltage regulation objectives simultaneously. Furthermore, a novel event-triggered communication strategy is proposed, in which the triggered condition is designed by combining state-dependent tolerance with nonnegative offset. Both the designs are based on Lyapunov-based approach to guarantee the convergence and global stability. By comparing the proposed controller and V–I droop controller from the stability point of view, the damping performance and the maximum CPL capability are same, which means the proposed controller can perverse the damping performance. Experimental results in a dc MG setup are shown to prove the effectiveness of the proposed method including robust and resiliency performance especially under the communication delay and communication failure operation. Furthermore, the communication traffic between periodic and event-triggered communication are compared to verify that the proposed controller can decrease the communication traffic tremendously. Furthermore, communication delay effect is so important that it will be analyzed in our future study from the theoretical viewpoint.

APPENDIX
EXAMPLE

$$\begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{array}\!\!\begin{array}{c} \begin{array}{cccccc} \textcircled{1} & \textcircled{2} & \textcircled{3} & \textcircled{4} & \textcircled{5} & \textcircled{6} \end{array} \\ \begin{bmatrix} -1 & 0 & 0 & 0 & 1 & 0 \\ 0 & -1 & 0 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 & 0 & 1 \\ 0 & 0 & 0 & 0 & -1 & 1 \end{bmatrix} \\ B \end{array}, \quad \begin{array}{c} \begin{bmatrix} G_{15} & 0 & 0 & 0 & 0 \\ 0 & G_{25} & 0 & 0 & 0 \\ 0 & 0 & G_{36} & 0 & 0 \\ 0 & 0 & 0 & G_{46} & 0 \\ 0 & 0 & 0 & 0 & G_{56} \end{bmatrix} \\ W \end{array}$$

Fig. 26. Numerical Model of Fig. 1.

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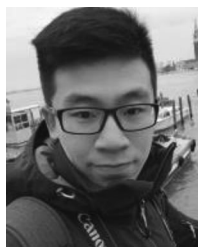

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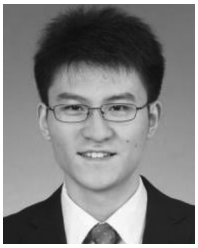

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