Design of a 10-kV·A Soft-Switching Solid-State Transformer (S4T)

Hao Chen, *Student Member, IEEE*, and Deepak Divan, *Fellow, IEEE*

***Abstract*—The soft-switching solid-state transformer (S4T) employs only 12 main active devices and an auxiliary resonant circuit to implement a bidirectional solid-state transformer, with an attractive feature of achieving a full range of zero-voltage-switching conditions for all the main devices. This paper covers detailed design of the power stage, auxiliary resonant circuit, and control of the S4T. The high-frequency transformer is an essential element for the S4T, and it has a unique feature of dc-biased flux. Design of such a high-frequency transformer is also discussed in detail in this paper. Soft startup, shutdown, and fast dynamic response under load transients are also attractive behaviors because of the low inertia of the S4T. Experimental results from a 208-V/10-kV·A S4T unit are presented.**

***Index Terms*—High-frequency transformer, resonant, shutdown, soft switching, solid-state transformer (SST), startup, transient, zero-voltage switching (ZVS).**

I. Introduction

SINCE the first solid-state transformer (SST) concept was introduced almost 50 years ago as an isolated single-phase ac/ac converter [1], various approaches to implement the SST have been proposed. Indeed, the SST, combining a high-frequency galvanic isolation link and power electronics converters, helps saving significant volume and weight of magnetic materials because of the high-frequency isolation. In addition, it gives the features of bidirectional power flow control, VAr support, harmonics elimination, dc or multiterminal interfacing, voltage regulation, sag correction, and fault isolation. However, the existing technical challenges that prevent the SSTs from being deployed in the grid are the high fault current coordination (typically $>$ 10 kA) and high basic insulation level (typically $>$ 120 kV for a 13 kV grid). For the applications such as electrified transportation, photovoltaic and wind inverters, battery energy storage systems, and bidirectional drives, the SSTs do exhibit a great potential.

Existing topologies to implement the SST can be classified as single-/two-/three-stage converters. The single- and two-stage SSTs are typically configured using bidirectional ac switches to perform direct ac/ac or ac/dc conversion with high-frequency isolation. These topologies include isolated direct or indirect matrix converter [2]–[4], flyback ac/ac converter [5], resonant ac-link converter [6], [7], and the Dyna-C SST [8]–[10]. The three-stage SST, that is configured with a rectifier, an inverter, and a dual-active-bridge (DAB) dc/dc converter, is the most straightforward approach to implement the SST and perhaps offers the best performance and controllability [11]–[13]. However, all the existing SST topologies have one or more of the following issues: large number of devices/components and conversion stages, diode reverse recovery, transformer trapped leakage energy, and various hard-switching issues of high switching loss, spikes, resonance, and electromagnetic interference (EMI) [14]–[17].

Unlike existing SST topologies that typically have a complex structure, the patent-pending soft-switching solid-state transformer (S4T) that was introduced in [18]–[20] achieves the same level of SST functionalities with a simple and symmetrical architecture, minimal device and component count in the power flow path. Topologies for dc, single- and multiphase ac are feasible by reconfiguring the device legs, acting as a universal power converter. Scaling to medium voltage is also achievable by series stacking the converter modules. More importantly, the small rated auxiliary circuit of the S4T enables zero-voltage switching (ZVS) soft-switching property. Unlike the DAB converter, the S4T can achieve ZVS for all the main devices from no-load to full-load conditions, and features controlled *dv/dt* and *di/dt* rates. Different from typical resonant converters, the S4T achieves soft-switching property with a fixed switching frequency and maintains pulse-width modulation capability. Control of the S4T becomes much easier and reliable by removing the dead-time and overlap states that are typically required for voltage-source and current-source converters. Eliminating components such as electrolytic capacitors realizes high power density and long life. Converter startup and shutdown procedures are fast and soft, without causing any inrush or high stress for the components. The high-frequency transformer of the S4T temporarily stores energy in the form of dc flux. Actively controlling the dc current through the transformer avoids saturation of the core. The relative low magnetizing inductance helps achieve a compact transformer design. It also enables fast dynamic response to load transients.

The S4T concept and operating principles have been described in [18]. This paper will cover the detail design of the S4T, which includes the design of the power converter stage,

Manuscript received April 16, 2017; revised July 9, 2017; accepted August 21, 2017. Date of publication September 5, 2017; date of current version March 5, 2018. Recommended for publication by Associate Editor C. N. M. Ho. *(Corresponding author: Hao Chen.)*

H. Chen is with Tesla, Palo Alto, CA 94304 USA (e-mail: hchen95@gatech.edu).

D. Divan is with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA, and also with Varentec, Inc., Santa Clara, CA 95054 USA (e-mail: ddivan@gatech.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2749430

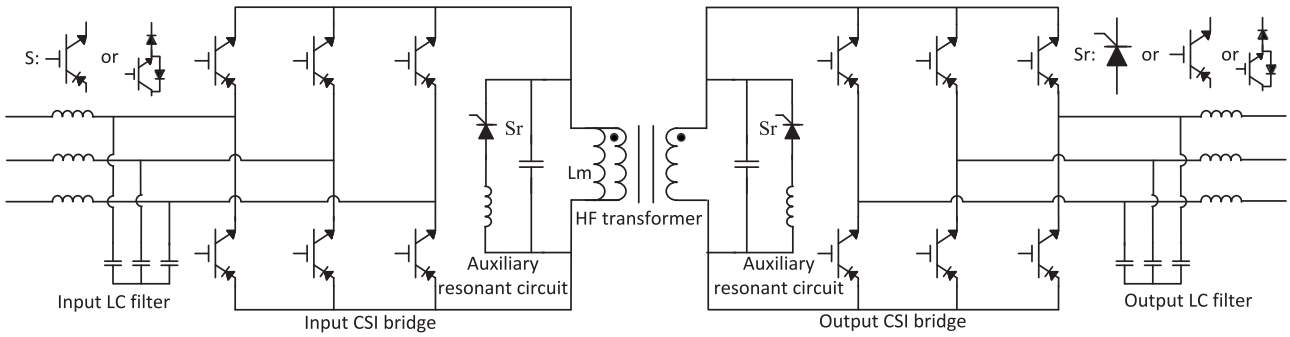


Fig. 1. Topology for the three-phase S4T.

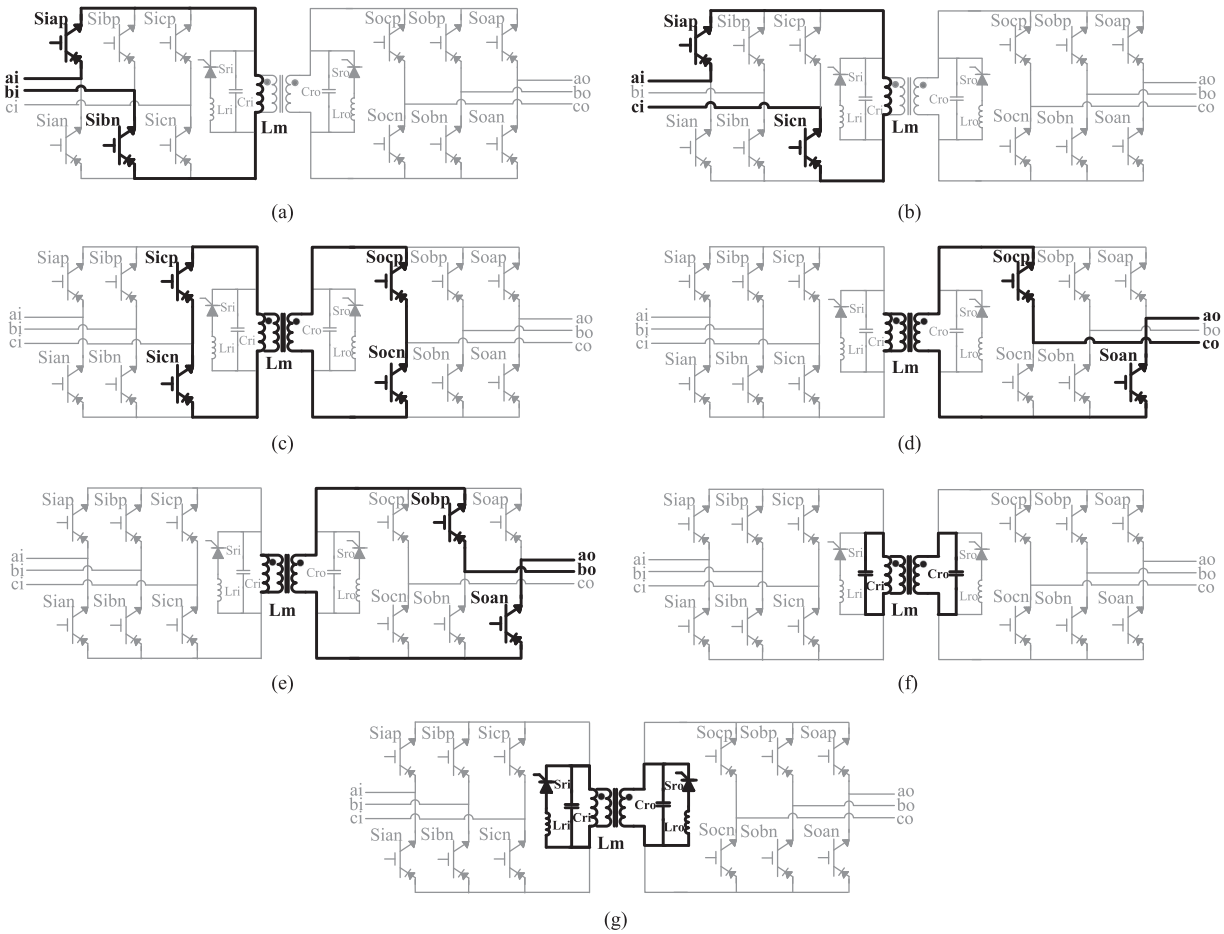


Fig. 2. Operating states over one switching cycle: (a) state 1—charging the magnetizing inductance with the first line-to-line input voltage, (b) state 2—charging the magnetizing inductance with the second line-to-line input voltage, (c) state 3—freewheeling, (d) state 4—discharging the magnetizing inductance with the first line-to-line output voltage, (e) state 5—discharging the magnetizing inductance with the second line-to-line output voltage [(a)–(e) are the five active states], (f) state 0—ZVS transition state, and (g) state 6—resonant state.

auxiliary resonant circuit, high-frequency transformer, and the state machine of the controller. Proper startup and shutdown procedures will be proposed to avoid inrush. Experimental results from a 208-V/10-kV·A S4T unit will be shown and discussed.

II. Operating Principle of the S4T

Fig. 1 shows the topology of the S4T, which consists of current-source inverter bridges on the input and the output sides, a high-frequency transformer, terminal *LC* filters, and auxiliary resonant circuits. The converter only requires 12 active devices and two low-rated auxiliary devices to fulfill all the SST functionalities. One switching cycle operation consists of two active charging states in which the transformer magnetizing inductance gets charged by the input as shown in Fig. 2(a) and (b), two active discharging states in which the magnetizing inductance gets discharged by the output as shown in Fig. 2(d) and (e), and one freewheeling state as shown in Fig. 2(c). When transitioning

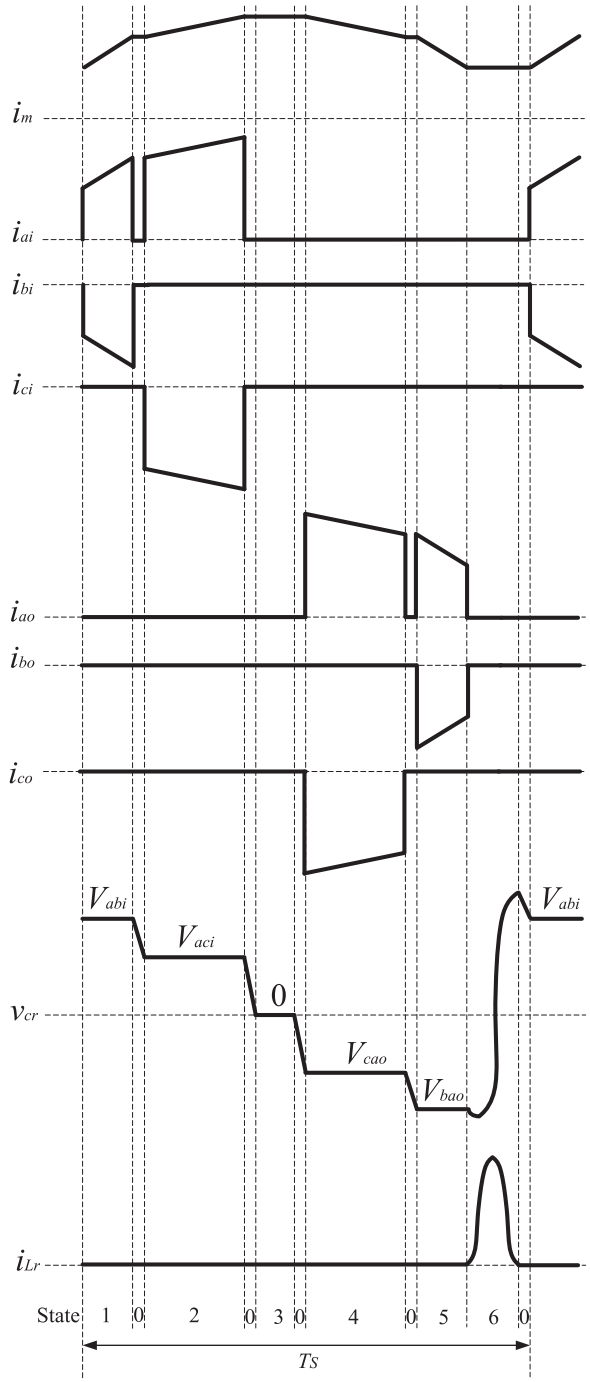


Fig. 3. Conceptualized waveforms [states 1–5 corresponds to Fig. 2(a)–(e), state 0 corresponds to Fig. 2(f), and state 6 corresponds to Fig. 2(g)].

from one active state to another, the auxiliary resonant circuit provides ZVS conditions for all the main devices as shown in Fig. 2(f). The auxiliary circuit is reset at the end of each switching cycle, setting up the conditions for soft-switching actions of the next switching cycle. Detailed operating principle can be found in [18]. Fig. 3 shows the conceptualized waveforms of the transformer magnetizing inductance current, the resonant capacitor voltage, the resonant inductor current, and the unfiltered three-phase input and output currents over one switching cycle T_S.

III. S4T Power Converter Design

A 10-kV·A S4T unit was developed to prove the concept. The input and output of the S4T were connected to the same 208 V three-phase power source and it was running to circulate power between the input and the output. The corresponding input/output current for the 10-kV·A S4T is thus 28 A, and the switching frequency is set to be 15 kHz. This section will present the detailed design of the S4T power stage, including the semiconductor devices, filters, sensors, and the auxiliary resonant circuit.

A. Semiconductors

The main devices of S4T are stressed at 2 p.u. current, the optimum value to maintain the transformer magnetizing current. However, since the duty cycle of each device is less than 0.5, the devices do not suffer from a heavy thermal burden. Converter's conduction loss highly depends on the RMS current, not the peak current. Therefore, the S4T's conduction loss is not high even though the peak current is 2 p.u. The semiconductors usually can be stressed at a high current level when the duty cycle is small. In addition, ZVS operation eliminates all switching losses, which further reduces the thermal stress on the S4T devices. Since the converter only has conduction loss, devices with low voltage drop are preferred such that overall efficiency is high.

The devices of the S4T should be able to conduct current in one direction but block voltage in both directions. This can be implemented using a reverse blocking insulated-gate bipolar transistor (RB-IGBT) or an IGBT/MOSEFT in series with a diode. Compared to the discrete solution, RB-IGBTs can provide a more compact design and lower conduction loss. It was reported in [21] that the overall voltage drop can be 25% less for the RB-IGBTs. However, these devices exhibit poor switching characteristics due to the high reverse recovery at turn-off. This in turn makes the RB-IGBTs to be effectively used in the S4T since all the main devices are switched under ZVS conditions. For the discrete solution, both silicon (Si) IGBTs and silicon-carbide (SiC) MOSFETs can be used. When the S4T is operated at full power level of 10 kV·A, the transformer magnetizing current is maintained at over 80 A. Since the S4T efficiency is dominated by conduction loss, Si IGBT is preferred over SiC MOSFETs here due to the lower voltage drop at that high current level.

B. Filters

Filters are needed at the input and output terminals to suppress the switching harmonics. Filter capacitors provide energy filtering on a switching cycle-to-cycle basis and ensure sinusoidal voltages on the input and the output. Filter capacitors should be large enough such that the voltage ripple is maintained within a typical range of 5–10%. Also, the reactive power effect of the capacitors should be considered when selecting the capacitance values. Different from the voltage-source converter, the capacitive filters of S4T offer very low *dv/dt*, low EMI, and low harmonic distortion across the unit terminals. Capacitor banks consisting of multiple parallel-connected large- and small-film

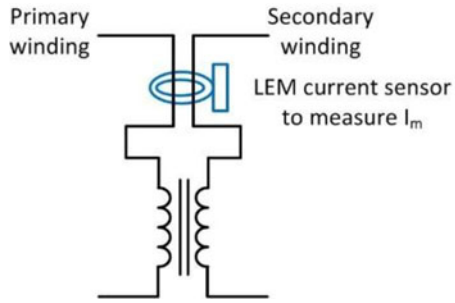


Fig. 4. LEM current sensor to measure the transformer magnetizing current.

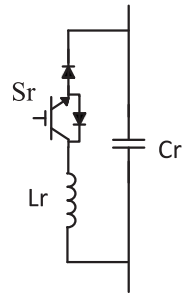


Fig. 5. Auxiliary resonant circuit of the S4T.

capacitors are used for the design to achieve small parasitic inductance. Large capacitors provide energy buffering for the entire switching cycle. Small capacitors are placed close to the devices, providing snubbering and low equivalent series inductance (ESL) path for the device switching transients.

Filter inductors ensure sinusoidal current injection into the input and the output. With filter capacitors being selected, the filter inductors should be sized such that the switching harmonics components are attenuated enough to meet the harmonics standard. The S4T has a capacitive filter structure, for which the filter inductor is connected with a shunt filter capacitor such that it does not see the switching voltage ripples as the conventional voltage-source converter. This leads to lower filter inductor losses. However, for some types of load such as motors, filter inductors are not needed due to the inductive property of these loads.

C. Sensors

Parameters needed to be sensed for the S4T include the transformer magnetizing current, filter capacitor voltages of the three-phase input and output, three-phase grid voltage, and three-phase line current. LEM sensors are used to sense all the voltages and currents, which give high-frequency resolution and dc signal sensing capability. To sense the dc magnetizing current, the positive terminals of both the primary winding and the secondary winding of the transformer pass through a LEM current sensor. The sum of the primary and secondary winding currents always equals to the magnetizing current. The magnetizing current measurement scheme is shown in Fig. 4.

D. Auxiliary Resonant Circuit

The auxiliary resonant circuit shown in Fig. 5, consisting of C_r, L_r, and S_r, is key to successful ZVS operation of the S4T over its designed load range. It provides soft-switching conditions for all the main devices. It is reset at each switching cycle by starting a resonant operation of L_r and C_r. C_r determines the *dv/dt* rate when the main devices are turned off, and thus it governs the turn-off loss of devices. L_r and C_r determine the length of the resonant period and the current stress of S_r. The design of the auxiliary resonant circuit is guided by the following objectives.

1) C_r should be selected such that device turn-off loss is minimized to almost zero;
2) the peak value of i_{Lr} should be within the safe operation area of the auxiliary device;
3) the RMS value of i_{Lr} should be minimized to reduce the circulating power loss occurred in the resonant operation period;
4) the resonating time period of L_r and C_r should be minimized such that most of the switching time period is used for transferring energy from the input to the output;
5) the peak voltage of v_{Cr} should be close to 1 p.u;
6) time duration of the ZVS transition should be long enough to ensure that the incoming turn-on device is gated-on within this transition state.

For objective 1, the *dv/dt* rate at the device turn-off transition is controlled by C_r, which in turn determines the device turn-off loss. Consider a converter rated at 208 V/10 kV·A, with a switching frequency of 15 kHz and L_m of 200 μH. Simulation results show that, in the steady-state operation at the full-load level of 10 kV·A, the devices are always switched around the three current levels of 70, 100, and 130 A. Fig. 6 shows the device turn-off loss versus different C_r values for the device of C2M0025120D at these three current levels. It can be seen from Fig. 6 that the turn-off loss is close to zero when C_r is larger than 0.1 μF. With 0.1 μF C_r, the corresponding *dv/dt* at 130 A is 1.3 kV/μs. As a comparison, the *dv/dt* for the Si IGBT NGTB50N120FL2WG is 6 kV/μs and for the SiC MOSFET C2M0025120D is 28.5 kV/μs, as given by the datasheet [23], [24].

The peak value and RMS value of the resonant current i_{Lr}, resonant time period T_r, and the peak value of v_{Cr} are all governed by the resonant state, which is governed by (1). The expressions of v_{Cr} and i_{Lr} are then given in (2). The peak current of i_{Lr} is obtained by having di_{Lr}/dt equal to zero, as given by (3). The resonant time period T_r shown in (4) is derived by having i_{Lr} equal to zero. The RMS value of i_{Lr} is calculated using (5). Finally, the peak value of v_{Cr}, given by (6), is obtained by having dv_{Cr}/dt equal to zero. Fig. 7 shows the peak value, RMS value of i_{Lr}, resonant period T_r, and the peak value of v_{Cr} versus different L_r and C_r values

$$\begin{cases} i_{Lr} + i_{Cr} = I_m \\ v_{Cr} = L_r \frac{di_{Lr}}{dt} \\ i_{Cr} = C_r \frac{dv_{Cr}}{dt} \end{cases} \quad \text{with the initial conditions of}$$

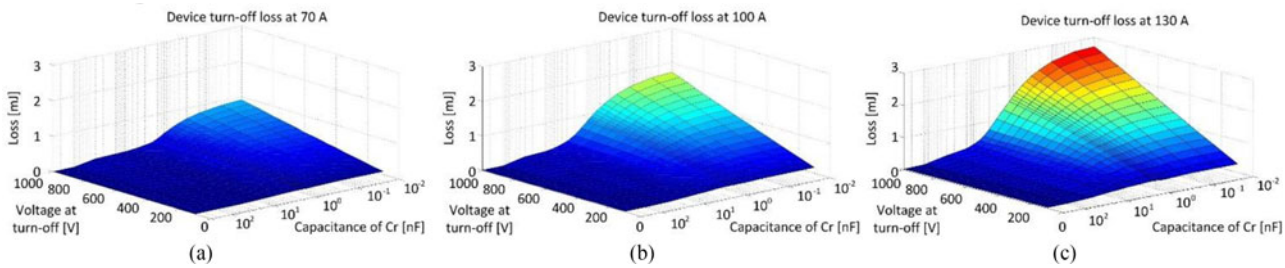


Fig. 6. Device turn-off loss versus C_r capacitance during the phase-leg transition at three turn-off current levels: (a) 70 A, (b) 100 A, and (c) 130 A.

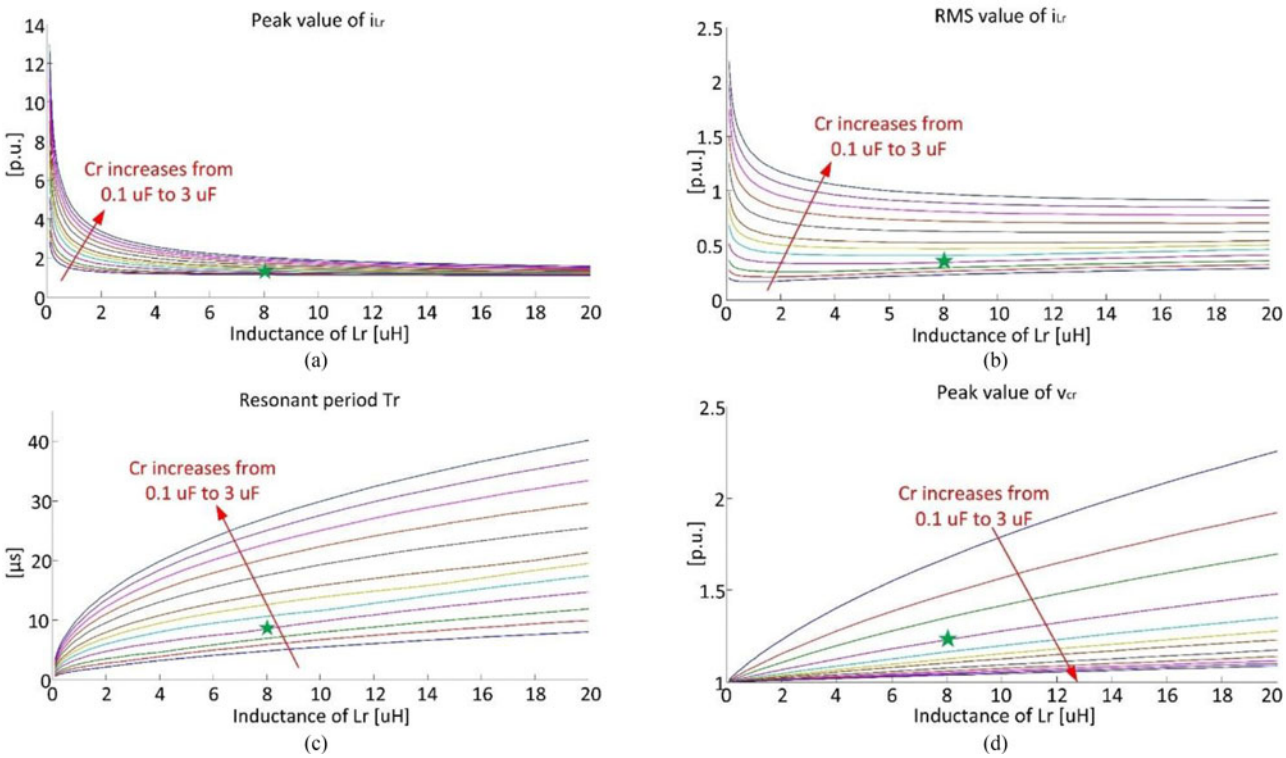


Fig. 7. Peak value, RMS value of i_{Lr}, resonant period T_r, and peak value of v_{Cr} versus different L_r and C_r values.

$$\begin{cases} v_{Cr}\left(t=0\right)=V_{Cr0} \\ i_{Lr}\left(t=0\right)=0 \end{cases} \tag{1}$$

$$\begin{cases} v_{Cr}=I_m\sqrt{\frac{L_r}{C_r}}\sin\left(\sqrt{\frac{1}{L_rC_r}}t\right)+V_{Cr0}\cos\left(\sqrt{\frac{1}{L_rC_r}}t\right) \\ i_{Lr}=I_m\left(1-\cos\left(\sqrt{\frac{1}{L_rC_r}}t\right)\right)+V_{Cr0}\sqrt{\frac{C_r}{L_r}}\sin\left(\sqrt{\frac{1}{L_rC_r}}t\right) \end{cases} \tag{2}$$

$$I_{Lr,pk}=I_m\left(1+\sqrt{\frac{L_rI_m^2}{C_rV_{Cr0}^2+L_rI_m^2}}\right)+C_rV_{Cr0}^2\sqrt{\frac{1}{L_rC_rV_{Cr0}^2+L_r^2I_m^2}} \tag{3}$$

$$T_r=\sqrt{L_rC_r}\left(2\pi-\sin^{-1}\frac{2V_{Cr0}I_m\sqrt{L_rC_r}}{L_rI_m^2+C_rV_{Cr0}^2}\right) \tag{4}$$

$$I_{Lr,\mathrm{rms}}=I_{Lr,\mathrm{pk}}\sqrt{\frac{T_r}{2T_{\mathrm{SW}}}} \tag{5}$$

$$V_{Cr,\mathrm{pk}}=I_m^2L_r\sqrt{\frac{1}{L_rC_rI_m^2+C_r^2V_{Cr0}^2}}+V_{Cr0}^2\sqrt{\frac{C_r}{L_rI_m^2+C_rV_{Cr0}^2}}. \tag{6}$$

It can be seen from Fig. 7 that a larger L_r leads to a lower peak and RMS value of i_{Lr}, but a longer resonant period T_r, and a higher peak value of V_{Cr}. Although a larger C_r also leads to a higher peak and RMS value of i_{Lr}, as well as a longer resonant period T_r, the peak value of V_{Cr} will become smaller. In addition, the *dv/dt* rate, controlled by C_r, should be low enough such that the devices can finish their switching action on time at the desired transition, considering the latency of the controller, the gate driver, and the device switching time.

As a result, the parameters of $L_r = 8\,\mu$H and $C_r = 0.4\,\mu$F, corresponding to the green star indicator shown in Fig. 7, are selected for the 208-V/10-kV·A S4T.

IV. High-Frequency Transformer Design

The high-frequency transformer of the S4T is a key element, which acts as an isolated energy transferring link with a limit amount of energy storage. The conceptualized waveform of Fig. 3 shows that the transformer magnetizing current has a dc offset value with high-frequency ac ripple on top of it. Therefore, the magnetizing inductance should be designed to have a certain value with dc current carrying capability. The transformer core needs to have an air gap to store dc energy. The transformer for the S4T should be designed with low core loss, low winding loss, and relatively low leakage.

As the S4T transformer needs to store dc flux, the transformer core design is driven by the core saturation limit. Appropriate core should be designed such that the flux density approaches the saturation level when magnetizing current reaches peak. Nanocrystalline core shows the best potential since it has high saturation flux density of 1.25 T and low core loss at high frequency. For the 10-kV·A S4T unit, the transformer with the magnetizing inductance of 200 μH and the current carrying capability of 120 A is designed.

The dc-biased feature indicates that the core is only operated in the first quadrant of the *B–H* curve while the third quadrant region is not utilized. Considering this, permanent magnets can be integrated with the magnetic materials to provide a prebiased flux for the core, leading to a hybrid design. The flux generated by the permanent magnets should be in a reverse direction to the flux excited by the windings. As shown in (7), the resultant equivalent flux density (B_{eq}) within the core will be the flux density of the excitation from the winding (B_w) minus the flux density caused by permanent magnets (B_{pm}). If the core flux density is kept below the saturation level (B_{sat}), more energy can be stored in the transformer, as shown in (8). In this way, the usable *B–H* curve of the core can be extended to the third quadrant, which helps reduce the amount of magnetic materials needed. A simple design to achieve this is by putting the permanent magnet inside the airgap. The permanent magnet is placed in a direction such that it tries to cancel the flux generated by the windings

$$B_{eq} = B_w - B_{pm} \le B_{sat} \tag{7}$$

$$B_w \le B_{sat} + B_{pm}. \tag{8}$$

Appropriate permanent magnet has to be selected for the hybrid high-frequency transformer. Besides the residual flux density, the permanent magnets have another two important parameters, the coercive force H_c and intrinsic coercive force H_{ci}. For proper operation, the magnetic field strength excited by the windings and seen by the permanent magnet should be kept on the right-hand side of H_c point, or at least the H_{ci} point. Violating this constraint will cause the demagnetization of the permanent magnets. For the hybrid transformer design, the consequence is that the permanent magnet flux will change its direction. In this case, rather than cancelling the flux excited by the winding, the permanent magnet flux will be added onto it and will further saturate the core. Coercive force H_c, intrinsic coercive force H_{ci}, residual flux density B_r, and maximum operating temperature $T_{\max}$ of various permanent magnets are given in Table I [31]. The material NdFeB is selected for the hybrid design since it has the largest coercive force H_c and intrinsic coercive force H_{ci} values. Meanwhile, its residual flux density is close to the saturation flux density of the nanocrystalline material, indicating that it can fully bias the core. However, analysis shown that the permanent magnet inside the airgap will see a field strength of 1634 kA/m when the S4T is fully loaded at 10 kV·A, which is larger than the H_{ci} value of NdFeb and indicates demagnetization of the permanent magnet.

TABLE I
Characteristics of Various Permanent Magnets

Materials	H_c (kA/ m)	H_{ci} (kA/ m)	B_r (T)	$T_{\max}$ (°C)
NdFeB (39H)	979	1671	1.28	150
SmCo	732	796	1.05	300
Alnico	51	51	1.25	540
Ceramic	255	259	0.39	300
Flexible	109	110	0.16	100

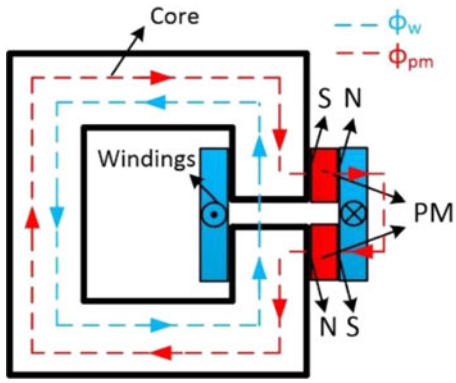


Fig. 8. Proposed hybrid transformer design with two pieces of permanent magnet placed on the side of the core around the air gap.

To avoid demagnetization, the permanent magnet should be placed out of the main flux path while providing dc flux bias to the core. Some design methodologies have been proposed in [25]–[28], but most of them involve a complicated core design. The design proposed in this paper is shown in Fig. 8, in which two pieces of permanent magnets are placed on the side of the core around the air gap. With the winding current direction shown in the figure, the direction of the flux generated by the winding Φ_w is counterclockwise, shown as the blue dash line. The permanent magnet on the top of the air gap is placed in a way that its south pole is facing toward the magnetic core, while the one below the air gap has its north pole facing toward the core. In this way, the two permanent magnets create a flux flowing path as shown in red dash line, which tends to cancel the flux generated by the winding. The cross-sectional area of the two permanent magnet should be the same as the core's such that enough biased flux is generated. For the selected core, the

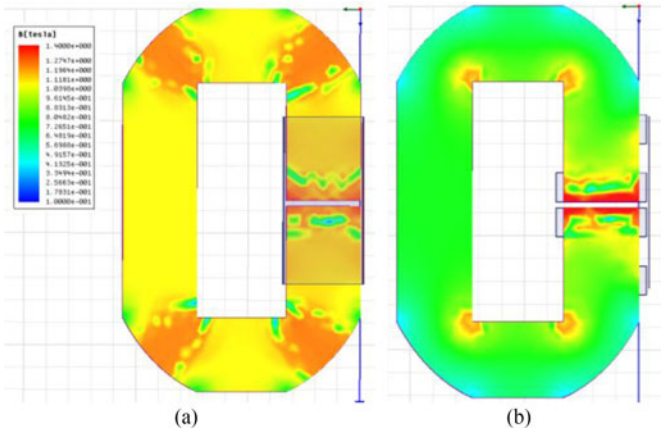
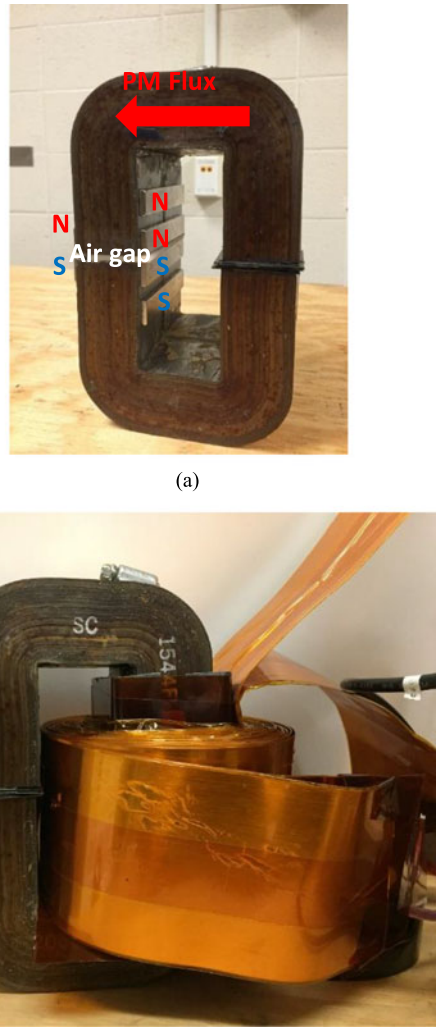


Fig. 9. Finite-element analysis simulation for the two transformers: (a) conventional transformer design with magnetics only and (b) hybrid transformer design with magnetics and permanent magnets.

required cross-sectional area of the permanent magnet should be 28 cm^2. Such a permanent magnet has a magnetic force larger than 100 lbs, which is very difficult and dangerous to work with. For the final design, three pairs of IMNB1122 Neodymium bars are used, each of which has a dimension of 3" × 0.5" × 0.13". Two pairs are placed on the outside of the core, and one pair is placed inside the core window.

As the S4T unit will be connected to the same voltage source, a 1:1 transformer turn ratio is needed. The windings of the transformer should be designed properly to maintain a low winding loss. The dc winding loss only depends on the resistivity of the conductor and typically has a low value. The ac winding loss, resulting from the skin effect and the proximity effect, may become significant as the frequency goes higher. One effective way of minimizing the winding loss is to use litz wires, which consist of many thin insulated wire strands. However, the litz-wire-based approach adds a significant cost to the design. It also leads to poor filling factor for the cores, and it may have higher resistance for dc current. A cost-effective method is to use the copper foil conductors with large conductor width, which is used in this design. The selected copper foil has a width of 7.62 cm and a thickness of 22 mil, which makes it properly fill in the core window and achieve low dc resistance when carrying 120 A peak current. The primary and secondary windings of the transformer have the same 12 turns, and they are fully interleaved to achieve low leakage inductance.

Two high-frequency transformers designed with conventional (without permanent magnets) and hybrid (with permanent magnets) methodologies are evaluated through experimental results. Both transformers use the same nanocrystalline core of SC2068M1. Since both transformers have the same size core, it is expected that the hybrid transformer can store much more energy than the conventional transformer. Finite-element analysis simulation is first performed for both the conventional transformer and the hybrid transformer using the same size of cores. The simulation results are shown in Fig. 9. For both transformers, the number of turns of the windings is 12, and the windings are excited by 160 A current. As shown in the results, with the same level of current excitation, the hybrid design has a much lower flux density due to the permanent magnet's flux cancelling effect. For the fabricated hybrid transformer, Fig. 10(a) shows the placement of the permanent magnets, and Fig. 10(b) shows the final fabricated transformer with windings.



(a)

(b)

Fig. 10. Fabricated hybrid transformer: (a) magnetic core and permanent magnets and (b) final fabricated hybrid transformer.

The two transformers are tested by injecting a current into them. In the test, a dc voltage, whose duration is controlled by a semiconductor device, is applied across one side of the transformer while keeping the other side open. Waveforms of the voltage applied across the transformer and the current through it for both transformers are shown in Fig. 11. For the conventional transformer, saturation is clearly indicated by the exponentially increasing current that occurs after reaching a certain level. However, for the hybrid transformer, the current continuously increases without any saturation. Fig. 12 shows the calculated inductance versus current curves for these two transformers. As shown, the conventional transformer magnetizing inductance quickly drops once the current exceeds 170 A, indicating saturation. However, for the hybrid transformer, the magnetizing

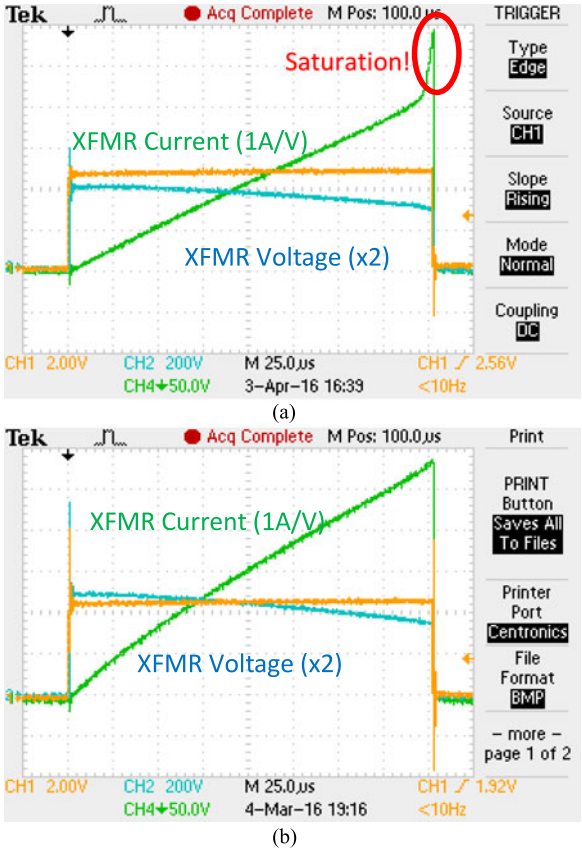


Fig. 11. Experimental current and voltage waveforms of the two transformers' tests: (a) waveforms for the conventional transformer and (b) waveforms for the hybrid transformer.

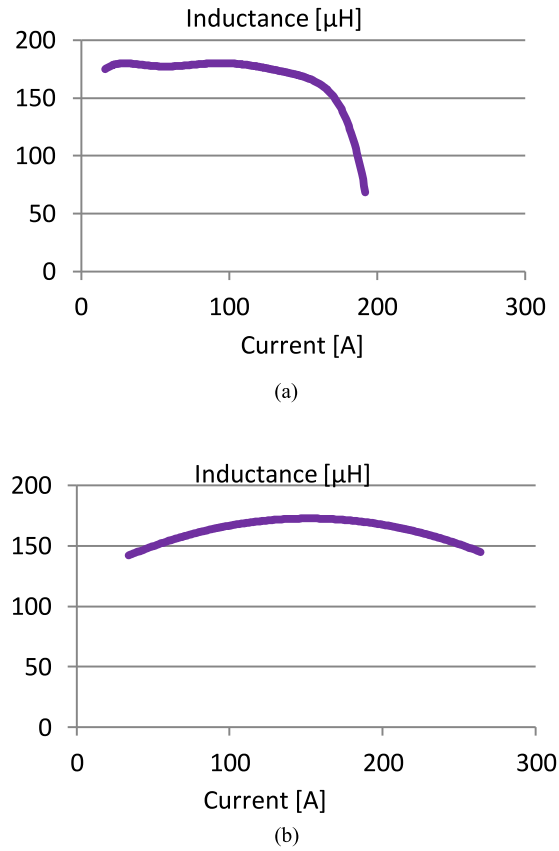


Fig. 12. Calculated magnetizing inductance versus current curves based on the results of Fig 11: (a) conventional transformer and (b) hybrid transformer.

inductance is still maintained at a higher value even when the current reaches 270 A. It should be noted here that the transformer for the S4T is alike the flyback transformer, for which the energy is stored in the magnetizing inductance. Therefore, for this transformer, the current flowing through the transformer winding represents the energy stored in the core.

Consider some inductance values from Fig. 12 for a comparison. The conventional design has a magnetizing inductance of 170 μH at 166 A and 160 μH at 176 A while the hybrid transformer shows an inductance of 170 μH at 220 A and 160 μH at 240 A. Therefore, with the same size of the magnetic core, the hybrid transformer design can store 75% more energy compared to the conventional design. In other words, to achieve the same amount of energy storage, the hybrid transformer design can reduce core materials by 63%.

V. State Machine to Control the S4T

A charge-control-based modulator, which was initially proposed to control a rectifier [22], is selected for controlling the S4T, in which the duty cycle of each state as shown in Figs. 2 and 3 is determined by the actual charge delivered to the specific terminal over each switching cycle. The closed-loop controller has been presented in detail in the companion paper [29]. This paper only covers the state machine that commands the converter switching from one state to another. In the steady state, the converter has two active charging states, two active discharging states, one freewheeling state, and six ZVS transitioning states over one switching cycle. Fig. 13 shows the state machine programmed in the field-programmable gate array (FPGA) for the S4T.

Conditions for normally transitioning from one state to another are described as below, which are also denoted as green arrows in Fig. 13. For the transitions from active states (states 4, 5, 1, 2,) to the ZVS transition state (state 0), the condition is that a required charge is delivered to specific terminals of the input or the output (i.e., charge control modulation). For transitions from state 0 to other states, the condition is that state 0 lasts for a duration of Δt. Δt should be selected such that after this amount of time duration, the resonant capacitor voltage is still higher than the incoming line-to-line voltage, ensuring ZVS turning-on of the incoming devices. Δt is set to be 100 ns for the designed S4T converter, considering the *dv/dt* rate when the S4T is running at full power level. For transitioning from the resonant state (state 6) to the ZVS transition state (state 0), the condition is that state 6 lasts for a duration of t_r. t_r should be selected large enough such that the resonant operation between L_r and C_r concludes and that the current through L_r reaches zero. t_r is selected to be 7.5 μs for the designed S4T converter, considering the resonant period of the 0.4 μF C_r and the 8 μH L_r. The condition for transitioning from the freewheeling state

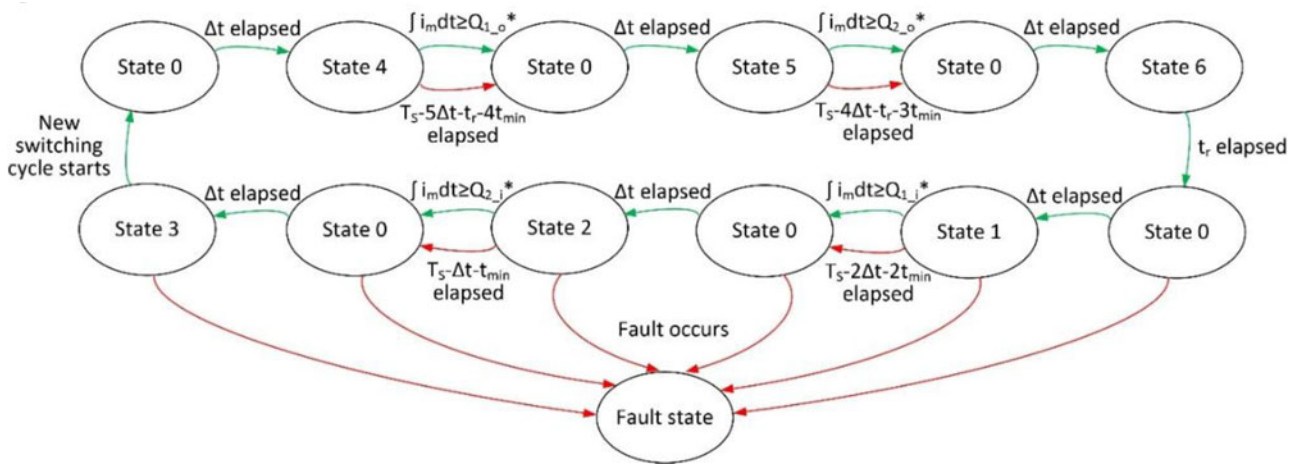


Fig. 13. State machine programmed in the FPGA to control the S4T.

(state 3 which is the last state for the entire switching cycle) to state 0 is the start of a new switching cycle.

All the above conditions are for the normal transitions from one state to another. However, for some cases, these transitioning conditions may not be satisfied. For example, the transformer magnetizing current may be too low such that it takes a very long time duration to deliver the required charge. Then, the converter will be staying at an active state for long time just because the transition condition is not met. As a result, the converter will not be able to cycle through all these states before the ending of the entire switching cycle. When a new cycle starts, the converter directly switches from the current state to state 0 and then to state 4. Taking a specific example, the converter stays at state 5 until the end of the switching cycle, because it cannot deliver the required charge to the second output phase pair. When a new switching cycle starts, the converter is forced to enter state 0 and then state 4. In this case, the resonant capacitor voltage directly jumps from a lower voltage level to a higher one, causing inrush current. To avoid this, alternative transitioning conditions are programmed, shown as red arrows in Fig. 13. In these alternative conditions, a "watch dog" timer initiates alternative action. The timer starts at the beginning of each switching cycle, and it is reset at the end of each cycle. If the "watch dog" finds that the converter stays within one state for a too long time, it will force the converter to enter the next state, regardless whether the normal transitioning conditions have been satisfied or not. The "watch dog" is programmed to make sure that the converter cycles through all the states, under both normal and abnormal conditions. The minimum time duration for each active state is $t_{\min}$, which is set to be 1 μs in the program.

VI. S4T Startup and Shutdown

The S4T does not have large dc energy storage capacitors, as for conventional voltage-source converters. As a result, during the converter startup and shutdown, it does not need to have an external startup circuit with large resistors and relays to suppress inrush current. However, the S4T still has small resonant capacitors connected in shunt with the high-frequency transformer.

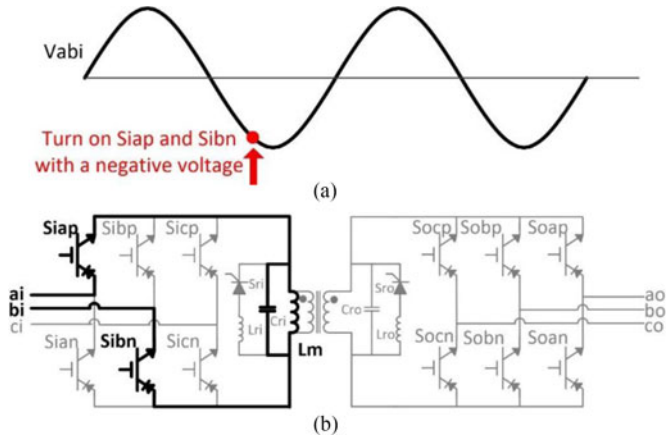


Fig. 14. Charging the resonant capacitors during startup: (a) input line-to-line voltage V_{abi} and (b) turn-on S_{iap} and S_{ibn} when V_{abi} is negative.

Although they have a very small capacitance value, hard startup and shutdown with a large line voltage directly applied across them still generate inrush current. The peak of the inrush current depends on the capacitance value and the parasitic inductance of the current loop that is typically very small. Hard startup and shutdown with Si devices may be acceptable since these devices can typically withstand much higher short-circuit current, but it may be problematic for SiC devices as their short-circuit current withstanding capability is low. Therefore, proper startup and shutdown procedures are needed to avoid inrush.

A. Startup

At startup, the resonant capacitor voltage should be charged without any inrush current. This can be achieved by turning on the devices whose corresponding input line-to-line voltage is negative. As shown in Fig. 14, devices S_{iap} and S_{ibn} are turned on when V_{abi} is negative. Devices do not conduct since they are reverse blocked. When the voltage V_{abi} crosses zero, S_{iap} and S_{ibn} start to conduct, and the capacitor voltage will be the same as V_{abi}. However, the resonant capacitors cannot be charged to

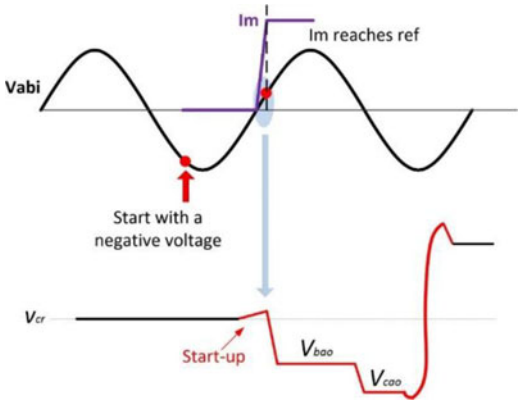


Fig. 15. Conceptualized startup waveforms of input line-to-line voltage V_{abi}, the magnetizing current I_m , and the resonant capacitor voltage V_{Cr} of the first switching cycle after the startup.

its peak voltage by V_{abi} only. Assuming a 180 μH transformer magnetizing inductance, the corresponding impedance at line frequency is only 0.068 Ω. As a result, when the line voltage reaches its peak to fully charge the resonant capacitors, the transformer magnetizing current already reaches several thousand amperes, which is definitely not desired.

The proper way of charging resonant capacitors is by using the energy of the transformer magnetizing inductance. When V_{abi} crosses zero, S_{iap} and S_{ibn} start to conduct, and the transformer magnetizing inductance is charged by V_{abi}. The magnetizing current I_m will quickly increase due to the low impedance of the transformer magnetizing inductance. As soon as I_m reaches a certain level, S_{iap} and S_{ibn} are turned off, and I_m charges the resonant capacitors to decrease their voltage V_{Cr} toward a negative value. Since resonant capacitors are quite small, I_m can charge it to a very large negative value. Then, the cycle-by-cycle operation can start in a way similar to the steady-state operation. The conceptualized startup waveforms are shown in Fig. 15 as the input line-to-line voltage V_{abi}, the magnetizing current I_m, and the resonant capacitor voltage V_{Cr} of the first switching cycle after the startup. It should be noted that, even during the startup procedure, all devices are switched under soft-switching conditions.

Fig. 16 shows the experimental results during startup. The external push button to start up the converter is triggered at an arbitrary instant. However, since the input line-to-line voltage of V_{abi} (green curve in Fig. 16) is positive at this moment, devices are not turned on. Once V_{abi} reaches a negative value, S_{iap} and S_{ibn} are turned on but they do not conduct. When V_{abi} crosses zero in a positive direction, S_{iap} and S_{ibn} are forward biased, and I_m quickly builds up. Once I_m reaches a certain level, the normal cycle-by-cycle operation starts. Zoomed-in waveforms of the magnetizing current and two resonant capacitor voltages are shown in Fig. 16(b).

It should be noted that the startup sequence can be initiated with any phase pair, e.g., phase *b* and phase *c*, or phase *c* and phase *a*, by turning on the devices corresponding to these phase legs. The startup sequence remains the same as introduced before for these cases.

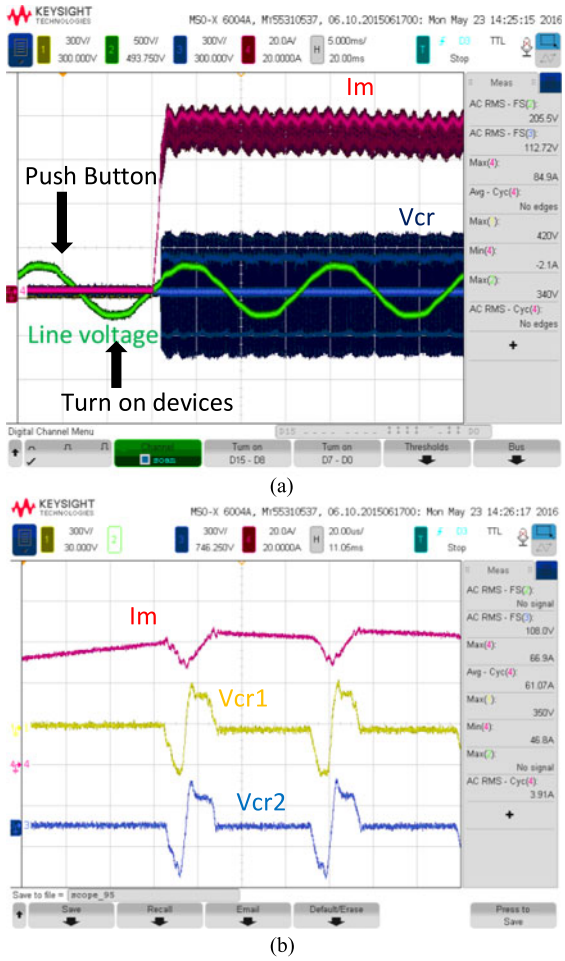


Fig. 16. Startup experimental waveforms of: (a) input line-to-line voltage (CH2, 500 V/div), magnetizing current (CH4, 20 A/div), and resonant capacitor voltage (CH3, 300 V/div) and (b) zoomed-in waveforms of the magnetizing current (CH4, 20 A/div) and two resonant capacitor voltages V_{cr1} (CH1, 300 V/div) and V_{cr2} (CH3, 300 V/div).

B. Shutdown

Converter shutdown is accomplished by turning on devices in the same leg. The magnetizing current then circulates within that leg and starts to decrease toward zero due to the voltage drop across the devices. The shutdown operation can be performed by any of the device legs of the input and output bridges. However, only one device leg of the input or output bridge can be turned on (or simultaneously turn on one device leg of both the input and output bridges). Otherwise, the bridge will formulate a current flowing path from the input/output terminal to the transformer if two or more legs are turned on simultaneously, which will either develop a huge transformer magnetizing current due to the low impedance of the transformer magnetizing inductance, or deliver a large dc current to the passive load. Fig. 17 shows that the converter is shut down by turning on devices S_{icp} and S_{icn}.

However, converter shutdown cannot be performed at an arbitrary instant. Turning on devices within the same leg when the resonant capacitors have a negative voltage will develop inrush current through devices. Therefore, the shutdown can only be

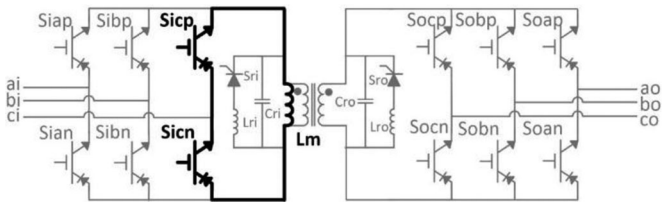


Fig. 17. Converter shutdown by turning on devices S_{icp} and S_{icn}.

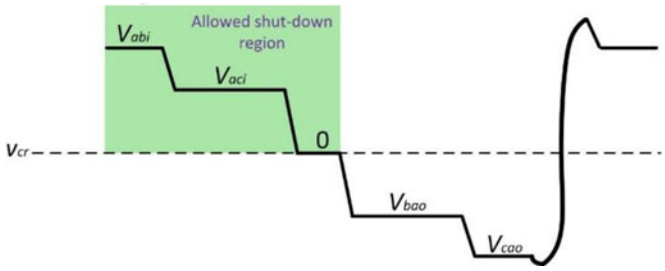


Fig. 18. Allowed shutdown region with respect to the resonant capacitor voltage.

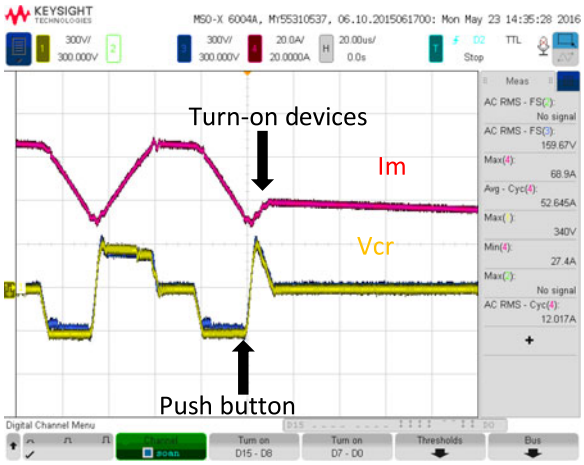


Fig. 19. Shutdown experimental waveforms of: magnetizing current (CH4, 20 A/div) and two resonant capacitor voltages V_{cr1} (CH1, 300 V/div) and V_{cr2} (CH3, 300 V/div).

activated when the capacitor voltage is positive. The allowed shutdown region with respect to the resonant capacitor voltage V_{Cr} is shown in Fig. 18. If V_{Cr} is positive, shutdown can be immediately started by turning on devices within the same leg. Since V_{Cr} is positive, the devices are reverse blocked, and no current flows through them. Magnetizing current I_m then discharges the capacitor, having V_{Cr} decreases. Once V_{Cr} drops to zero, devices conduct, and I_m circulates through the device leg and starts dropping toward zero. However, if a shutdown command is happened to be applied when V_{Cr} is negative, the converter will continue its normal operation until V_{Cr} becomes positive, and then it will start the shutdown sequence. It should be noted that during the shutdown procedure, devices are also operated under soft-switching conditions.

Fig. 19 shows the experimental results during the converter shutdown. The external push button to shut down the converter is triggered at an arbitrary instant. However, since the capacitor

TABLE II
PARAMETERS OF THE 10-KV·A S4T UNIT

Power rating	Input/output voltage/current	Switching frequency	Magnetizing inductance
10 kV·A	208 V/28 A	15 kHz	200 μH
Filter capacitor	Filter inductor	Resonant capacitor	Resonant inductor
60 μF	150 μH	0.4 μF	8 μH

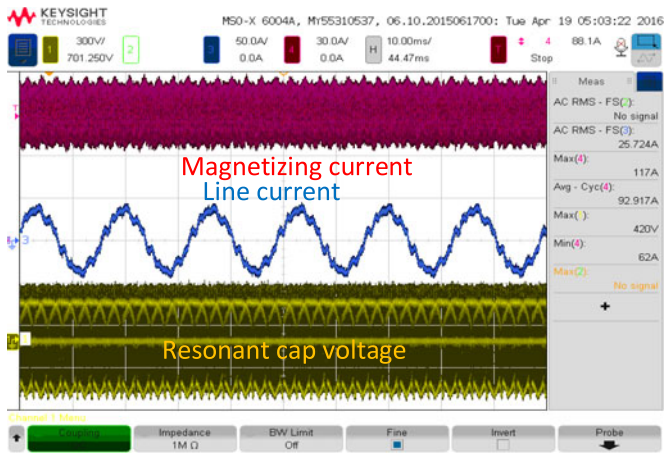


Fig. 20. Experimental waveforms of transformer magnetizing current (CH4, 30 A/div), line current (CH3, 50 A/div), and resonant capacitor voltage (CH1, 300 V/div).

voltage V_{Cr} is negative at this moment, the shutdown sequence is not initiated. The converter continues its normal operation until V_{Cr} becomes positive. Then, the devices are turned on, but they are reverse blocked. V_{Cr} quickly drops to zero due to the discharging effect of I_m. Devices are forward biased as soon as V_{Cr} drops to zero. Then, I_m circulates through these devices and starts decreasing toward zero.

VII. 10-KV·A S4T EXPERIMENTAL RESULTS

Based on the previous design optimization, the detailed parameters of the 10-kV·A S4T is listed in Table II. Description of the 10-kV·A S4T setup has been covered in the companion paper [29]. Two tests are carried out to demonstrate the 10-kV·A S4T unit operation. First, the input and output of the S4T are connected to the same power supply to circulate power. Then, it is tested with three-phase resistive loads connected on the output side. For the power circulating test, the S4T unit is operated at 208 V and injects a line current of 25.7 A, corresponding to a power level of 9.3 kV·A. The transformer magnetizing current reaches a steady-state level of 93 A, with a peak current of 117 A. Fig. 20 shows the experimental waveforms of the transformer magnetizing current, line current, and resonant capacitor voltage. The zoomed-in cycle-to-cycle waveforms for magnetizing current, resonant capacitor voltage, and resonant inductor current are shown in Fig. 21, which closely match the conceptualized waveforms. Fig. 22 shows the waveforms of one ZVS switching transient. It can be seen that before the device is turned on, the voltage across it already drops to zero, indicating

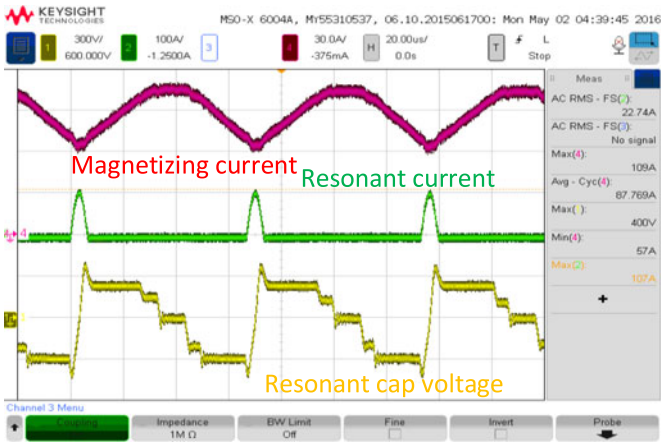


Fig. 21. Zoomed-in cycle-to-cycle waveforms for magnetizing current (CH4, 30 A/div), resonant capacitor voltage (CH1, 300 V/div), and resonant inductor current (CH2, 100 A/div).

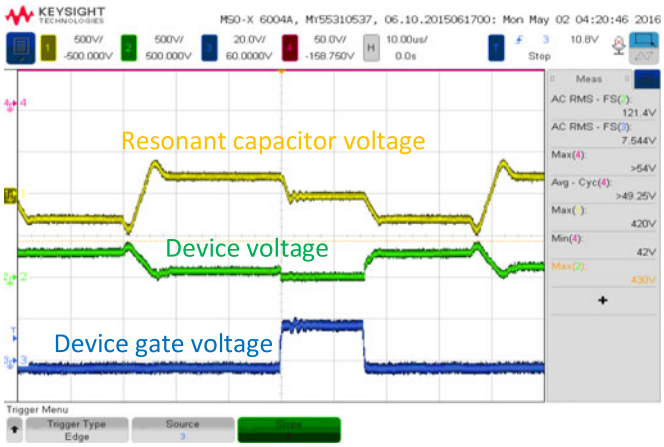


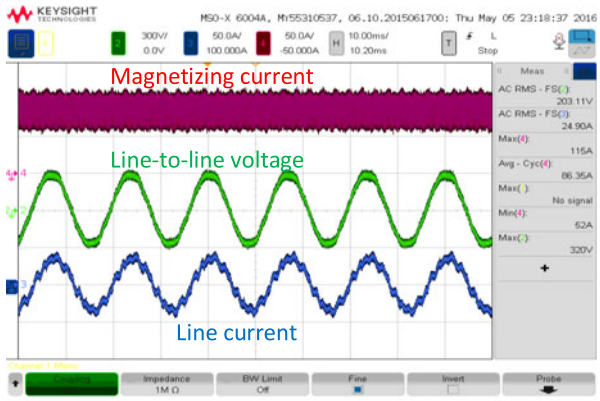
Fig. 22. One ZVS switching transient waveforms of resonant capacitor voltage (CH1, 500 V/div), device voltage (CH2, 500 V/div), and device gate voltage (CH3, 20 V/div).

zero turning-on loss. When the device is turned off, the voltage across it increases with a significantly reduced *dv/dt* rate, indicating a reduced turning-off loss. The S4T is tested with power flow in both directions. Fig. 23(a) and (b) shows the waveforms of the forward and reverse power flow, respectively.

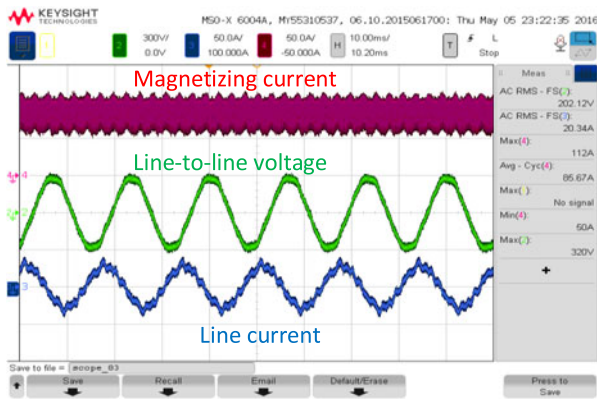
The S4T unit is then tested with a three-phase resistive load connected to the three-phase output on the secondary side. Three resistors are connected in delta and each one has a resistance of 22.6 Ω. Fig. 24 shows the experimental waveforms of the transformer magnetizing current and the current through the resistive loads. As shown in the figure, purely sinusoidal currents are injected to the load, in spite of the high-frequency ripples on the transformer magnetizing current.

The S4T is capable to inject leading/lagging reactive power on both the input/output sides. Also, it works well under unbalanced conditions as well as voltage swing and sag conditions without disturbing the loads. These results have been included in the companion paper [29].

The S4T exhibits fast dynamic response to load transients, mainly because of the light inertia of the system (relatively small magnetizing inductance and thus low intermediate energy stored



(a)



(b)

Fig. 23. Experimental waveforms of transformer magnetizing current (CH4, 50 A/div), line-to-line voltage (CH2, 300 V/div), and line current (CH3, 50 A/div) for two power flow directions: (a) forward power flow and (b) reverse power flow.

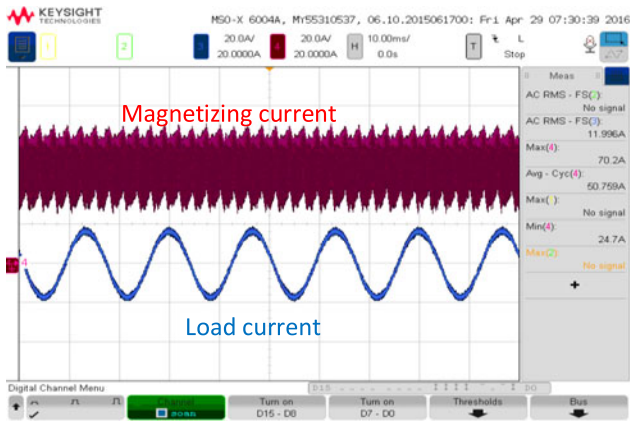


Fig. 24. Experimental waveforms of resistive loads test: transformer magnetizing current (CH4, 20 A/div) and current through the resistive load (CH3, 20 A/div).

in the transformer) along with proper control. Small magnetizing inductance indicates that the magnetizing current can be quickly built up and driven down through proper volt-sec control. Also, the controller for the S4T has a feedforward loop that ensures fast dynamic response to load changes, which has been discussed in detail in the companion paper [29]. The S4T performance under load transient is also tested. Both load step-up and step-down transient operations are demonstrated. Fig. 25 shows the

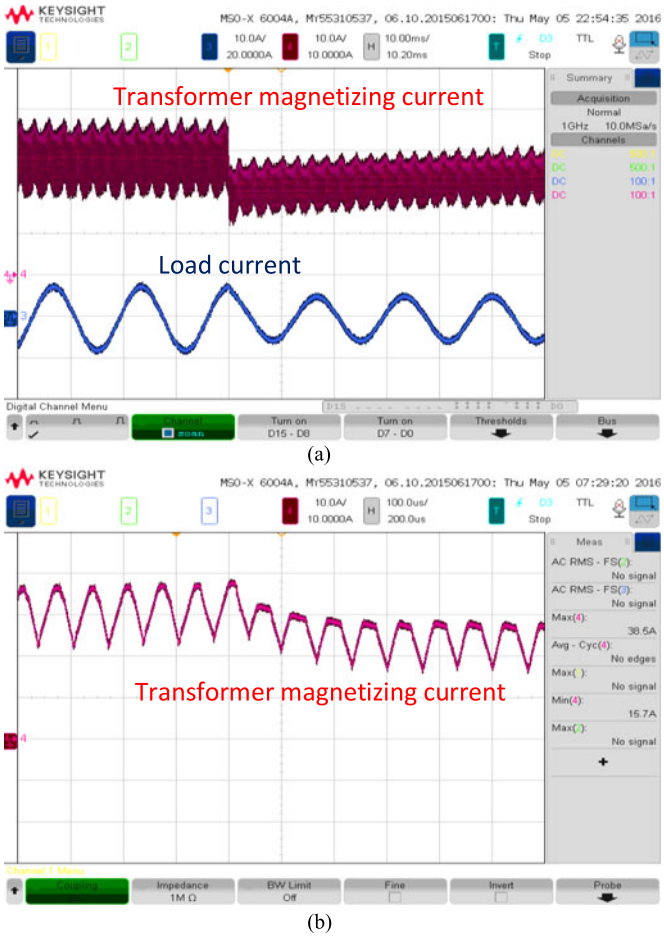


Fig. 25. Transient performance under load step-down change: (a) transformer magnetizing current (CH4, 10 A/div) and load current (CH3, 10 A/div) and (b) zoomed-in waveforms of the transformer magnetizing current (CH4, 10 A/div).

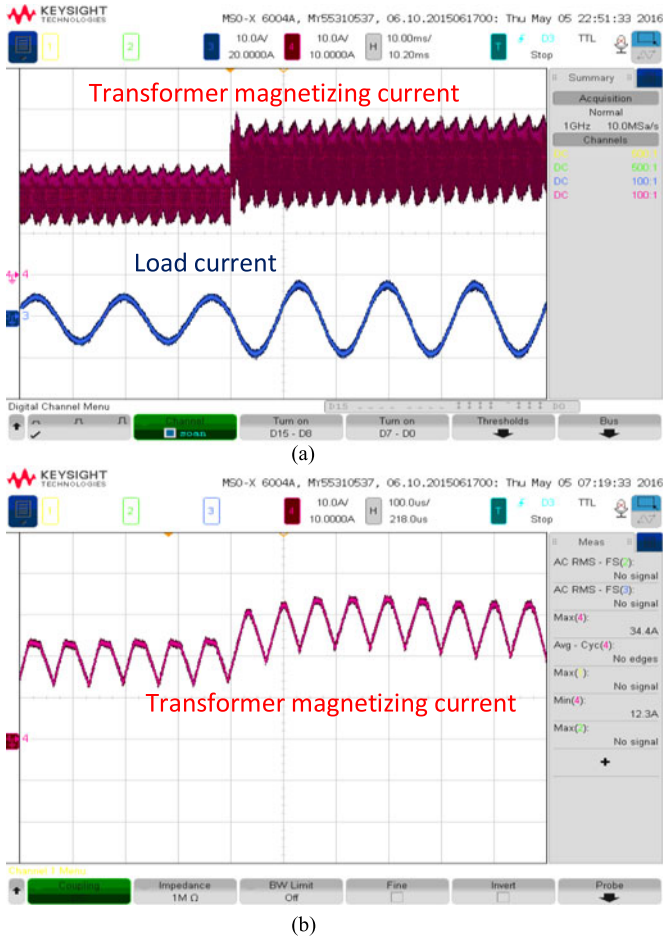


Fig. 26. Transient performance under load step-up change: (a) transformer magnetizing current (CH4, 10 A/div) and load current (CH3, 10 A/div) and (b) zoomed-in waveforms of the transformer magnetizing current (CH4, 10 A/div).

experimental results when the load current peak value decreases from 8 to 5 A. The transformer magnetizing current quickly changes from 30 to 20 A to accommodate the load step-down change. As shown in the zoomed-in waveforms of Fig. 25(b), the transformer magnetizing current is driven down to the new reference within three switching cycles, which shows a very fast dynamic response. This allows almost instantaneous response to the change of the fundamental frequency load. Being able to operate a 20 A dc current instead of 30 A under light-load conditions can reduce losses by over 33%. Fig. 26 shows the experimental results when the load current peak value increases from 5 to 8 A. The transformer magnetizing current quickly increases from 20 to 30 A to accommodate the load step-up change. As shown in the zoomed-in waveforms of Fig. 26(b), the transformer magnetizing current is built up to the new reference within three switching cycles.

Fig. 27 shows the loss measurement results at different dc currents and line voltages. Lower dc current corresponds to lower load. The transformer loss is estimated to be 74 W at full power and the remaining is mainly the conduction loss of the semiconductors. From this curve, the S4T unit shows an efficiency of ~89% for 40% load at 200 V. It can be seen

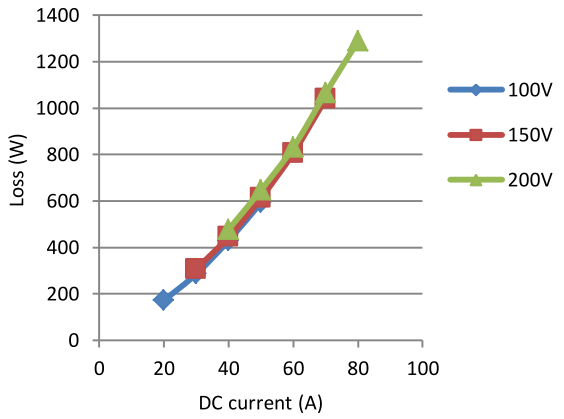


Fig. 27. Measured converter loss with different dc currents and line voltages.

from Fig. 27 that the converter loss increases with current as expected, but is almost independent of voltage levels. This clearly shows that ZVS condition is created for all devices and proves the soft-switching feature of the S4T. It is predicted that the converter can achieve significantly higher efficiency at higher voltage and higher power levels. Simulation results show

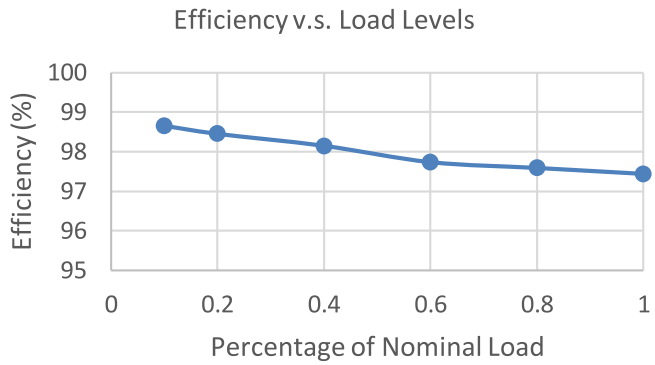


Fig. 28. Estimated efficiency curve of a 480 V/ 50 kV·A S4T across the entire load range.

that a 480 V/50 kV·A unit with the 1200 V/400 A IGBTs can have an efficiency higher than 97%. Fig. 28 shows the estimated efficiency curve of a 480 V/50 kV·A S4T when operating from 10% load to full load. Different from typical voltage-source converters, the efficiency of the S4T does not drop at light load. This is because that the S4T can dynamically change the dc current with respect to load levels. When the load drops to a low level, the dc current decreases accordingly, which ensures that the overall efficiency will not be impacted.

The S4T has lots of interesting features that improve the converter's reliability and robustness. Different from conventional voltage-source converters, the S4T does not have large dc capacitors, which typically have poor reliability and can generate inrush current at startup, shutdown, and fault transients. The S4T has inherent current limiting capability and it never causes short-circuit fault. This eliminates the use of desaturation for the gate drivers. Besides that, the S4T is also more robust than conventional current-source converters. Interrupting current flow path in a current-source converter leads to voltage spikes with high *dv/dt*. However, the resonant capacitor of the S4T significantly reduces the *dv/dt* rate when main devices are opened under fault. Protecting devices from overvoltage fault can be easily achieved by using Metal-oxide varistor (MOVs). All these ensure high reliability and robustness of the S4T. Comparison between the S4T and conventional DAB-based multistage SST has been given in the companion paper [29]. Scaling to medium voltage and high power can be achieved by stacking S4T modules, which has been discussed in [29] and [30].

VIII. Conclusion

This paper presented the detailed design of a three-phase S4T based on a patent-pending topology. The S4T realizes all the SST functionalities with minimal device and component count in the power flow path, and achieves a full range of soft switching for all the main devices. The reduced *di/dt* and *dv/dt* rates due to the soft switching address all the associated parasitic issues such as current and voltage spikes, resonance, noise, and EMI. Detailed design considerations for the converter power stage, auxiliary resonant circuit, and control are covered in this paper. The high-frequency transformer, transferring energy from input to output through the magnetic flux that is temporarily stored in the core, has a unique feature of dc-biased flux. A hybrid high-frequency transformer design methodology proposed in this paper enhances the core utilization by incorporating permanent magnets. The S4T can be started up and shut down through proper procedures without causing any inrush, and the device soft-switching feature is maintained through these procedures. The 10-kV·A S4T unit demonstrates the converter operation in steady state and under load transients. Both forward and reverse power flow operations are achieved. The S4T exhibits fast response under load transients. It can dynamically change the transformer magnetizing current according to load levels, without causing any disturbance to the load demand.

The S4T holds the promise of high efficiency with a simple circuit structure. It can find a wide range of applications such as dc energy storage interface, uninterrupted power supply systems, electrified transportation, space and weight critical applications, smart distribution systems, flexible ac transmission systems, and high-voltage direct current systems.

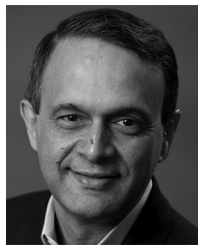
References

[1] W. McMurray, "Power converter circuits having a high frequency link," U.S. Patent 3 581 212, 1970.
[2] H. J. Cha and P. N. Enjeti, "A three-phase AC/AC high-frequency link matrix converter for VSCF applications," in *Proc. IEEE Power Electron. Spec. Conf.*, 2003, pp. 1971–1976.
[3] J. Kolar and G. Ortiz, "Solid-state transformers: Key components of future traction and smart grid systems," in *Proc. Int. Power Electron. Conf.*, 2014, pp. 1–15.
[4] K. Basu, A. Shahani, A. K. Sahoo, and N. Mohan, "A single-stage solid-state transformer for PWM AC drive with source-based commutation of leakage energy," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1734–1746, Mar. 2015.
[5] M. D. Manjrekar, R. Kieferndorf, and G. Venkataramanan, "Power electronic transformers for utility applications," in *Proc. IEEE Ind. Appl. Conf.*, 2000, pp. 2496–2502.
[6] R. Limpaecher and E. R. Limpaecher, "Charge transfer apparatus and method therefore," U.S. Patent 9 329 596, 2000.
[7] H. Keyhani, H. A. Toliyat, M. Harfman-Todorovic, R. Lai, and R. Datta, "An isolated resonant AC-Link three-phase AC-AC converter using a single HF transformer," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5174–5183, Oct. 2014.
[8] D. M. Divan, A. Prasai, and H. Chen, "Isolated dynamic current converters," U.S. Patent 9 065 321 B2, Aug. 8, 2013.
[9] H. Chen, A. Prasai, and D. Divan, "Dyna-C: A minimal topology for bidirectional solid state transformers," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 995–1005, Feb. 2017.
[10] H. Chen, A. Prasai, R. Moghe, K. Chintakrinda, and D. Divan, "A 50 kVA three-phase solid state transformer based on the minimal topology: Dyna-C," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8216–8137, Dec. 2016.
[11] T. Zhao, L. Yang, J. Wang, and A. Q. Huang, "270 kVA solid state transformer based on 10 kV SiC power devices," in *Proc. IEEE Elect. Ship Technol. Symp.*, 2007, pp. 145–149.
[12] S. Falcones, X. Mao, and R. Ayyanar, "Topology comparison for solid state transformer implementation," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, 2010, pp. 1–8.
[13] J. W. Kolar and J. Huber, "Solid-state transformer—Key design challenges, applicability, and future concepts," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2016.
[14] A. Prasai *et al.*, "Dyna-C: Experimental results for a 50 kVA 3-phase to 3-phase solid state transformer," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2014, pp. 2271–2277.
[15] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.

[16] X. She, X. Yu, F. Wang, and A. Q. Huang, "Design and demonstration of a 3.6-kV–120-V/10-kVA solid-state transformer for smart grid application," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 3982–3996, Aug. 2014.
[17] H. Chen and D. Divan, "High speed switching issues of high power rated silicon-carbide devices and the mitigation methods," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 2254–2260.
[18] H. Chen and D. Divan, "Soft-switching solid state transformer (S4T)," in *Proc. IEEE Energy Convers Congr. Expo.*, 2016, pp. 1–10.
[19] H. Chen and D. Divan, "Soft-switching solid state transformer (S4T)," U.S. Patent filed with USPTO, 2016.
[20] H. Chen, "Soft-switching solid state transformer (S4T)," Ph.D. dissertation, Elect. Comp. Eng., Georgia Inst. Technol., Atlanta, GA, USA, Dec. 2016.
[21] E. R. Motto, J. F. Donlon, M. Tabata, H. Takahashi, Y. Yu, and G. Majumdar, "Application characteristics of an experimental RB-IGBT (reverse-blocking IGBT) module," in *Proc. IEEE Ind. Appl. Conf.*, 2004, pp. 1540–1544.
[22] K. Wang, D. Boroyevich, and F. C. Lee, "Charge control of three-phase buck PWM rectifiers," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2000, pp. 824–831.
[23] *IGBT—Field Stop II*, On Semiconductor, Phoenix, AZ, USA, NGTB50N120FL2WG Datasheet, 2015.
[24] *Silicon Carbide Power MOSFET C2MTM MOSFET Technology*, Wolfspeed, Durham, NC, USA, C2M0025120D Datasheet, 2015.
[25] G. Shane, "Permanent magnet inductor design for reduced mass inductive components," Ph.D. dissertation, Dept. Elect. Eng., Purdue Univ., West Lafayette, IN, USA, 2012.
[26] P. Pieteris, "Permanent magnet DC inductor," Patent US20100194512 (A1), Aug. 5, 2010.
[27] T. Ishibashi and K. Terasono, "DC reactor and inverter device," Patent JP2007123596 (A), May 17, 2007.
[28] R. Tominaga, "D. C. reactor," Patent EP0744757 (B1), Jul. 12, 1995.
[29] H. Chen and D. Divan, "Soft-switching solid state transformer (S4T)," *IEEE Trans. Power Electron.*, early access, 2017.
[30] H. Chen, A. Prasai, and D. Divan, "Stacked modular isolated dynamic current source converters for medium voltage applications," in *Proc. IEEE Appl. Power Electron. Conf.*, 2014, pp. 2278–2285.
[31] *Permanent Magnet Design Guidelines*, Total Magnetic Solutions, Dubois, PA, USA. 2000. [Online]. Available: http://www.magnetsales.com/design/DesignG.htm

Hao Chen (S'13) received the B.S. degree from Nanjing University of Science and Technology, Nanjing, China, in 2008, the M.S. degree from Illinois Institute of Technology, Chicago, IL, USA, in 2010, and the Ph.D. degree from Georgia Institute of Technology, Atlanta, GA, USA, in 2016, all in electrical engineering.

From 2010 to 2012, he was an Electrical Engineer with Varentec, San Jose, CA, where he worked on various projects including solid-state transformers, dynamic VAr compensators, and voltage compensation for distribution system. He is currently a Senior Electronic Design Engineer at Tesla, Palo Alto, CA, USA.



Deepak Divan (S'78–M'78–SM'91–F'98) received the B.Tech. degree from the Indian Institute of Technology, Kanpur, India, in 1975, and the M.Sc. and Ph.D. degrees from the University of Calgary, Calgary, AB, Canada, in 1979 and 1983, respectively, all in electrical engineering.

He is currently the John E. Pippin Chair Professor and the Director of the Center for Distributed Energy, Georgia Institute of Technology, Atlanta, GA, USA. From 2011 to 2015, he was the President and CTO of Varentec, Santa Clara, CA, USA, a company focused on grid edge control that is funded by clean-tech venture capital firm Khosla Ventures and investor Bill Gates. He currently serves as the Chief Scientist and Founder of Varentec. He is also the Scientific Founder of two additional companies—Innovolt, based in Atlanta, which makes next-generation power protection and asset management devices and where he serves on the Board, and Soft Switching Technologies Corporation, where he served as the CEO and developed a range of devices to help manufacturing facilities ride-through power disturbances. He has also been a Professor in electric engineering at the University of Wisconsin–Madison, Madison, WI, USA. He has more than 250 papers and 50 issued and pending patents.

Dr. Divan is a member of the U.S. National Academy of Engineering. He is the first recipient of the IEEE William E. Newell Power Electronics Award, and the President of the IEEE Power Electronics Society.