Combined Multilevel and Two-Phase Interleaved *LLC* Converter With Enhanced Power Processing Characteristics and Natural Current Sharing

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***Abstract*—This paper introduces a new two-phase interleaved flying-capacitor *LLC* converter topology with high output current applications. Compared to a conventional two-phase *LLC* converter, the new converter adds a single capacitor that contributes to lower voltage stress on the primary side's switches, automatically balances the current distribution between the phases, and enhances the power processing capabilities. All the attractive features of *LLC* converters are preserved, such as zero-voltage switching on the primary side's MOSFETs, zero-current switching on the secondary side's power devices, narrow switching frequency range, and simple design. Full principle of operation and analysis of the converter are described, as well as the converter's primary characteristics and the impact of nonideal components on the current sharing behavior. A 600 W, 400 V-to-12 V experimental prototype is used as a showcase of the attractive features of the new converter, demonstrating excellent current sharing, simple implementation, and high efficiency of up to 97.3%.**

***Index Terms*—Current sharing, *LLC* converters, multilevel converters, resonant power conversion.**

I. Introduction

TODAY's power converters are required to deliver more power and achieve high efficiency over a wide load range. The *LLC* resonant converter topology is able to address such challenges and is advantageous in front-end dc–dc conversion applications as a result of the zero-voltage switching (ZVS) for the primary side's MOSFETs and zero-current switching (ZCS) for the secondary side's power devices [1]–[5]. In addition, it features narrow switching frequency range to facilitate regulation, fast transient response, and relatively low cost mainly due to incorporation of the transformer's leakage inductance as the resonant inductor. In particular, in its half-bridge implementation, the topology has been widely and successfully applied to flat panel TVs, 80+ ATX, and small form factor PCs, where the requirements on efficiency and power density of their switching mode power supplies are getting more and more stringent.

In high power applications where the current stress in a converter becomes high, paralleling of two (or more) converters, namely, multiphase operation, is a good solution for distribution of the current stress and it has been broadly investigated for both pulse width modulation (PWM) [6]–[10] and resonant converters [11]–[13]. It has been found that multiphase operation of *LLC* converters introduces implementation challenges that are typically related to the load current sharing between the converter's phases [11]–[24]. Current sharing is required to increase the power processing capability, maintain high efficiency, and improve the reliability since the thermal stress is better distributed. Therefore, current sharing is considered mandatory in multiphase *LLC* converters operation.

The main reason for an unbalanced load sharing between converter's phases lays in the difference between the components of the resonant networks. When interleaving phases, since the operation hinges on equivalent switching frequency of the different phases, mismatches in the resonant tank components impact the current distribution between the phases [13]. This is because only one phase operates at the frequency where the required voltage gain is achieved. Even small differences, within the resonant components values' tolerances, can have a severe effect on the current sharing and one phase will deliver most of the load current when other phases deliver a significantly smaller portion of it [19]. Several solutions have been proposed to achieve current sharing [12]–[24]. These solutions are used to match the resonant tanks components' values and can be classified as active or passive. In the active solutions, additional circuitry is added in order to control the resonant tank capacitance [13], [14] or inductance [15], to control the switching frequency [16], or to control the phase shift between the phases in case of three-phase structure [17]. However, these solutions suffer from complex control and implementation issues, high component count, and high cost. The passive solutions use a common capacitor [18] or common inductor [19], [20] for impedance matching of the phases [21]. Another passive solution that achieves good current sharing is based on series-input connected capacitors [22], [23].

To further improve the power processing capability of *LLC* resonant converters, multilevel operation has been investigated [25]. This approach provides lower voltage stress on the primary side's power devices and allows for the use of lower voltage rated MOSFETs with lower $R_{\mathrm{DS(on)}}$ per silicon area. The use of lower voltage rated MOSFETs reduces the conduction losses for a given area while maintaining very low switching losses due to ZVS. Another important feature of the multilevel operation is that the required dead-time and magnetizing inductance current to achieve ZVS can be decreased since lower energy is stored in the parasitic capacitances of the MOSFETs, which further improves the efficiency of the converter.

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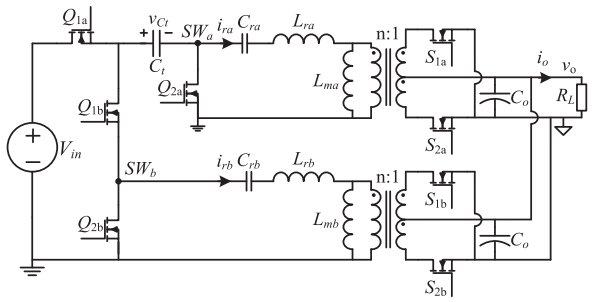

Fig. 1. Two-phase interleaved flying-capacitor *LLC* (TIFLLC) converter topology.

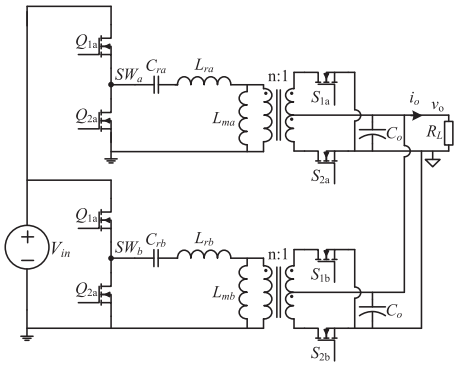

Fig. 2. Conventional two-phase *LLC* converter.

The objective of this study is to introduce a new two-phase interleaved flying-capacitor *LLC* (TIFLLC) resonant converter topology that combines multiphase and multilevel operations. The new topology, shown in Fig. 1, incorporates a flying-capacitor that lowers the voltage stress on the primary side's MOSFETs, balances the currents delivered by the two phases, and enhances the power processing characteristics. A significant advantage of the TIFLLC converter topology is that it preserves the benefits of conventional *LLC* converters such as soft-switching on all power devices, wide load range, narrow switching frequency range, as well as excels with high efficiency. These advantages make the topology an attractive candidate for high output current applications.

The rest of the paper is organized as follows: Section II presents the TIFLLC converter topology principle of operation and provides typical key waveforms of the new converter. Design considerations and details regarding the flying-capacitor are provided in Section III. Next, the current sharing and enhanced power processing characteristics are described and analyzed in Section IV. Implementation of the TIFLLC prototype and experimental results are provided in Section V. Section VI concludes the paper.

II. Principle of Operation

The TIFLLC converter, shown in Fig. 1, combines the benefits of a switched capacitor circuit and a series-resonant *LLC* converter. This topology adds a single capacitor C_t to the component count of a conventional two-phase *LLC* converter, depicted in Fig. 2. The converter's configuration and waveforms resemble the ones of the two-phase interleaved *LLC* converter, with the benefits of lower voltage stress transistors.

The operation of the TIFLLC converter is similar to the one of a conventional two-phase interleaved *LLC* converter with 180° phase delay, i.e., when the switching node (SW_a or SW_b) of one phase is high, then the switching node of the other phase is low. However, it should be noted that while in the conventional two-phase interleaved *LLC* converter, the phase delay between the phases can be arbitrarily selected (typically selected to be 90° to reduce the output voltage ripple), the 180° phase delay in the TIFLLC converter cannot be changed and therefore it does not contribute to output voltage ripple reduction. Therefore, two switching states are recognized as shown in Fig. 3 with the corresponding waveforms (obtained by a Powersim, Inc (PSIM) simulation) shown in Fig. 4: State I: phase *a* is ON and phase *b* is OFF; State II: phase *a* is OFF and phase *b* is ON.

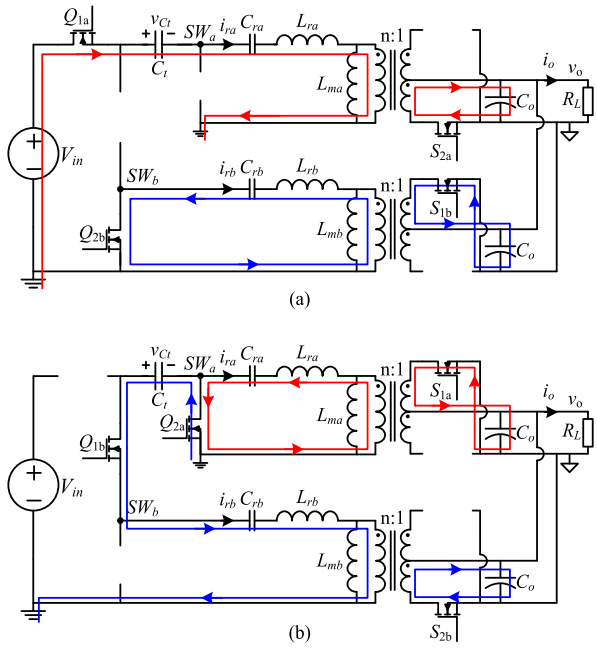

Fig. 3. Current paths in the TIFLLC converter: (a) State I: phase *a* is ON and phase *b* is OFF, and (b) State II: phase *a* is OFF and phase *b* is ON.

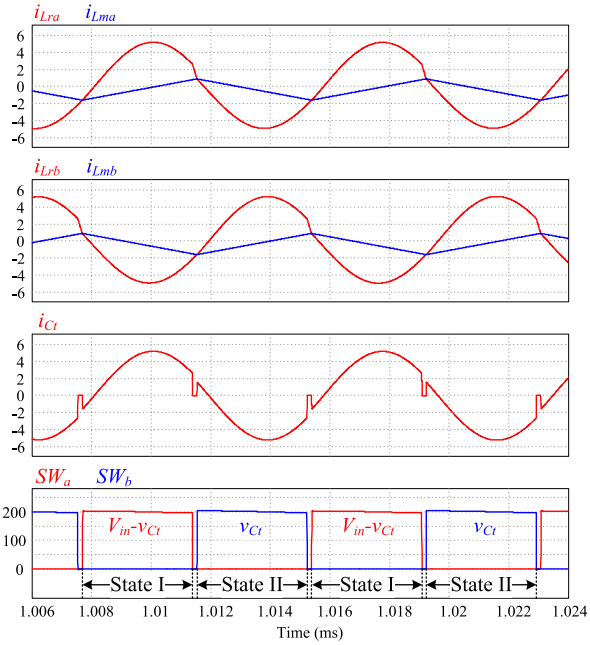

Fig. 4. Typical waveforms of the TIFLLC converter.

In state I, depicted in Fig. 3(a), switches Q_{1a} and Q_{2b} are ON, the input voltage connects to phase *a* through the flying-capacitor C_t and the applied voltage on its resonant tank is $V_{\rm in} - V_{Ct}$ while the resonant tank of phase *b* connects to ground via Q_{2b}. At the secondary side, switches S_{2a} and S_{1b} are ON for synchronous rectification operation. State II is shown in Fig. 3(b). Here, switches Q_{1b} and Q_{2a} are ON and the flying-capacitor acts as the source for phase *b*, imposing a voltage of V_{Ct} on its resonant tank while the resonant tank of phase *a* connects to ground; switches S_{1a} and S_{2b} are ON for synchronous rectification of the output current. As in conventional *LLC* resonant converters, dead-time between the two switching states is added to facilitate ZVS for the primary side's MOSFETs, and ZCS is obtained for the secondary side's power devices. It should be noted that C_t is designed to be significantly larger than the resonant capacitors and therefore it acts as a voltage source that has minor effect or none on the resonant behavior of the converter's phases. Further design details regarding the flying-capacitor are provided in Section III.

As can be observed from Figs. 3 and 4, the operation of the TIFLLC converter topology resembles a two-phase interleaved *LLC* converter with two input voltages for each phase that sum to $V_{\rm in}$. As will be detailed in the next section, these input voltages adapt their value based on the voltage gain per phase and as a result, high immunity is achieved to mismatches between the phases' resonant components. In addition, the use of a flying-capacitor naturally equalizes the current distribution the current between the phases, which in turn, enhances the power processing characteristics of the converter.

III. Analysis of Primary Characteristics for the TIFLLC Converter Topology

The flying-capacitor used in the TIFLLC converter introduces several interesting characteristics. The applied voltage on the switching nodes $\rm SW_a$ and $\rm SW_b$ is half of the input voltage which lowers the voltage stress on three out of the four primary side's MOSFETs by half. It also allows for lenient conditions to achieve ZVS on all the primary side's MOSFETs since the voltage swing on these transistors during the commutation period is only half the input voltage. Moreover, the applied voltage on the resonant tank is also lowered by half and allows a design of a resonant network with lower impedance, i.e., lower inductance for the same switching frequency. Another very important property that will be detailed in the next section is the charge-balance on the flying-capacitor that provides current distribution between the converter's phases.

The voltage of the flying-capacitor v_{Ct} is assumed constant V_{Ct} for a duration of a switching cycle due to its low voltage ripple. The flying-capacitor's voltage ripple Δv_{Ct} depends primarily on the load current and it is designed to be small, i.e., no more than 5% of the nominal value of V_{Ct} that typically equals $V_{\rm in}/2$. This selection of a sufficiently high flying-capacitor value also guarantees that the tanks' resonant frequency is not affected by this capacitor. The expression for Δv_{Ct} is calculated by the charge being transferred in each state, and can be expressed as

$$\Delta v_{Ct} = \frac{I_{\rm out}}{4nf_sC_t} \tag{1}$$

where $I_{\rm out}$ is the load current, f_s is the switching frequency, and *n* is the transformer's turns ratio.

The dc voltage of the flying-capacitor in the ideal case, i.e., the case of identical resonant components for both phases, equals $V_{\rm in}/2$. For any other case, there may be a drift of V_{Ct} which is a result of the gain difference between the phases. Under first harmonic approximation, the normalized voltage gains G_a and G_b (for phases *a* and *b*, respectively) are expressed as (obtained by the equivalent circuit shown in Fig. 5):

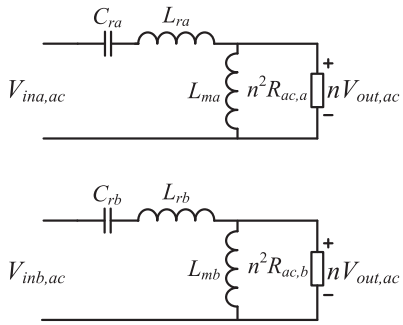

Fig. 5. Equivalent model of the TIFLLC converter using first harmonic approximation.

$$G_a(f_s) = \frac{nV_{\rm out,ac}}{V_{{\rm in}a,{\rm ac}}} = \frac{1}{\left(1+\frac{L_{ra}}{L_{ma}}-\frac{L_{ra}}{L_{ma}}\frac{1}{f_{na}^2}\right)+j\frac{\sqrt{L_{ra}/C_{ra}}}{n^2R_{{\rm ac},a}}\left(f_{na}-\frac{1}{f_{na}}\right)} \tag{2}$$

$$G_b(f_s) = \frac{nV_{\rm out,ac}}{V_{{\rm in}b,{\rm ac}}} = \frac{1}{\left(1+\frac{L_{rb}}{L_{mb}}-\frac{L_{rb}}{L_{mb}}\frac{1}{f_{nb}^2}\right)+j\frac{\sqrt{L_{rb}/C_{rb}}}{n^2R_{{\rm ac},b}}\left(f_{nb}-\frac{1}{f_{nb}}\right)} \tag{3}$$

where $V_{{\rm in}a,{\rm ac}}$ and $V_{{\rm in}b,{\rm ac}}$ are the ac input voltages of the phases *a* and *b*, respectively, given by

$$V_{{\rm in}a,{\rm ac}} = \frac{V_{\rm in}-V_{Ct}}{2}, \quad V_{{\rm in}b,{\rm ac}} = \frac{V_{Ct}}{2} \tag{4}$$

and f_{na}, f_{nb} are the normalized switching frequencies of phases *a* and *b*, defined as

$$f_{na} = \frac{f_s}{f_{ra}} = \frac{f_s}{1/2\pi\sqrt{L_{ra}C_{ra}}}, \quad f_{nb} = \frac{f_s}{f_{rb}} = \frac{f_s}{1/2\pi\sqrt{L_{rb}C_{rb}}}. \tag{5}$$

Using (2)–(4) and after some manipulations, the flying-capacitor voltage can be extracted and expressed as

$$V_{Ct}(f_s) = \frac{V_{\rm in}}{1+\frac{|G_b(f_s)|}{|G_a(f_s)|}}. \tag{6}$$

This implies that in case that the voltage gains of the phases are not equal, e.g., due to components' tolerances, the voltage deviates from the $V_{\rm in}/2$ value and also depends on the switching frequency. Fig. 6 shows the variance in flying-capacitor voltage as a result of components' difference between the phases as a function of the normalized switching frequency, where in each case a different component has been changed and the case study parameters are detailed in Table I. It can be observed that for higher output power, the voltage deviation from 200 V is smaller compared to lower output power. It can also be observed that the overall deviation, even for the lower power case, is relatively

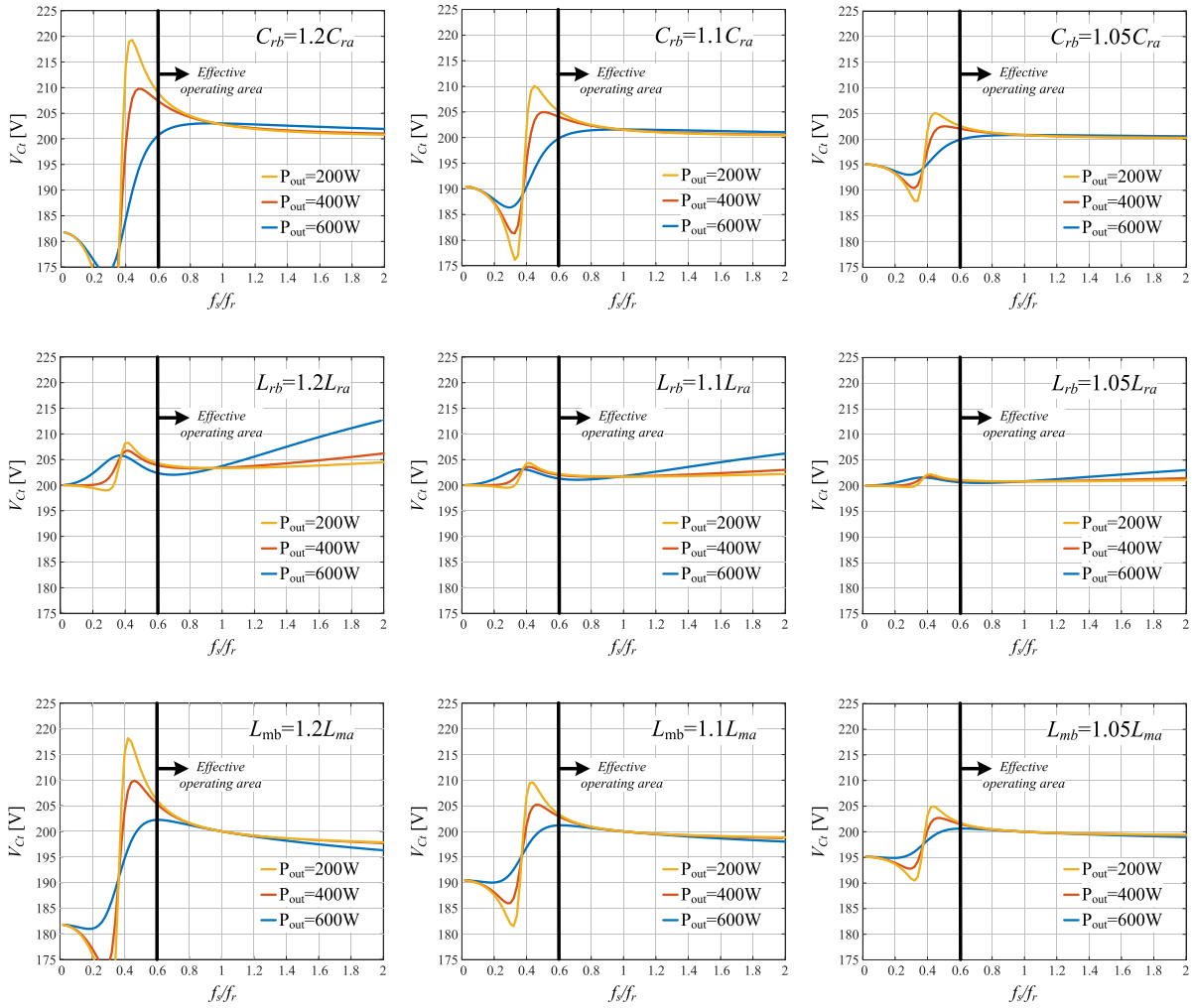

Fig. 6. Flying-capacitor voltage as a function of the switching frequency for phases with different resonant tank's parameters.

TABLE I
CASE STUDY PARAMETERS VALUES

Component	Value/Type
Input voltage V_{in}	400 V
Output voltage V_o	12 V
Transformers' turns ratio n	8
Phase a resonant frequency f_r	∼150 kHz
Phase a resonant capacitor C_{ra}	44 nF
Phase a resonant inductor L_{ra}	25 μH
Phase a magnetizing inductor L_{ma}	150 μH

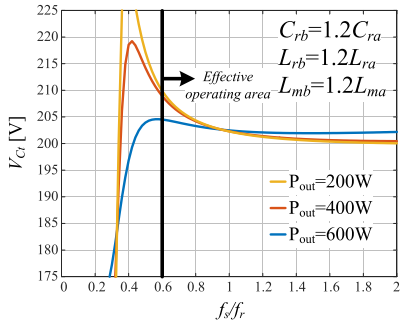

Fig. 7. Flying-capacitor voltage as a function of the switching frequency for worst-case resonant tank component's variation between the phases.

small for the switching frequency's area of interest (marked with arrow on Fig. 6) where ZVS on the primary-side's MOSFETs is achieved and the voltage gain is not highly dependent on the load, i.e., above $0.6f_r$. Lower frequencies than $0.6f_r$ may enter the capacitive region for some load conditions which may result in high switching losses and reduced efficiency. It should be noted that the value of $0.6f_r$ is only relevant for the presented case study and it is different for every converter's design. Fig. 7 presents the variance in the flying-capacitor voltage for the worst-case scenario where all the resonant tank's components of one phase have 20% variation compared to the other phase. As can be observed, even for such extreme conditions, the voltage deviation is small and therefore has minor effect on the converter's operation.

As in any capacitor based multilevel converter, there is an issue during start-up operation when the flying-capacitor is discharged of voltage stress on some of the MOSFETs. A possible solution to solve this problem and avoid any high inrush current to charge the flying-capacitor has been presented in [26], where an additional switch and a resistor have been connected in parallel with a low-voltage MOSFET to limit any inrush current during start-up. Since the required capacitance of the flying-capacitor in the TIFLLC converter is relatively small, its charging time can be much shorter than an overall start-up procedure that includes soft-start.

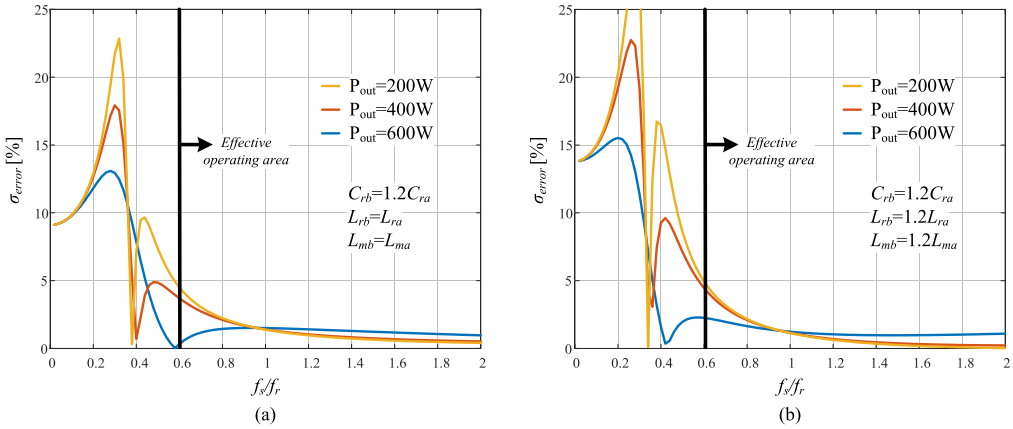

Fig. 8. Current error between the phases as a function of the switching frequency for: (a) $C_{rb} = 1.2C_{ra}$, (b) worst-case component's mismatch: $C_{rb} = 1.2C_{ra}$, $L_{rb} = 1.2L_{ra}$, and $L_{mb} = 1.2L_{ma}$.

IV. Current Sharing Under Parameter Variations

Current sharing of multiphase *LLC* converters has been widely investigated in [12]–[24]. In the TIFLLC converter topology, the charge-balance of the flying-capacitor assists in passive current sharing between the phases. Two MOSFETs conduct the current of the flying-capacitor: these are Q_{1a} during state I and Q_{1b} during state II, i.e.,

$$i_{Ct} = \begin{cases} i_{Q1a} & \text{@stateI} \\ -i_{Q1b} & \text{@stateII} \end{cases}. \tag{7}$$

Since charge-balance on this capacitor exists, the average current through it must be zero, and the average currents through these two MOSFETs in every switching cycle are equal, i.e.,

$$\langle i_{Q1a} \rangle = \langle i_{Q1b} \rangle . \tag{8}$$

Neglecting power loss in the system and assuming that the efficiency is high, the following holds:

$$\begin{aligned} P_{\text{in},a} &= P_{\text{out},a} \\ P_{\text{in},b} &= P_{\text{out},b} \end{aligned} \tag{9}$$

where P_{in} and P_{out} are the average input and output powers of each phase. The equality of (9) can be rewritten as

$$\begin{aligned} P_{\text{in},a} &= \langle v_{\text{in},a} \rangle \langle i_{\text{in},a} \rangle = \frac{V_{\text{in}} - V_{Ct}}{2} \langle i_{Q1a} \rangle \\ &= I_{\text{out},a}^2 R_{\text{ac},a} = V_{\text{out}} I_{\text{out},a} \\ P_{\text{in},b} &= \langle v_{\text{in},b} \rangle \langle i_{\text{in},b} \rangle = \frac{V_{Ct}}{2} \langle i_{Q1b} \rangle = I_{\text{out},b}^2 R_{\text{ac},b} = V_{\text{out}} I_{\text{out},b} \end{aligned} \tag{10}$$

where $I_{\text{out},a}$ and $I_{\text{out},b}$ are the average output currents of the phases. From (8) to (10), it can be derived that the ratio between the two phases' output currents equals the ratio between the input voltages of the two phases, i.e.,

$$\frac{I_{\text{out},a}}{I_{\text{out},b}} = \frac{V_{\text{in},a}}{V_{\text{in},b}} = \frac{V_{\text{in}} - V_{Ct}}{V_{Ct}}. \tag{11}$$

The expression in (11) provides an insight into the current sharing mechanism that is achieved with the usage of the flying-capacitor. The voltage V_{Ct}, as opposed to V_{in}, can dynamically change and as a result both $V_{\text{in},a}$ and $V_{\text{in},b}$ would vary accordingly. In the case that both the input and output voltages are common for the two phases, a mismatch of the resonant components results in voltage gains G_a and G_b that differ from the effective input-to-output ratio. The operation of the flying-capacitor automatically corrects the effective phase's input voltage (and as a result the input-to-output ratio) to comply with the variation in the voltage gain. It should be noted that this balancing action of the input voltages of the phases exceeds beyond the simplistic property of components variations for other parameters of the system such as the turn ratios of the phases' transformers.

Using the expression given in (6) and after some manipulations, the ratio between the phases' output currents can be expressed as

$$\frac{I_{\text{out},a}}{I_{\text{out},b}} = \frac{G_b}{G_a} \tag{12}$$

where G_a and G_b are given in (2) and (3). The current error between the two phases (the ratio between the difference and sum of the output currents, as defined in [19]), can be now expressed as

$$\sigma_{\text{error}} = \left| \frac{G_a - G_b}{G_a + G_b} \right|. \tag{13}$$

Fig. 8 shows the value of (13) as a function of the switching frequency and the output power for a case of a converter with parameters that are presented in Table I, and the variation in the resonant capacitor of phase b is by 20% compared to the resonant capacitor of phase a, and for the worst-case scenario where all the resonant tank' components have 20% variation. It can be observed that for a switching frequency higher than $0.6f_r$, the current error is less than 5% for both cases, which is an attractive attribute for passive current sharing even at such an extreme case of components' difference.

The very good current distribution in the TIFLLC converter topology also contributes to enhanced power processing characteristics. The 180° phase delay between the converter phases provides an interesting feature when Q_{2a} is ON. During the period of state II, Q_{2a} has two main purposes, one is applying a low potential path for the resonant current of phase a, i.e., zero voltage on the resonant tank. The second is connecting the negative port of the flying-capacitor to ground in order to apply V_{Ct} on the resonant tank of phase b. Therefore, Q_{2a} participates in the operation of both phases and during state II it passes resonant currents of the two phases simultaneously. Since at this state the resonant currents are in opposite direction (the current in phase a is negative whereas the current in phase b is positive), the net current flowing through Q_{2a} is zero, as shown in Fig. 9. The main contribution to the current rms value of Q_{2a} is its current during the dead-time, where the current magnitude equals to the resonant current magnitude, which is not zero. This translates into a more relaxed selection of this switch and

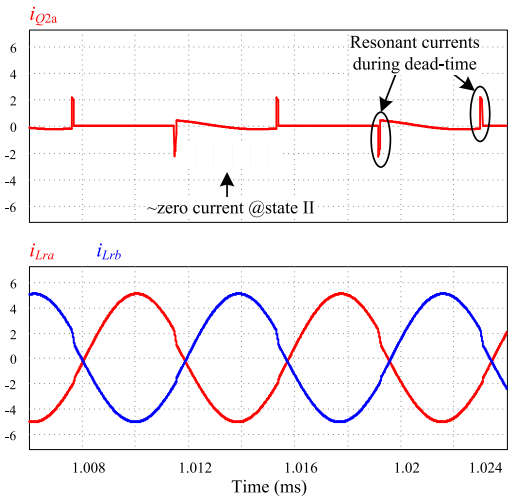

Fig. 9. Zero current characteristic of Q_{2a}.

TABLE II
EXPERIMENTAL PROTOTYPE'S PARAMETERS VALUES

Component	Value/Type
Input voltage $V_{\rm in}$	400 V
Output voltage V_o	12 V
Flying capacitor C_t	3 μF
Output capacitance $C_{\rm out}$	1 mF
Phase a transformer's turns ratio n_a	9
Phase b transformer's turns ratio n_b	9.3
Phase a resonant frequency f_{ra}	~138 kHz
Phase b resonant frequency f_{rb}	~130 kHz
Phase a resonant capacitor C_{ra}	66 nF $\pm$ 10%
Phase b resonant capacitor C_{rb}	66 nF $\pm$ 10%
Phase a resonant inductor L_{ra}	20 Mh
Phase b resonant inductor L_{rb}	23 μH
Phase a magnetizing inductance L_{ma}	150 μH
Phase a magnetizing inductance L_{mb}	155 μH
Primary-side gate drivers	UCC27714

implies that a higher ON-resistance MOSFET with lower capacitances is sufficient for the tasks required by Q_{2a}. This selection does not compromise on the efficiency of the converter, which in fact, improves and benefit from a lower required magnetizing inductance circulating current and gate driving requirements.

V. EXPERIMENTAL RESULTS

To validate the operation of the TIFLLC converter operation, a 600 W, 400 V-to-12 V prototype was built and tested. The transformers of both phases were hand made to create a difference between the resonant components of the phases and their measured leakage and magnetizing inductance are detailed in Table II. In addition, to further create a difference between the phases' parameters, the turn ratios of the transformers were designed to be not equal. The rest of components values and parameters of the TIFLLC experimental prototype are presented in Table II. The converter is digitally controlled using an Altera FPGA [27] using fully digital high-performance ADC and DPWM peripherals as detailed in [28] and [29].

The control scheme that was used in this study is described by the simplified block diagram of the TIFLLC controller, depicted in Fig. 10. A window-ADC samples the output voltage and compares it with a reference value $V_{\rm ref}$ to create an error signal $v_e[n]$ that is the input of a digital PID compensator. A PID compensation scheme is used to obtain high loop-gain

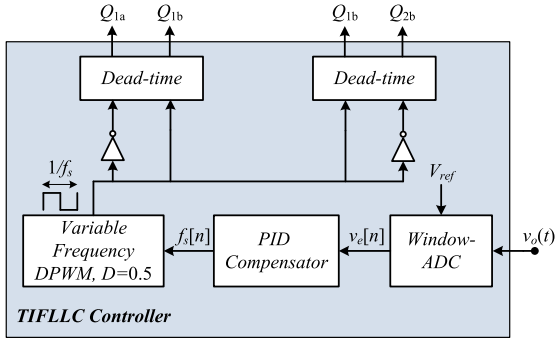

Fig. 10. Simplified block diagram of the TIFLLC controller.

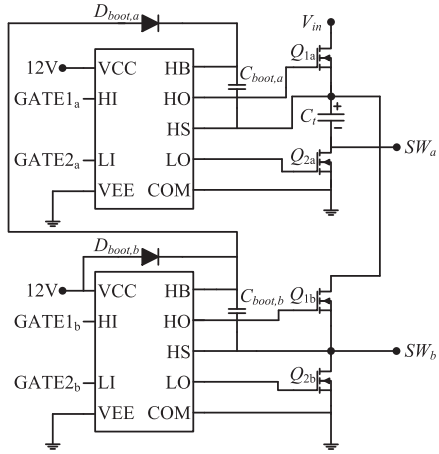

Fig. 11. Gates drivers' realization in the TIFLLC converter.

bandwidth and its output is the frequency of the DPWM $f_s[n]$. The output of the DPWM is a square wave with frequency f_s and 0.5 duty-ratio. The square wave is then inverted to create two square waves with 180° phase delay. At last, two dead-time units are used to create sufficient dead-time between the high and low side gate signals of each phase in order to obtain ZVS on the primary-side's MOSFETs.

A. Implementation of the Primary-Side's MOSFETs Gate Drivers

Although the two phases of the TIFLLC converter are not conventional half-bridges, its gate drive circuitry is similar to the gate drive circuitry of a two conventional half-bridges transistors assemblies, except for a slight modification in the charging path of the boot capacitor of phase a. A simple bootstrap driver cannot be employed for this case since its source ($\rm SW_a$) does not meet ground at any time and its bootstrap capacitor would not charge by a drive voltage referenced to ground. To overcome this obstacle, instead of connecting the bootstrap diode of phase a's driver ($D_{{\rm boot},a}$) to a ground referenced drive voltage, it connects the bootstrap capacitor of phase b's driver $C_{{\rm boot},b}$, as shown in Fig. 11. This way when Q_{1b} is ON, $C_{{\rm boot},a}$ is charged by $C_{{\rm boot},b}$ through $D_{{\rm boot},a}$ in a similar operation to the one of diode-capacitor charge pump. The other MOSFETs driving is simple: Q_{1b} and Q_{2b} are standard high-side and low-side MOSFETs driven by a dual bootstrap driver configuration and Q_{2a} is driven by the low-side driver of the dual bootstrap driver that also drives Q_{1a}. The component count of the driving configuration remains the same as the component count of a conventional two-phase *LLC* converter.

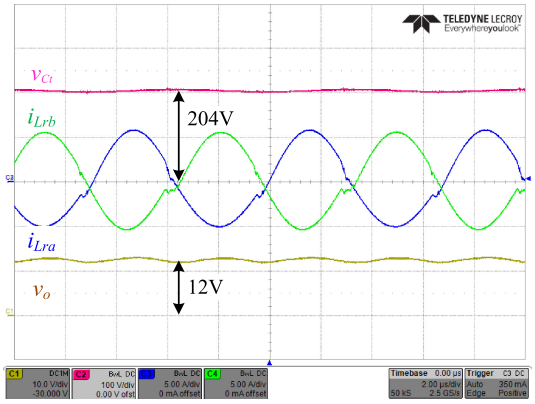

Fig. 12. Experimental waveforms of the TIFLLC converter. C1—output voltage v_o (5 V/div), C2—flying-capacitor voltage v_{Ct} (100 V/div), C3—phase *a* primary-side resonant tank current i_{Lra} (5 A/div), and C4—phase *b* primary-side resonant tank current i_{Lrb} (5 A/div). Time scale is 2 μs/div.

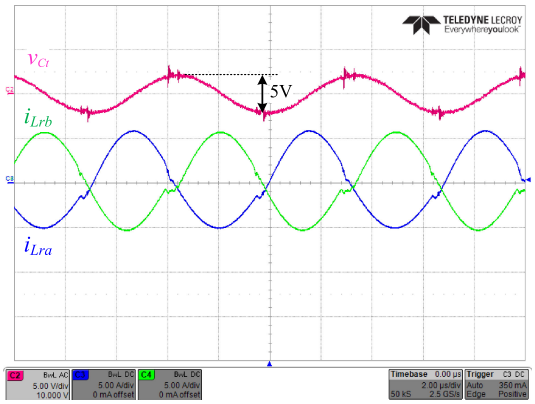

Fig. 13. Experimental waveforms of the TIFLLC converter. C2—flying-capacitor voltage v_{Ct} (5 V/div, ac coupled), C3—phase *a* primary-side resonant tank current i_{Lra} (5 A/div), and C4—phase *b* primary-side resonant tank current i_{Lrb} (5 A/div). Time scale is 2 μs/div.

B. Experimental Results

Figs. 12–14 show the converter's waveforms for output current of 50 A (full load). Fig. 12 shows the flying-capacitor voltage, output voltage, and the primary-side's currents of the two phases. As can be observed, in spite of the difference between the parameters of the phases, the phases' currents are almost equal with a very small difference between them, with a measured current error of 0.4%. In addition, the flying-capacitor voltage is 204 V which is very close to $V_{\text{in}}/2$, as expected by the theoretical analysis from Section III. It should be noted that the output voltage ripple is measured at around 1 V, which is the worst-case voltage ripple due to operation in full load and a result of relatively small output capacitance used in the experimental prototype. Depicted in Fig. 13 is the voltage ripple of the flying-capacitor Δv_{Ct} with a magnitude of around 5 V, which is approximately 2.5% of V_{Ct}. Fig. 14 depicts the switching nodes SW_a and SW_b. As can be observed, ZVS of the primary-side's MOSFETs is obtained and the voltage of the switching nodes is around 200 V (half of V_{in}) when they are high. Fig. 15 presents the measured current error for the full load range of the converter when the resonant capacitors have equal values (as in Table II) and when one of the resonant capacitors (C_{ra}) has been replaced with significantly small capacitor (55 nF instead of 66 nF) which represents a 20% difference between the phases' capacitors. The

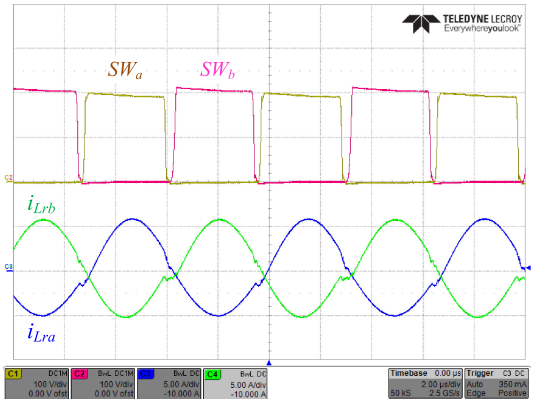

Fig. 14. Experimental waveforms of the TIFLLC converter. C1—switching node voltage of phase *a* SW_a (100 V/div), C2—switching node voltage of phase *b* SW_b (100 V/div), C3—phase *a* primary-side resonant tank current i_{Lra} (5 A/div), and C4—phase *b* primary-side resonant tank current i_{Lrb} (5 A/div). Time scale is 2 μs/div.

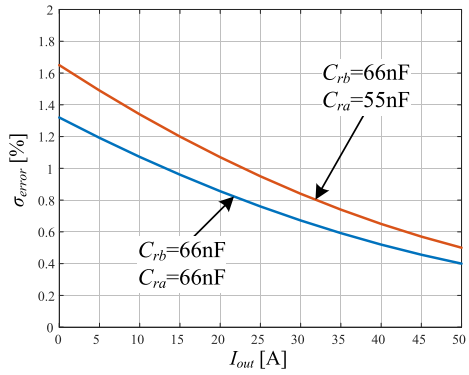

Fig. 15. Measured current error between the phases of the experimental prototype.

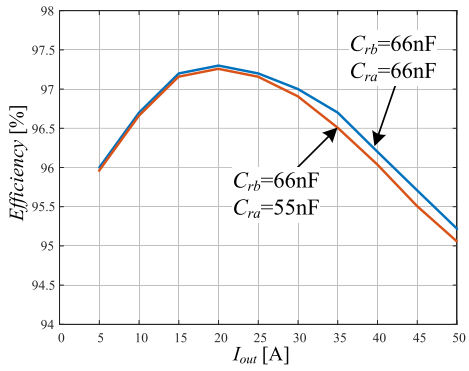

Fig. 16. Efficiency measurements of the experimental prototype.

results are in very good agreement with the analysis from Section IV, verifying the natural current sharing between the phases and the small current error even at large components mismatch. Efficiency measurements of the converter for the two setups are provided in Fig. 16, demonstrating a peak efficiency of 97.3% and above 96% for most of the load range. It can also be observed that the variation of the resonant capacitor has negligibly small effect on efficiency, and its effect is only noticeable at high output currents which is reasonable due to the fact that the conduction losses are dominant and the current sharing error is slightly higher, resulting in one phase that is less efficient than the other.

VI. Conclusion

A new two-phase interleaved flying capacitor *LLC* converter topology has been presented in this study. The topology comprises two-phases for high current delivery and uses a flying-capacitor to lower the voltage stress on the switches, naturally balance the current distribution between the phases, and enhance the power processing capabilities. The converter preserves all the benefits of conventional *LLC* converters while maintaining low sensitivity to resonant tank parameters mismatches and conventional driving circuitry with no extra components. Full principle of operation has been described, as well as the converter's primary characteristics and the impact of nonideal components on the current-sharing behavior. The experimental results of the new converter are in excellent agreement with the theoretical analysis, showing promising power processing characteristics and making the converter an attractive candidate as a front-end converter for high output current applications.

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