Buck–Boost Dual-Leg-Integrated Step-Up Inverter With Low THD and Single Variable Control for Single-Phase High-Frequency AC Microgrids

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***Abstract*—To support the development of high-frequency ac microgrids in terms of compact design, high-voltage gain and low total harmonic distortion (THD), a buck–boost dual-leg-integrated step-up inverter is proposed in this paper. The inverter is formed by integrating a buck–boost converter into a conventional single-phase full-bridge inverter by sharing the upper switch and the body diode of the lower switch in both bridge-legs. Consequently, the component count is significantly reduced over the step-up inverter counterparts. In addition, to address the drawbacks of hybrid modulation methods adopted by existing dual-leg-integrated inverters, such as double-variable control, and high THD of output voltage/current at high input voltage and heavy load conditions, unipolar frequency doubling sinusoidal pulse width modulation scheme is adopted in this inverter. As a result, the modulation ratio *M* becomes the only control variable to regulate the output voltage/current and the control is simplified. The THD of the proposed inverter output can remain low throughout the entire input voltage range and load power range. This paper presents the topology derivation procedure, operation principle, and steady-state characteristics of the proposed inverter. To validate the effectiveness of theory, experimental results of a 400 W hardware prototype, where the output voltage frequency is at 500 Hz, are reported.**

***Index Terms*—High frequency, inverters, microgrid, step-up, unipolar frequency doubling sinusoidal pulse width modulation (SPWM).**

I. Introduction

MICROGRIDS operating in a higher than utility frequency (i.e., 500 Hz–1 kHz) have several advantages. These include improved power quality due to easier filtering of high-order harmonics by using smaller power transformers, filter capacitors and inductors, higher power density and reliability, lower cost and simpler transformation structure, more compatible with operating high-frequency electric machines, higher operation efficiency of induction motors and fluorescent lights, and a better platform for using flywheels as an alternative dynamic storage unit [1]–[3]. Hence, recently high-frequency ac (HFAC) microgrids have attracted an increasing interest [4], [5].

One critical component of HFAC microgrids is the dc/ac inverters, which interface with dc-based renewable sources, energy storage elements and loads, and convert the dc power to HFAC [6]. To realize the potential and merits of higher line frequency operation, the inverters are expected to have fewer components, simpler structure, and higher reliability. Furthermore, for situations where the output voltage of PV panels varies widely with environmental conditions and temperature, or the output voltage of small wind turbines under low wind speed usually are very low, the inverters connected to these sources should provide a voltage boost function.

A commonly used topology for the single-phase HFAC system is a resonant inverter, which includes a high-frequency full-bridge structure for dc to HFAC conversion, and followed by a resonant tank for producing a near sinusoidal voltage/current to feed the distribution bus [7]. The resonant inverter offers high conversion efficiency at high frequency (usually higher than 20 kHz) and produces an output voltage/current with low total harmonic distortion (THD). However, an important feature of the resonant inverter is that its switching frequency should equal the ac frequency. Therefore, when it is used in HFAC microgrids, where the bus frequency is 1 kHz for instance, the size of resonant element does not reduce much as compared with its high-frequency pulse width modulation (PWM) counterpart. Another challenge of this topology is that it requires an input voltage much higher than the amplitude of ac voltage to operate because of its voltage step-down property. The topology hence is not suitable for the aforementioned low and varying input voltage sources. A simple solution to stepping up the inverter output voltage is to add a step-up line frequency transformer [8]. This solution can result in high power supply volume, weight, and cost and reduced power density. Another option is to adopt a two-stage structure, where the front-end circuit is a step-up converter (e.g., boost, buck–boost, etc.) and the rear-end circuit is

Manuscript received January 10, 2017; revised April 10, 2017 and June 12, 2017; accepted August 6, 2017. Date of publication August 20, 2017; date of current version March 5, 2018. This work was supported in part by the National Natural Science Foundation of China under Grants 51607098 and 51577164, in part by the Science Project of State Grid Corporation under Grant SGJSSZ00FZWT1601138, and in part by Applied Basic Research Project of Nantong under Grant GY12015007. Recommended for publication by Associate Editor F. Gao. *(Corresponding author: Ling Qin.)*

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Digital Object Identifier 10.1109/TPEL.2017.2742667

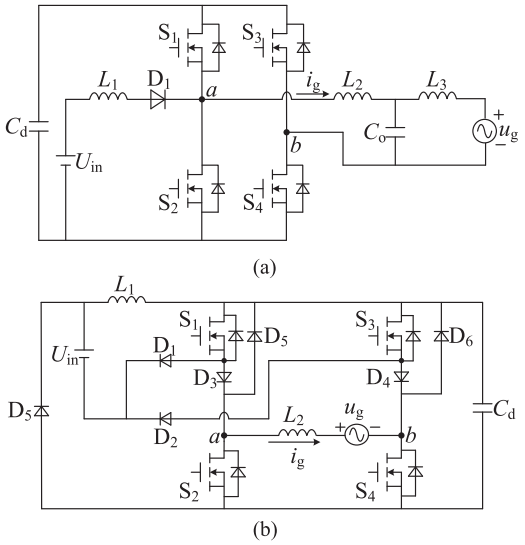

Fig. 1. Integrated inverter. (a) Single-leg-integrated inverter reported in [24]. (b) Dual-leg-integrated inverter reported in [27].

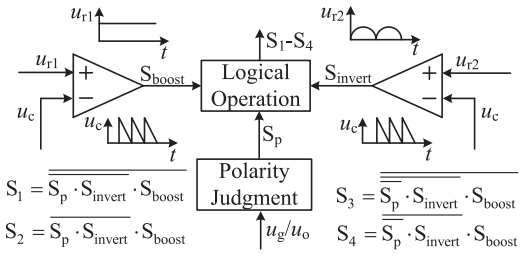

Fig. 2. Hybrid modulation method of the dual-leg-integrated inverter.

the conventional full-bridge inverter [9]. These two-stage step-up inverters can operate with a wide range of input voltages. For instance, in the PV generating application, the front dc/dc converter performs a maximum power point tracking (MPPT) control, and the latter *H*-bridge performs a grid-feeding control. Hence, the complexity of control algorithms can be reduced as they can be implemented separately [10]. Furthermore, if the isolated dc/dc converter is used as the first-stage circuit, the leakage current commonly existed in the conventional nonisolated PV inverter can be suppressed fundamentally. However, the abovementioned merits are obtained at the expense of the loss of integration, and smaller power density. On the other hand, the efficiency of two-stage system is limited by the product of efficiencies of the individual stages [11], [12]. In [13], Hu *et al*. proposed an HFAC single-stage inverter integrated with a coupled inductor bridge-leg to achieve high-voltage gain, soft switching, and electric isolation. However, its THD is very high due to the square output voltage waveform, which will seriously deteriorate the power quality of HFAC microgrids [1].

In the HFAC microgrid, since the ac bus can be generally isolated from the utility grid by a transformer-isolated ac/ac bidirectional interface converter, the common leakage current problem in the inverter due to interfacing with PV panels can be avoided. Hence, nonisolated single-stage step-up inverters may be a better alternative for HFAC microgrids owing to their highly integrated power-stage design, high-voltage gain, and low THD. The reported single-stage step-up inverters can be generally categorized into five types: current-fed inverter [14], [15], Z-source inverter [16]–[18], combined inverter [19]–[22], active buck–boost inverter [23], and integrated inverter [24]–[27]. Compared with the first four types, the integrated inverters significantly reduce the amount of components by sharing of the power switches, and consequently they have simpler structure, higher reliability, and are more suitable for HFAC microgrids.

The integrated inverters can be classified into single-leg-integrated [24] and dual-leg-integrated [25]–[27] inverters, as shown in Fig. 1. Compared with the single-leg-integrated inverters, the dual-leg-integrated inverters have higher voltage gain and lower voltage stress and therefore they are the focus of this paper. From the perspective of superposition principle, the dual-leg-integrated inverter operation has two processes: voltage boosting and inversion. Although the existing dual-integrated inverters adopt different control strategies, including proportional integration (PI) control, one-cycle control, and hysteresis control, the modulation methods used are similar, as shown in Fig. 2. Under this modulation, the boosting control signal $S_{\rm boost}$ and the inversion control signal $S_{\rm invert}$ are superimposed by the logical operation to obtain all the driving signals. During half ac line period of the output voltage, one bridge-leg operates in PWM mode to boost the input voltage, while the other one works in sinusoidal pulse width modulation (SPWM) mode to regulate the waveform of output current (grid-connected system) or output voltage (standalone system). During the next half ac line period, the two legs exchange their operation modes. Since this modulation method combines PWM and SPWM together, it is called hybrid modulation in this paper. Hybrid modulation is helpful to significantly reduce the double-frequency current ripple through the boosting inductor and easily increase the voltage gain. However, it needs two control variables (duty cycle D of $S_{\rm boost}$ and modulation ratio M of $S_{\rm invert}$) and output voltage polarity signal $S_{\rm p}$, the control circuit and algorithm are relatively complex in comparison to the traditional unipolar SPWM scheme and unipolar-frequency-doubling (UFD) SPWM scheme. Another critical issue is that D may be less than M at high input voltage and heavy load. This is so-called overmodulation. At this time, during some switching periods, the upper switch of the SPWM leg will lose its duty cycle, which will increase THD significantly.

Besides, the existing integrated inverters are mostly deduced from the boost converter. There are only a few articles on the buck–boost-integrated inverter. In [27], Hugo *et al*. have successfully integrated a buck–boost converter into a full-bridge inverter by sharing of the upper switches of the H-bridge inverter, but this new topology uses more diodes than its boost-integrated inverter counterpart. This paper proposes an improved buck–boost-integrated inverter, which further shares the lower switches as the freewheeling diodes of buck–boost converters and thereby reducing the amount of diodes from five to two. In addition, this paper adopts the traditional UFD-SPWM to achieve boosting and inversion control. Under this modulation, M becomes the only control variable to regulate the output voltage/current and the output voltage polarity no longer needs be measured. Moreover, voltage gain of the proposed inverter under UFD-SPWM increases with M. Hence, as long as the

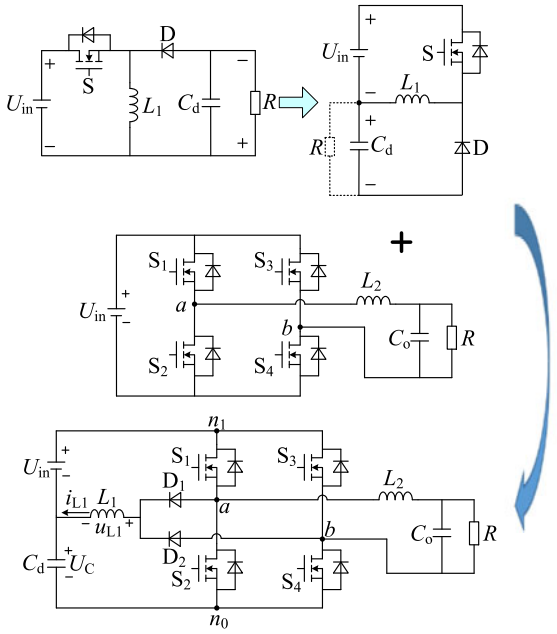

Fig. 3. Proposed step-up inverter and its derivation steps.

input voltage meets the requirement of voltage gain, M will be less than 1 and overmodulation will not occur. As a result, THD can remain low for the entire allowable input voltage range and load power range.

The paper is organized as follows: In Section II, the topology and its derivation process are introduced. Its operation principles in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are analyzed in detail, respectively. It is then followed by analyses of the voltage gain and the input inductance in Section III. Finally, in Section IV, the effectiveness of the proposed improved inverter is verified by a 400 W prototype, where the switching frequency is at 50 kHz and the output voltage frequency is at 500 Hz.

II. Novel Buck–Boost-Integrated Step-Up Inverter

A. Proposed Inverter and its Derivation Procedure

The proposed single-phase buck–boost-integrated step-up inverter and its derivation steps are shown in Fig. 3. As can be seen, it is derived from the buck–boost converter and the conventional full-bridge inverter by sharing the switches, where S_1 and S_3 correspond to the switch S in the buck–boost converter, while S_2 and S_4 work as the diode D. The function of boost inductor L_1 is similar to that in the buck–boost converter. Diodes D_1 and D_2 can prevent the energy stored in the capacitor C_d from discharging by L_1 and the switches S_2 and S_4. Compared with the traditional two-stage step-up inverters, the proposed inverter reduces switch count, voltage stress across the capacitor C_d and the number of power conversion stages, and hence it has a simpler structure, lower cost, and higher efficiency.

B. Operation Principle

In this paper, the proposed inverter is modulated by the conventional UFD-SPWM method. Table I shows the switching

TABLE I
Switching Sequences of the Proposed Inverter

Switching sequences	Positive half-cycle	Negative half-cycle
1	S_1S_4 on, S_2S_3 off	S_2S_3 on, S_1S_4 off
2	S_1S_3 on, S_2S_4 off	S_1S_3 on, S_2S_4 off
3	S_1S_4 on, S_2S_3 off	S_2S_3 on, S_1S_4 off
4	S_2S_4 on, S_1S_3 off	S_2S_4 on, S_1S_3 off

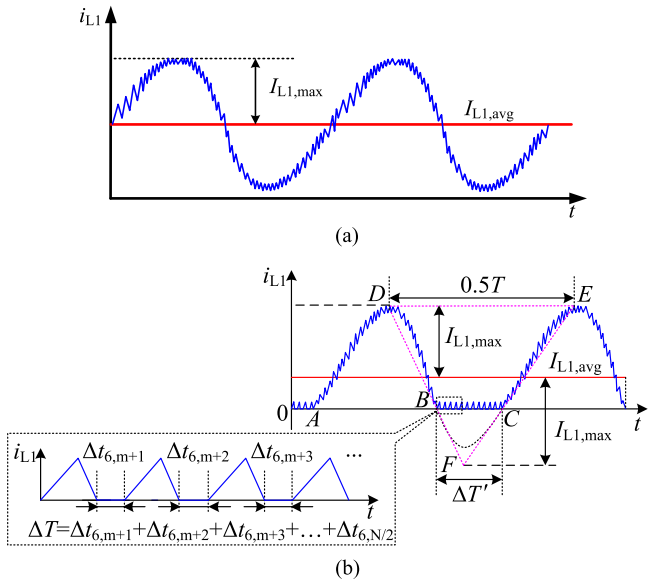

Fig. 4. Sketch of $i_{L1}(t)$. (a) CCM. (b) DCM.

sequences during one switching period. According to the switching sequences, the operation principle of the circuit can be analyzed. Since the operating processes during the positive- and negative half-period of the sinusoidal modulation wave are similar, here only the positive half-period is described.

In addition, due to the instantaneous power pulsation with twice the line frequency, the boosting inductor current $i_{L1}(t)$ will contain a second-order ripple, as shown in Fig. 4. $I_{L1,avg}$ (the average of $i_{L1}(t)$) rises with the increase of load power. So, $I_{L1,avg}$ will be higher than $I_{L1,max}$ (the amplitude of second-order ripple) under heavy load, as shown in Fig. 4(a). Instead, $I_{L1,avg}$ may be lower than $I_{L1,max}$ under light load, as shown in Fig. 4(b). Obviously, $i_{L1}(t)$ is always continuous in Fig. 4(a), but becomes discontinuous in BC section in Fig. 4(b). Therefore, the former operation mode is named as CCM, while the latter is DCM. The operation principles in these two modes are different and need to be analyzed separately.

For convenience of analysis, it is assumed that the inverter is operating in steady state and the following assumptions are made during one switching cycle:

1) the inductors and capacitors are all ideal elements;
2) the turn-on and turn-off of switches are fulfilled instantly, so the shoot-through will not happen and the dead time of drive signals can be zero;
3) the capacitor C_d is sufficiently large that it can be equivalent to a constant voltage source U_C;

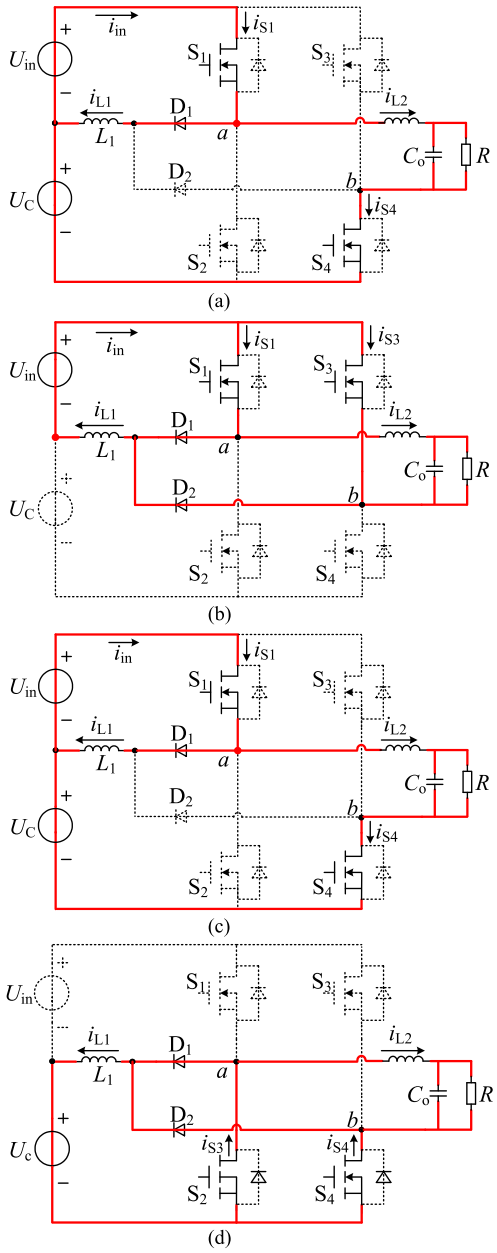

Fig. 5. Equivalent modal diagrams of CCM. (a) Stage 1: $[t_0 - t_1]$. (b) Stage 2: $[t_1 - t_2]$. (c) Stage 3: $[t_2 - t_3]$. (d) Stage 4: $[t_3 - t_4]$.

4) the input voltage $U_{\rm in}$ is constant;
5) the voltage drop between n_1 and n_0 is called dc-link voltage $U_{\rm dc}$, where $U_{\rm dc} = U_{\rm n1} - U_{\rm n0} = U_{\rm in} + U_{\rm C}$;
6) the load R is a pure resistance and $R << 1/\omega C_{\rm o}$, where ω is the line angular frequency. Hence, the current $i_{\rm L2}$ through the output inductor L_2 has the same phase with the output voltage u_o.

Based on these assumptions, the circuit operations in one switching cycle can be divided into several stages, and each dynamic equivalent circuit of the stages is shown in Figs. 5 and 6.

1) CCM: The circuit operations in one switching cycle can be divided into four stages in CCM. Fig. 7(a) shows the relevant waveforms. The detailed analysis is given as follows.

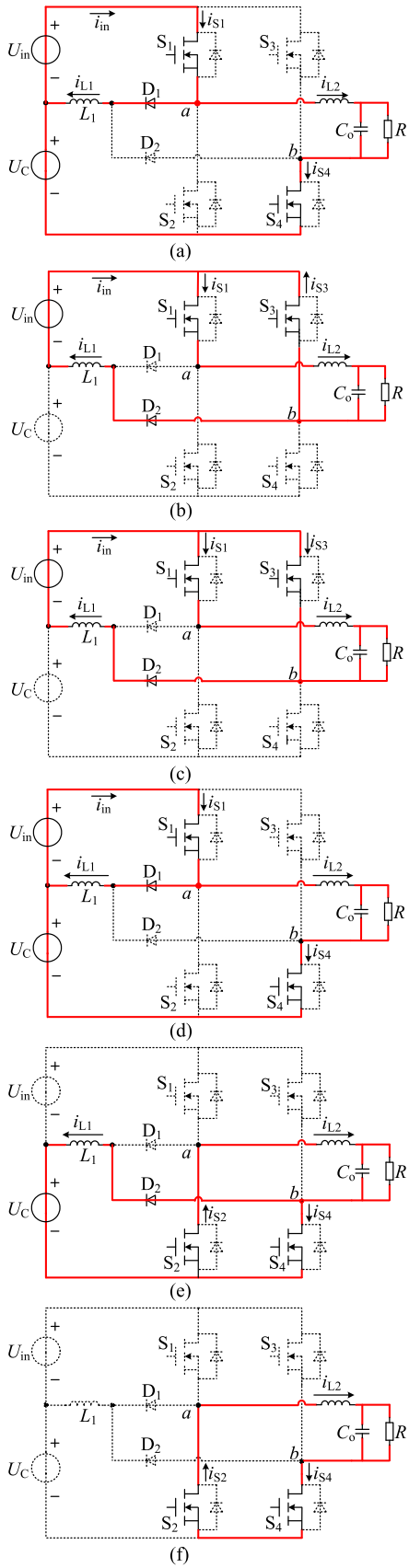

Fig. 6. Equivalent modal diagrams of DCM. (a) Stage 1: $[t_0 - t_1]$. (b) Stage 2: $[t_1 - t_2]$. (c) Stage 3: $[t_2 - t_3]$. (d) Stage 4: $[t_3 - t_4]$. (e) Stage 5: $[t_4 - t_5]$. (f) Stage 6: $[t_5 - t_6]$.

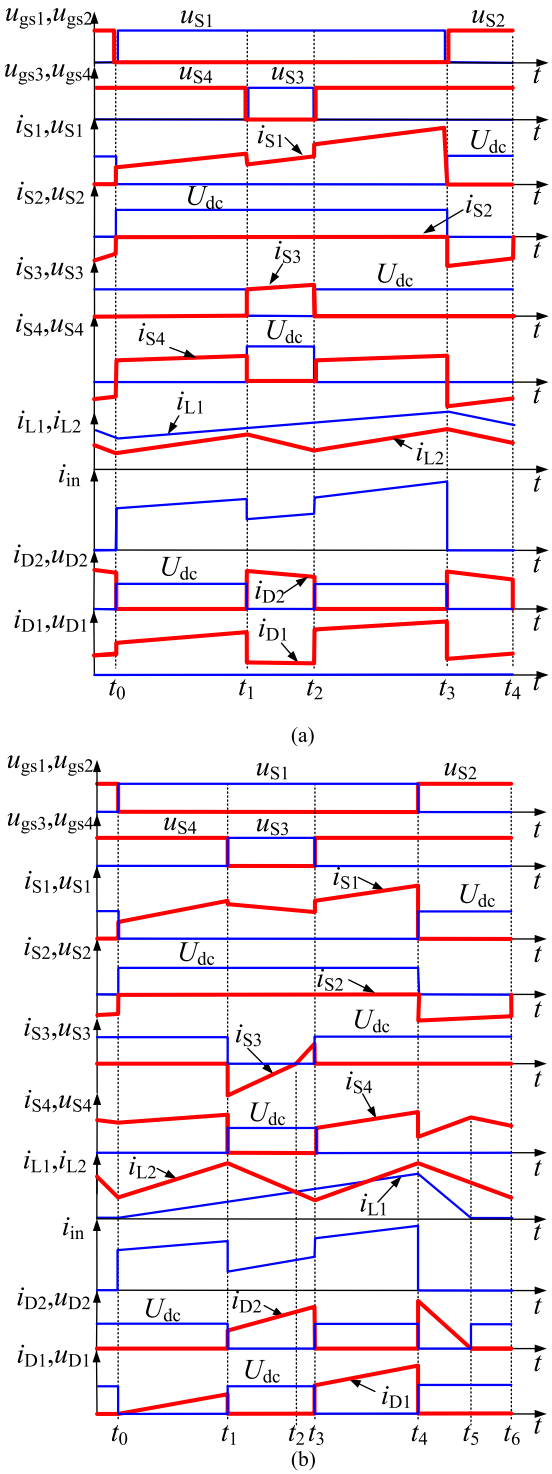

Fig. 7. Main waves of the proposed inverter. (a) CCM and DCM (in the AB section). (b) DCM (in the BC section).

Stage 1 [$t_0 - t_1$; see Fig. 5(a)]: Before $t = t_0$, the switches S_2 and S_4 and the diodes D_1 and D_2 maintain the turn-on state, while the current $i_{L1}(t)$ and $i_{L2}(t)$ linearly decrease. This stage starts when S_2 turns off and S_1 turns on at $t = t_0$. At this moment, D_2 is reverse biased and both $i_{L1}(t)$ and $i_{L2}(t)$ begin linearly increasing. The relevant equation can be described as

$$i_{L1}(t) = \frac{U_{in}}{L_1}(t - t_0) + i_{L1}(t_0). \tag{1}$$

Stage 2 [$t_1 - t_2$; see Fig. 5(b)]: At the instant $t = t_1$, S_4 turns off and S_3 turns on. Then, D_2 is forward biased again. During this stage, $i_{L1}(t)$ keeps increasing, while $i_{L2}(t)$ continues to freewheel via D_2, U_{in}, and S_1.

Stage 3 [$t_2 - t_3$; see Fig. 5(c)]: At the instant $t = t_2$, S_3 turns off and S_4 turns on. During this stage, the operating process is the same as that during Stage 1.

Stage 4 [$t_3 - t_4$; see Fig. 5(d)]: At the instant $t = t_3$, S_1 turns off and S_2 turns on. $i_{L1}(t)$ starts to decrease and freewheel by D_1, D_2, S_2, and S_4. This stage will end at the instant $t = t_4$, then the next switching cycle begins, repeating the above process. The relevant equation can be described as

$$i_{L1}(t) = -\frac{U_C}{L_1}(t - t_3) + i_{L1}(t_3). \tag{2}$$

2) DCM: As shown in Fig. 4(b), $i_{L1}(t)$ is discontinuous only in the BC section, which means the inverter's working process in the AB section is same as that in CCM and will not repeat here. While the inverter's operation in one switching cycle in the BC section can be divided into six stages. Fig. 7(b) shows the relevant waveforms. The detailed analysis is given as follows:

Stage 1 [t_0, t_1; see Fig. 6(a)]: Before $t = t_0$, the switches S_2 and S_4 remain in the turn-on state. At the instant $t = t_0$, S_2 turns off and S_1 turns on. During this stage, the operating process is similar with Stage 1 in CCM except $i_{L1}(t_0)$ equals to zero.

Stage 2 [t_1, t_2; see Fig. 6(b)]: At the instant $t = t_1$, S_4 turns off and S_3 turns on. $i_{L2}(t)$ has to freewheel via S_3 and S_1. The potential of point b will be higher than that of point a because of the inverse direction of voltage drop across the on-state resistance of S_1 and S_3. As a result, D_1 is reverse biased and D_2 is forward biased. During this stage, $i_{L1}(t)$ continues to linearly increase. At the instant $t = t_2$, $i_{L1}(t) = i_{L2}(t)$, Stage 2 is end.

Stage 3 [t_2, t_3; see Fig. 6(c)]: From the instant $t = t_2$, $i_{L1}(t)$ continues to increase and is higher than $i_{L2}(t)$. Hence, the current $i_{S3}(t)$ changes its direction and starts to rise from zero. Since $i_{S3}(t)$ is far smaller than $i_{S1}(t)$, the voltage across S_3 is smaller than that across S_1. In other words, the potential of point b is still higher than that of point a. As a result, D_1 keeps blocking and D_2 is in on state.

Stage 4 [t_3, t_4; see Fig. 6(d)]: At the instant $t = t_3$, S_1 turns on, S_2 turns off, and Stage 4 starts. The operation process during this stage is similar with Stage 1.

Stage 5 [t_4, t_5; see Fig. 6(e)]: At the instant $t = t_4$, S_1 turns off and S_2 turns on. Both $i_{L1}(t)$ and $i_{L2}(t)$ start to decrease and $i_{L2}(t)$ has to freewheel via S_2 and S_4. The potential of point b will be higher than that of point a because of the inverse direction of voltage drop across the on-state resistance of S_2 and S_4. Hence, D_1 is reverse biased and D_2 is forward biased. The expression of $i_{L1}(t)$ is similar to (2).

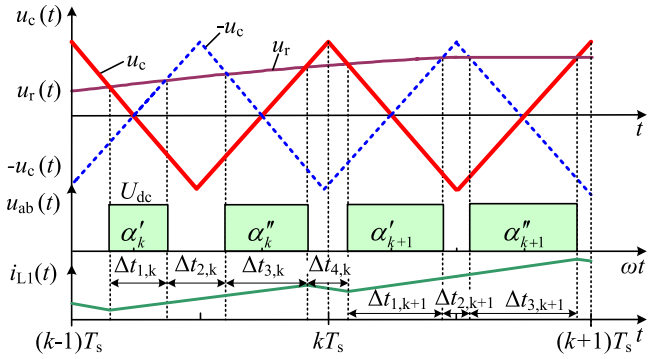

Fig. 8. Detail waveforms during positive half-period of u_r.

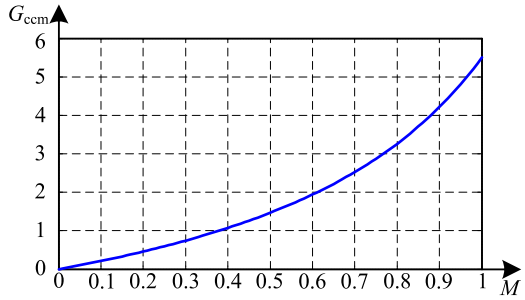

Fig. 9. Relationship curve of G_{ccm} versus M.

Stage 6 [t_5, t_6; see Fig. 6(f)]: At the instant $t = t_5$, $i_{L1}(t)$ decreases to zero, and D_2 turns off. During this stage, $i_{L1}(t)$ keeps zero and $i_{L2}(t)$ freewheels through S_2 and S_4. This stage will end at the instant $t = t_6$, then the next switching cycle begins, repeating the above process.

III. Steady Characteristic Analysis

A. Voltage Gain

1) CCM: It is assumed that carrier ratio equals *N* here. That is, according to the triangular carrier period (i.e., switching period T_s), each modulated wave period (i.e., output voltage period *T*) can be equally divided into *N* sections. Fig. 8 shows the partial detail waveforms of modulation signal $u_r(t)$, carrier signal $u_c(t)$, $u_{ab}(t)$ (voltage between point a and b), and boosting inductor current $i_{L1}(t)$, where $(k-1)T_s$ and kT_s are the starting time and the terminal time of the kth triangular carrier, respectively, while α'_k and α''_k are the zero-crossing phase of $u_c(t)$.

From Figs. 7 and 8, the increment and drop of $i_{L1}(t)$ during the kth triangular carrier period can be obtained as

$$\Delta I_{L1,r\_ccm} = \frac{U_{in}T_s\left[2 + M\left(\sin\alpha'_k + \sin\alpha''_k\right)\right]}{4L_1} \tag{3}$$

$$\Delta I_{L1,f\_ccm} = \frac{U_C T_s\left[2 - M\left(\sin\alpha''_k + \sin\alpha'_{k+1}\right)\right]}{4L_1} \tag{4}$$

where $M = U_{rm}/U_{cm} = U_{om}/U_{dc}$ is the modulation ratio, U_{rm} and U_{cm} are the amplitudes of $u_r(t)$ and $u_c(t)$, respectively. U_{om} is the fundamental amplitude of $u_{ab}(t)$ and also the amplitude of output voltage $u_o(t)$. The detail deducing process of (3) and (4) is given in the Appendix.

Then, the total increment and drop of $i_{L1}(t)$ during one positive half-period of $u_r(t)$ can be written as

$$\Delta I^{+}_{L1,ccm} = \frac{TU_{in}}{4L_1} + \frac{U_{in}T_sM}{4L_1}\sum_{k=1}^{N/2}\left(\sin\alpha'_k + \sin\alpha''_k\right) \tag{5}$$

$$\Delta I^{-}_{L1,ccm} = \frac{TU_C}{4L_1} - \frac{U_C T_s M}{4L_1}\sum_{k=1}^{N/2}\left(\sin\alpha''_k + \sin\alpha'_{k+1}\right). \tag{6}$$

According to voltage-second balance of L_1, we can obtain

$$\Delta I^{+}_{L1,ccm} = \Delta I^{-}_{L1,ccm}. \tag{7}$$

Substituting (5) and (6) into (7), we obtain

$$U_C = \frac{M}{N\sin\left(\frac{\pi}{N}\right)} \times \left\{U_{in}\left[\sin\left(\frac{N-1}{2N}\pi\right) + \sin\left(\frac{N+1}{2N}\pi\right)\right] + U_C\left[\sin\left(\frac{N+1}{2N}\pi\right) + \sin\left(\frac{N+3}{2N}\pi\right)\right]\right\} + U_{in} \approx U_{in} + \frac{2U_{om}}{\pi}. \tag{8}$$

The detail deducing process of (8) is given in the Appendix. In addition, we have

$$U_{om} = MU_{dc} = M(U_C + U_{in}). \tag{9}$$

Hence, the voltage gain of the proposed step-up inverter in CCM is deduced as

$$G_{ccm} = \frac{U_{om}}{U_{in}} \approx \frac{2\pi M}{\pi - 2M}. \tag{10}$$

From (10), it is observed that the modulation ratio M is the unique factor influencing the inverter's voltage gain in CCM. Fig. 9 depicts the relationship curve of G_{ccm} versus M. Apparently, G_{ccm} increases with M and could reach 4.2 when $M = 0.9$, which is much higher than the maximum voltage gain ($G = 1.3$) in [24].

2) DCM: As shown in Fig. 7, whether inverter operates in CCM or DCM, its operation process when $i_{L1}(t)$ is increasing during every switching period is the same. Therefore, the total increment of $i_{L1}(t)$ in DCM must be same as the one in CCM. That is

$$\Delta I^{+}_{L1,dcm} = \Delta I^{+}_{L1,ccm} = \frac{TU_{in}}{4L_1} + \frac{U_{in}T_sM}{4L_1}\sum_{k=1}^{N/2}\left(\sin\alpha'_k + \sin\alpha''_k\right). \tag{11}$$

It can be further seen that the operation process when $i_{L1}(t)$ is declining in the AB section in DCM is also same as that in CCM. Thus, the drop of $i_{L1}(t)$ during this section can be explained by (6). However, different from CCM, there are six stages during one switching cycle in the BC section in DCM, while $i_{L1}(t)$ descends during Stage 5 and equals to zero during

Stage 6, as shown in Fig. 4(b). It is assumed that there are m switching periods included in the AB section and (N/2–m) switching periods included in the BC section. Then, the drop of $i_{\mathrm{L1}}(t)$ during a switching period in the BC section be deduced as

$$\Delta I_{\mathrm{L1,fBC\_dcm}} = \frac{U_{\mathrm{C}}}{L_1}\left\{\frac{T_{\mathrm{s}}}{2} - \frac{MT_{\mathrm{s}}}{4}\left[\sin\alpha''_k + \sin\alpha'_{k+1}\right] - \Delta t_{6,k}\right\} \tag{12}$$

where $\Delta t_{6,k}$ is the duration of Stage 6 in the kth switching period and $k \in [m+1, N/2]$, as shown in Fig. 4(b). From (4) and (12), we can get the total drop of $i_{\mathrm{L1}}(t)$ during the positive half-period in DCM

$$\Delta I^{-}_{\mathrm{L1,dcm}} = \frac{TU_{\mathrm{C}}}{4L_1} - \frac{U_{\mathrm{C}}T_{\mathrm{s}}M}{4L_1}\sum_{k=1}^{N/2}\left(\sin\alpha''_k + \sin\alpha'_{k+1}\right) - \frac{\Delta TU_{\mathrm{C}}}{L_1} \tag{13}$$

where ΔT is the total duration when $i_{\mathrm{L1}} = 0$, as shown in Fig. 4.

There is $\Delta I^{+}_{\mathrm{L1,dcm}} = \Delta I^{-}_{\mathrm{L1,dcm}}$ according to the voltage-second balance of L_1, so we can obtain

$$U_{\mathrm{C}} \approx \frac{U_{\mathrm{in}} + \frac{2U_{\mathrm{om}}}{\pi}}{1 - \frac{4\Delta T}{T}} = \frac{U_{\mathrm{in}} + \frac{2U_{\mathrm{om}}}{\pi}}{1 - \frac{4k\Delta T'}{T}} \tag{14}$$

where $k = \Delta T/\Delta T'$ and $\Delta T'$ is the duration of the BC section. The detailed deducing process of (13) and (14) is also given in the Appendix.

According to (14), the voltage gain in DCM can be deduced:

$$G_{\mathrm{dcm}} = \frac{U_{\mathrm{om}}}{U_{\mathrm{in}}} = \frac{(2 - 4kf\Delta T')M}{\left(1 - 4kf\Delta T' - \frac{2M}{\pi}\right)} \tag{15}$$

where $f = 1/T$ is the frequency of the sinusoidal modulation wave and the fundamental output voltage.

The approximate analytic expression of $\Delta T'$ can be obtained with geometric method. From Fig. 4(b), we can see that point D and point E are the adjacent positive amplitude point of $i_{\mathrm{L1}}(t)$, respectively. Connecting DB and EC to the point F and according to the similar triangles theorem, we can obtain

$$\Delta T' \approx \frac{T\left(I_{\mathrm{L1,max}} - I_{\mathrm{L1,avg}}\right)}{4I_{\mathrm{L1,max}}}. \tag{16}$$

Since $i_{\mathrm{L1}}(t)$ is fluctuating with $2f$, its total increment during a positive half-period of $u_{\mathrm{r}}(t)$ will be $\Delta I^{+}_{\mathrm{L1,ccm}} = 4I_{\mathrm{L1,max}}$, and then (11) can be simplified and transformed as

$$I_{\mathrm{L1,max}} \approx \frac{U_{\mathrm{in}}T}{4L_1}\left(\frac{1}{4} + \frac{M}{2\pi}\right). \tag{17}$$

Assuming that the inverter's loss is very small, and then $P_{\mathrm{o}} = U_{\mathrm{in}}I_{\mathrm{in}}$, where I_{in} is the input average current. Considering the average current through the capacitor C_{d} is zero during one period of $u_{\mathrm{r}}(t)$, the average of $i_{\mathrm{L1}}(t)$ will equal I_{in}, that is

$$I_{\mathrm{L1,avg}} = I_{\mathrm{in}} = \frac{P_{\mathrm{o}}}{U_{\mathrm{in}}}. \tag{18}$$

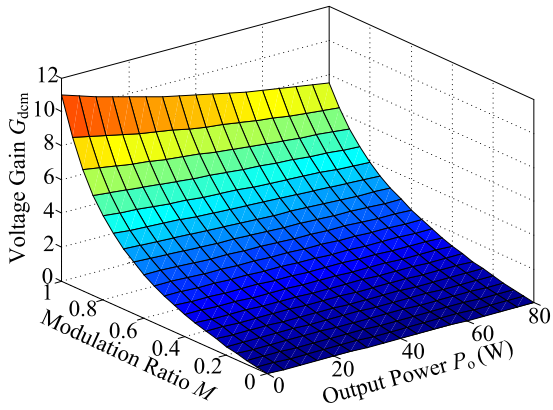

Fig. 10. Relationships among G, P_{o} and M.

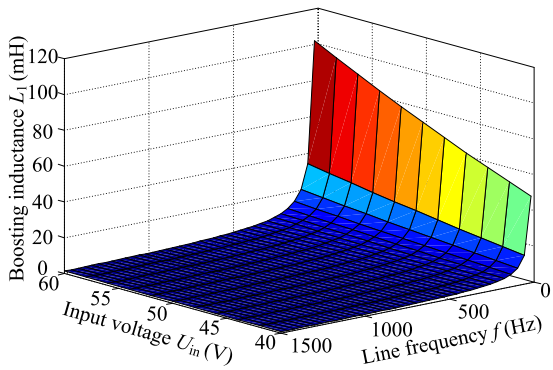

Fig. 11. Variation of L_1 with U_{in} and f when $P_{\mathrm{o,max}} = 400\mathrm{W}$.

Substituting (17) and (18) into (16), we have

$$\Delta T' = \frac{T}{4} - \frac{4\pi P_{\mathrm{o}}L_1}{U^2_{\mathrm{in}}(\pi + 2M)}. \tag{19}$$

According to (15) and (19), we have

$$G_{\mathrm{dcm}} = \frac{M\left[(2-k)(\pi+2M)\pi U^2_{\mathrm{in}} + 16\pi^2 kfP_{\mathrm{o}}L_1\right]}{(\pi - \pi k - 2M)U^2_{\mathrm{in}}(\pi + 2M) + 16\pi^2 kfP_{\mathrm{o}}L_1}. \tag{20}$$

In this case, the duration of stage 6 is about one-fifth of T_{s}. Therefore, k is approximately equal to 0.2. Fig. 10 shows the three-dimensional relationship among G_{dcm}, P_{o} and M, when $U_{\mathrm{in}} = 42$ V, $k = 0.2$, $f = 500$ Hz and $L_1 = 2$ mH. It can be found that G_{dcm} increases with the increase of M or the decrease of P_{o}.

B. Boosting Inductance L_1

According to (5), we can have

$$\begin{aligned} L_1 &= \frac{U_{\mathrm{in}}T}{4\Delta I^{+}_{\mathrm{L1,ccm}}} + \frac{U_{\mathrm{in}}T_{\mathrm{s}}M}{4\Delta I^{+}_{\mathrm{L1,ccm}}\sin\left(\frac{\pi}{N}\right)} \times\left[\sin\left(\frac{N-1}{2N}\pi\right) + \sin\left(\frac{N+1}{2N}\pi\right)\right] \\ &\approx \frac{U_{\mathrm{in}}}{2fI_{\mathrm{L_1,pp}}}\left(\frac{1}{4} + \frac{M}{2\pi}\right) \end{aligned} \tag{21}$$

TABLE II
PERFORMANCE COMPARISON OF DIFFERENT SINGLE-STAGE STEP-UP INVERTERS. (A) PASSIVE COMPONENT. (B) ACTIVE COMPONENTS

			Inductance/current stress			Capacitance/voltage stress		
			L_1	L_2	L_3	C_{d1}	C_{d2}	C_o
Current source inverter[15]			11mH/13.8A	2mH/5.2A	--	10μF/200V	--	0.3μF/200V
Z-source inverter [8]			unsuitable	unsuitable	unsuitable	unsuitable	unsuitable	unsuitable
Combined inverter [19]			0.03mH/44.5A	0.03mH/44.5A	2mH/5.2A	10μF/250V	10μF/250V	0.3μF/200V
Active buck-boost inverter [23]			0.161mH/38.8A	--	--	--	--	0.3μF/200V
Dual-leg-integrated inverter	Literature [26] (Hybrid modulation)		Coupling inductance 0.041mH/10.5A		2mH/5.2A	200μF/250V	--	0.3μF/200V
	Literature [27] (Hybrid modulation)		0.58 mH/10.5A	--	2mH/5.2A	90μF/250V	--	0.3μF/200V
	The proposed inverter	(UFD-SPWM)	2mH/10.5A	--	2mH/5.2A	470μF/200V	--	0.3μF/200V
		(Hybrid modulation)	0.35mH/10.5A					

(a)

		Switches				Diodes			
Current source inverter[15]		S_1-S_4				D_1-D_4			
		U_{om}				U_{om}			
		7.9A/162V				7.9A/162V			
Z-source inverter [8]		unsuitable				unsuitable			
Combined inverter [19]		S_1,S_3		S_2,S_4		None			
		(U_{in}+U_{om})		(U_{in}+U_{om})					
		13A /199V		8A/199V					
Active buck-boost inverter [23]		S_1, S_3	S_2, S_4	S_5-S_6	S_7-S_8	None			
		U_{in}	U_{in}	U_{om}	U_{om}				
		15.4A/42V	21.9A/42V	15.4A/155V	21.9A/155V				
Dual-leg-integrated inverter	Literature [26] (Hybrid modulation)	S_1,S_3		S_2,S_4		D_1,D_2		D_3	
		$U_{in}\frac{1+nD_{bst}}{1-D_{bst}}$		$U_{in}\frac{1+nD_{bst}}{1-D_{bst}}$		$U_{in}\frac{1+nD_{bst}}{1-D_{bst}}$		$U_{in}\frac{1+n}{1-D_{bst}}$	
		3A/210V		14.8A/210V		12.9A/210V		4A/356V	
	Literature [27] Hybrid modulation	S_1,S_3		S_2,S_4		D_1-D_4	D_{1A}, D_{3A}	D_{1B}, D_{3B}	D_B
		11.4A/256V		2.9A/210V		1A/210V	3A/256V	9.1A/245V	5.9A/249 V
	The proposed inverter (UFD-SPWM)	S_1,S_3		S_2,S_4		D_1,D_2			
		$2U_{in}+\frac{2U_{om}}{\pi}$		$2U_{in}+\frac{2U_{om}}{\pi}$		$2U_{in}+\frac{2U_{om}}{\pi}$			
		8.5A/182V		3.4A/182V		7.2A/178V			
	(Hybrid modulation)	$U_{in}\frac{1}{1-D_{bst}}$		$U_{in}\frac{1}{1-D_{bst}}$		$U_{in}\frac{1}{1-D_{bst}}$			
		7.7A/210V		3A/210V		6.6A/206V			

(b)

where $I_{\mathrm{L1,pp}} = 0.5\Delta I^{+}_{\mathrm{ccm}} = 2I_{\mathrm{L1,max}}$ is the peak–peak value of $i_{\mathrm{L1}}(t)$. Obviously, $i_{\mathrm{L1}}(t)$ will be discontinuous when $I_{\mathrm{L1,pp}} \le 2I_{\mathrm{L1,avg}}$. In general, this case is designed to appear under 40% of rated load power $P_{\mathrm{o,max}}$. Thus, based on (10), (18), and (21), we can obtain the boosting inductance

$$L_1 \ge \frac{U_{\mathrm{in}}^2(\pi U_{\mathrm{in}} + 2U_{\mathrm{om}})}{6.4 f P_{\mathrm{o,max}}(\pi U_{\mathrm{in}} + U_{\mathrm{om}})}. \tag{22}$$

Fig. 11 shows the variation of L_1 with U_{in} and f when $P_{\mathrm{o,max}} = 400$ W. As can be seen, the lower limit of L_1 is inversely proportional to f. Therefore, the size and weight of L_1 will be significantly reduced when the proposed inverter is used in HFAC microgrid over other traditional 50 Hz applications.

C. Decoupling Capacitance C_{d}

The decoupling capacitor C_{d} is to buffer the difference of instantaneous power between the source and the load. Therefore, the voltage across C_{d} contains a double-line frequency pulsation. Supposing the desired low ripple is $\Delta U_{\mathrm{C}} = 0.02U_{\mathrm{C}}$, the

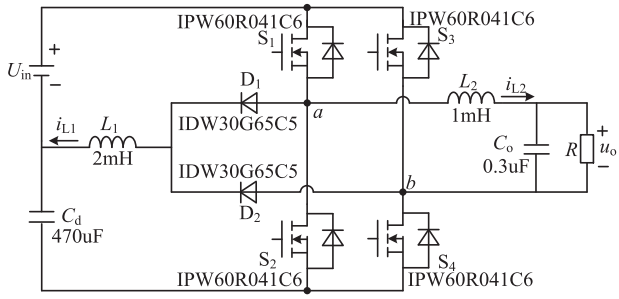

Fig. 12. Implemented power stage circuit of the prototype.

requirement of decoupling capacitance can be given as [28]

$$C_{\mathrm{d}} \ge \frac{P_{\mathrm{o,max}}}{2\pi f \Delta U_{\mathrm{C}} U_{\mathrm{C}}} = \frac{P_{\mathrm{o,max}}}{0.04\pi f U_{\mathrm{C}}^2} \tag{23}$$

where $P_{\mathrm{o,max}}$ is the maximum output power, U_{c} is the average voltage across C_{d}. If $U_{\mathrm{C}} = 160$ V, $P_{\mathrm{o,max}} = 400$ W, and $f = 500$ Hz, we can obtain $C_{\mathrm{d}} \ge 249\,\mu$F. Here, $C_{\mathrm{d}} = 470\,\mu$F is

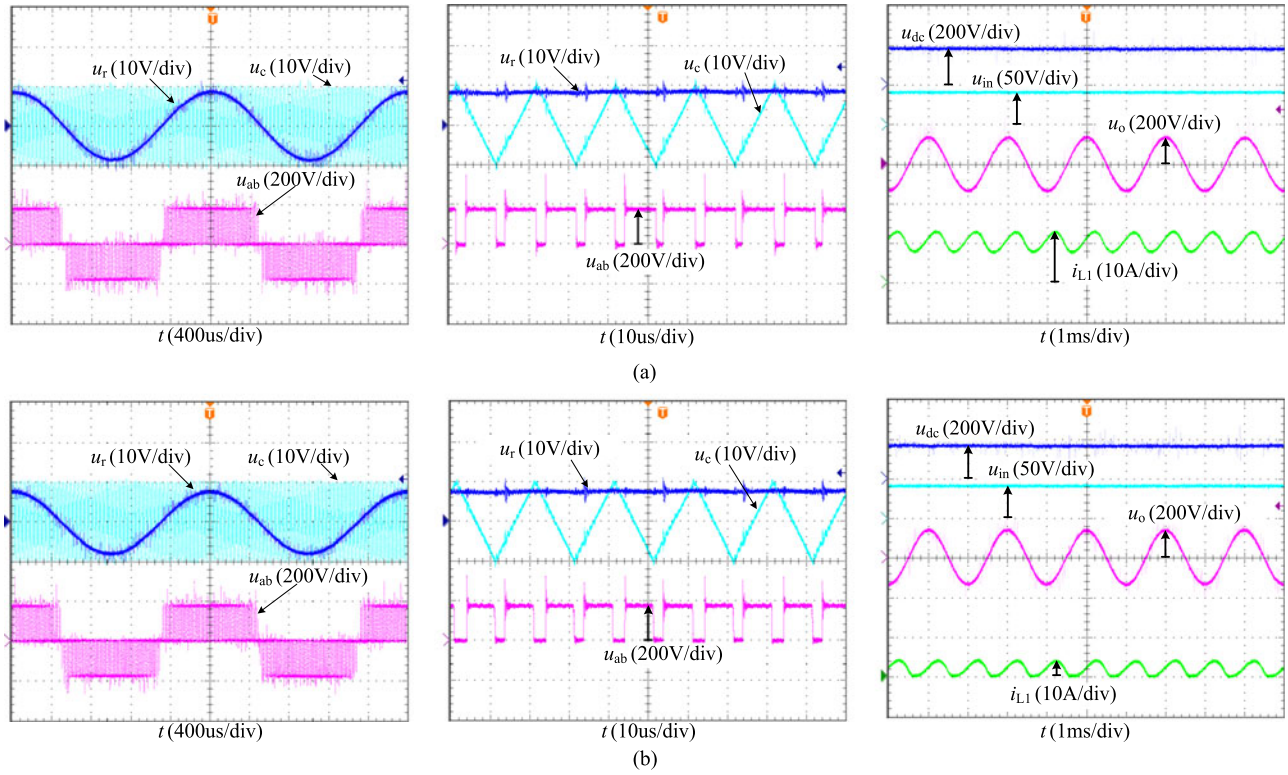

Fig. 13. Experimental results when the monopole frequency doubling SPWM modulation is adopted. (a) $P_o = 400$ W. (b) $P_o = 80$ W.

chosen. Furthermore, as can be seen from Fig. 11, $L_1 \approx 2$ mH under such working conditions.

Other key features in terms of component count, the capacitance, inductance, and electric stress of the proposed inverter and existing typical single-stage inverters have been compared in Table II. The device current stress expressions of the inverters are not given due to their complexity and difficulty to compare intuitively. Hence, the voltage stress expressions and the simulation values of electric stress under the same working condition ($U_{in} = 42$ V, $U_o = 110$ V, $f_s = 50$ kHz, $f = 500$ Hz, $P_o = 400$ W) are provided in this table. Since the voltage gain of the single-phase Z source inverter is low (usually less than 2), it is unsuitable for this application. Therefore, the parameters of Z source inverter are not given here. From Table II, we can see that, except the current-fed inverter, all these inverters show their respective advantages in the fields, such as the inductance, capacitance, the elements number, and electric stress. However, it is obvious that the proposed dual-leg-integrated inverter has less components and smaller current stress of power switches when compared with other traditional single-stage boosting inverters, which results in a simpler structure and lower conduction losses. Furthermore, it can also be found that the passive component requirements of the decoupling capacitance C_d and output *LC* filter are similar under both the hybrid modulation and the UFD-SPWM. However, to obtain the same desired current ripple, the inductance L_1 under UFD-SPWM is much larger than that under hybrid modulation, which is also the main demerit of the dual-leg-integrated inverters under the UFD-SPWM.

IV. Experiment Results

A 400 W prototype of the proposed buck–boost dual-leg-integrated step-up inverter was built and tested in lab to verify its feasibility. The main objective of the paper is to investigate the capability of the inverter to produce high voltage gain and high-quality output voltage. Hence, we have designed the inverter for islanded mode. The specifications are described as follows: input voltage is $U_{in} = 42 - 54$V, the RMS and frequency of output voltage are $U_o = 110$ V and $f = 500$ Hz, respectively. The maximum output power is $P_{o,max} = 400$ W, and the switching frequency is $f_s = 50$ kHz. The implemented power stage circuit is shown in Fig. 12.

Fig. 13(a) and (b) depicts the experiment waveforms of $u_r(t)$, $u_c(t)$, $u_{ab}(t)$, $u_{in}(t)$, $u_o(t)$, and $i_{L1}(t)$ when the buck–boost-integrated inverter is at 400 and 80 W, respectively. It can be seen that this inverter adopts UFD-SPWM and its input voltage U_{in} equals to 42 V, while output voltage RMS is controlled to 110 V both in CCM and DCM, which means the proposed inverter under UFD-SPWM can boost the input voltage. Moreover, in both operation modes, the voltage gain *G* equals to 3.7, but the modulation ration M is measured as 0.87 (CCM) and 0.81 (DCM), respectively. According to Figs. 9 and 10, the theoretical value of *M* is 0.85 (CCM) and 0.78 (DCM) under the same operation condition, which approximately agree with the experimental results.

Fig. 14 shows the transient waveforms when the inverter transitions between CCM and DCM at $U_{in} = 42$ V. In the experiments, the set point of the load will be changed at the time t_{switch} to initiate the operation mode switch. It can be seen that

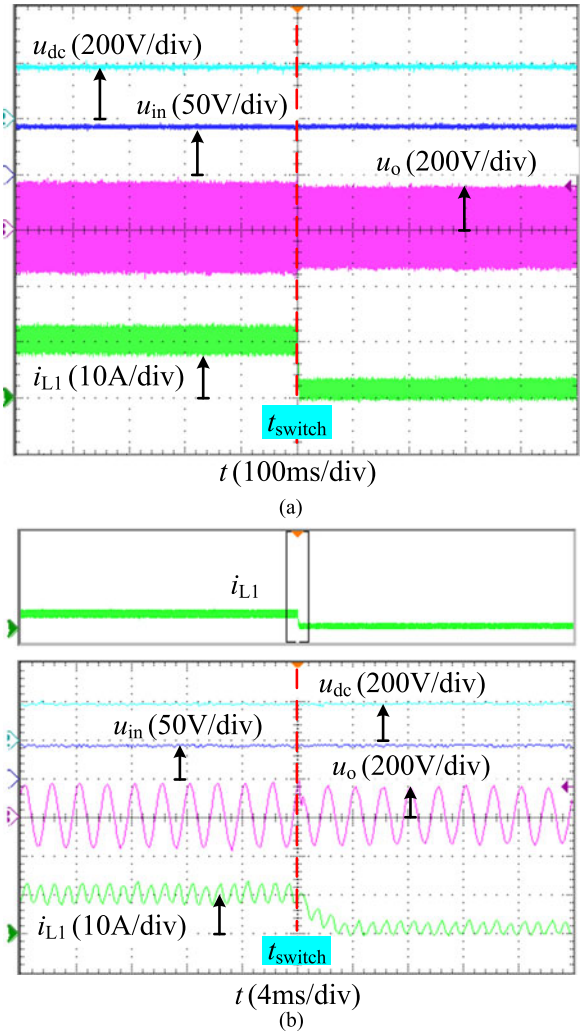

Fig. 14. Experimental results when $U_{in} = 42$ V under load variation. (a) Overall results. (b) Partial enlargement.

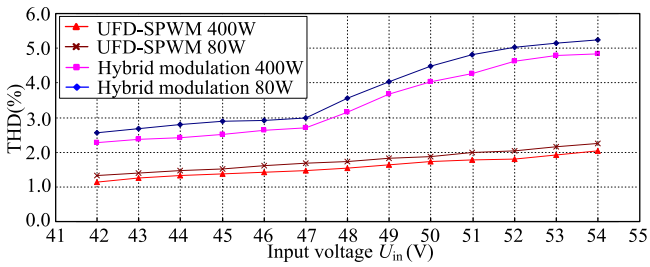

Fig. 15. THD of output voltage with different modulation method.

the inverter works in CCM before the time t_{switch}, as shown in Fig. 14(b). At this moment, u_o is kept stable and its RMS is 110 V. After t_{switch}, the current i_{L1} becomes discontinuous and u_o quickly restore to stability after 4 ms (i.e., two line period), which demonstrates that the proposed inverter can work well under load variation with UFD-SPWM modulation.

The THD of the presented inverter under UFD-SPWM as well as hybrid modulation is measured in Fig. 15. As can be

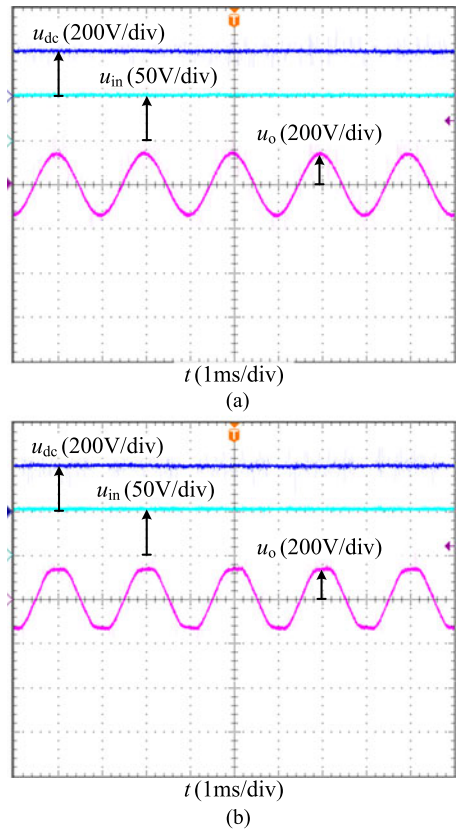

Fig. 16. Experimental waveform of u_o when $P_o = 400$ W and $U_{in} = 54$ V with different modulation methods. (a) UFD-SPWM. (b) Hybrid modulation.

seen, the THD of the proposed inverter adopting UFD-SPWM is less than 3% and is always below than that under the hybrid modulation. The reason lies in that only one bridge-leg of the inverter is under SPWM in hybrid modulation case. That is, the hybrid modulation is in fact a unipolar SPWM method. It is clear that the output voltage quality of unipolar SPWM is worse than that of UFD-SPWM. Furthermore, it also can be found that the THD under UFD-SPWM is barely affected by the input voltage and load power. However, when the inverter adopts the hybrid modulation method, the THD will become worse with the increase of input voltage under heavy load and high input voltage. This is because in this case (hybrid modulation), u_{r1} will be less than u_{r2}, as shown in Fig. 2, which leads to the overmodulation of SPWM bridge-leg and then results in the output voltage distortion. However, this situation will not occur in UFD-SPWM.

Fig. 16 shows the output voltage waveforms when the inverter at $U_{in} = 54$ V and $P_o = 400$ W adopts UFD-SPWM and hybrid modulation, respectively. It can be seen that, although the experimental condition is the same, the output voltage waveform distorts in the latter case, which also proves the above analysis.

Moreover, to further show the performance of the proposed inverter, Fig. 17 shows the simulation results under grid- connected mode with UFD-SPWM. As can be seen, in both the cases of $\cos\varphi = 1$(output current i_g is in phase with the grid voltage u_g) and $\cos\varphi = 0.707$ (i_g is 45° lagging u_g), the

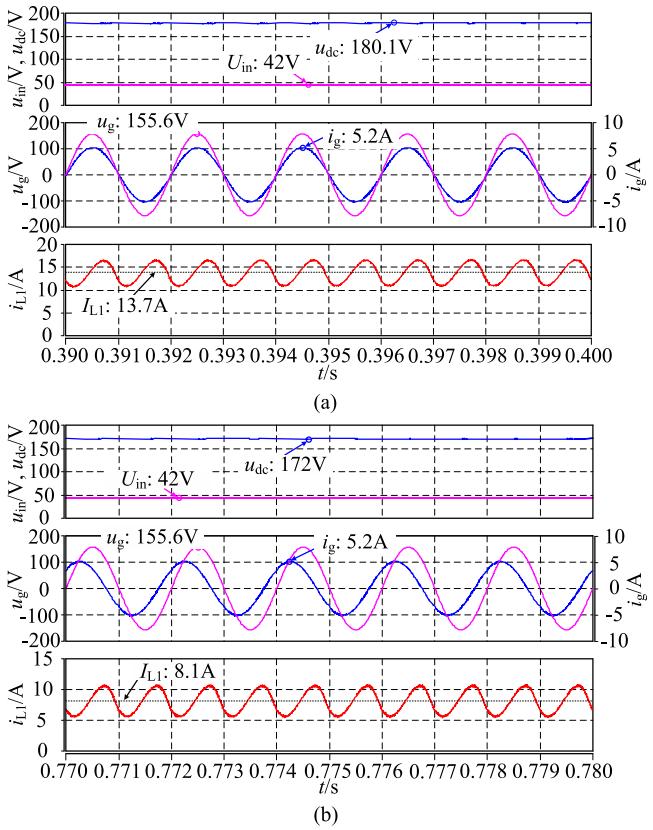

Fig. 17. Simulation results under grid-connected mode. (a) Active current injection ($\cos\varphi = 1$). (b) Reactive current injection ($\cos\varphi = 0.707$).

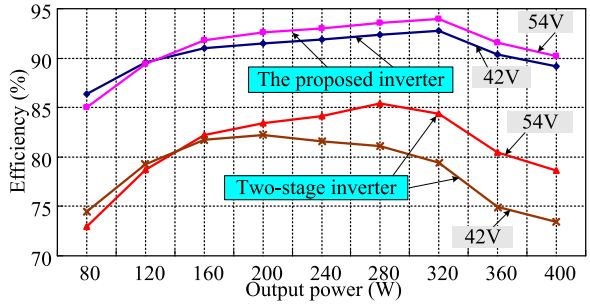

Fig. 18. Measured efficiency of the proposed inverter and the conventional two-stage step-up inverter.

proposed inverter can boost the input voltage with high-quality grid-connected current.

Fig. 18 shows the efficiency curves of the proposed inverter and the two-stage single-phase step-up inverter. In this two-stage inverter, the front-end circuit is a conventional buck–boost converter, and the rear-end one is a voltage-fed full-bridge inverter. It can be seen that the efficiency of the proposed inverter is apparently higher than that of the two-stage inverter under the same working conditions. One of the reasons is that the buck–boost diode is integrated with the two lower switches working under synchronous rectification mode, which decreases the conduction loss of the diode. Another important reason is that the decoupling capacitor $C_{\rm d}$ in this proposed inverter is connected in series with the input power source, which achieves higher gain under the same duty cycle D (or modulation ratio M). This structure is very similar to partial power converter [29]–[30]. Hence, its efficiency can be improved based on the same principle. Furthermore, it is found that the efficiency of the proposed inverter increases with $U_{\rm in}$ and reaches its maximum 94% when $U_{\rm in} = 54$ V and $P_{\rm o} = 320$ W.

V. Conclusion

To satisfy the performance requirements (i.e., high integration and high voltage gain, and lower THD) of renewable energy interface inverter in a single-phase HFAC microgrid, this paper proposed and analyzed a buck–boost step-up inverter adopting the UFD-SPWM method. The investigation shows that the proposed inverter has advantages of fewer components over other single-phase single-stage step-up inverters. In addition, when UFD-SPWM is adopted, the inverter can attain high-voltage gain, consequently allowing operation from low dc input voltage. More importantly, its control is relatively simple due to the single control variable M and its THD will be lower and not be deteriorated by the high input voltage and heavy load, unlike the hybrid modulation counterpart. It should be noted that the operation principle and characteristics are analyzed under the assumption that the load is purely resistive. Hence, the above-mentioned conclusions can also be suitable for the grid-feeding applications with unity power factor.

Appendix

A. Deducing Process of (3) and (4)

As shown in Fig. 8, based on impulse equivalency, we can have

$$U_{\rm dc}\Delta t_{1,k} = \int_{(k-1)T_{\rm s}}^{(k-\frac{1}{2})T_{\rm s}} u_{\rm o}dt = \int_{(k-1)T_{\rm s}}^{(k-\frac{1}{2})T_{\rm s}} U_{\rm om}\sin(\omega t)dt = \frac{2U_{\rm om}}{\omega}\sin\left(\frac{1}{4}\omega T_{\rm s}\right)\sin\alpha'_k \tag{A-1}$$

where $\Delta t_{1,k}$ is the duration of Stage 1 in the kth switching period, $\alpha'_k = \omega(kT_{\rm s} - \frac{3}{4}T_{\rm s})$.

Since $T_{\rm s}/T << 1$, we have

$$\sin\left(\frac{1}{4}\omega T_{\rm s}\right) = \sin\left(\frac{\pi}{2}\times\frac{T_{\rm s}}{T}\right) \approx \frac{\pi T_{\rm s}}{2T}. \tag{A-2}$$

Substituting (A-2) into (A-1), we obtain

$$\Delta t_{1,k} = \frac{U_{\rm om}T_{\rm s}}{2U_{\rm dc}}\sin\alpha'_k = \frac{MT_{\rm s}}{2}\sin\alpha'_k. \tag{A-3}$$

In a similar way, the duration of Stage 3 in the kth switching period can be obtained as

$$\Delta t_{3,k} = \frac{MT_{\rm s}}{2}\sin\alpha''_k \tag{A-4}$$

where $\alpha''_{\rm k} = \omega(kT_{\rm s} - \frac{1}{4}T_{\rm s})$.

The duration of Stage 2 and Stage 4 in the kth switching period can be expressed as

$$\Delta t_{2,k} = \frac{\frac{T_s}{2} - \Delta t_{1,k}}{2} + \frac{\frac{T_s}{2} - \Delta t_{3,k}}{2} = \frac{T_s}{2} - \frac{MT_s}{4}\left(\sin\alpha'_k + \sin\alpha''_k\right) \quad \text{(A-5)}$$

$$\Delta t_{4,k} = \frac{\frac{T_s}{2} - \Delta t_{3,k}}{2} + \frac{\frac{T_s}{2} - \frac{MT_s}{2}\sin\alpha'_{k+1}}{2} = \frac{T_s}{2} - \frac{MT_s}{4}\left(\sin\alpha''_k + \sin\alpha'_{k+1}\right). \quad \text{(A-6)}$$

During every switching period in CCM, $i_{L1}(t)$ increases from Stage 1 to Stage 3, and descends in Stage 4. The increment of $i_{L1}(t)$ in first three stages during the kth switching period can be shown as

$$\Delta I_{L1,r\_ccm1} = i_{L1}(t_1) - i_{L1}(t_0) = \frac{U_{in}MT_s}{2L_1}\sin\alpha'_k \quad \text{(A-7)}$$

$$\Delta I_{L1,r\_ccm2} = i_{L1}(t_2) - i_{L1}(t_1) = \frac{U_{in}}{L_1}\left[\frac{T_s}{2} - \frac{MT_s}{4}\left(\sin\alpha'_k + \sin\alpha''_k\right)\right] \quad \text{(A-8)}$$

$$\Delta I_{L1,r\_ccm3} = i_{L1}(t_3) - i_{L1}(t_2) = \frac{U_{in}MT_s}{2L_1}\sin\alpha''_k. \quad \text{(A-9)}$$

The increment of $i_{L1}(t)$ during the kth switching period is

$$\Delta I_{L1,r\_ccm} = \Delta I_{L1,r\_ccm1} + \Delta I_{L1,r\_ccm2} + \Delta I_{L1,r\_ccm3} = \frac{U_{in}T_s\left[2 + M\left(\sin\alpha'_k + \sin\alpha''_k\right)\right]}{4L_1}. \quad \text{(A-10)}$$

According to (A-6), the drop of $i_{L1}(t)$ during the kth switching period can be obtained as

$$\Delta I_{L1,f\_ccm} = \frac{U_C}{L_1}\Delta t_{4,k} = \frac{U_C T_s\left[2 - M\left(\sin\alpha''_k + \sin\alpha'_{k+1}\right)\right]}{4L_1}. \quad \text{(A-11)}$$

Obviously, here (A-10) is (3), while (A-11) is (4).

B. Deducing Process of (8)

Substituting (5) and (6) into (7), we obtain

$$\frac{TU_{in}}{4L_1} + \frac{U_{in}T_sM}{4L_1}\sum_{k=1}^{N/2}\left(\sin\alpha'_k + \sin\alpha''_k\right) = \frac{TU_C}{4L_1} - \frac{U_C T_s M}{4L_1}\sum_{k=1}^{N/2}\left(\sin\alpha''_k + \sin\alpha'_{k+1}\right). \quad \text{(A-12)}$$

By transforming and simplifying, we can obtain

$$U_C = U_{in} + U_{in}\frac{M}{N}\sum_{k=1}^{N/2}\left(\sin\alpha'_k + \sin\alpha''_k\right) + U_C\frac{M}{N}\sum_{k=1}^{N/2}\left(\sin\alpha''_k + \sin\alpha'_{k+1}\right). \quad \text{(A-13)}$$

From (A-1) and (A-4), we can have

$$\sum_{k=1}^{N/2}\left(\sin\alpha'_k + \sin\alpha''_k\right) = \frac{\sin(\frac{\pi}{2})}{\sin\frac{\pi}{N}}\sin\left(\frac{N-1}{2N}\pi\right) + \frac{\sin(\frac{\pi}{2})}{\sin\frac{\pi}{N}}\sin\left(\frac{N+1}{2N}\pi\right) \quad \text{(A-14)}$$

$$\sum_{k=1}^{N/2}\left(\sin\alpha''_k + \sin\alpha'_{k+1}\right) = \frac{\sin(\frac{\pi}{2})}{\sin\frac{\pi}{N}}\sin\left(\frac{N+1}{2N}\pi\right) + \frac{\sin(\frac{\pi}{2})}{\sin\frac{\pi}{N}}\sin\left(\frac{N+3}{2N}\pi\right). \quad \text{(A-15)}$$

Substituting (A-14) and (A-15) into (A-13), and supposing N is large enough, we have

$$U_C = \frac{M}{N\sin\left(\frac{\pi}{N}\right)} \times \left\{U_{in}\left[\sin\left(\frac{N-1}{2N}\pi\right) + \sin\left(\frac{N+1}{2N}\pi\right)\right] + U_C\left[\sin\left(\frac{N+1}{2N}\pi\right) + \sin\left(\frac{N+3}{2N}\pi\right)\right]\right\} + U_{in} \approx U_{in} + \frac{2U_{om}}{\pi}. \quad \text{(A-16)}$$

Obviously, (A-16) is the same with (8).

C. Deducing Process of (12)–(14)

As shown in Fig. 4(b), it is assumed that there are m switching periods included in the AB section and (*N*/2-*m*) switching periods included in the BC section. During every switching cycle in the BC section, $i_{L1}(t)$ descends in Stage 5 and equals to zero in Stage 6. The duration of Stages 5 and 6 are defined as $\Delta t_{5,k}$ and $\Delta t_{6,k}$, separately, where $k \in [m+1,\ N/2]$. The drop of $i_{L1}(t)$ during a switching period in the BC section can be expressed as

$$\Delta I_{L1,fBC\_dcm,k} = \frac{U_C\Delta t_{5,k}}{L_1} = \frac{U_C}{L_1}\left[\frac{T_s}{2} - \frac{MT_s}{4}\left(\sin\alpha''_k + \sin\alpha'_{k+1}\right) - \Delta t_{6,k}\right]. \quad \text{(A-17)}$$

The inverter's operation process in the AB section is similar with that in CCM. Therefore, according to (A-11) and (A-17), the total drop of $i_{L1}(t)$ during the positive half-period in DCM

$$U_{\mathrm{C}} = \frac{U_{\mathrm{in}} + \frac{U_{\mathrm{in}} M}{N} \sum_{k=1}^{N/2} (\sin \alpha'_k + \sin \alpha''_k) + \frac{U_{\mathrm{C}} M}{N} \sum_{k=1}^{N/2} (\sin \alpha''_k + \sin \alpha'_{k+1})}{1 - \frac{4\Delta T}{T}} \tag{A-20}$$

can be expressed as

$$\Delta I^{-}_{\mathrm{L1,dcm}} = \sum_{k=1}^{m} \Delta I_{\mathrm{L1,fAB\_dcm},k} + \sum_{k=m+1}^{N/2} \Delta I_{\mathrm{L1,fBC\_dcm},k}$$

$$= \frac{TU_{\mathrm{C}}}{4L_1} - \frac{U_{\mathrm{C}} T_{\mathrm{s}} M}{4L_1} \sum_{k=1}^{N/2} (\sin \alpha''_k + \sin \alpha'_{k+1}) - \frac{U_{\mathrm{C}} \Delta T}{L_1} \tag{A-18}$$

where $\Delta I_{\mathrm{L1,fAB\_dcm,k}}$ is the drop of $i_{\mathrm{L1}}(t)$ during a switching period in the AB section, ΔT is the total duration when $i_{\mathrm{L1}} = 0$. Here, (A-18) is (13)

Since $\Delta I^{-}_{\mathrm{L1,dcm}} = \Delta I^{+}_{\mathrm{L1,dcm}} = \Delta I^{+}_{\mathrm{L1,ccm}}$, we can have

$$\frac{TU_{\mathrm{in}}}{4L_1} + \frac{U_{\mathrm{in}} T_{\mathrm{s}} M}{4L_1} \sum_{k=1}^{N/2} (\sin \alpha'_k + \sin \alpha''_k)$$

$$= \frac{TU_{\mathrm{C}}}{4L_1} - \frac{U_{\mathrm{C}} T_{\mathrm{s}} M}{4L_1} \sum_{k=1}^{N/2} (\sin \alpha''_k + \sin \alpha'_{k+1}) - \frac{U_{\mathrm{C}} \Delta T}{L_1} \tag{A-19}$$

Substituting (A-14) and (A-15) into (A-20), as shown at the top of this page, we obtain

$$\begin{aligned} U_{\mathrm{C}} &= \frac{M}{1 - \frac{4\Delta T}{T}} \left\{ \frac{U_{\mathrm{in}}}{N} \left[\frac{\sin(\frac{\pi}{2})}{\sin \frac{\pi}{N}} \sin \left(\frac{N-1}{2N} \pi \right) \right. \right. \\ &\quad \left. + \frac{\sin(\frac{\pi}{2})}{\sin \frac{\pi}{N}} \sin \left(\frac{N+1}{2N} \pi \right) \right] \\ &\quad + \frac{U_{\mathrm{C}}}{N} \left[\frac{\sin(\frac{\pi}{2})}{\sin \frac{\pi}{N}} \sin \left(\frac{N+1}{2N} \pi \right) \right. \\ &\quad \left. \left. + \frac{\sin(\frac{\pi}{2})}{\sin \frac{\pi}{N}} \sin \left(\frac{N+3}{2N} \pi \right) \right] + \frac{U_{\mathrm{in}}}{M} \right\} \\ &\approx \frac{U_{\mathrm{in}} + \frac{2U_{\mathrm{om}}}{\pi}}{1 - \frac{4\Delta T}{T}}. \end{aligned} \tag{A-21}$$

Here, (A-21) is (14).

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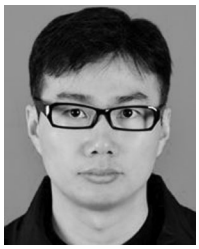

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