A New Inductive Power Transfer Topology Using Direct AC–AC Converter With Active Source Current Waveshaping

Suvendu Samanta, *Student Member, IEEE* and Akshay Kumar Rathore, *Senior Member, IEEE*

(Highlighted Paper)

***Abstract*—Generally, in wireless inductive power transfer (IPT) system, the power is processed through multiple power transfer stages and this leads to lower efficiency and higher cost of the system. Recent research shows that the use of a direct ac–ac converter in an IPT system compensates these limitations significantly. However, one of the major challenges of the IPT circuit with direct ac–ac converter is to achieve multiple control goals through a single converter. These include load power requirement, maintaining high-quality source current and achieving soft switching of inverter switches, etc. In the existing literatures, the research is more focused on meeting load power requirement and soft switching of inverter switches. The major focus of this paper is to propose, analyze, and control a new IPT power converter topology using current-fed direct ac–ac converter. Compare with existing buck derived, i.e., voltage source ac–ac converter topologies, the proposed topology is boost derived; therefore, active source current waveshaping is easily obtained. The complete control is carried out through two loops, where the outer output current loop ensures load requirements and inner loop maintains the high-quality grid current. The detail of steady-state and dynamic analysis and design procedure of the converter is presented. Experimental results obtained from a 1.2-kW lab-build prototype are included to verify the analysis and proposed control.**

***Index Terms*—AC–AC converter, inductive power transfer (IPT), resonant converter, wireless power transfer (WPT).**

I. INTRODUCTION

IN RECENT years, research on wireless power transfer (WPT) technology has gained significant popularity due to availability of high-power and high switching frequency semiconductor devices. This technology finds very suitable applications in areas, such as electric vehicle (EV) [1]–[17], electronic gadgets, implants, chemical factory, mining, underwater vehicles, and equipment [18]–[19]. The implementation of this technology in EV battery charging application is very significant because it can reduce the battery storage requirement through opportunistic charging techniques [1]. Also, the charging process is very convenient even in hostile environments, such as snow, water, dirt, and wind. Although both inductive and capacitive power transfer technologies are very popular in WPT area, the inductive power transfer (IPT) technology is more suitable in higher power application because of higher power density [1], [20].

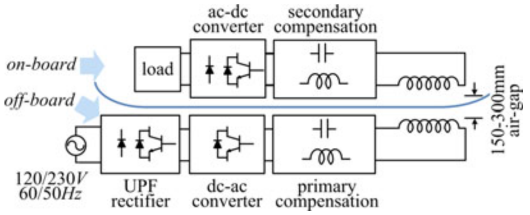

Fig. 1. Typical multistage IPT system for EV charging applications.

Generally, power in an IPT system is processed through multiple power processing stages, as shown in Fig. 1. This system is most popular because all control goals are very effectively achieved through this system. The first stage, unity power factor (UPF) rectifier maintains the high-quality source current while maintaining a fixed dc bus voltage. The next dc–ac inverter stage produces high-frequency ac for transferring power wirelessly while ensuring load requirements and soft switching of inverter switches. The last stage is the ac–dc rectification stage.

Recent research on IPT area shows that the first two power processing stages, i.e., the UPF rectifier and high-frequency dc–ac inverter can be replaced by a single-stage direct ac–ac converter [5], [21]–[24]. Thus, short lived bulky dc capacitor is removed from powertrain with a consideration that the load accepts rectified sinusoidal current. However, in case the load does not accept this current profile, then a reasonable size dc capacitor can be connected at the output of the converter. The direct ac–ac converter has to meet the following three major control requirements:

1) high-quality source current;
2) load power; and
3) soft switching of inverter switches.

Moghaddami *et al.* [22] report variable switching frequency 50% fixed duty cycle charge control technique for three-phase to

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Manuscript received May 11, 2017; revised July 24, 2017; accepted August 26, 2017. Date of publication September 6, 2017; date of current version March 5, 2018. Recommended for publication by Associate Editor J. Acero. *(Corresponding author: Akshay Kumar Rathore.)*

The authors are with the Department of Electrical and Computer Engineering, Concordia University, Montreal, QC H3G 1M8, Canada (e-mail: s_amanta@encs.concordia.ca; akshay.k.rathore@ieee.org).

This paper has supplementary downloadable material available at http://ieeexplore.ieee.org.

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Digital Object Identifier 10.1109/TPEL.2017.2750081

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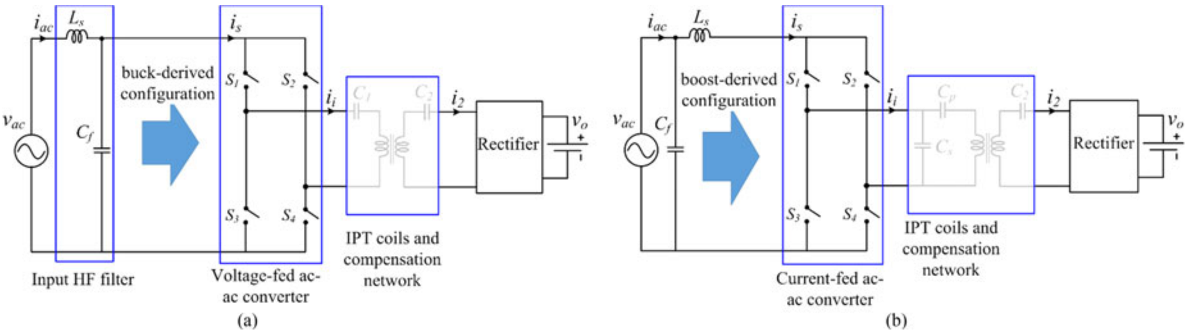


Fig. 2. (a) General powertrain of the existing IPT topology with direct ac–ac converter, and (b) required topology for PFC.

single-phase matrix converter. The required number of switches is less and the control technique ensures soft switching of all the ac–ac converter switches. Bac *et al*. [23] present phase shift modulation of three-phase to single-phase matrix converter for a series–series compensated IPT converter. The required number of semiconductor switches is less and overall converter efficiency is high. However, without directly controlling the source current, it is difficult to maintain the high-quality grid current. In conventional multistage IPT topologies, the converter before the resonant tank is generally a voltage source inverter (VSI). A VSI imposes to select primary tank network as series *LC* [2]–[3], [12], [14], [16], *LCL* [19], [25], or *LCCL* [5], [19], [26]. Generally, these same tanks are used to realize the IPT topology with direct ac–ac converter because their properties are well established in the literature [5], [21]–[23]. However, when these tanks are used in single-stage direct ac–ac converter, the input to the converter is required to be VSI. Therefore, from source side, all these existing ac–ac converter topologies have buck-derived structure that is generally not preferred for power factor correction (PFC). Therefore, similar to regular buck-derived PFCs, the source current quality with the existing ac–ac converters are highly compromised. With this understanding, it is clear that the preferred selection of ac–ac converter will be a current-source topology.

Current-fed nonresonant converters are often used for fuel cell vehicles and solar cell applications [27]–[29]. Current-fed full-bridge and half-bridge resonant IPT converters are reported for EV applications [9], [13], [17] and current-fed push–pull resonant IPTs are reported for biomedical implants [30]–[32]. The advantage of push–pull configuration in IPT application is that only two controlled devices or MOSFETs are required and gate driver circuit is very simple due to common potential of source terminals [30], [33]. Generally, control of these converters is done through a variable switching frequency fixed duty cycle method. The switching frequency is solely determined by the inverter output voltage v_i and it is done by sensing zero crossing of v_i. This helps us to achieve both zero voltage switching (ZVS) turn-on and turn-off of both the switches [30]–[32].

However, in an IPT powertrain, where input to the matrix converter is line frequency ac, the existing push–pull converter will find challenges due to requirement of extra control for maintaining source current quality. Although there is an inductor at input to the push–pull converter, but the boost-mode operation of the converter is not possible due to fixed 50% duty cycle. Other challenge of this control method is to startup the converter, detection of ZVS operating points, and avoiding frequency bifurcation [multiple zero-phase angle (ZPA) points] [30]. For these reasons, the applications of these topologies are generally limited to low power such body implants [17], [31], [32].

This paper proposes a new IPT topology using full-bridge current-fed direct ac–ac converter and it is a boost-derived topology, i.e., the input to the converter is current source. The modulation is carried out through variable duty cycle of the devices. In the primary side, a parallel–series (*CCL*) type tank network is selected to ensure compatibility between ac–ac converter and tank network. The proposed boost-derived ac–ac converter topology is controlled through two-loop control method. The outer output current loop meets the load requirement whereas the inner loop directly controls the source current. Therefore, the high-quality source current is ensured. From [9] and [17], it is clear that by the operating output side of an ac–ac converter in lagging power factor region, ZVS of the inverter switches is always achieved. Therefore, all the basic control requirements are met by this converter.

II. PROPOSED DIRECT AC–AC CONVERTER

A. *Derivation of the Proposed IPT Topology*

Most of the existing ac–ac converters for IPT applications have buck-derived structure, as shown in Fig. 2(a) and the analysis is carried out considering resistive load connected either directly with receiver coil (RC) side tank or at the output of rectifier [5], [22]–[23]. Therefore, the matrix converter perceives the load as linear load. However, these topologies will fail to control input current when a stiff dc voltage load, such as battery, is connected at rectifier output. The practical interpretation of it is that the buck-derived ac–ac converter topology does not get sufficient input voltage around zero crossing to feed power to high-voltage output dc bus. Table I lists several important aspects of different IPT topologies with direct ac–ac converter reported in the literature. It is clear that the boost-derived topology is suitable for this application to achieve PFC, as shown in Fig. 2(b).

Fig. 3 shows complete circuit of the proposed IPT topology, where the transmitter coil (TC) side tank is parallel–series (*CCL*) and the RC side is series *LC* type. The basic operation of this converter is very much similar to a boost-derived PFC. When the current through the source inductor L_s is required

TABLE I
QUALITATIVE COMPARISON OF DIFFERENT IPT TOPOLOGIES WITH DIRECT AC–AC CONVERTER REPORTED IN THE LITERATURE

Topology	Tank Configuration	Control Technique	f_s (kHz)	Load Demand Fulfilled	Dynamic Model	Achieved High-Quality Source Current	Soft Switching	Power Level
Single-stage three-phase [22]	TC: *LC* series RC: *LC* parallel	Variable f_s;	12.3; ZCD required	Yes, using power regulation control mode	No	THD 14.3%, P.F. 0.59–0.67	Yes, ZCS of all devices	267 W
SiC-based matrix converter [23]	TC: *LC* series RC: *LC* series	Fixed f_s phase shift modulation	50	Not reported	No	No	Not achieved	300 W
Direct ac–ac converter for IPT [24]	TC: *LC* series RC: Not reported	Variable f_s, energy injection and free oscillation	30; ZCD required	Not reported	No	Not reported	Yes, ZCS of all devices	10 W
MC with *LCCL* tank [5]	TC: *LCCL* RC: *LCCL*	Fixed f_s and variable duty cycle modulation	20; ZCD required	Yes	No	Yes, for *R* load and with active control of vehicle-side H-bridge	Not reported	1 kW
Proposed converter	TC: parallel–series (*CCL*) RC: *LC* series	Fixed f_s and variable duty cycle modulation	50	Yes, using the outer output current loop	Yes	Yes, THD <5% PF: UPF	both ZVS and ZCS of two switches	1.2 kW

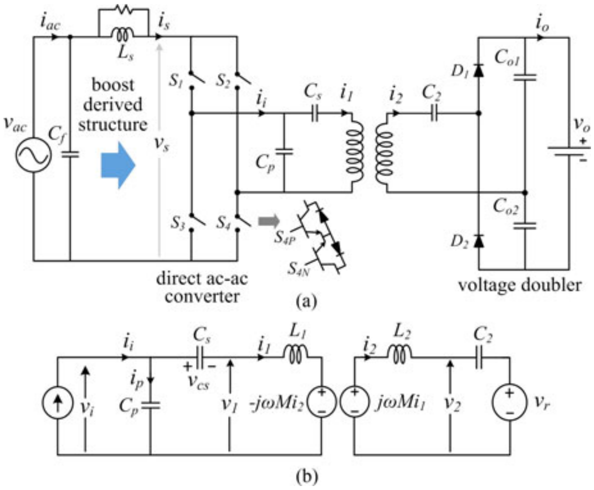


Fig. 3. Proposed ac–ac converter for IPT applications.

to be raised then the ac–ac converter is switched such that L_s directly gets connected to source voltage $v_{\rm ac}$ through converter switches. During other times, L_s is connected to the transmitter-side tank network through ac–ac converter switches. Because the input to the ac–ac converter is stiff current, the transmitter-side tank network is required to be parallel. Parallel tank has several advantages in IPT systems. The high volume of reactive component of current passes through the parallel capacitor C_p without flowing though the inverter switches; therefore, inverter switch current stress is generally lower. Also, the coil current profile is very close to sinusoidal because the parallel capacitor C_p offers much lower impedance to higher order harmonics compare to TC. Input inductor L_s provides natural short-circuit protection during inverter fault [9], [17]. Moreover, compare with the conventional parallel *LC* tank, the proposed converter has an extra series capacitor connected with TC to reduce the switch voltage stress and to improve the quality of TC current. Also, with parallel tank the lagging power factor for ZVS of inverter switches is obtained below resonance frequency, whereas for series tank, it is achieved above resonance frequency.

In the receiver side, a capacitor C_2 is connected in series with RC to achieve the required compensation and this ensures least number of components in the RC side. The rectifier in the RC side is selected to be a voltage doubler to achieve higher voltage gain while reducing the number of rectifier diodes. The steady-state operation of the converter during one inverter switching cycle is explained here.

B. Steady-State Operation

To explain the operation, consider that $S_1 - S_4$ are matrix converter switches, i.e., two switches connected in reverse direction to achieve bidirectional voltage and current controlling facility. During positive half of the input voltage, $v_{\rm ac}$ only four switches are given switching frequency pulses. These switches are named as $S_{1P} - S_{4P}$, respectively. Similarly, during negative half of input voltage, remaining four switches of the ac–ac converter are given switching frequency pulses and these are named as $S_{1N} - S_{4N}$, respectively. In this paper, only one switching cycle of an ac–ac converter during positive half of source voltage is presented in detail. The operation of the converter during negative half of source voltage is exactly similar, where $S_{1N} - S_{4N}$ take the position of $S_{1P} - S_{4P}$, respectively. During positive half of source voltage $S_{1N} - S_{4N}$ are kept permanently OFF, whereas during negative half-cycle of source voltage, $S_{1P} - S_{4P}$ are kept OFF permanently. It is confirmed that operating the inverter at lagging power factor region ensures ZVS turn-on of the switches [13]. Therefore, in the steady-state operation, ac–ac converter output voltage v_i is considered to be leading with respect to current i_i. To achieve the control goals, a unipolar modulation scheme is adopted, i.e., turn-on time of S_1 and S_3 is same but phase shifted by 180°. Similarly, turn-on time of S_2 and S_4 is same but phase shifted by 180°. Also, a

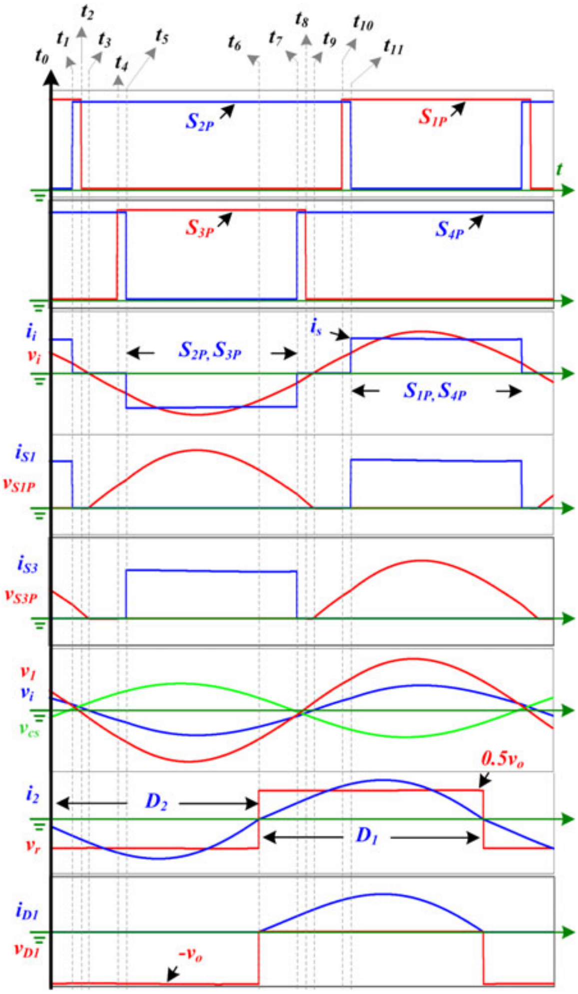


Fig. 4. Steady-state operating waveforms of one switching cycle during positive half of source voltage.

slight overlap between complementary switch pairs $S_1 - S_2$ and $S_3 - S_4$ is always maintained to provide continuous current path to input inductor L_s. Compare with the voltage-fed converter, one difference is that the complementary switching signals are not given within the leg switches, rather it is given to two top switches and two bottom switches. This technique is usual for current-fed inverters.

Interval 1 $(t_0 - t_1)$*:* During this interval, the ac–ac converter switches S_{1P} and S_{4P} are ON. Therefore, the input inductor current i_s flows through the TC-side tank network. Fig. 4 shows voltage and current waveforms of different circuit components and Fig. 5(a) shows the equivalent circuit of this switching interval. The voltages and currents of TC-side components are given as

$$L_s \frac{di_s}{dt} = v_{\text{ac}} - v_i, \qquad i_{S1} = i_{s4} = i_s. \tag{1}$$

During this interval, in the receiver side the RC current is rectified by diode D_2. The voltages and currents of RC-side elements are given as

$$v_{D1} = v_{o1} + v_{o2}, \qquad i_{D2} = i_2 \tag{2}$$

$$C_{o1} \frac{dv_{o1}}{dt} = -i_o, \qquad C_{o2} \frac{dv_{o2}}{dt} = i_2 - i_o. \tag{3}$$

Interval 2 $(t_1 - t_5)$*:* Interval $t_1 - t_2$ is switching overlap period between switches S_{1P} and S_{2P}. The duration of overlap period is almost negligible compare with one complete switching cycle but sufficient enough to transfer the input current from incoming to outgoing device. Since the voltage across S_{2P} is positive at time instant t_2, S_{2P} immediately starts conducting and current through S_{1P} is transferred even before its gate pulse is removed. Thus, at instant t_1 switch S_{2P} experience hard turn-on, whereas at instant t_2 switch S_{1P} experiences zero current turn-off. The equivalent circuit of this interval is shown in Fig. 5(b). The voltages and currents of TC-side components are given as

$$L_s \frac{di_s}{dt} = v_{\text{ac}}, \qquad i_{S3} = i_{s2} = i_s. \tag{4}$$

At instant t_2, the gate pulse of S_{1P} is removed. However, the equivalent circuit of the converter remains the same, as shown in Fig. 5(b), because current commutation from switch S_{1P} to switch S_{2P} is already occurred. At instant t_4, the overlap period of S_{3P} and S_{4P} starts. However, at this instant, the converter output voltage v_i is negative and the voltage across S_3 is negative. Although S_{3P} is triggered but S_{3N} blocks this negative voltage present across S_3. Thus, S_{4P} keeps on conducting without transferring current i_i to S_{3P}. Therefore, S_{3P} is switched ON at zero voltage. The overlap period of S_{3P} and S_{4P} gets over at instant t_5 and the equivalent circuit of the converter from t_1 to t_5 remains the same, as shown in Fig. 5(b). From Fig. 5(b), it is clear that this interval $(t_1 - t_5)$ is similar to the conventional boost converter turn-on period.

Interval 3 $(t_5 - t_6)$*:* At instant t_5, gating signal of S_{4P} is removed and it experiences hard turn-off. Although the voltage across S_{3P} is negative but source inductor current i_s forces S_{3P} to conduct because i_s has no alternate path. In this interval $t_5 - t_6$, the source current flows through the TC tank network. The equivalent circuit of the converter circuit is shown in Fig. 5(c). It is clear that this interval is similar to turn-off time period of the conventional boost converter, where input inductor is directly connected to output. The current and voltage expressions of this interval are given as

$$L_s \frac{di_s}{dt} = v_{\text{ac}} + v_i, \qquad i_{S2} = i_{s3} = i_s. \tag{5}$$

Interval 4 $(t_6 - t_7)$*:* Although at time instant t_6, there is no switching transition in the TC side but the current through the RC changes its polarity at this instant. Thus, the rectifier diode D_1 commutates D_2 and rectifies the RC coil current. The equivalent circuit of this interval is shown in Fig. 5(d). The voltage and current expressions of receiver-side components during this

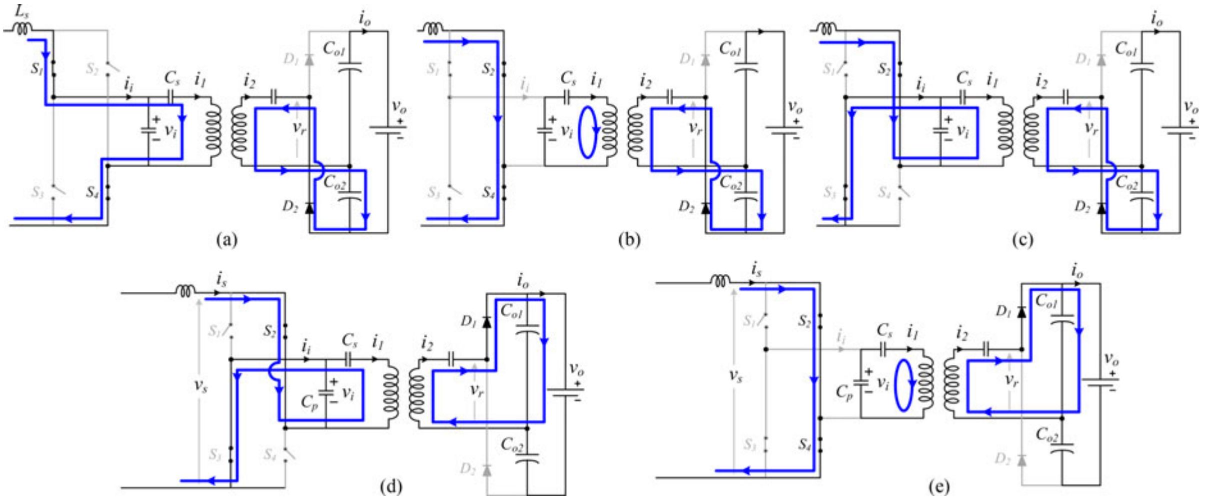


Fig. 5. Equivalent circuit during different intervals of operation.

interval are given as

$$v_{D2} = v_{o1} + v_{o2}, \qquad i_{D1} = i_2 \tag{6}$$

$$C_{o1}\frac{dv_{o1}}{dt} = i_2 - i_o, \qquad C_{o2}\frac{dv_{o2}}{dt} = -i_o. \tag{7}$$

Interval 5 $(t_7 - t_{11})$*:* At instant t_7, S_{4P} is triggered and the interval $t_7 - t_{11}$ is switching overlap period. Similar to interval 2, switch S_{4P} immediately commutates S_{3P} because of the positive voltage present across S_{4P}. Therefore, S_{4P} experiences hard turn-on at instant t_7 and S_{3P} experiences ZCS turn-off at instant t_8. It is clear that S_{1P} and S_{3P} experience both turn-on and turn-off soft switching, whereas both S_{2P} and S_{4P} experience hard turn-on and hard turn-off. The equivalent circuit of the converter during interval t_7–t_{11} is shown in Fig. 5(e). The steady-state operation of the converter circuit repeats in this order.

III. CONVERTER DESIGN

In this section, a general converter design procedure is reported and later a specific design example is presented. For a conventional transmitter parallel and receiver series tank network, the required compensation capacitances to achieve ZPA at ac–ac converter output are derived as [19]

$$C_2 = \frac{1}{\omega_o^2 \times L_2} \tag{8}$$

$$C_p = \frac{L_1}{\frac{\omega_o^4 M^4}{R_{oeq}^2} + \omega_o^2 L_1^2} \tag{9}$$

where ω_o is the resonance frequency in rad/s, L_1, L_2, and M are self-inductances of TC, RC, and mutual inductance of the coils, respectively. R_{oeq} is equivalent load resistance at the ac side of the rectifier. However, in the proposed topology, one extra capacitor is connected in series with TC to improve the performance of the conventional transmitter parallel and receiver series compensated IPT circuit. Therefore, in the presence of a series capacitor C_s, the required parallel capacitor value modifies as

$$C_p = \frac{L_1 - \frac{1}{\omega_o^2 \times C_s}}{\frac{\omega_o^4 M^4}{R_{\mathrm{oeq}}^2} + \omega_o^2\left(L_1 - \frac{1}{\omega_o^2 \times C_s}\right)^2}. \tag{10}$$

In this paper, the value of series capacitor C_s is chosen such that at resonance frequency the effective value of impedance offered by TC self-inductance becomes half. Therefore, the simplified value of parallel capacitor becomes

$$C_p = \frac{0.5 L_1}{\frac{\omega_o^4 M^4}{R_e^2} + 0.25\omega_o^2 L_1^2}. \tag{11}$$

Applying Kirchhoff's current law (KCL) at the RC side of the converter equivalent circuit shown in Fig. 3(b), the rectifier input current in terms of output current is derived as

$$I_2 = \frac{\pi}{\sqrt{2}}.I_o. \tag{12}$$

Applying power balance between output and input of the rectifier and using (12), the rectifier input ac voltage rms is derived as

$$V_r = \frac{2\sqrt{2}}{\pi} \times \frac{V_o}{2} = \frac{\sqrt{2}}{\pi}.V_o. \tag{13}$$

Since this RC-side rectifier is a passive rectifier, the voltage V_r and current I_2 are in same phase and these phasors are considered as reference phasors. Referring to the coupled inductor equivalent circuit of the coupled IPT coils, as shown in Fig. 3(b), and applying Kirchhoff's Voltage Law (KVL) at the RC-side loop, the TC current is derived as

$$I_1 = -j\frac{V_r}{\omega_o M}. \tag{14}$$

Using this current expression and adding the induced voltage in TC due to RC current, the TC voltage is derived as

$$V_1 = \frac{L_1}{M}V_r - j\frac{\omega_o M}{R_{\mathrm{oeq}}}V_r. \tag{15}$$

Using (14) and (15) and applying KVL and KCL at the TC tank network, the ac–ac converter output voltage and current are

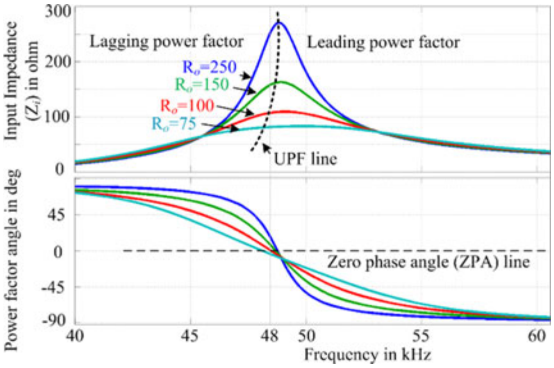


Fig. 6. Variation of tank network input impedance with switching frequency.

derived as

$$V_i = \left(\frac{L_1}{M} - \frac{1}{\omega_o^2 M C_s}\right) V_r - j\frac{\omega_o M}{R_{oeq}} V_r \tag{16}$$

$$I_i = \frac{\omega_o^2 M C_p}{R_{oeq}} V_r + j\frac{V_r}{\omega_o M}\left(\omega_o^2 C_p L_1 + \frac{C_p}{C_s} - 1\right). \tag{17}$$

A. Soft Switching

Referring to the steady-state operation, to achieve ZVS turn-on and ZCS turn-off of converter switches S_1 and S_3, the operating power factor of ac–ac converter output is required to be lagging. Therefore, it is important to know the operating power factor of a converter. From Fig. 3(b) equivalent circuit, the impedance at the input of tank network is derived as

$$Z_i = \frac{1}{j\omega C_p} // \left[\left\{j\omega\left(L_1 - M\right) + \frac{1}{j\omega C_p}\right\} + \left\{j\omega M // \left(j\omega\left(L_2 - M\right) + \frac{1}{j\omega C_p} + R_{oeq}\right)\right\}\right]. \tag{18}$$

Fig. 6 shows the variation of tank network input impedance and phase angle with change in the operating frequency. It is clear that below the resonance frequency, the operating power factor is lagging, and on the other side it is leading power factor. This is an advantage of this tank network that the lagging power factor operation is achieved below the resonance frequency, whereas for series *LC* tank, it occurs above the resonance frequency.

B. Design Example

Referring to Fig. 3(b) equivalent circuit, the total volt-amp transferred from transmitter to RC is given as

$$\mathrm{VA}_{\mathrm{TC-RC}} = \left(-j\omega_o M I_2\right) \times I_1. \tag{19}$$

Using (12), the real power transferred from TC to RC is derived from (19) as

$$P_{\mathrm{TC-RC}} = \frac{\pi}{\sqrt{2}}\,\omega M I_o I_1. \tag{20}$$

TABLE II
CIRCUIT PARAMETERS

Parameters	Selected Values
Input voltage, V_{ac}	200 V ac, 60 Hz
Rated output power	1200 W
Switching frequency	48 kHz
TC coil inductance, L_1	132 μH
RC coil inductance, L_2	137 μH
Mutual inductance, *M*	29.5μH
Tank capacitors, C_p, C_s, C_2	1 55 nF, 155 nF, 82 nF
Input inductor, L_s	1.3 mH
Input filter capacitor, C_f	2.2 μF
Output capacitors, C_{o1}, C_{o2}	5 μF
Output voltage	270 V dc
Inner loop controller, H_i	$\frac{0.3}{s/15\,000+1}$
Outer loop controller, H_o	$25/s$

From (20), it is clear that the amount of real power transferred wirelessly from coil to coil is directly dependent on operating frequency, coil mutual inductance, and TC coil current. Generally, during design of the converter, the rated real power transfer is given and output current I_o is calculated using it. Therefore, with given switching frequency, only two design parameters are unknown, i.e., M and TC coil current I_1. In the reported IPT converter, designs generally choose a suitable value of TC coil current based on litz wire current carrying capacity. This selection directly impact on mutual inductance and IPT pad size. Once the mutual inductance is known, the coil self-inductance is determined from the actual coil. Generally, for a given M, the longer airgap distance leads to larger IPT coil and for shorter airgap the coil size is smaller. The remaining tank circuit parameters and voltage and current ratings of converter switches and diodes are calculated from the general expressions presented before. The maximum switching frequency current ripple of the input ac inductor L_s is possible when the converter operates at full duty cycle and input ac voltage is at peak value. Therefore, the inductance of input inductor is given as

$$L_s = \frac{\sqrt{2}\, V_{\mathrm{ac}} \times T_s}{2\Delta I_s} \tag{21}$$

where $T_s = 1/f_s$ and ΔI_s is the peak-to-peak current ripple in inductor L_s current. Also, the capacitances of output capacitors are calculated as

$$C_{o1} = C_{o2} = \frac{T_s/2 \times I_o}{\Delta V_{o1}} = \frac{T_s/2 \times I_o}{\Delta V_{o2}} \tag{22}$$

where ΔV_{o1} and ΔV_{o2} are peak-to-peak voltage ripple across capacitor C_{o1} and C_{o2}, respectively. The input inductor L_s is calculated considering a 20% ripple in inductor current and output capacitors C_{o1} and C_{o2} are calculated considering 5% switching frequency ripple at output voltage V_o. Table II lists the designed circuit parameters for a 1.2-kW IPT system with a supply voltage 200 V, 60 Hz ac. This system is used later for experimental verification.

IV. PROPOSED CONTROL TECHNIQUE

The proposed IPT topology is controlled through the two-loop control method. From the steady-state operation, it is clear that the basic operation of this ac–ac converter is similar to a boost converter. When switches in same leg are $\mathrm{O_N}$ simultaneously, i.e., either $S_1 - S_3$ or $S_2 - S_4$ are $\mathrm{O_N}$, it is similar to

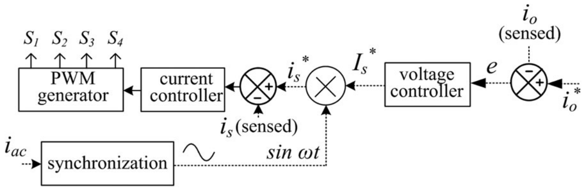


Fig. 7. Block diagram of complete control loop.

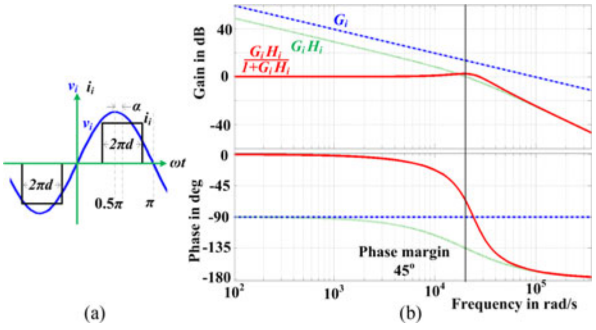


Fig. 8. (a) AC–AC converter output voltage and current waveforms. (b) Bode plot of inner current loop.

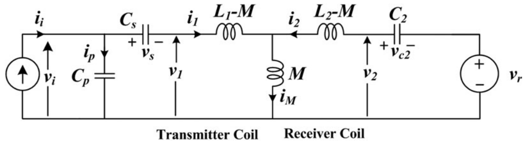


Fig. 9. Transformer equivalent circuit of the tank network.

boost converter switch turn-on interval. Similarly, when either diagonal $(S_1 - S_4)$ or off-diagonal $(S_2 - S_3)$ switch pairs are $\mathrm{O_N}$ then the converter input gets directly connected to the output capacitor and it is equivalent to boost converter turn-off time interval.

The outer output current loop is used to regulate the converter output current, whereas the inner input inductor current loop is used to achieve UPF at ac–ac converter input. The detailed control loop diagram is presented Fig. 7. The input voltage polarity determines which switch set will be triggered. When input voltage polarity is positive, switches $S_{1P} - S_{4P}$ are triggered and similarly $S_{2N} - S_{4N}$ are triggered when input voltage is negative.

C. Inner Input Current Control Loop

The input of the inner loop is duty cycle and output is source-side inductor current i_s. The dynamic expression of inductor current for a switching cycle is given as

$$L_s \frac{di_s}{dt} = v_{\text{ac}} - v_s \tag{23}$$

where v_{ac} is source voltage and v_s is voltage at ac–ac converter input. All these state variables are considered to be average value over a converter switching cycle. Fig. 8(a) shows typical voltage and current waveform at ac–ac converter output. Considering the duty cycle of the ac–ac converter switch S_1 is "d" $(0 \leq d \leq 0.5)$, the converter average input voltage in terms of output rms voltage is derived as

$$v_s = \frac{2\sqrt{2}}{\pi} V_i \times \cos\alpha \times \sin\pi d \tag{24}$$

where α is power factor angle at ac–ac converter output. Since the resonant tank is designed such that the ac–ac converter output power factor is close to unity. Therefore, for simplicity in derivation, cos α is considered unity. Considering small perturbations $(\tilde{i}_s, \tilde{v}_{\text{ac}}, \tilde{V}_i, \tilde{d})$ around the equilibrium points $(i_s, v_{\text{ac}}, V_i, d)$

$$L_s \frac{d\left(i_s + \tilde{i}_s\right)}{dt} = \left(v_{\text{ac}} + \tilde{v}_{\text{ac}}\right) - \frac{2\sqrt{2}}{\pi}\left(V_i + \tilde{V}_i\right) \times \sin\pi\left(d + \tilde{d}\right). \tag{25}$$

Therefore, applying Laplace transformation, the control to output transfer function for inner loop is derived as

$$G_i\ (s) = \frac{\tilde{i}_s\,(s)}{\tilde{d}\,(s)} = -\frac{2\sqrt{2}\,V_i\cos\pi d}{\pi} \times \frac{1}{sL_s}. \tag{26}$$

For a typical value of converter output voltage and duty cycle obtained from the steady-state operation, the frequency response of G_i is plotted in Fig. 8(b). A first-order transfer function H_i is used to get a phase margin around 45° and 40 dB attenuation at switching frequency. Fig. 8(b) shows the bode plot of compensated plant transfer function $G_i H_i$ and closed-loop transfer function $G_i H_i/(1 + G_i H_i)$. The gain crossover frequency is around 11 k rad/s and this indicates that the closed-loop settling time is around 0.36 ms.

D. Outer Output Voltage Control Loop

The input to this outer loop is line frequency ac current i_s and the output is output voltage for resistive load or output current for a battery load. For simplicity, the outer loop plant transfer function is split as

$$G_o\ (s) = \frac{i_o\,(s)}{v_r\,(s)} \times \frac{v_r\,(s)}{i_i\,(s)} \times \frac{i_i\,(s)}{i_s\,(s)}. \tag{27}$$

In (27), the three parts represent rectifier, resonant tank, and ac–ac converter transfer functions, respectively. To derive the voltage gain of the tank, a transformer equivalent circuit of the tank network is drawn, as shown in Fig. 9. From Fig. 9, the voltage across magnetizing inductance is derived as

$$V_M = V_r - I_2\,Z_2 = V_r - \frac{V_r}{R_{oeq}} Z_2 \tag{28}$$

where $s = j\omega$ and R_{oeq} is equivalent load resistance at the input of voltage doubler circuit. Applying power balance at the input and output of voltage doubler circuit, R_{oeq} in terms of output resistance is calculated as

$$R_{oeq} = \frac{2}{\pi^2} \cdot \frac{V_o}{I_o} = \frac{2}{\pi^2} R_o \tag{29}$$

$$Z_2 = s\,(L_2 - M) + \frac{1}{sC_2}. \tag{30}$$

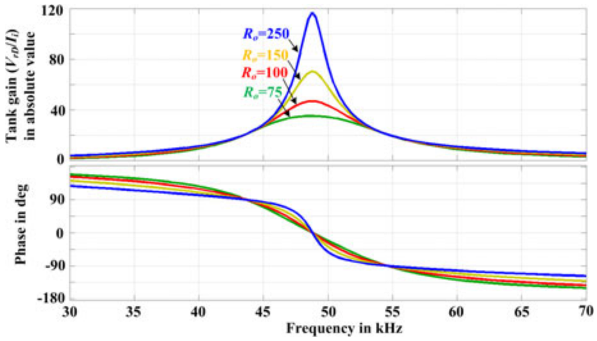


Fig. 10. Frequency response of the tank network.

Therefore, using (28), the current-fed converter output voltage is derived as

$$V_i = V_r\left(1+\frac{Z_2}{R_{\text{oeq}}}\right)+V_r\left\{\frac{1}{sM}\left(1+\frac{Z_2}{R_{\text{oeq}}}\right)+\frac{1}{R_{\text{oeq}}}\right\}Z_1 \tag{31}$$

where

$$Z_1 = s\left(L_1 - M\right) + \frac{1}{sC_s}. \tag{32}$$

The voltage gain expression of the tank network is (V_r/V_i). However, the input to the tank network is actually I_i. Thus, the gain of the tank network is (V_r/I_i) and it is derived as

$$I_i = sC_pV_i + I_1 = V_r\left[(1+sC_pZ_1)\left\{\frac{1}{sM}\left(1+\frac{Z_2}{R_{\text{oeq}}}\right)+\frac{1}{R_{\text{oeq}}}\right\}+sC_p\left(1+\frac{Z_2}{R_{\text{oeq}}}\right)\right]. \tag{33}$$

Fig. 10 shows the gain (V_r/I_i) and phase $(\angle V_r/I_i)$ plot of the tank network of the proposed converter for different equivalent load resistances.

The dynamic expressions of the output capacitors are given as

$$C_{o1}\frac{dv_{o1}}{dt} = 0.5\left\langle i_2\right\rangle - i_o \tag{34}$$

$$C_{o2}\frac{dv_{o2}}{dt} = 0.5\left\langle i_2\right\rangle - i_o \tag{35}$$

where C_{o1} and C_{o2} are two output capacitors and v_{o1} and v_{o2} are their voltages, respectively. All these state variables are average values over a converter switching cycle. Since i_2 is switching frequency ac quantity and its average value over a switching cycle is zero, half-cycle average of i_2 as $\langle i_2\rangle$ is considered here. Considering $C_{o1} = C_{o2} = C_o$, the dynamic expression is derived by adding (34) and (35) as

$$C_oR_o\frac{di_o}{dt} = \frac{\langle v_r\rangle}{R_{\text{oeq}}} - 2i_o. \tag{36}$$

Applying Laplace transformation, the gain expression is derived as

$$\frac{i_o(s)}{\langle v_r\rangle(s)} = \frac{\pi^2}{8R_o}\times\frac{1}{sC_oR_o+2}. \tag{37}$$

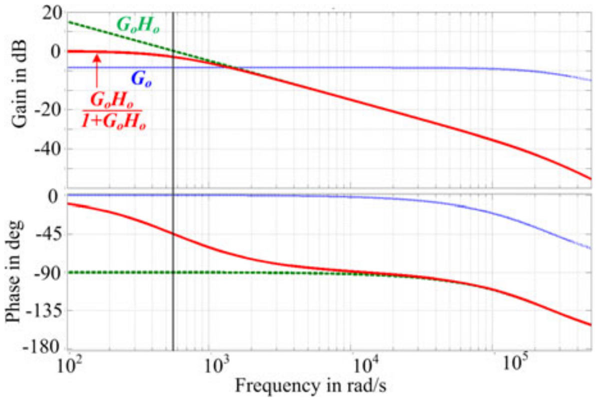


Fig. 11. Bode plot of outer loop.

The ac–ac converter output current i_i is a quasi-square wave with an amplitude of i_s, as shown in Fig. 8(a). Extracting fundamental component from the Fourier series of i_i, the ac–ac converter output to input current gain expression is given as

$$\langle\, i_i \rangle = \frac{8}{\pi^2}\, i_s \sin \pi d. \tag{38}$$

Therefore, the overall system transfer function is derived as

$$G_o\ (s) = \frac{k}{R_o}\ \sin \pi d \times \frac{1}{sC_oR_o+2} \tag{39}$$

where k represents tank gain at operating switching frequency and it is obtained from Fig. 10. The bode plot of the plant transfer function is shown in Fig. 11. A simple integrator listed in Table II is used to get gain crossover frequency around 5.5 rad/s and attenuation to second harmonic (120 Hz) around 40 dB. This design indicates a closed-loop settling time around 0.75 s.

V. EXPERIMENTAL RESULTS AND DISCUSSIONS

The detail circuit parameters for a 1.2-kW lab-prototype are listed in Table II. The ac–ac converter switches are MOSFETs with manufacturer part number C2M0080120D. The tank capacitors are all Epcos make 700 V rms film capacitors. The IPT coils are circular type and the airgap between the TC and RC is around 25 cm. The major focus of this paper is to verify the performances of the proposed converter and not the IPT coil design; therefore, the details of circular coil design are not included here and it can be found in [17], [19], [25], and [34]. It is already proven that the leakage flux can be kept well within the specified limit with the use of proper aluminum shielding [34]. However, when this IPT pad is used for direct ac–ac converter, there might be some low frequency (60 Hz, 120 Hz) flux present around the coil surroundings. Nonetheless, from fundamental point of view, this pulsating low-frequency leakage flux cannot impact any object when the switching frequency leakage flux is kept within regulated limit. This is because the rms values of induced voltage in this foreign object due to TC and RC are given as

$$V_{1\text{F}} = 2\pi f M_{1\text{F}} I_1 \quad \text{and} \quad V_{2\text{F}} = 2\pi f M_{2\text{F}} I_2 \tag{40}$$

respectively, where M_{1F} and M_{2F} are mutual coupling of the foreign object with TC and RC, respectively, and f is frequency of pulsating flux. Therefore, the impact of this low-frequency

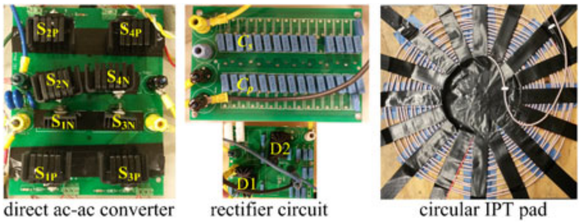


Fig. 12. Experimental setup.

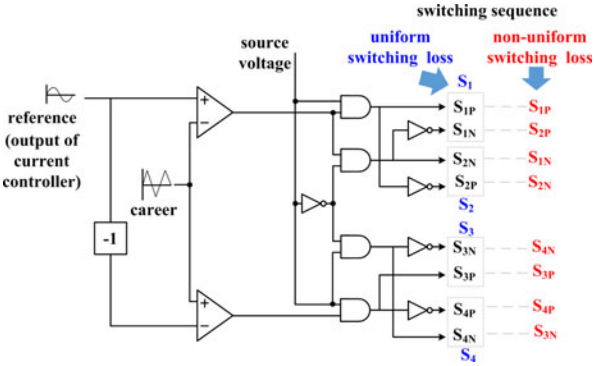


Fig. 13. Switching sequence logic for uniform switching loss distribution.

pulsating magnetic field is about 1000 times lower than the switching frequency field. It is similar to a conductor that carries the line frequency current and a low-frequency magnetic field exists around the conductor. This does not have significant impact on regular devices working nearby.

The rectifier-side diodes are 400 V fast recovery diodes and manufacturer part number is SCS215KGC. The ac–ac converter MOSFETs are driven with Semikron make SKHI 61(R) gate driver with rated switching frequency 50 kHz. Fig. 12 shows the experimental setup and a 60 cm diameter circular coil.

From practical implementation point of view, nonuniform power loss distribution leads to uneven structure of the converter in terms of heat sink design. Therefore, a simple logic circuit can be used such that during positive half-cycle of line frequency the switches S_1 and S_3 experience soft switching and during negative half-cycle S_2 and S_4 experience soft switching. Therefore, this will make the converter size regular and suitable for practical implementation. Fig. 13 shows this logic structure where the usual switching sequence is shown in red color and it leads to soft switching of S_1 and S_3 and hard switching of S_2 and S_4, repeatedly. However, during the negative half of input voltage the switching sequence can be interchanged, as shown with blue color in Fig. 13, leading to uniform switching loss distribution among all the four sets of devices.

Fig. 14 shows typical gating signals of the proposed ac–ac converter switches when duty cycle of S_1 (or S_3) is $D = 0.35$. The overlap duration between the complementary gating signals S_1 and S_2 is around 250 ns and this is enough to turn ON and turn OFF the MOSFETs. Figs. 15–20 show experimental results of the converter when the load is resistive, whereas Figs. 21–24 show results when load is stiff dc voltage. Since all the results have a line frequency and switching frequency components, line frequency views are shown in the middle figures, whereas switching frequency views of the waveforms are shown in two sides. The zoomed view in the left side of every figure shows zoomed view at line frequency peak, whereas the right-side figure shows zoomed view at off-peak of line frequency.

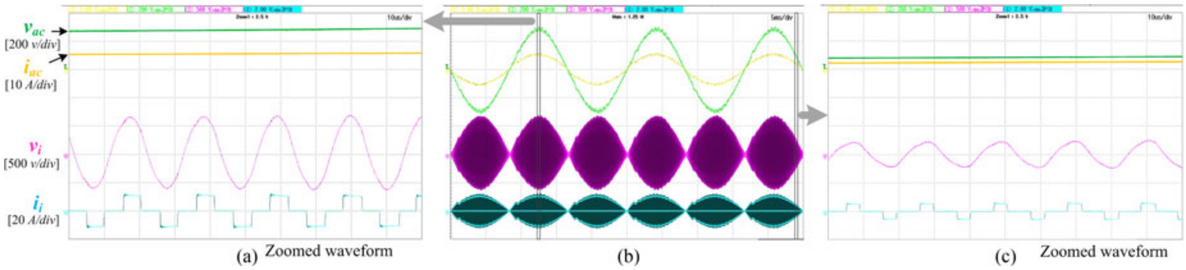
Fig. 14. Gate pulse sequence.

Fig. 15 shows experimental results of source voltage, current, ac–ac converter output voltage and current for 1200 W power output, and corresponding input voltage is 200 V, 60 Hz ac and output voltage is 300 V dc. Since ac–ac converter input current predominantly contains line frequency and switching frequency components, the small input filter is sufficient enough to filter out the switching frequency components. The total harmonic distortion (THD) of the source current is around 4.0% and it is well within the IEEE 519–1992 specified standard (5%). From Fig. 15(a) and (c) zoomed waveform, it is clear that the ac–ac converter output current waveform is a quasi-square but the voltage is very close to sinusoidal.

Fig. 16 shows the voltage and current waveforms of both the transmitter and RCs. In Fig. 16(a) and (c), zoomed waveforms show switching frequency view at around source voltage peak (90°) and 45° from zero crossing, respectively. Due to the presence of parallel capacitor, the TC coil voltage and current profiles are very close to sinusoidal. Compare with parallel capacitor in conventional parallel *LC* tank, the parallel capacitor C_p in the proposed *CCL* tank offers much lower impedance to higher order harmonics. This is because the capacitance value of C_p in the *CCL* tank is approximately twice than that of simple parallel *LC* tank.

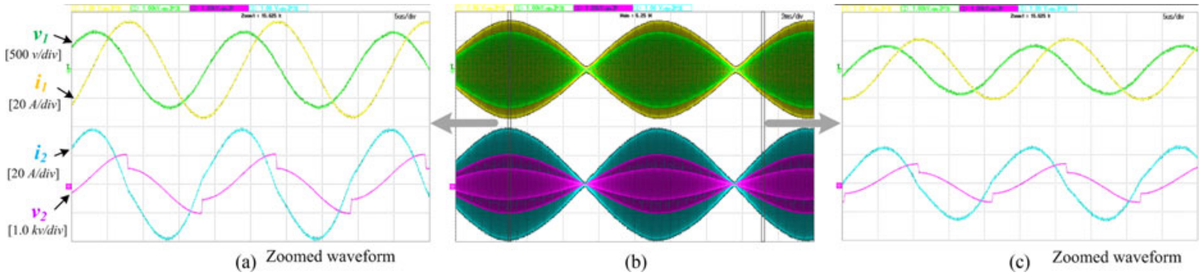
Fig. 17 shows gating signal of S_{1P} and voltages across TC-side tank elements. These results show the advantage of *CCL* tank network over simple parallel *LC* tank. Without the presence of series capacitor C_s, the converter switches would get directly TC coil voltage that is quite high [13]. Fig. 18 shows input and output voltages and currents of the proposed *CCL* primary and *LC* series secondary tank network. The operating power factor at the ac–ac converter output is lagging and it is suitable for the soft-switching operation. Also, in the receiver side, the rectifier diodes turns ON and turns OFF at zero current. This ensures zero reverse recovery of these rectifier diodes.

Fig. 19 shows soft-switching performance of converter switches S_{1P} and S_{3P}. In lagging power factor, switch S_{1P} is triggered when voltage across switch S_1 is negative and this negative voltage is blocked by S_{1N}. Therefore, switch S_{1P} does not start conducting immediately and this results ZVS of S_{1P}. However, after the overlap period, the complementary switch of S_1, i.e., S_2 is turned OFF and S_1 is forced to take the input current i_s. Also, before turn-off of S_1, the complementary switch S_2 is triggered to maintain required overlap. Since voltage across S_2 is positive, S_2 immediately commutates S_1. Thus, switch S_1



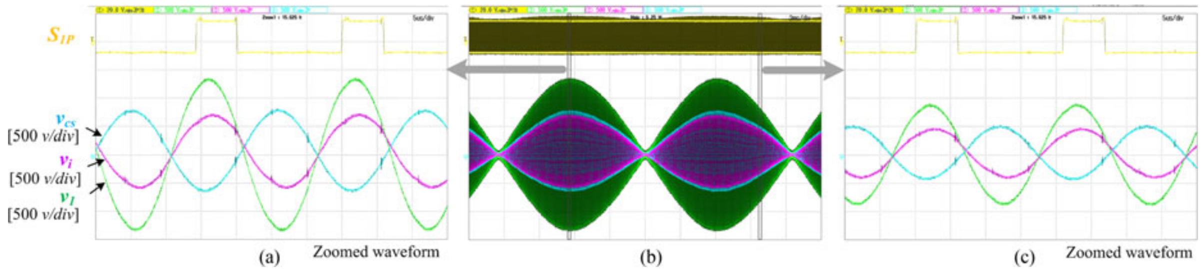
(a) Zoomed waveform (b) (c) Zoomed waveform

Fig. 15. Experimental results of grid voltage, current, and ac–ac converter output voltage and current waveforms when $V_{\mathrm{ac}} = 200\ \mathrm{V\,ac}$, $P_o = 1.2\ \mathrm{kW}$, and $V_o = 300\ \mathrm{V}$. (a) Zoomed view at line frequency peak, (b) line frequency view, and (c) zoomed view at off peak of line frequency.



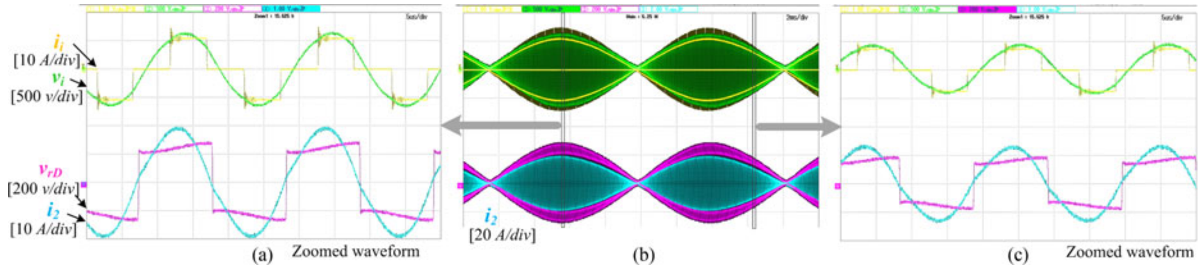
(a) Zoomed waveform (b) (c) Zoomed waveform

Fig. 16. Experimental results: transmitter and RC voltages and currents when $V_{\mathrm{ac}} = 200\ \mathrm{V}$ ac, $P_o = 1.2\ \mathrm{kW}$, and $V_o = 300\ \mathrm{V}$.



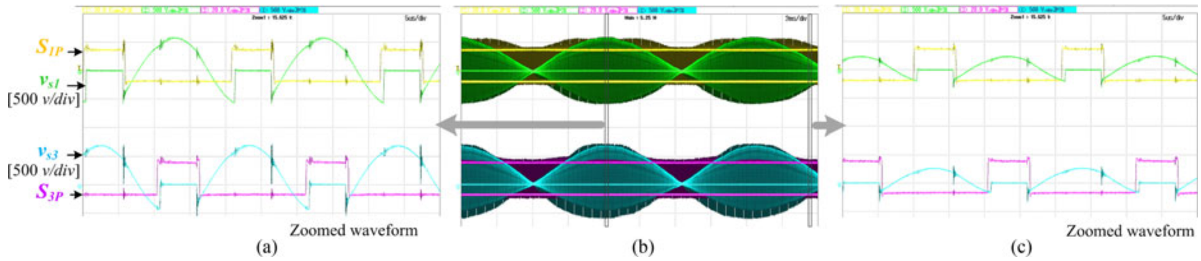
(a) Zoomed waveform (b) (c) Zoomed waveform

Fig. 17. Experimental results: gate pulse of switch S_{1P} and voltages across different elements (C_s, C_p, TC) in the TC-side tank network.



(a) Zoomed waveform (b) (c) Zoomed waveform

Fig. 18. Experimental results: input and output voltages and currents of the resonant tank network.



Zoomed waveform (a) (b) Zoomed waveform (c)

Fig. 19. Experimental results: Soft switching of ac–ac converter switches S_{1P} and S_{3P}.

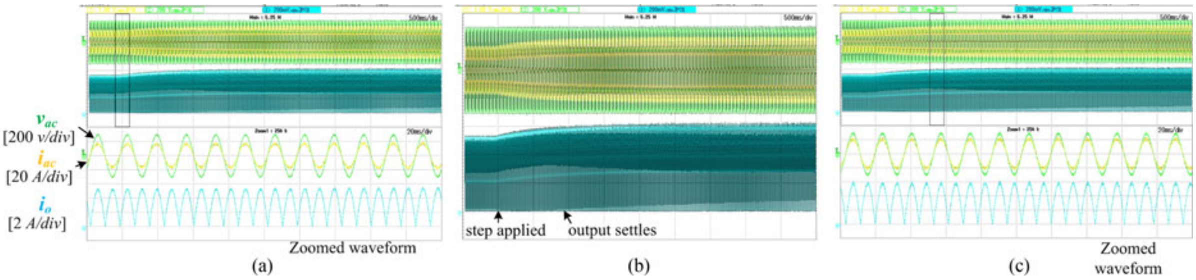


Fig. 20. Dynamic response of the proposed converter for a load step from 70% of rated load to rated load.

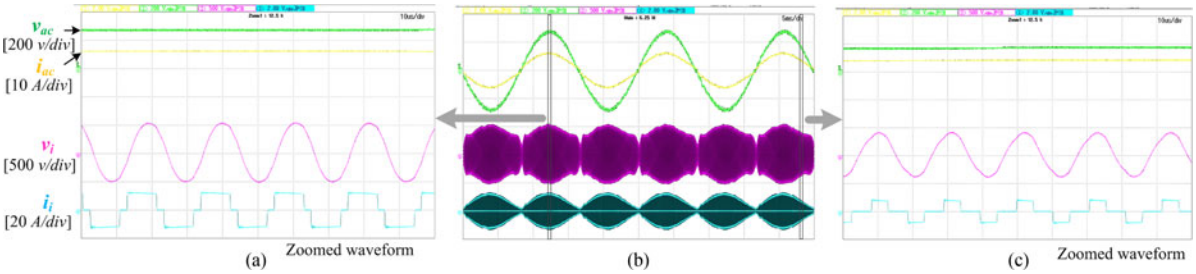


Fig. 21. Experimental results of grid voltage, current, and ac–ac converter output voltage and current waveforms when $V_{\mathrm{ac}} = 200\ \mathrm{V\,ac}, P_o = 1260\ \mathrm{W}$, and $V_o = 270$ V stiff dc. (a) zoomed view at line frequency peak, (b) line frequency view, and (c) zoomed view at off peak of line frequency.

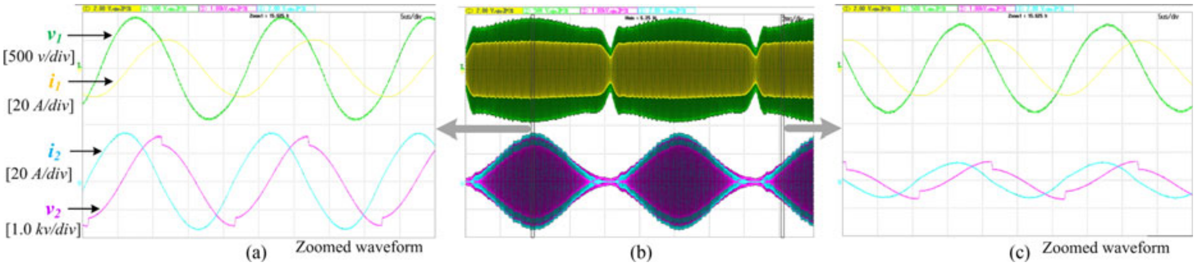


Fig. 22. Transmitter and RC voltages and currents when $V_{\mathrm{ac}} = 200\ \mathrm{V\,ac}, P_o = 1.2$ kW, and $V_o = 270$ V stiff dc.

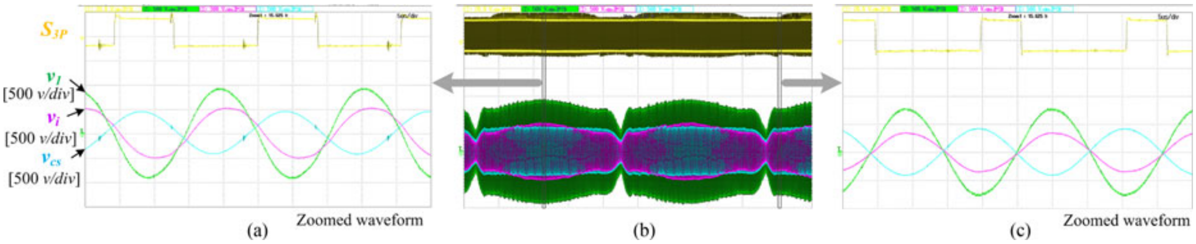


Fig. 23. Gate pulse of switch S_{3p} and voltages across different elements (C_s, C_p, TC) in the TC-side tank network.

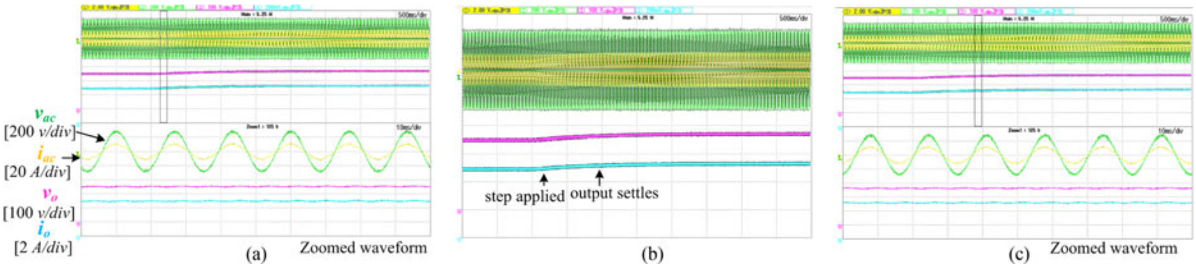


Fig. 24. Dynamic performance of the converter for a step change in output current reference from 4.4 to 5.5 A.

turns OFF at zero current. During this operation, switch S_2 experiences hard switching during both turn-on and turn-off. Similar soft-switching turn-on and turn-off characteristics are obtained for switch S_3, as shown in Fig. 19.

Fig. 20 shows dynamic response of the converter when a load step commends form 70% of rated load (0.84 kW) to rated load (1.2 kW) is applied. The outer loop fulfills the load requirements while inner input current loop ensures the high-quality source current. The load current settles at around 0.75 s and this verifies the dynamic model of the converter. Since there is no bulky electrolytic capacitor to filter out the second harmonic, the load current contains second harmonics. These results are significant when the load is resistive.

When living object detection function detects an intrusion into the active region then the load power must be reduced abruptly from full load to light load. This control command can be directly applied to inner input current control loop for faster response and safety. Although the current quality deteriorates at light load but total demand distortion is calculated to be 4.6% and it is well within the IEEE 512-1992 standards. There are several techniques to improve the performance of the converter at light load similar to boost-derived PFCs, such as on/off control and digital phase leading filter current compensation. [36]–[38]. However, these topics are another broad area of research, therefore, it can be considered as future research.

Literature study shows that this rectified sinusoidal current is acceptable for several battery charging applications [35]. However, in case the load does not accept this current profile then a reasonable size dc capacitor can be connected at the output of the converter. This study shows that the converter is capable to deliver power in either cases.

To verify the performance of the converter for battery charging applications a stiff dc voltage load is connected at the converter output. Fig. 21 shows experimental results of grid voltage, current, and ac–ac converter output voltage and current waveforms when $V_{\mathrm{ac}} = 200V$ ac, $P_o = 1260$ W, and $V_o = 270$ V fixed dc. The THD of this current is calculated to be around 4.5% and it is well within the IEEE 519-1992 specified standards. From Fig. 21(a), it is seen that unlike resistive load, here the ac–ac converter output voltage does not follow line frequency sinusoidal envelope. This voltage does not reduce significantly toward the zero crossing of line frequency. This is because the load is stiff dc voltage and to pump the charge to this high dc voltage around line frequency zero crossing, the TC side has to maintain significant amount of voltage. This fact is evident from Fig. 21(a) and (c) zoomed waveform of i_i that toward zero crossing the boosting feature of ac-ac converter becomes high. This phenomenon of the converter is very similar to boost-derived PFCs. Also, from steady-state operation interval II, it is clear that current through S_1 is transferred to S_2 before the gate pulse of S$_1$ is withdrawn. Therefore, S_1 experiences soft turn-off and S_2 experiences hard turn-on. Again, in interval II of steady-state operation, the device S_4 keeps on conducting when S_3 is given getting pulse. This leads to soft turn-on of S_3 and hard turn-on of S_4.

Fig. 22 shows TC and RC voltages and current profiles. Similar to earlier results, the TC coil receives very high-quality sinusoidal current. As discussed, the TC-side coil voltage and current envelope does not follow the sinusoidal trend of the line frequency because of stiff dc output voltage. Fig. 23 shows gating signal of switch S_{2P} and voltages across TC tank network elements. Similar to earlier, the magnitude of voltage across parallel capacitor V_i is a fraction of TC voltage V_1 because of the presence of series capacitor C_s. Since V_i directly determines the ac–ac converter switch voltage stress, therefore, *CCL* tank is superior in terms of inverter switch voltage rating. Fig. 24 shows dynamic performance of the converter when a step change in load current reference is given from 4.4 to 5.5 A. The outer output current loop is capable to meet load demand within the designed settling time, i.e., around 0.75 s, while the inner loop maintains the high-quality source current.

VI. CONCLUSION

The contribution and focus of this paper is to propose, analyze, and develop a new power electronics system using the direct ac–ac converter for WPT applications. Compare with the existing buck-derived ac–ac converters for IPT systems, the proposed ac–ac converter topology is boost derived. This ac–ac converter is fed from a current source; therefore, it is very much similar to boost-derived PFC topology. This enables us to achieve the high-quality source current by controlling the source inductor current. To match compatibility between ac–ac converter and tank network, a parallel–series (*CCL*) tank network in the TC side is selected. This *CCL* tank improves the overall performance of the converter viz., lower switch voltage stress and high-quality TC current. The proposed two-loop control scheme is simple and capable of meeting all the control goals viz., load power demand and source current control and soft switching of inverter switches. Detail of the steady-state operation, dynamic model, and design of converter circuit is reported. However, coils or magnetics design is not the focus of this paper. The experimental results obtained from a 1.2-kW proof-of-concept scale down lab-prototype verifies the analysis and performance of the proposed converter.

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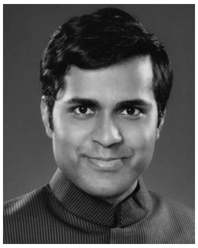
Suvendu Samanta (S’16) received the B.E. degree from the Indian Institute of Engineering Science and Technology Shibpur (formerly Bengal Engineering and Science University), Howrah, India, in 2009, and the M.Tech. degree from Indian Institute of Technology Kanpur, Kanpur, India, in 2013, both in electrical engineering. He is currently working toward the Ph.D. degree in the Department of Electrical and Computer Engineering (ECE), Concordia University, Montreal, QC, Canada.

He was with Coal India Ltd. as a Operation and Maintenance Engineer of Electrical and Mechanical Section from 2009 to 2011. From April 2014 to April 2016, he was a Research Engineer in the ECE Department, National University of Singapore, Singapore. His research interests include modeling and control of power electronic converters especially in wireless power transfer applications.



Akshay Kumar Rathore (M’05–SM’12) received the M.Tech. degree from the Indian Institute of Technology (BHU), Varanasi, India, in 2003. He received the Ph.D. degree from the University of Victoria, Victoria, BC, Canada, in 2008.

He had two subsequent Postdoctoral Research Appointments with the University of Wuppertal, Germany, and University of Illinois at Chicago, Chicago, IL, USA. From November 2010 to February 2016, he was an Assistant Professor in the Department of Electrical and Computer Engineering, National University of Singapore, Singapore. He is currently an Associate Professor in the Department of Electrical and Computer Engineering, Concordia University, Montreal, QC, Canada. He has published more than 180 research papers in international journals and conferences including 62 IEEE Transactions. His research is mainly focused on current-fed converters and multilevel inverters. He is leading the area of current-fed power electronics and contributed to analysis, design, and development of new classes of such converters.

Dr. Rathore is an Associate Editor of IEEE Transactions on Industry Applications, IEEE Transactions on Industrial Electronics, IEEE Transactions on Transportation Electrification, IEEE Transactions on Sustainable Energy, and IEEE Journal of Emerging Selected Topics in Power Electronics. He is the Paper Review Chair of the IEEE Transactions on Industry Applications for Industrial Automation and Control. He is a Distinguished Lecturer and the Executive Board Member-at-Large of IEEE Industry Applications Society. He received the Gold Medal during his M.Tech. degree for securing highest academic standing among all electrical engineering specializations, and the University Ph.D. Fellowship and the Thouvenelle Graduate Scholarship during his Ph.D. degree. He also received the 2013 IEEE IAS Andrew W. Smith Outstanding Young Member Achievement Award, 2014 Isao Takahashi Power Electronics Award, and the 2017 IEEE IES Early Career Award.