A Dual Active Bridge Converter With an Extended High-Efficiency Range by DC Blocking Capacitor Voltage Control

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***Abstract*—A Dual active bridge (DAB) converter can achieve a wide high-efficiency range when its input and output voltages are equal, assuming a 1:1 turns ratio for its isolation transformer. If its input or output voltage is doubled, efficiency of the DAB will drop significantly, because of the introduction of the hard switching and high circulating power. Thus, a new modulation scheme has been proposed, whose main idea is to introduce a voltage offset across the dc blocking capacitor connected in series with the transformer. Operational principle of the proposed modulation has been introduced, before analyzing its soft-switching area and circulating power mathematically. The final modulation scheme is not difficult to implement, but can help the DAB achieve soft switching, low circulating power, and thereby high efficiency, even with its input or output voltage doubled. These features have been verified by experimental results obtained with a 1.2-kW prototype.**

***Index Terms*—Circulating power, dual active bridge (DAB) converters, high efficiency, modulation, soft switching.**

I. Introduction

THE dual active bridge (DAB) converter was originally proposed in [1] for high efficiency and high power density applications. Lately, because of its advantages such as bidirectional power flow and galvanic isolation at high frequency, DAB has become a promising interface for solid state transformers, electric vehicles (EVs), medium voltage direct current (MVDC) grids, etc., [2]–[5]. DAB can elementarily be of the voltage-fed (VF) [1]–[24] or current-fed (CF) [25], [26] type, shown in Fig. 1(a) and (b). The former is well known, comprising two full-bridges isolated by a transformer in series with an inductor. The topology is thus simple and symmetrical. In contrast, the latter is essentially a merger of a VF-DAB converter and an interleaved buck–boost converter with two common shared legs. In Fig. 1(b), the shared legs are formed by switches $Q_5' \sim Q_8'$. The sharing permits a CF-DAB converter to have a wider voltage range with soft switching than the VF-DAB converter. The principle behind is to use the buck–boost converter of the CF-DAB converter to provide a flexible voltage ratio, while providing charging/discharging current with a smaller ripple to the battery, considered as an example load in Fig. 1(b). The smoother current is undeniably due to the presence of $L_{\rm DC1}$ and $L_{\rm DC2}$, and is certainly an advantage of the CF-DAB converter. Nevertheless, its drawbacks cannot be ignored.

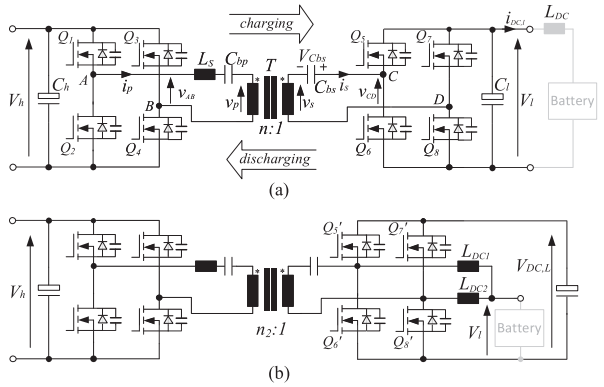

Fig. 1. Illustrations of (a) voltage-fed and (b) current-fed dual active bridge converters.

First, the CF-DAB converter has an asymmetrical structure, which will frequently lead to uneven distribution of current stresses within the common legs. Using notations indicated in Fig. 1(b), it means current stresses experienced by Q_6' and Q_8' will be higher than Q_5' and Q_7'. Soft switching during charging and discharging will hence be, respectively, easier and harder to achieve for Q_6' and Q_8' than Q_5' and Q_7' [25], [26]. Moreover, to achieve the same battery voltage, the low-voltage full bridge of the CF-DAB may need a dc bus voltage higher than that of VF-DAB. It can in fact be doubled, if voltage gain of the buck–boost converter in the CF-DAB is 0.5. Voltage stresses experienced by power devices and dc bus capacitors of the low-voltage full bridge are hence higher, resulting in higher power losses and costs. It is also true that the dc current ripple of VF-DAB to the battery in Fig. 1(a) is larger than that of

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CF-DAB, because of L_{DC1} and L_{DC2} in the latter in Fig. 1(b). But, if a smaller current ripple is necessary for the VF-DAB, an inductor L_{DC} can be connected between C_l and the battery, as also shown in Fig. 1(a). The inductor L_{DC} can physically be smaller than L_{DC1} and L_{DC2}, because of the additional filtering effect contributed by C_l. On the other hand, L_{DC1} and L_{DC2} receive pulsating voltages with duty cycle around 0.5 [24]–[26] from a full bridge. VF-DAB converter is, therefore, still popular [1]–[24], and has hence been chosen for investigation in this paper. Because of that prefix VF will be dropped from here on with DAB referring only to VF-DAB converter.

As for its modulation, the conventional method is the single phase shift (SPS) modulation, which is known to be simple and effective for controlling the amount and direction of power through the DAB [1]. It requires both full bridges to generate square waveforms with 50% duty ratio, and by regulating phase angle between them, power can be controlled. Nevertheless, challenges still exist in terms of maintaining soft switching, even when input or output voltage of the converter varies widely. Such variations typically occur when a DAB is interfaced to the battery of an uninterruptible power supply, EV or static energy storage plant. It is, hence, important to preserve soft switching over a wide voltage range for the DAB, in order to keep power losses of the DAB low, especially with a high switching frequency. Moreover, hard switching may induce a high di/dt, which may cause high voltage spikes to appear across parasitic inductances. In turn, the voltage spikes may damage power semiconductors. It is, therefore, necessary to develop methods for DAB modulation that can guarantee soft switching over a wide voltage range.

One method is to vary the switching frequency, while the DAB is still modulated using SPS. No doubt, simplicity of SPS has been retained [6], but a variable switching frequency will increase complexities associated with electromagnetic interference filter design and other implementation issues. Under light-load conditions, switching frequency of the DAB may also become extremely high, in order to guarantee soft switching. Consequently, most modulation strategies in the literature have retained a fixed switching frequency [7]–[24], while exploring other means for widening the soft-switching range and reducing circulating power in the DAB, in order to increase its efficiency. One technique extended from SPS is to lower the duty ratio of one full bridge to below 0.5. The resulting scheme is referred to as extended phase shift (EPS) modulation [7]–[13], which, as proven, can help the DAB achieve lower current stresses and an improved overall efficiency. But, with only one full bridge having a variable duty ratio, the DAB controlled by EPS exhibits asymmetrical performances during charging and discharging.

To retain symmetry with the same duty ratios set for both full bridges, dual phase shift (DPS) modulation has been proposed [14], [15]. Compared with EPS, no extra complexity has been introduced by DPS, despite its improved performances, which can still be optimized by adding a third control parameter to form the triple phase shift (TPS) modulation [16]–[22]. Control parameters of TPS are, thus, the two independent duty ratios of the two full bridges, and the phase angle between them. These three parameters must be regulated according to the load, input, and output voltages of the DAB, in order to optimize the soft-switching range, reduce current stresses, and thereby increase efficiency of the converter. Their design procedure requires the soft-switching boundaries and circulating power of the DAB to be mapped first. For that, either the current-based [12], [13], [20] or energy-based [7], [9], [11] soft-switching analytical technique can be applied, even though the latter is considered more accurate [22]. Besides, nonlinearity of capacitance has been considered in that technique to further improve accuracy of the soft-switching mapping [22].

During operation, the optimal set of three parameter values can then be obtained from the map, according to the prevailing load, input, and output voltages of the DAB. The map can be realized by a numerical look-up table [21] or an analytical calculation procedure [20], [22]. The former is simple, but a large memory is usually needed for data storage. The latter does not require a memory, but it may be computationally intensive. Nevertheless, implementations of both techniques, and in general, most advanced modulation schemes, are significantly tougher than SPS, because of more control parameters to tune. In contrast, SPS only needs a PI or other regulator for generating an appropriate phase angle from the output voltage, current or power error, depending on the applications. However, SPS can only ensure load-independent soft switching when the DAB output voltage is the same as its input voltage, if a 1:1 isolation transformer is assumed. Otherwise, the desired soft-switching area will shrink significantly.

To avoid the degradation, an improved SPS scheme has been proposed in a conference version of this paper [23]. The idea is to introduce a voltage offset across the dc blocking capacitor, placed in series with the isolation transformer, when the output voltage of the DAB is twice its input voltage. Then, by regulating only the phase angle between the two full bridges, a wide soft-switching range can be obtained without complicating its implementation. Operational principles of the new modulation scheme have been presented in [23], where soft switching and circulating power during charging have been analyzed briefly. In this paper, more scenarios have been considered with more analyses related to soft switching and circulating power provided during charging, as well as discharging. More test results have also been obtained for verification. To better organize the expanded content, Section II of the paper begins by introducing operational principles of the proposed modulation. Soft-switching area mapping is then demonstrated in Section III, before analyzing circulating power in Section IV. Selection of the dc blocking capacitor is discussed in Section V. A comparison of the different modulation schemes is summarized in Section VI. Finally, yet importantly, experimental results obtained from a 1.2 kW prototype are described in Section VII. The paper is concluded in Section VIII.

II. Operational Principles

A DAB converter consists of two full bridges assembled with switches $Q_1 \sim Q_8$, an isolation transformer T with turns ratio of $n:1$, an inductor L_s, two dc blocking capacitors C_{bp} and C_{bs}, and two dc bus capacitors C_h and C_l, shown in Fig. 1(a).

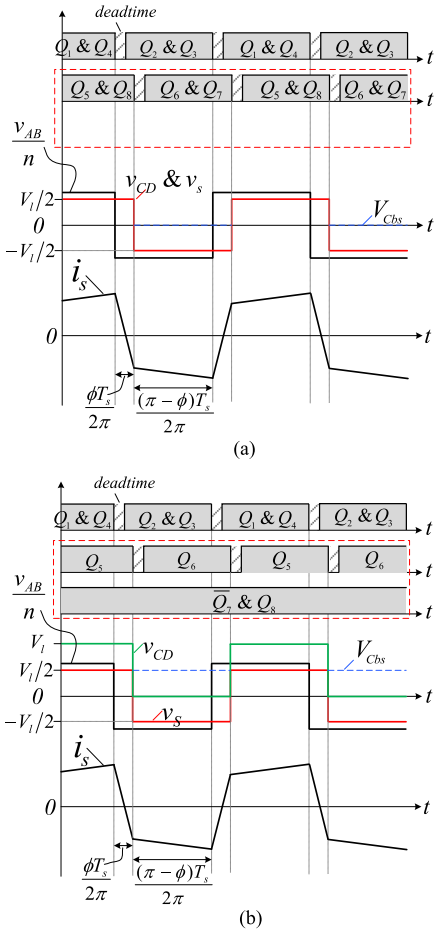


Fig. 2. Gate signals, voltages and currents of DAB controlled by (a) conventional SPS and (b) proposed modulation.

Besides, v_p and v_s are input and output voltages of the transformer, i_p and i_s are primary and secondary currents of the transformer, and v_{AB} and v_{CD} are pulsed voltages at the alternating terminals of the two full bridges. Among the components, C_{bp} and C_{bs} may not be necessary, if an alternative method is included for preventing magnetic saturation of the transformer. Although saturation issues in the DAB has rarely been studied in the literature, there are still a few existing solutions like peak current control [29] and "magnetic ear" [30], [31]. Peak current sampling may however be easily distorted by noises, especially at a high switching frequency. As for magnetic ear, it requires an auxiliary core and an extra circuit [30], [31], which have somehow made it complex. It is, therefore, easier to include dc blocking capacitors C_{bp} and C_{bs}, as illustrated in Fig. 1(a). To control it, conventional SPS scheme for the DAB converter is denoted in Fig. 2(a), where both full bridges are modulated to generate two ac square voltages v_{AB} and v_{CD} with 50% duty ratio each. Since dc offsets of these square voltages are ideally zero, corresponding dc voltage drops across C_{bp} and C_{bs} are also zero. Phase angle between the square voltages can then be regulated for controlling power delivered by the converter. Conventional SPS is thus easy to realize with high efficiency obtained whenever output voltage V_l is close to 1 per unit (p.u.), if reflected input voltage V_h/n is also normalized to 1 p.u. On the other hand, if V_l is increased to 2 p.u., hard switching occurs, causing efficiency to drop and voltage stress to rise. Evidences demonstrating these effects can be found in Sections III and V. To rectify, a new modulation method for addressing V_l close to 2 p.u. is proposed and illustrated in Fig. 2(b), where gate signals of the new scheme are noticed to be nearly similar to those of conventional SPS. The new scheme however keeps Q_7 always OFF and Q_8 always ON, instead of pulse-width modulating them. Terminal D in Fig. 1(a) is thus clamped to the lower dc rail of the output full bridge. Spontaneously, v_{CD} changes from a pure ac voltage to one with a dc component, as seen in Fig. 2(b). Since the duty ratio of v_{CD} is still 50%, the dc component in v_{CD} is simply $V_l/2$.

This dc component will drop across blocking capacitor C_{bs}, implying secondary transformer voltage v_s is still an ac voltage with 50% duty ratio and no dc offset. Its amplitude has however become $V_l/2$. Relying on the same SPS principle, power delivered by the converter can then be controlled by regulating phase angle between v_{AB} and v_s, or v_{AB} and v_{CD}, since v_s and v_{CD} have the same phase. No extra complexity has hence been introduced by the proposed method. Moreover, because v_s has become $V_l/2$ or 1 p.u. whenever V_l is at 2 p.u., performance of the proposed method is comparable to that of conventional SPS when V_l is close to 1 p.u. The same method and dc component can also be introduced across the dc blocking capacitor C_{bp} at the input side whenever the reflected input voltage V_h/n is much higher than the output voltage V_l. The purpose is to again widen the soft-switching range to improve efficiency. Since the concept remains mostly unchanged, especially when applied to the symmetrical DAB topology, related analyses in the next section onwards will only be presented once for the example of $V_l \approx \frac{V_h}{n} = 1$ p.u.

III. Soft-Switching Boundaries

A. Charging Mode

Before efficiency of the DAB can be evaluated, its soft-switching range must be determined. For that, I_1 and I_2 in Fig. 3 must be calculated, since they are among the main factors affecting zero voltage switching (ZVS) of the converter. Three scenarios covering all possibilities caused by different polarities of I_1 and I_2 are thus included for evaluation in Fig. 3. For comparison, the evaluation has also been performed for conventional SPS with zero dc blocking voltage or $V_{Cbs} = 0$ and proposed method with $V_{Cbs} = V_l/2$. Details derived are presented as follows.

-Applying conventional SPS with zero dc component or $V_{Cbs} = 0$

$$\begin{cases} I_2 - \dfrac{\phi T_s * \left(\dfrac{V_h}{n} + V_l\right)}{2\pi \dfrac{L_s}{n^2}} = -I_1 \\ I_2 = I_1 - \dfrac{(\pi - \phi)\, T_s * \left(\dfrac{V_h}{n} - V_l\right)}{2\pi \dfrac{L_s}{n^2}} \end{cases} \tag{1}$$

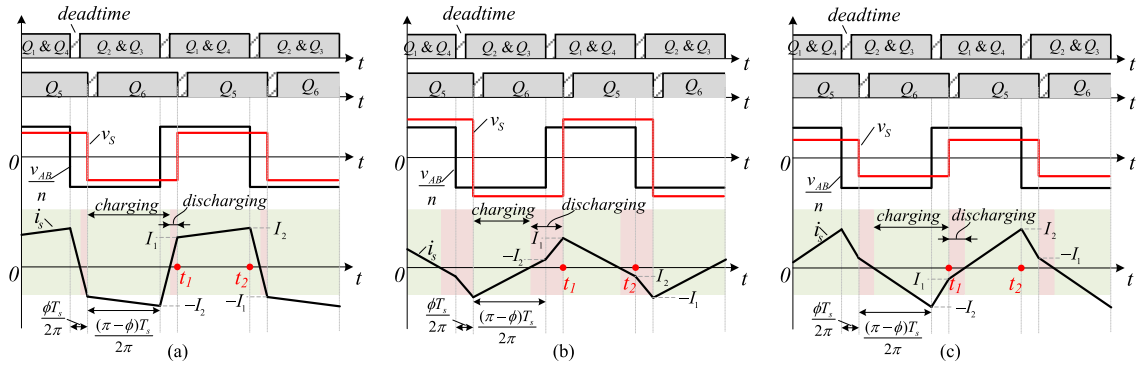


Fig. 3. Gate signals, voltages, and currents of DAB when charged with (a) $I_1 \geq 0$, $I_2 \geq 0$, (b) $I_1 \geq 0$, $I_2 < 0$, and (c) $I_1 < 0$, $I_2 \geq 0$.

$$\begin{cases} I_1 = \dfrac{\pi n^2 V_l - (\pi - 2\phi)\, n V_h}{4\pi f_s L_s} \\ I_2 = \dfrac{\pi n V_h - (\pi - 2\phi)\, n^2 V_l}{4\pi f_s L_s} \end{cases}. \tag{2}$$

By solving simple trigonometry common to Fig. 3(a)–(c), two common equations for representing them are obtained in (1), which upon rearranged, give (2). Equivalent circuits for representing the input and output full bridges during turn on transient are also shown in Fig. 4(a) and (c), where $C_{oss,Qx}$ $(x = 1 \sim 6)$ is the internal capacitor in parallel with each power switch Q_x. Moreover, because of symmetry of the topology, only events associated with Q_2 of the input full bridge and Q_5 of the output full bridge will be considered. Beginning with Q_2, dynamic equations relating its capacitor $C_{oss,Q2}$ and series inductor L_s in Fig. 4(a) can be expressed as

$$\begin{cases} L_s \dfrac{di_p(t)}{dt} = v_{C_{oss,Q2}}(t) - \left[V_h - v_{C_{oss,Q3}}(t)\right] - nV_l \\ \quad = 2v_{C_{oss,Q2}}(t) - nV_l - V_h \\ C_{oss,Q2} \dfrac{dv_{C_{oss,Q2}}(t)}{dt} = -\dfrac{1}{2} i_p(t) \\ i_p(0) = \dfrac{I_2}{n} \\ v_{C_{oss,Q2}}(0) = V_h \end{cases}. \tag{3}$$

Its capacitor voltage can then be derived as (4) with ω_1 defined in (5)

$$v_{C_{oss,Q2}}(t) = \frac{V_h - nV_l}{2}\cos(\omega_1 t) - \frac{I_2 \omega_1 L_s}{2n}\sin(\omega_1 t) + \frac{V_h + nV_l}{2} \tag{4}$$

$$\omega_1 = \frac{1}{\sqrt{L_s C_{oss,Q2}}}. \tag{5}$$

By reorganizing (4), (6) is obtained with the definition of θ_1 given in (7). From (6) and noting that ZVS of Q_2 will only happen when its capacitor voltage reaches zero by resonance, ZVS boundary condition of the input full bridge can subsequently be deduced as (8). Substituting (5)–(8) then leads to (9). Next, deadtime must be considered, and should properly be controlled so that the turn on of switch happens when its capacitor voltage falls to the minimum, in order to produce minimum turn-on loss. Based on this criterion and according to (6), a guideline for setting deadtime of the input full bridge modulated with SPS in the charging mode can be derived as (10). Substituting (5) and (7) into (10) then yields (11)

$$v_{C_{oss},Q2}(t) = \begin{cases} -\sqrt{\left(\dfrac{V_h - nV_l}{2}\right)^2 + \left(\dfrac{I_2 \omega_1 L_s}{2n}\right)^2}\cos(\omega_1 t - \theta_1) \\ \quad + \dfrac{V_h + nV_l}{2}, \quad (V_h < nV_l) \\ \sqrt{\left(\dfrac{V_h - nV_l}{2}\right)^2 + \left(\dfrac{I_2 \omega_1 L_s}{2n}\right)^2}\cos(\omega_1 t + \theta_1) \\ \quad + \dfrac{V_h + nV_l}{2}, \quad (V_h \geq nV_l) \end{cases} \tag{6}$$

$$\theta_1 = \arcsin\left[\frac{\frac{I_2 \omega_1 L_s}{2n}}{\sqrt{\left(\frac{V_h - nV_l}{2}\right)^2 + \left(\frac{I_2 \omega_1 L_s}{2n}\right)^2}}\right] \tag{7}$$

$$\sqrt{\left(\frac{V_h - nV_l}{2}\right)^2 + \left(\frac{I_2 \omega_1 L_s}{2n}\right)^2} \geq \frac{V_h + nV_l}{2} \tag{8}$$

$$I_2 \geq 2n\sqrt{\frac{nV_h V_l C_{oss,Q2}}{L_s}} \tag{9}$$

$$T_{\mathrm{dead},h,c} = \begin{cases} \theta_1/\omega_1, & (V_h < nV_l) \\ (\pi - \theta_1)/\omega_1, & (V_h \geq nV_l) \end{cases} \tag{10}$$

$$T_{\mathrm{dead},h,c} = \begin{cases} \sqrt{L_s C_{oss,Q2}}\arcsin \\ \quad \left[\sqrt{\dfrac{I_2^2 L_s}{n^2 C_{oss,Q2}(V_h - nV_l)^2 + I_2^2 L_s}}\right], \quad (V_h < nV_l) \\ \sqrt{L_s C_{oss,Q2}}\left\{\pi - \arcsin\right. \\ \quad \left.\left[\sqrt{\dfrac{I_2^2 L_s}{n^2 C_{oss,Q2}(V_h - nV_l)^2 + I_2^2 L_s}}\right]\right\}, \quad (V_h \geq nV_l) \end{cases} \tag{11}$$

As for the output full bridge, its ZVS analysis is easier, because after $t = t_1$, i_s has a relatively small di/dt, and can hence

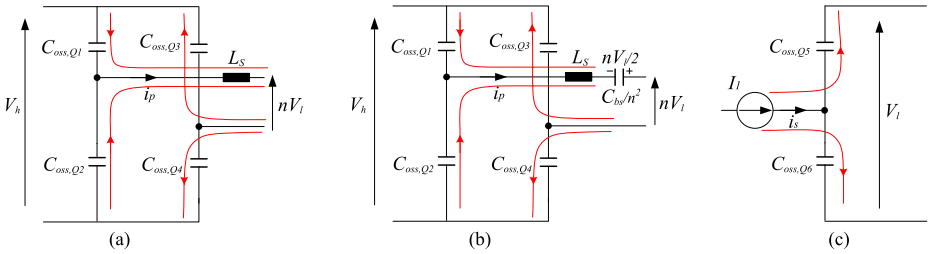


Fig. 4. Equivalent circuits of (a) input full bridge at $t = t_2$ with $V_{Cbs} = 0$, (b) input full bridge at $t = t_2$ with $V_{Cbs} = \frac{V_l}{2}$, and (c) output full bridge at $t = t_1$ with $V_{Cbs} = 0$ or $\frac{V_l}{2}$, during ZVS charging.

be assumed constant at I_1 over a short duration. The turn-on transient of Q_5 can hence be viewed as the discharge of its capacitor $C_{oss,Q5}$ by a constant current $I_1/2$, rather than resonance between L_s and $C_{oss,Q5}$. To discharge voltage of $C_{oss,Q5}$ from V_l to 0 then requires (12) to be met, from which ZVS boundary condition of the output full bridge can be derived as (13). It should however be noted that to find the smallest I_1 using (13), deadtime of the output full bridge must be independently set, which for this work, it is set as $T_{\text{dead},l,c} = 200$ ns during charging

$$\frac{I_1}{2} T_{\text{dead},l,c} \geq C_{oss,Q5} V_l \tag{12}$$

$$I_1 \geq \frac{2C_{oss,Q5} V_l}{T_{\text{dead},l,c}}. \tag{13}$$

-Applying proposed modulation with nonzero dc component or $V_{Cbs} = V_l/2$.

With the proposed modulation scheme, the three scenarios shown in Fig. 3 for the conventional SPS scheme are still applicable, but V_{Cbs} has now changed from 0 to $V_l/2$, and V_s has become $V_l/2$. The equations in (1) then become those in (14), which upon rearranged, yield (15)

$$\begin{cases} I_2 - \dfrac{\phi T_s * \left(\dfrac{V_h}{n} + \dfrac{V_l}{2}\right)}{2\pi \dfrac{L_s}{n^2}} = -I_1 \\ I_2 = I_1 - \dfrac{(\pi - \phi) T_s * \left(\dfrac{V_h}{n} - \dfrac{V_l}{2}\right)}{2\pi \dfrac{L_s}{n^2}} \end{cases} \tag{14}$$

$$\begin{cases} I_1 = \dfrac{\pi n^2 V_l - 2(\pi - 2\phi) n V_h}{8\pi f_s L_s} \\ I_2 = \dfrac{2\pi n V_h - (\pi - 2\phi) n^2 V_l}{8\pi f_s L_s} \end{cases}. \tag{15}$$

In addition, equivalent circuit of the input full bridge during the turn on transient has changed from Fig. 4(a) and (b) due to the extra dc voltage drop across C_{bs} introduced by the modulation scheme. The voltage drop will however not affect equivalent circuit of the output full bridge, which is thus the same as in Fig. 4(c). Returning to Fig. 4(b), dynamic equations for representing the input full bridge can be derived as

$$\begin{cases} L_s \dfrac{di_p(t)}{dt} = v_{C_{oss,Q2}}(t) - \left[V_h - v_{C_{oss,Q3}}(t)\right] \\ \quad + \dfrac{nV_l}{2} - nV_l = 2v_{C_{oss,Q2}}(t) - \dfrac{nV_l}{2} - V_h \\ C_{oss,Q2} \dfrac{dv_{C_{oss,Q2}}(t)}{dt} = -\dfrac{1}{2} i_p(t) \\ i_p(0) = \dfrac{I_2}{n} \\ v_{C_{oss,Q2}}(0) = V_h \end{cases}. \tag{16}$$

From (16), capacitor voltage across Q_2 can further be derived as the following with ω_2 defined as (18)

$$v_{C_{oss},Q2}(t) = \frac{2V_h - nV_l}{4} \cos(\omega_2 t) - \frac{I_2 \omega_2 L_s}{2n} * \sin(\omega_2 t) + \frac{2V_h + nV_l}{4} \tag{17}$$

$$\omega_2 = \frac{1}{\sqrt{L_s C_{oss,Q2}}}. \tag{18}$$

With (17) reorganized, (19) is obtained with θ_2 defined in (20). ZVS boundary condition of the input full bridge can then be obtained by demanding $v_{C_{oss},Q2}$ in (19) to become zero. The resulting condition is given in (21), from which (22) can be derived. By next applying the same principle as discussed earlier for SPS, an equation for properly determining deadtime for the input full bridge with the proposed scheme in charging mode can be obtained as (23). Substituting (18) and (20) into (23) eventually yields (24) for computing deadtime that will ensure ZVS for the input full bridge. As for the output full bridge, its ZVS boundary condition remains the same as (13), since the same equivalent circuit in Fig. 4(c) for the output full bridge can be used for representing SPS, as well as the proposed modulation

$$v_{C_{oss},Q2}(t) = \begin{cases} -\sqrt{\left(\dfrac{2V_h - nV_l}{4}\right)^2 + \left(\dfrac{I_2 \omega_2 L_s}{2n}\right)^2} \cos(\omega_2 t - \theta_2) \\ \quad + \dfrac{2V_h + nV_l}{4}, \quad (2V_h < nV_l) \\ \sqrt{\left(\dfrac{2V_h - nV_l}{4}\right)^2 + \left(\dfrac{I_2 \omega_2 L_s}{2n}\right)^2} \cos(\omega_2 t + \theta_2) \\ \quad + \dfrac{2V_h + nV_l}{4}, \quad (2V_h \geq nV_l) \end{cases} \tag{19}$$

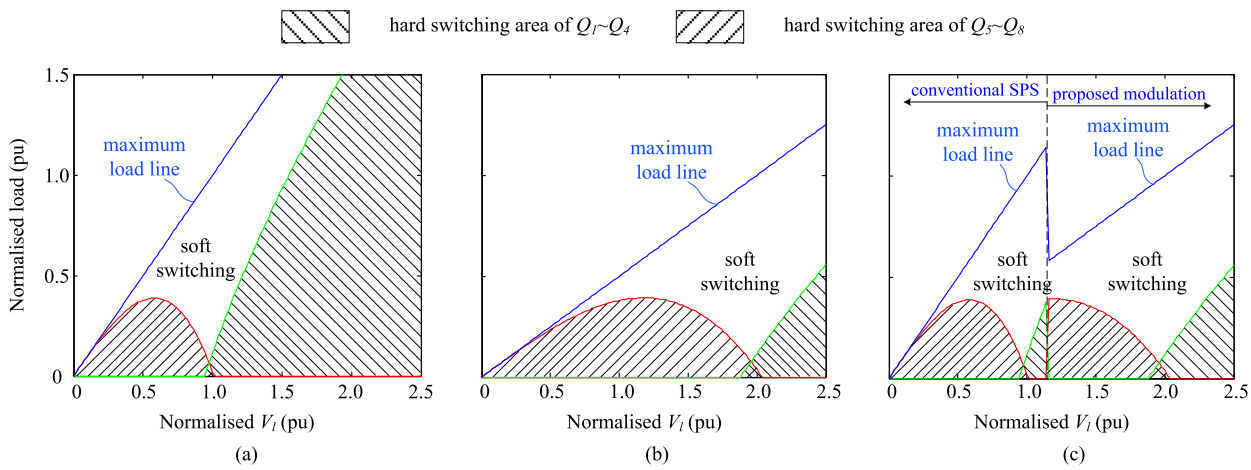


Fig. 5. Maps obtained with (a) conventional SPS, (b) proposed modulation, and (c) hybrid modulation for showing soft-switching and hard-switching regions of DAB during charging at different loads and output dc voltages.

$$\theta_2 = \arcsin\left[\frac{\frac{I_2\omega_2 L_s}{2n}}{\sqrt{\left(\frac{2V_h - nV_l}{4}\right)^2 + \left(\frac{I_2\omega_2 L_s}{2n}\right)^2}}\right] \tag{20}$$

$$\sqrt{\left(\frac{2V_h - nV_l}{4}\right)^2 + \left(\frac{I_2\omega_2 L_s}{2n}\right)^2} \geq \frac{2V_h + nV_l}{4} \tag{21}$$

$$I_2 \geq n\sqrt{\frac{2nV_h V_l C_{oss,Q2}}{L_s}} \tag{22}$$

$$T'_{\text{dead},h,c} = \begin{cases} \theta_2/\omega_2, & (2V_h < nV_l) \\ (\pi - \theta_2)/\omega_2, & (2V_h \geq nV_l) \end{cases} \tag{23}$$

$$T'_{\text{dead},h,c} = \begin{cases} \sqrt{L_s C_{oss,Q2}}\arcsin\left[\sqrt{\frac{4I_2^2 L_s}{n^2 C_{oss,Q2}(2V_h - nV_l)^2 + 4I_2^2 L_s}}\right], & (2V_h < nV_l) \\ \sqrt{L_s C_{oss,Q2}}\left\{\pi - \arcsin\left[\sqrt{\frac{4I_2^2 L_s}{n^2 C_{oss,Q2}(2V_h - nV_l)^2 + 4I_2^2 L_s}}\right]\right\}, & (2V_h \geq nV_l) \end{cases} \tag{24}$$

Now, from (2), (9), (13), (15), (22), and (25), maps for showing soft-switching and hard-switching regions of the DAB during charging with different loads, output voltage levels and modulation schemes are obtained, as provided in Fig. 5. Parameter values used for plotting the maps are also listed in Table II, where the load used for normalization is the maximum load obtained when $\phi = \frac{\pi}{2}$ and $V_l = 1$ p.u. in (25). Particularly, the map in Fig. 5(a) has shown that DAB with SPS has kept a wide soft-switching range at V_l close to 1 p.u., but as V_l deviates from unity, this range narrows significantly. A similar pattern applies to the proposed modulation scheme in Fig. 5(b), except the widest soft-switching range has moved from $V_l = 1$ to 2 p.u. Thus, if SPS is used around $V_l = 1$ p.u. and the proposed modulation is activated around $V_l = 2$ p.u. to form a hybrid modulation scheme, two wide soft-switching ranges can be obtained at V_l close to 1 and 2 p.u., as shown in Fig. 5(c)

$$P = \begin{cases} \frac{nV_h V_l}{2\pi^2 f_s L_s}\phi(\pi - \phi), & (V_{Cbs} = 0) \\ \frac{nV_h V_l}{4\pi^2 f_s L_s}\phi(\pi - \phi), & \left(V_{Cbs} = \frac{V_l}{2}\right) \end{cases}. \tag{25}$$

B. Discharging Mode

Similarly, during discharging, there are three scenarios determined by the polarities of I_1 and I_2, as shown in Fig. 6, where I_2 and I_1 are still aligned with the turn off of Q_1 at t_2 and Q_6 at t_1, respectively. Evaluation of their soft-switching ranges can hence also be performed for SPS and the proposed modulation, as presented below.

-Applying conventional SPS with no dc voltage component or $V_{Cbs} = 0$

$$\frac{I_2}{2n}T_{\text{dead},h,d} \geq C_{oss,Q2}V_h \tag{26}$$

$$I_2 \geq \frac{2C_{oss,Q2}V_h}{nT_{\text{dead},h,d}}. \tag{27}$$

By solving common trigonometry found in Fig. 6(a)–(c), expressions for I_1 and I_2 during discharging can be obtained, but are not provided here, since they are similar to those in (2) derived earlier for the charging mode. Equivalent circuits of the converter during discharging are, however, different from those during charging, and are hence provided in Fig. 7. Particularly, in Fig. 7(a), discharging current flowing through $C_{oss,Q2}$ at the input full bridge has been assumed constant, since i_s has a relatively small di/dt. ZVS boundary condition of the input full bridge can thus be determined by solving (26) to obtain (27), where deadtime $T_{\text{dead},h,d}$

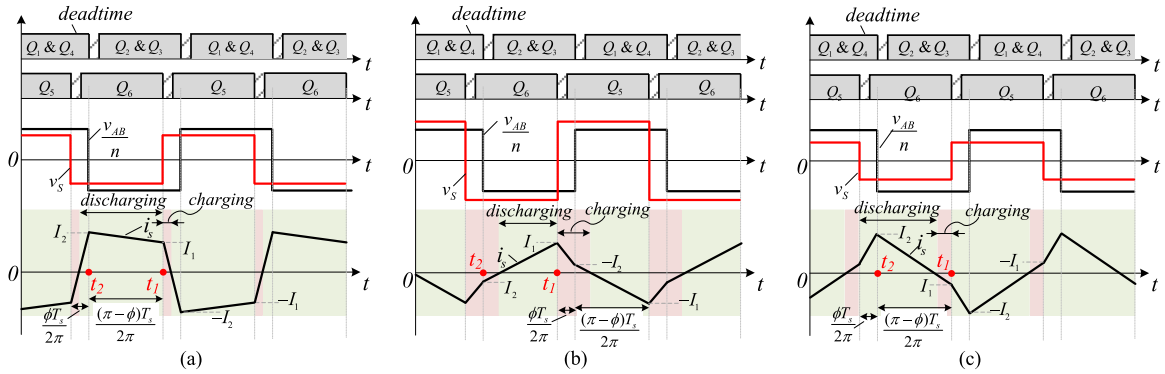


Fig. 6. Gate signals, voltages, and currents of DAB during discharging with (a) $I_1 \geq 0$, $I_2 \geq 0$, (b) $I_1 \geq 0$, $I_2 < 0$, and (c) $I_1 < 0$, $I_2 \geq 0$.

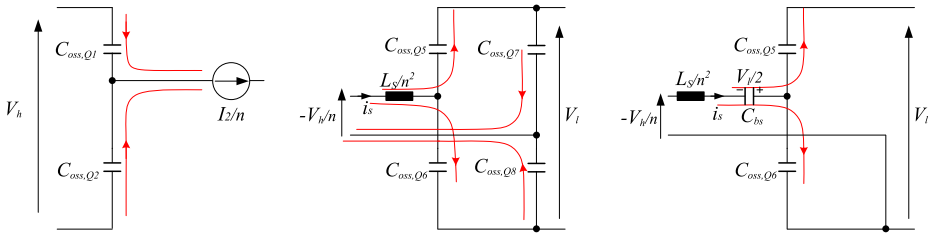


Fig. 7. Equivalent circuits of (a) input full bridge at $t = t_2$, (b) output full bridge at $t = t_1$ with $V_{Cbs} = 0$, and (c) output full bridge at $t = t_1$ with $V_{Cbs} = \frac{V_l}{2}$, during ZVS discharging.

has been set to 200 ns. On the other hand, equivalent circuit of the output full bridge is provided in Fig. 7(b), from which dynamic equations for relating capacitor $C_{oss,Q5}$ and series inductor L_s/n^2 are derived as (28). Voltage across $C_{oss,Q5}$ is then determined as (29), where ω_3 in it is defined as (30)

$$\begin{cases} \dfrac{L_s}{n^2}\dfrac{di_s(t)}{dt} = v_{C_{oss,Q8}}(t) - \dfrac{V_h}{n} - \left[V_l - v_{C_{oss,Q5}}(t)\right] \\ \quad = 2v_{C_{oss,Q5}}(t) - V_l - \dfrac{V_h}{n} \\ C_{oss,Q5}\dfrac{dv_{C_{oss,Q5}}(t)}{dt} = -\dfrac{1}{2}i_s(t) \\ i_s(0) = I_1 \\ v_{C_{oss,Q5}}(0) = V_l \end{cases} \tag{28}$$

$$v_{C_{oss,Q5}}(t) = \frac{nV_l - V_h}{2n}\cos(\omega_3 t) - \frac{I_1\omega_3 L_s}{2n^2}\sin(\omega_3 t) + \frac{nV_l + V_h}{2n} \tag{29}$$

$$\omega_3 = \frac{n}{\sqrt{L_s C_{oss,Q5}}}. \tag{30}$$

To again ensure voltage of $C_{oss,Q5}$ does reach zero, (33) is derived, which upon reorganized, gives (34). Equation (34) is, thus, the boundary condition of the output full bridge, which upon fulfilled, guarantees ZVS of Q_5 when driven by SPS during discharging. With deadtime considered, its duration for the output full bridge is obtained as (35) based on the same explanation discussed earlier for the charging mode. Substituting (30) and (32) into (35) finally leads to (36)

$$v_{C_{oss,Q5}}(t) = \begin{cases} \sqrt{\left(\dfrac{nV_l - V_h}{2n}\right)^2 + \left(\dfrac{I_1\omega_3 L_s}{2n^2}\right)^2}\cos(\omega_3 t + \theta_3) \\ \quad + \dfrac{nV_l + V_h}{2n}, \quad (V_h < nV_l) \\ -\sqrt{\left(\dfrac{nV_l - V_h}{2n}\right)^2 + \left(\dfrac{I_1\omega_3 L_s}{2n^2}\right)^2}\cos(\omega_3 t - \theta_3) \\ \quad + \dfrac{nV_l + V_h}{2n}, \quad (V_h \geq nV_l) \end{cases} \tag{31}$$

$$\theta_3 = \arcsin\left[\frac{\frac{I_1\omega_3 L_s}{2n^2}}{\sqrt{\left(\frac{nV_l - V_h}{2n}\right)^2 + \left(\frac{I_1\omega_3 L_s}{2n^2}\right)^2}}\right] \tag{32}$$

$$\sqrt{\left(\frac{nV_l - V_h}{2n}\right)^2 + \left(\frac{I_1\omega_3 L_s}{2n^2}\right)^2} \geq \frac{nV_l + V_h}{2n} \tag{33}$$

$$I_1 \geq 2\sqrt{\frac{nV_h V_l C_{oss,Q5}}{L_s}} \tag{34}$$

$$T_{\mathrm{dead},l,d}=\begin{cases}\left(\pi-\theta_3\right)/\omega_3, & \left(V_h<nV_l\right)\\ \theta_3/\omega_3, & \left(V_h\geq nV_l\right)\end{cases} \tag{35}$$

$$T_{\mathrm{dead},l,d}=$$
$$\begin{cases}\dfrac{\sqrt{L_sC_{oss,Q5}}}{n}\left\{\pi-\right.\\ \left.\arcsin\left[\sqrt{\dfrac{I_1^2L_s}{C_{oss,Q5}(nV_l-V_h)^2+I_1^2L_s}}\right]\right\}, & \left(V_h<nV_l\right)\\ \dfrac{\sqrt{L_sC_{oss,Q5}}}{n}\\ \arcsin\left[\sqrt{\dfrac{I_1^2L_s}{C_{oss,Q5}(nV_l-V_h)^2+I_1^2L_s}}\right], & \left(V_h\geq nV_l\right)\end{cases}. \tag{36}$$

-Applying proposed modulation with nonzero dc voltage component or $V_{Cbs}=V_l/2$.

After changing to the proposed modulation, (14) can again be obtained by solving trigonometry found in Fig. 6(a)–(c), from which similar expressions for I_1 and I_2 as in (15) can be derived. Equivalent circuit for the output full bridge during ZVS has however changed from Fig. 7(b) to (c), since V_{Cbs} has changed from 0 to $V_l/2$. Dynamic equations for relating capacitor $C_{oss,Q5}$ and series inductor L_s/n^2 in Fig. 7(c) can hence be derived as (37), from which voltage across $C_{oss,Q5}$ can be obtained as (38) with ω_4 defined as (39). Voltage across $C_{oss,Q5}$ in (38) can further be reorganized as (40) with θ_4 defined as (41). Appropriate boundary condition is then acquired as (42), before simplifying to (43). According to (40), deadtime of the discharging output full bridge using the proposed modulation scheme can also be expressed as (44), which upon substituted with expressions for ω_4 in (39) and θ_4 in (41), yields (45)

$$\begin{cases}\dfrac{L_s}{n^2}\dfrac{di_s\left(t\right)}{dt}=-\dfrac{V_h}{n}+\dfrac{V_l}{2}-\left[V_l-v_{C_{oss,Q5}}\left(t\right)\right]\\ \qquad=v_{C_{oss,Q5}}\left(t\right)-\dfrac{nV_l+2V_h}{2n}\\ C_{oss,Q5}\dfrac{dv_{C_{oss,Q5}}\left(t\right)}{dt}=-\dfrac{1}{2}i_s\left(t\right)\\ i_s\left(0\right)=I_1\\ v_{C_{oss,Q5}}\left(0\right)=V_l\end{cases} \tag{37}$$

$$v_{C_{oss},Q5}\left(t\right)=\frac{nV_l-2V_h}{2n}\cos\left(\omega_4t\right)-\frac{I_1\omega_4L_s}{n^2}\sin\left(\omega_4t\right)+\frac{nV_l+2V_h}{2n} \tag{38}$$

$$\omega_4=\frac{n}{\sqrt{2L_sC_{oss,Q5}}} \tag{39}$$

$$v_{C_{oss},Q5}\left(t\right)=\begin{cases}\sqrt{\left(\dfrac{nV_l-2V_h}{2n}\right)^2+\left(\dfrac{I_1\omega_4L_s}{n^2}\right)^2}\\ \cos\left(\omega_4t+\theta_4\right)+\dfrac{nV_l+2V_h}{2n}, & \left(2V_h<nV_l\right)\\ -\sqrt{\left(\dfrac{nV_l-2V_h}{2n}\right)^2+\left(\dfrac{I_1\omega_4L_s}{n^2}\right)^2}\\ \cos\left(\omega_4t-\theta_4\right)+\dfrac{nV_l+2V_h}{2n}, & \left(2V_h\geq nV_l\right)\end{cases} \tag{40}$$

$$\theta_4=\arcsin\left[\frac{\frac{I_1\omega_4L_s}{n^2}}{\sqrt{\left(\frac{nV_l-2V_h}{2n}\right)^2+\left(\frac{I_1\omega_4L_s}{n^2}\right)^2}}\right] \tag{41}$$

$$\sqrt{\left(\frac{nV_l-2V_h}{2n}\right)^2+\left(\frac{I_1\omega_4L_s}{n^2}\right)^2}\geq\frac{nV_l+2V_h}{2n} \tag{42}$$

$$I_1\geq2\sqrt{\frac{nV_hV_lC_{oss,Q5}}{L_s}} \tag{43}$$

$$T'_{\mathrm{dead},l,d}=\begin{cases}\left(\pi-\theta_4\right)/\omega_4, & \left(2V_h<nV_l\right)\\ \theta_4/\omega_4, & \left(2V_h\geq nV_l\right)\end{cases} \tag{44}$$

$$T'_{\mathrm{dead},l,d}=$$
$$\begin{cases}\dfrac{\sqrt{2L_sC_{oss,Q5}}}{n}\left\{\pi-\right.\\ \left.\arcsin\left[\sqrt{\dfrac{2I_1^2L_s}{C_{oss,Q5}(nV_l-2V_h)^2+2I_1^2L_s}}\right]\right\}, & \left(2V_h<nV_l\right)\\ \dfrac{\sqrt{2L_sC_{oss,Q5}}}{n}\\ \arcsin\left[\sqrt{\dfrac{2I_1^2L_s}{C_{oss,Q5}(nV_l-2V_h)^2+2I_1^2L_s}}\right], & \left(2V_h\geq nV_l\right)\end{cases}. \tag{45}$$

From (2), (15), (25), (27), (34), and (43), maps in Fig. 8 can then be obtained for projecting soft-switching and hard-switching regions of the DAB when it discharges with different load and output dc voltage conditions. Specifically, the first two maps in Fig. 8(a) and (b) show that conventional SPS achieves the widest soft-switching range when V_l is close to 1 p.u., while the proposed modulation has its widest soft-switching range moved close to $V_l=2$ p.u. Therefore, if modulation is switched from conventional SPS to the proposed scheme as V_l increases from 1 to 2 p.u., the converter will favorably have two widest soft-switching ranges located at close to $V_l=1$ and 2 p.u.

IV. Circulating Power

It should be emphasized that identification of soft-switching boundaries above is mainly related to switching losses of devices such as MOSFETs used for this work. Another critical factor affecting efficiency of a DAB is its circulating power, known to

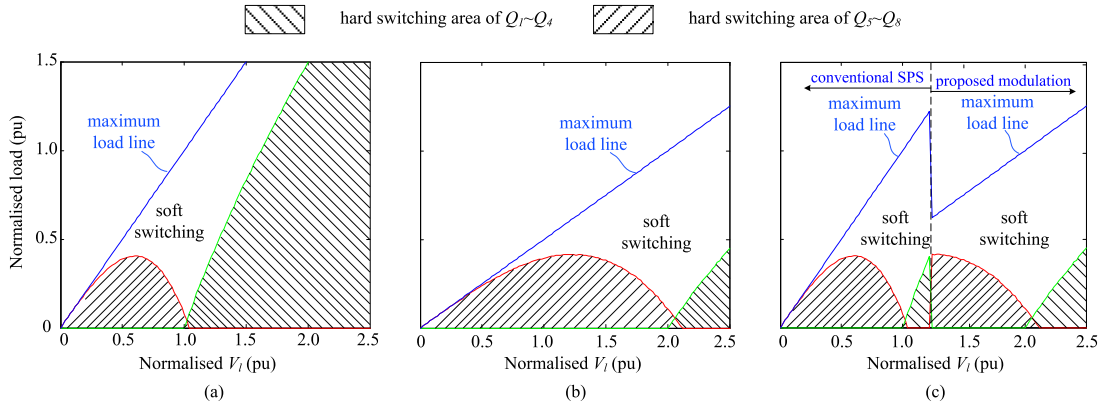


Fig. 8. Maps obtained with (a) conventional SPS, (b) proposed modulation, and (c) hybrid modulation for showing soft-switching and hard-switching regions of DAB during discharging at different loads and output voltages.

raise conduction losses of the MOSFETs and passive components. Circulating power of the converter is therefore determined for SPS and the proposed modulation. More specifically, it is determined by calculating discharging power when the DAB is charged as in Fig. 3, and charging power when the DAB is discharged as in Fig. 6. The observation noted is charging and discharging of the DAB have no influence on the circulating power. The factor that affects it is the voltage offset V_{Cbs}. More details are provided as follows for each of the studied schemes.

-Applying conventional SPS with no dc voltage component or $V_{Cbs} = 0$.

In this case, amplitudes of v_{AB} and v_s are V_h and V_l, respectively, and by multiplying v_s and i_s during discharging in Fig. 3(a)–(c) or charging in Fig. 6(a)–(c), (46)–(48) can be obtained. Further simplification and consolidation lead to the more compact expression in (49) for circulating power.

If $I_1 \geq 0$ && $I_2 \geq 0$, then

$$Q = \frac{\frac{I_1}{2} * \frac{I_1}{I_1+I_2} * \frac{\phi T_s}{2\pi} * V_l}{0.5T_s}. \tag{46}$$

If $I_1 \geq 0$ && $I_2 < 0$, then

$$Q = \frac{\left[\frac{-I_2}{2} * \frac{-I_2}{I_1-I_2} * \frac{(\pi-\phi)T_s}{2\pi} + \frac{-I_2+I_1}{2} * \frac{\phi T_s}{2\pi}\right] * V_l}{0.5T_s}. \tag{47}$$

If $I_1 < 0$ && $I_2 \geq 0$, then

$$Q = \frac{\frac{-I_1}{2} * \frac{-I_1}{-I_1+I_2} * \frac{(\pi-\phi)T_s}{2\pi} * V_l}{0.5T_s} \tag{48}$$

$$Q = \begin{cases} \dfrac{\phi I_1^2 V_l}{2\pi\left(I_1+I_2\right)}, & \left(I_1 \geq 0 \text{ and } I_2 \geq 0\right) \\ \dfrac{\left[(\pi-\phi)\, I_2^2 + \phi(I_1-I_2)^2\right] V_l}{2\pi\left(I_1-I_2\right)}, & \left(I_1 \geq 0 \text{ and } I_2 < 0\right) \\ \dfrac{(\pi-\phi)\, I_1^2 V_l}{2\pi\left(-I_1+I_2\right)}, & \left(I_1 < 0 \text{ and } I_2 \geq 0\right) \end{cases}. \tag{49}$$

-Applying proposed modulation with nonzero dc voltage component or $V_{Cbs} = V_l/2$.

A change to the proposed modulation will still keep amplitude of v_{AB} at V_h, but will change that of v_s to $V_l/2$. Equations (46)–(48) will then change to (50)–(52), respectively, which upon consolidated, lead to the compact circulating power expression in (53). Additionally, it should be mentioned that active power of the DAB can still be computed using (25), even if operation changes from charging to discharging.

If $I_1 \geq 0$ && $I_2 \geq 0$, then

$$Q = \frac{\frac{I_1}{2} * \frac{I_1}{I_1+I_2} * \frac{\phi T_s}{2\pi} * \frac{V_l}{2}}{0.5T_s}. \tag{50}$$

If $I_1 \geq 0$ && $I_2 < 0$, then

$$Q = \frac{\left[\frac{-I_2}{2} * \frac{-I_2}{I_1-I_2} * \frac{(\pi-\phi)T_s}{2\pi} + \frac{-I_2+I_1}{2} * \frac{\phi T_s}{2\pi}\right] * \frac{V_l}{2}}{0.5T_s}. \tag{51}$$

If $I_1 < 0$ && $I_2 \geq 0$, then

$$Q = \frac{\frac{-I_1}{2} * \frac{-I_1}{-I_1+I_2} * \frac{(\pi-\phi)T_s}{2\pi} * \frac{V_l}{2}}{0.5T_s} \tag{52}$$

$$Q = \begin{cases} \dfrac{\phi I_1^2 V_l}{4\pi\left(I_1+I_2\right)}, & \left(I_1 \geq 0 \text{ and } I_2 \geq 0\right) \\ \dfrac{\left[(\pi-\phi)\, I_2^2 + \phi(I_1-I_2)^2\right] V_l}{4\pi\left(I_1-I_2\right)}, & \left(I_1 \geq 0 \text{ and } I_2 < 0\right) \\ \dfrac{(\pi-\phi)\, I_1^2 V_l}{4\pi\left(-I_1+I_2\right)}, & \left(I_1 < 0 \text{ and } I_2 \geq 0\right) \end{cases}. \tag{53}$$

Then, according to (2), (15), (25), (49), and (53), circulating power of the DAB can be expressed as a function of load and output voltage. The function can be used for plotting maps for different modulation schemes, as provided in Fig. 9. Particularly, in Fig. 9(a), a wide range with low Q/P is achieved by the conventional SPS scheme close to $V_l = 1$ p.u., whereas in Fig. 9(b), the desired wide range has been shifted to $V_l = 2$ p.u. after activating the proposed scheme. Therefore, with a hybrid

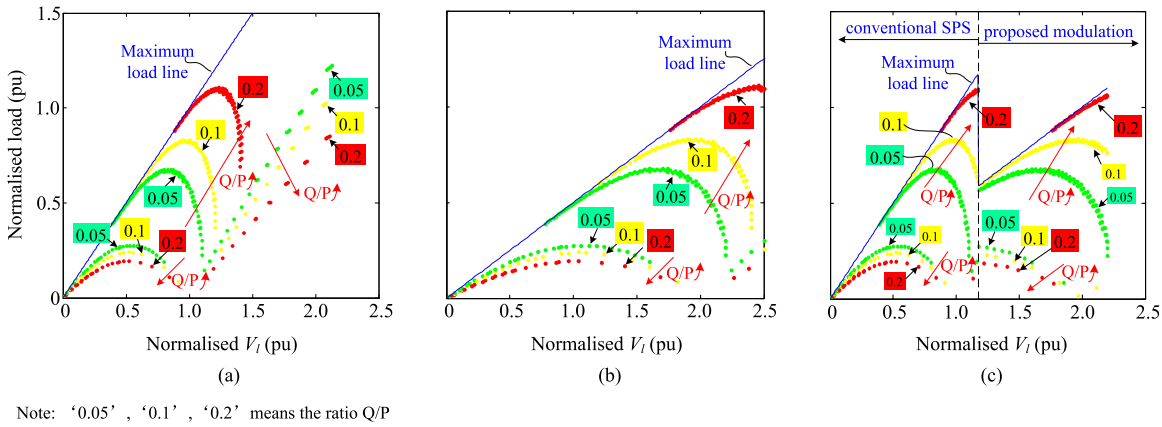


Fig. 9. Circulating powers of DAB with (a) conventional SPS, (b) proposed modulation, and (c) hybrid modulation at different loads and output dc voltages.

combination of both strategies, Fig. 9(c) expectedly confirms that wide ranges with low Q/P can be achieved near both $V_l = 1$ and 2 p.u.

Finally, for ease of comparison, soft switching, active power, and circulating power expressions of the DAB under different operating conditions are summarized in Table I. Collectively, they show that charging and discharging have no impact on the calculation of I_1, I_2, active power and circulating power, but they do affect the soft-switching conditions. In contrast, modulation methods influence all the mentioned parameters.

V. Selection of DC Blocking Capacitors

DC blocking capacitor C_{bs}, redrawn in Fig. 10(a), is for blocking dc voltage component of the output full bridge from appearing across the transformer. According to notations marked in Fig. 10(a), dc voltage across C_{bs} will then be $V_l/2$, if the proposed modulation is applied. To show that this dc capacitor voltage will automatically be sustained, the simple transformer representation shown in Fig. 10(a) will be considered, where L_m and i_m represent its magnetizing inductance and current, respectively. Corresponding magnetic B–H curve of the transformer is also shown in Fig. 10(b), where it should ideally be centered at the origin with no dc component introduced. Looping around the origin is then caused by $v_{\rm ac}$, which according to Fig. 10(a), is the ac component of v_{CD}. In case a disturbance now causes voltage of C_{bs} to become $V_{Cbs} > V_l/2$, winding voltage v_s of the transformer will undesirably have a negative dc component, whose effects are to shift the B–H curve in Fig. 10(b) to the third quadrant, and introduce a negative dc component to the magnetizing current i_m. According to Fig. 10(a), the negative dc current then discharges C_{bs}, causing its voltage V_{Cbs} to return to $V_l/2$. The same reasoning can be applied to an initial $V_{Cbs} < V_l/2$, which in that case, will cause C_{bs} to charge toward $V_{Cbs} = V_l/2$. It is hence appropriate to conclude that V_{Cbs} will eventually stabilize at $V_l/2$, regardless of its initial condition.

Another concern of the dc blocking capacitor C_{bs} is its voltage ripple caused by charging and discharging within a period. This voltage ripple, if too large, can affect proper operation of the DAB. It is thus analyzed by first solving trigonometry found in Figs. 3 and 6, from which maximum voltage ripple of C_{bs} is evaluated as follows.

If $I_1 \geq 0$ && $I_2 \geq 0$, then

$$\Delta V_{Cbs\max} = \frac{1}{C_{bs}}\left[\frac{I_1}{2} * \frac{I_1}{I_1+I_2} * \frac{\phi T_s}{2\pi} + \frac{I_1+I_2}{2} * \frac{(\pi-\phi)\,T_s}{2\pi} + \frac{I_2}{2} * \frac{I_2}{I_1+I_2} * \frac{\phi T_s}{2\pi}\right]. \quad (54)$$

If $I_1 \geq 0$ && $I_2 < 0$, then

$$\Delta V_{Cbs\max} = \frac{1}{C_{bs}}\left[\frac{-I_2}{2} * \frac{-I_2}{I_1-I_2} * \frac{(\pi-\phi)\,T_s}{2\pi} + \frac{-I_2+I_1}{2} * \frac{\phi T_s}{2\pi} + \frac{I_1}{2} * \frac{I_1}{I_1-I_2} * \frac{(\pi-\phi)\,T_s}{2\pi}\right]. \quad (55)$$

If $I_1 < 0$ && $I_2 \geq 0$, then

$$\Delta V_{Cbs\max} = \frac{1}{C_{bs}}\left[\frac{I_2}{2} * \frac{I_2}{-I_1+I_2} * \frac{(\pi-\phi)\,T_s}{2\pi} + \frac{I_2-I_1}{2} * \frac{\phi T_s}{2\pi} + \frac{-I_1}{2} * \frac{-I_1}{-I_1+I_2} * \frac{(\pi-\phi)\,T_s}{2\pi}\right]. \quad (56)$$

By simplifying (54) to (56), a more compact form of the maximum voltage ripple is acquired as

$$\Delta V_{Cbs\max} = \begin{cases} \dfrac{\left[\pi(I_1+I_2)^2 - 2\phi I_1 I_2\right] T_s}{4\pi C_{bs}\,(I_1+I_2)}, & (I_1 \geq 0 \text{ and } I_2 \geq 0) \\ \dfrac{\left[\pi\left(I_1^2+I_2^2\right) - 2\phi I_1 I_2\right] T_s}{4\pi C_{bs}\,(I_1-I_2)}, & (I_1 \geq 0 \text{ and } I_2 < 0) \\ \dfrac{\left[\pi\left(I_1^2+I_2^2\right) - 2\phi I_1 I_2\right] T_s}{4\pi C_{bs}\,(I_2-I_1)}, & (I_1 < 0 \text{ and } I_2 \geq 0) \end{cases} \quad (57)$$

Pictorially, voltage ripple of C_{bs} can also be illustrated in Fig. 11, where Fig. 11(a) shows it increasing with load and V_l. Despite that, its amplitude has been kept under 0.02 p.u. over almost the full operational range, even with only 22 μF used as C_{bs}. No doubt, changing the capacitance will influence the

TABLE I
SOFT-SWITCHING CONDITIONS AND CIRCULATING POWER EXPRESSIONS OF DAB WITH DIFFERENT MODULATION METHODS AND OPERATIONAL MODES

		Soft switching condition		Active power	Circulating power
		Input side full bridge	Output side full bridge		
Charging mode	SPS	$I_2 \geq 2n\sqrt{\frac{nV_hV_lC_{oss,Q2}}{L_s}}$ $I_2 = \frac{\pi nV_h-(\pi-2\phi)n^2V_l}{4\pi f_sL_s}$	$I_1 \geq \frac{2C_{oss,Q5}V_l}{T_{\mathrm{dead},l,c}}$ $I_1 = \frac{\pi n^2V_l-(\pi-2\phi)nV_h}{4\pi f_sL_s}$	$\frac{nV_hV_l}{2\pi^2f_sL_s}\phi(\pi-\phi)$	$\begin{cases}\frac{\phi I_1^2V_l}{2\pi(I_1+I_2)}, & (I_1\geq 0 \text{ and } I_2\geq 0)\\ \frac{[(\pi-\phi)I_2^2+\phi(I_1-I_2)^2]V_l}{2\pi(I_1-I_2)}, & (I_1\geq 0 \text{ and } I_2< 0)\\ \frac{(\pi-\phi)I_1^2V_l}{2\pi(-I_1+I_2)}, & (I_1< 0 \text{ and } I_2\geq 0)\end{cases}$
	Proposed scheme	$I_2 \geq n\sqrt{\frac{2nV_hV_lC_{oss,Q2}}{L_s}}$ $I_2 = \frac{2\pi nV_h-(\pi-2\phi)n^2V_l}{8\pi f_sL_s}$	$I_1 \geq \frac{2C_{oss,Q5}V_l}{T_{\mathrm{dead},l,c}}$ $I_1 = \frac{\pi n^2V_l-2(\pi-2\phi)nV_h}{8\pi f_sL_s}$	$\frac{nV_hV_l}{4\pi^2f_sL_s}\phi(\pi-\phi)$	$\begin{cases}\frac{\phi I_1^2V_l}{4\pi(I_1+I_2)}, & (I_1\geq 0 \text{ and } I_2\geq 0)\\ \frac{[(\pi-\phi)I_2^2+\phi(I_1-I_2)^2]V_l}{4\pi(I_1-I_2)}, & (I_1\geq 0 \text{ and } I_2< 0)\\ \frac{(\pi-\phi)I_1^2V_l}{4\pi(-I_1+I_2)}, & (I_1< 0 \text{ and } I_2\geq 0)\end{cases}$
Discharging mode	SPS	$I_2 \geq \frac{2C_{oss,Q2}V_h}{nT_{\mathrm{dead},h,d}}$ $I_2 = \frac{\pi nV_h-(\pi-2\phi)n^2V_l}{4\pi f_sL_s}$	$I_1 \geq 2\sqrt{\frac{nV_hV_lC_{oss,Q5}}{L_s}}$ $I_1 = \frac{\pi n^2V_l-(\pi-2\phi)nV_h}{4\pi f_sL_s}$	$\frac{nV_hV_l}{2\pi^2f_sL_s}\phi(\pi-\phi)$	$\begin{cases}\frac{\phi I_1^2V_l}{2\pi(I_1+I_2)}, & (I_1\geq 0 \text{ and } I_2\geq 0)\\ \frac{[(\pi-\phi)I_2^2+\phi(I_1-I_2)^2]V_l}{2\pi(I_1-I_2)}, & (I_1\geq 0 \text{ and } I_2< 0)\\ \frac{(\pi-\phi)I_1^2V_l}{2\pi(-I_1+I_2)}, & (I_1< 0 \text{ and } I_2\geq 0)\end{cases}$
	Proposed scheme	$I_2 \geq \frac{2C_{oss,Q2}V_h}{nT_{\mathrm{dead},h,d}}$ $I_2 = \frac{2\pi nV_h-(\pi-2\phi)n^2V_l}{8\pi f_sL_s}$	$I_1 \geq 2\sqrt{\frac{nV_hV_lC_{oss,Q5}}{L_s}}$ $I_1 = \frac{\pi n^2V_l-2(\pi-2\phi)nV_h}{8\pi f_sL_s}$	$\frac{nV_hV_l}{4\pi^2f_sL_s}\phi(\pi-\phi)$	$\begin{cases}\frac{\phi I_1^2V_l}{4\pi(I_1+I_2)}, & (I_1\geq 0 \text{ and } I_2\geq 0)\\ \frac{[(\pi-\phi)I_2^2+\phi(I_1-I_2)^2]V_l}{4\pi(I_1-I_2)}, & (I_1\geq 0 \text{ and } I_2< 0)\\ \frac{(\pi-\phi)I_1^2V_l}{4\pi(-I_1+I_2)}, & (I_1< 0 \text{ and } I_2\geq 0)\end{cases}$

TABLE II
PERFORMANCE COMPARISON OF VARIOUS MODULATION SCHEMES FOR DAB CONVERTERS

	SPS [5]	EPS [27]	DPS [15]	TPS [28]	Quasi-SPS (proposed)	Quasi-EPS
Max power	1 p.u.	1 p.u.	1 p.u.	1 p.u.	0.5 p.u.	0.5 p.u.
Voltage range with high efficiency	Narrow (around 1 p.u.)	Medium	Medium	Wide	Narrow (around 2 p.u.)	Medium (around 2 p.u.)
Independent control freedom degree	1	2	2	3	1	2
Control complexity	Low	Medium	Medium	High	Low	Medium
Nonlinearity	Low	Medium	Medium	High	Low	Medium

voltage ripple. Some typical variations for demonstrating it are included in Fig. 11(b), where $V_l = 1$ p.u. in case of SPS and 2 p.u. in case of the proposed PWM. Other than voltage ripple, current stress experienced by the capacitor may also be critical, since it may cause damages due to overheating. Connecting capacitors in parallel to share the current stress is, thus, relatively common. The same considerations may also be applied to C_{bp} on the other side of the transformer, as shown in Fig. 1(a). Its blocked dc voltage will then be $V_h/2$, instead of $V_l/2$.

VI. COMPARISON WITH OTHER MODULATION SCHEMES

As explained, by inserting a voltage offset across the dc blocking capacitor C_{bs}, the DAB converter in Fig. 1(a) can achieve improved performance when its dc output voltage is around 2 p.u. This method should preferably be used in situation, where the pulsating voltage generated by the output full bridge contains both a nonzero dc component and a symmetrical ac component. Any asymmetrical ac voltage will significantly complicate the converter operation. Thus, for a two-level full bridge, the symmetrical ac component can only be a square waveform with 50% duty cycle, if a nonzero dc component must be produced too. An example waveform labeled as v_s is provided in Fig. 2(b). On the other hand, voltage waveform generated by the input full bridge can be more flexible with duty cycle of either 50% symmetrical or less than 50% asymmetrical. The former corresponds to the technique proposed, which for easier identification among other techniques compared in this section, is referred to as quasi-SPS. The latter is then named as quasi-EPS, where EPS means extended phase shift modulation discussed in [7]–[13] and mentioned in Section I. Other acronyms of techniques, such as DPS and TPS, have also been mentioned in Section I.

Performance expectations of the six techniques, notated as SPS, EPS, DPS, TPS, quasi-SPS and quasi-EPS, have then been summarized in Table II, where the first four techniques have clearly been mentioned as able to improve efficiency of the DAB. However, their implementation complexities may be burdensome, as compared to SPS. More specifically, there are

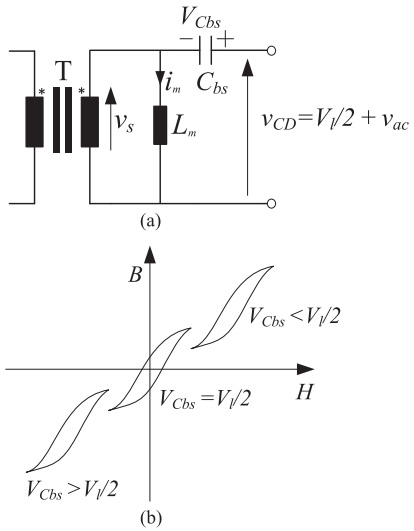
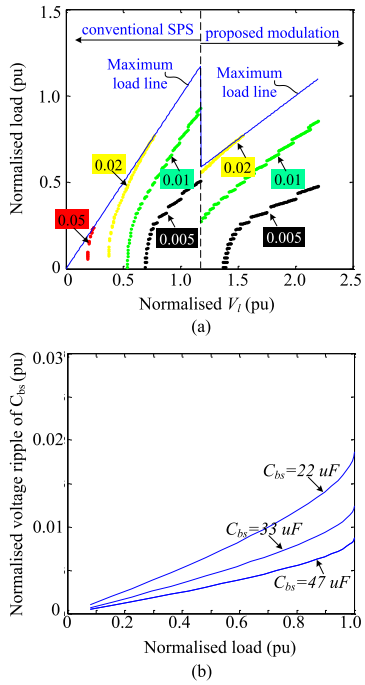


Fig. 10. Illustrations of (a) transformer equivalent circuit and (b) its B–H curves for demonstrating voltage stability of dc blocking capacitor.



Note: '0.005', '0.01', '0.02', '0.05' means the normalized voltage ripple of C_{bs}

Fig. 11. Voltage ripple across C_{bs} as (a) function of load and V_l when $C_{bs} = 22\,\mu$F, and (b) function of load and capacitance when $V_l = 1$ p.u. in case of SPS or $V_l = 2$ p.u. in case of proposed scheme.

two parameters of EPS or DPS, and three parameters of TPS that need tuning for controlling the delivered power. Impacts of these parameters on efficiency are also coupled, making it tough to locate their optimal values that will maximize efficiency. Although analytical methods have since been proposed for finding the optimal operating point, they usually rely on offline look-up tables to avoid excessive computational burdens [22]. Such offline tables will usually compromise dynamics of the DAB, which may be why no simulation and experimental

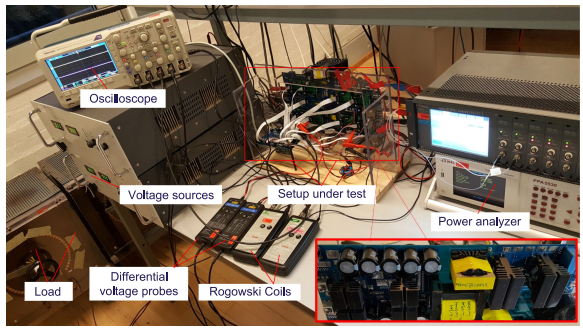


Fig. 12. Experimental platform.

TABLE III
PARAMETERS USED FOR EXPERIMENTS

Parameters	Values
Nominal power	1500 W
Input side voltage V_h	200 V
Turn ratio of the transformer $n:1$	3.5:1
Output side voltage V_l	0.8 ∼ 2.2 p.u. (1 pu $= V_h/n = 57$ V)
Series inductor L_s	40 μH
Switching frequency f_s	100 kHz
DC blocking capacitor C_{bp}	10 μF × 8
DC blocking capacitor C_{bs}	10 μF × 15
Energy related output capacitors $C_{oss,Q1} \sim C_{oss,Q4}$ (IPW65R080CFD)	158 pF
Energy related output capacitors $C_{oss,Q5} \sim C_{oss,Q8}$ (IPP110N20N3 G)	401 pF × 2 (two in parallel)

results have been included in the literature for dynamic verification. Other methods suggested are to fix one parameter of EPS or DPS, or two parameters of TPS, leaving only 1 DOF for tuning. No doubt, tuning has become much easier, but optimal efficiency cannot always be guaranteed. Attractiveness of these techniques are therefore not always justified, especially if they introduce strong nonlinearities to the DAB, which may toughen its controller design and stability analysis. As a result, SPS and its improvements such as the quasi-SPS proposed in this paper may be better choices, if dynamics and simple analysis for predicting stability are of greater concerns [32]–[34].

VII. Experimental Results

A test platform has been established for verification, as shown in Fig. 12. Parameters used for the tests have also been provided in Table III. As a start, Fig. 13 shows that by using the proposed modulation at $V_l = 2$ p.u. during charging, the converter produces the same transformer current and voltage as those of the conventional SPS scheme at $V_l = 1$ p.u. Design challenges imposed on the transformer, in terms of adapting well over a wide V_l range from 1 to 2 p.u., can hence be reduced. Moreover, it can be seen that v_{CD} has changed from an ac waveform with voltage levels $\pm V_l$ to an ac+dc waveform with voltage levels V_l and 0, when changed from SPS to the proposed modulation. As a result, voltage drop V_{Cbs} across the dc blocking capacitor has changed from 0 to $V_l/2$.

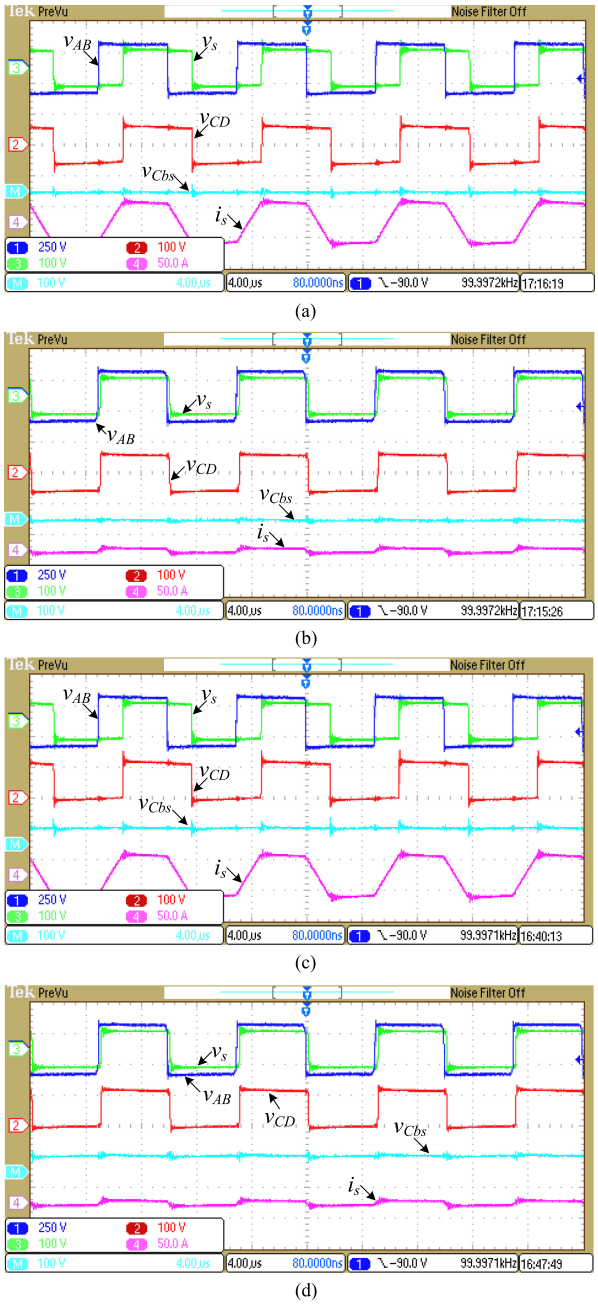


Fig. 13. Voltage and current waveforms of DAB during charging when (a) $V_l = 1$ p.u. with full load and conventional SPS, (b) $V_l = 1$ p.u. with 1/6 load and conventional SPS, (c) $V_l = 2$ p.u. with full load and proposed modulation, and (d) $V_l = 2$ p.u. with 1/6 load and proposed modulation.

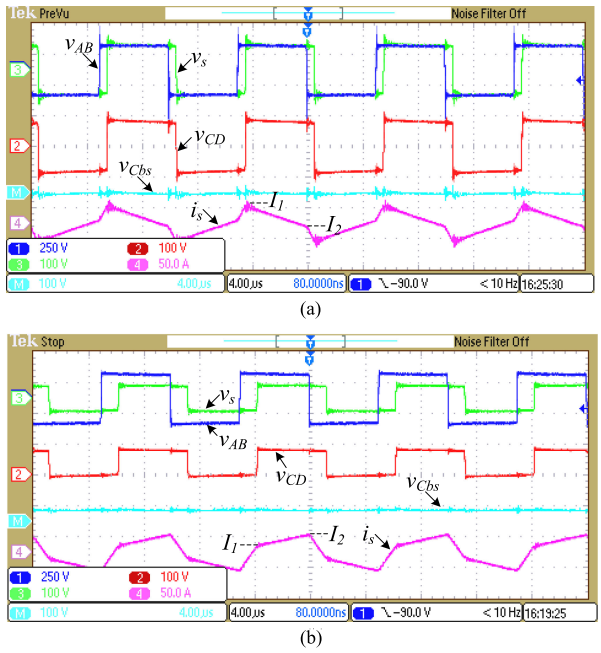


Fig. 14. Voltage and current waveforms obtained with (a) conventional SPS and (b) proposed modulation when $V_l = 1.4$ p.u. during charging.

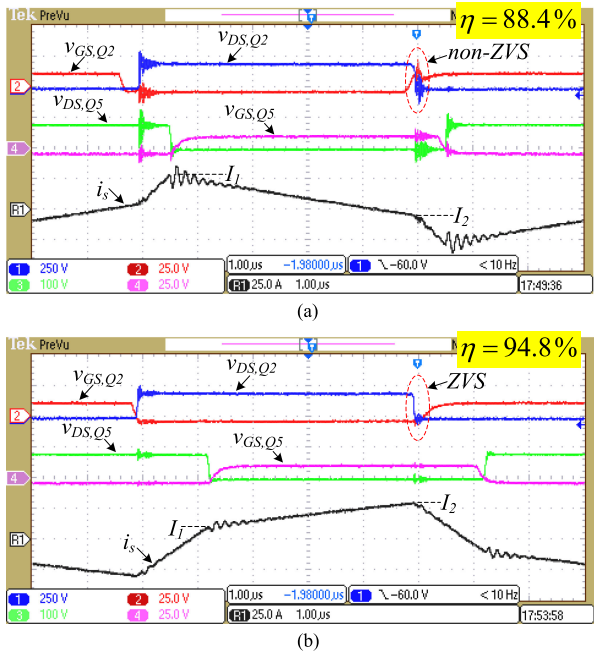


Fig. 15. ZVS performances obtained with (a) conventional SPS and (b) proposed modulation when $V_l = 1.4$ p.u. during charging.

Next, Fig. 14 shows different internal voltage and current waveforms of the converter during charging for the two modulation schemes. With the proposed modulation, v_s is obviously halved. Gradient di/dt in between I_1 and I_2 is thus increased, resulting in a larger I_2. According to the soft-switching conditions listed in Table I, a larger I_2 in turn helps the input full bridge to achieve ZVS, as proven by waveforms shown in Fig. 15. As a result, efficiency of the DAB with the proposed modulation has increased from 88.4% to 94.8%. Here, efficiency of the converter has been thoroughly measured with a Precision Power Analyzer PPA5530. The values read during charging have been tabulated in Table IV and plotted as curves in Fig. 16. Clearly, Fig. 16(a) confirms that with SPS, efficiency of the DAB peaks close to $V_l = 1$ p.u., before drastically dropping as V_l increases. On the other hand, Fig. 16(b) shows that with SPS replaced by the proposed modulation when V_l rises above 1.3 p.u., efficiency of the DAB reverses and peaks again as V_l approaches 2 p.u.. Corresponding results for the discharging mode have also been given fromFigs. 17 to 20 and in Table V. Similar improvements, like a second peak efficiency close to $V_l = 2$ p.u., have again

TABLE IV
EFFICIENCY OF DAB DURING CHARGING

			Load (W)													
			200	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500
V_l (p.u.)	PWM 1	0.8	0.881	0.923	0.946	0.962	0.962	0.957	0.950	0.942	0.933					
		1.0	0.912	0.970	0.973	0.970	0.967	0.964	0.960	0.956	0.950	0.944	0.932			
		1.2	0.744	0.826	0.875	0.912	0.940	0.956	0.956	0.955	0.952	0.949	0.945	0.941	0.933	
		1.4	0.630	0.713	0.785	0.831	0.860	0.884	0.904	0.924	0.934	0.943	0.941	0.940	0.935	0.931
	PWM 2	1.4	0.871	0.905	0.930	0.945	0.955	0.948	0.941	0.926						
		1.6	0.892	0.922	0.946	0.963	0.963	0.958	0.952	0.944	0.931					
		1.8	0.906	0.944	0.970	0.971	0.967	0.963	0.958	0.953	0.947	0.937				
		2.0	0.907	0.972	0.972	0.970	0.967	0.965	0.961	0.957	0.951	0.947	0.935			
		2.2	0.824	0.886	0.932	0.956	0.964	0.964	0.961	0.959	0.954	0.951	0.946			

Note: "PWM 1" is the conventional SPS, "PWM 2" is the proposed modulation.

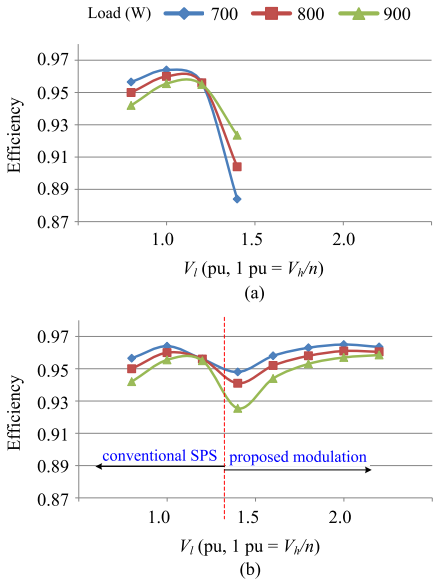


Fig. 16. Efficiencies of DAB obtained with (a) conventional SPS and (b) hybrid modulation during charging.

been observed with the proposed scheme. Efficient bidirectional features of the DAB have hence been ensured by simply activating the proposed modulation. It should however be mentioned that for optimal overall performance, the converter should be designed to deliver maximum load close to 1 or 2 p.u., at which efficiency peaks, rather than between them, where a minimum exists.

At times, it may also be of interest to analyze internal heat distribution among components of the DAB. For that, calculated loss breakdown is shown in Fig. 21, in case of V_l changing from 1 to 2 p.u. As seen, when V_l changes from 1 to 1.4 p.u., SPS modulation causes iron losses of the transformer P_{T_Fe} and inductor P_{Ls_Fe} to increase, since magnetic flux density B_m increases with voltage. Meanwhile, the output full bridge at a higher voltage changes from soft switching to hard switching, since I_2 changes from positive to negative. Its turn-on losses will hence increase significantly, as seen in Figs. 15 and 19. Simultaneously, turn-off losses of the input full bridge will also increase due to a higher I_1, as seen in–Figs. 15(a) and 19(a).

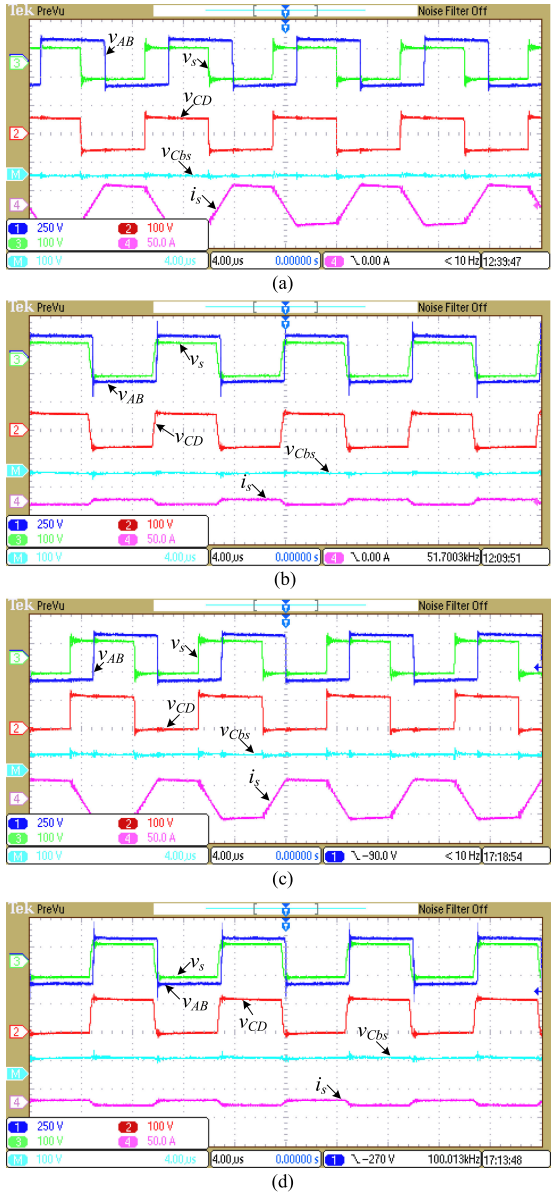


Fig. 17. Voltage and current waveforms of DAB during discharging when (a) $V_l = 1$ p.u. with full load and conventional SPS, (b) $V_l = 1$ p.u. with 1/6 load and conventional SPS, (c) $V_l = 2$ p.u. with full load and proposed modulation, and (d) $V_l = 2$ p.u. with 1/6 load and proposed modulation.

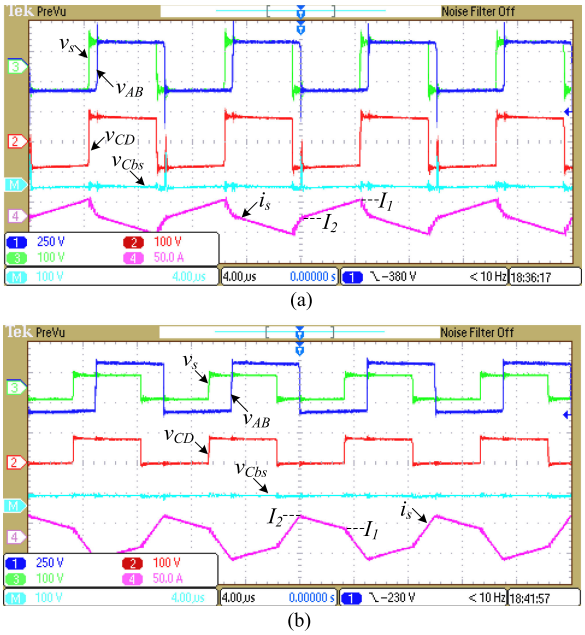


Fig. 18. Voltage and current waveforms obtained with (a) conventional SPS and (b) proposed modulation when $V_l = 1.4$ p.u. during discharging.

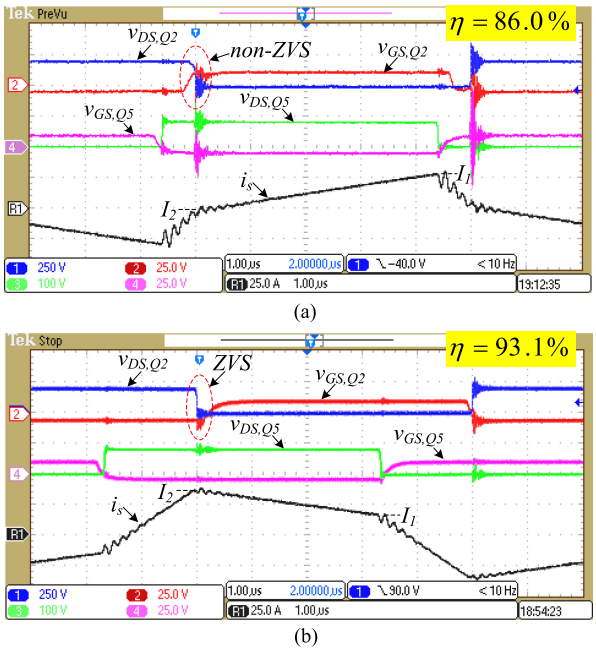


Fig. 19. ZVS performances obtained with (a) conventional SPS and (b) proposed modulation when $V_l = 1.4$ p.u. during discharging.

Instead, if SPS is replaced by the proposed modulation at $V_l = 1.4$ p.u., I_2 returns to positive, and the output full bridge changes from hard switching to soft switching again. Turn-off losses of the input full bridge also decreases, as I_1 becomes smaller. As V_l increases further to 2 p.u., I_2 becomes smaller, while I_1 becomes larger. Their respective effects are lower turn-off losses for the output full bridge and higher turn-off losses for the input full bridge. Deeper reduction of losses as V_l approaches 2 p.u. may also be justified from the smaller circulating power read from

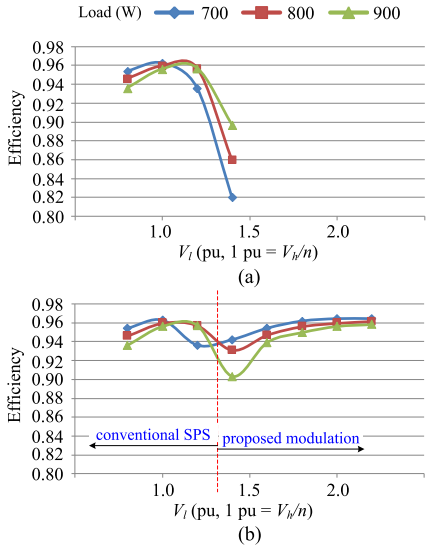


Fig. 20. Efficiencies of DAB obtained with (a) conventional SPS and (b) hybrid modulation during discharging.

Fig. 9, which will cause conduction losses of the full bridges and inductive components to be smaller. Magnetically, it should separately be emphasized that at $V_l = 1.4$ p.u., activation of the proposed modulation causes winding voltages to nearly halve. That causes iron losses of the transformer to drop prominently, but as V_l approaches 2 p.u., they increase with the winding voltages. This trend is however not followed by iron losses of the inductors, whose voltages and, hence, iron losses decrease, as V_l increases toward 2 p.u.

Next, dynamic transitions between charging and discharging modes of the DAB with the proposed modulation are shown in Fig. 22. As expected, the mode changes are realized by regulating phase angle between v_{AB} and v_{CD} from lagging to leading, and vice versa, as reflected by the two zoomed-in views at the top of Fig. 22. Transitions between SPS and the proposed modulation are also shown in Fig. 23, which according to the zoomed-in views at the top of the figure, have been realized gradually, rather than abruptly. To explain, it should be recapped that the proposed modulation requires phase leg formed by Q_7 and Q_8 to have zero duty cycle, while SPS requires it to have 50% duty cycle. These two requirements, respectively, result in those two v_{CD} waveforms shown in the first and third zoomed-in views at the top of Fig. 23. A smoother transition between them will then require the duty cycle to change gradually between 0 and 50%. As an example, an intermediate middle zoomed-in view has been inserted at the top of Fig. 23. That view shows a nonzero duty cycle smaller than 50% for the phase leg formed by Q_7 and Q_8, which has in turn caused v_{CD} to be positive over half a period, but negative over an interval shorter than half a period. In the remaining time, v_{CD} is at zero. Voltage v_{CD} is thus asymmetrical, which will in turn cause current i_s to become asymmetrical during the transitional time between modulation schemes. Nevertheless, the illustrated gradual transition is smooth with no large overshoot in voltage or current observed.

TABLE V
EFFICIENCY OF DAB DURING DISCHARGING

			Load (W)													
			200	300	400	500	600	700	800	900	1000	1100	1200	1300	1400	1500
V_l (p.u.)	PWM 1	0.8	0.906	0.933	0.953	0.963	0.959	0.954	0.946	0.936	0.916					
		1.0	0.876	0.924	0.965	0.970	0.966	0.963	0.960	0.956	0.950	0.942	0.931			
		1.2	0.730	0.805	0.855	0.892	0.918	0.936	0.957	0.957	0.956	0.952	0.947	0.940	0.934	
		1.4	0.568	0.628	0.680	0.732	0.781	0.820	0.860	0.897	0.920	0.934	0.942	0.946	0.941	0.939
	PWM 2	1.4	0.881	0.911	0.934	0.949	0.950	0.942	0.931	0.903						
		1.6	0.890	0.929	0.954	0.962	0.960	0.954	0.947	0.939	0.927					
		1.8	0.926	0.965	0.971	0.969	0.966	0.962	0.956	0.950	0.943	0.932				
		2.0	0.869	0.911	0.952	0.970	0.967	0.964	0.960	0.956	0.950	0.942	0.933			
		2.2	0.801	0.847	0.897	0.927	0.954	0.964	0.962	0.958	0.955	0.950	0.942			

Note: "PWM 1" is the conventional SPS, "PWM 2" is the proposed modulation.

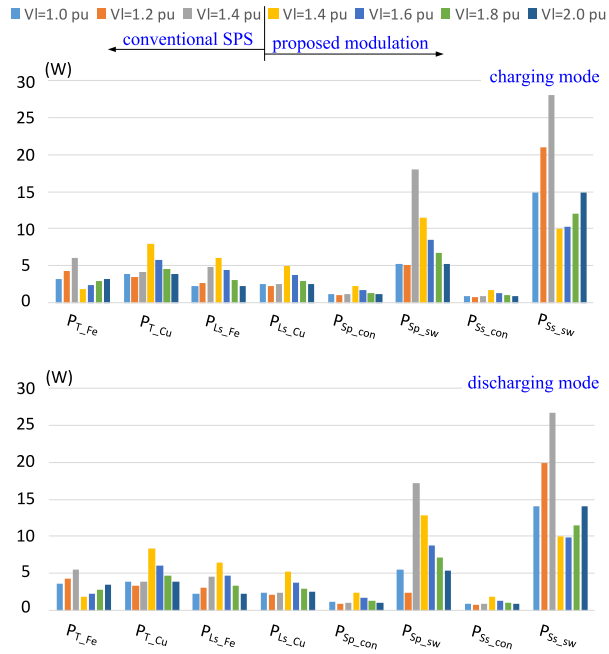


Fig. 21. Loss breakdown of DAB at 800 W with different V_l.

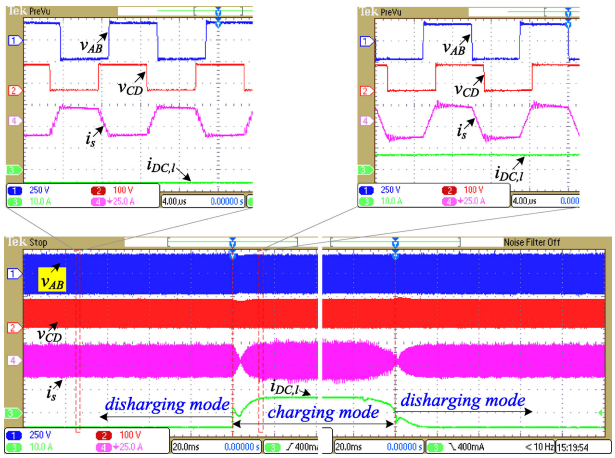


Fig. 22. Transitions between charging and discharging of DAB when controlled by proposed modulation.

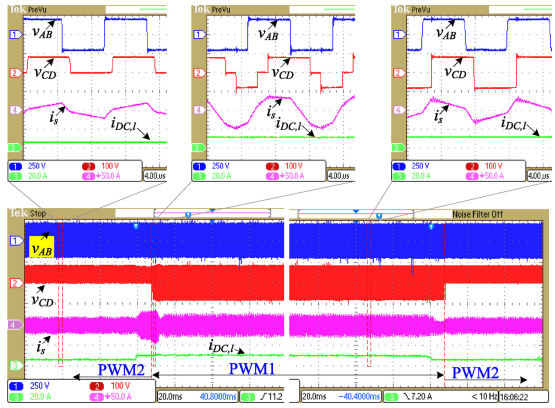


Fig. 23. Gradual transitions between conventional SPS and proposed modulation.

VIII. CONCLUSION

Conventional phase-shifted DAB converter can operate at a high efficiency, when its input and output dc voltages are close to 1 p.u., after accounting for transformer turns ratio. Such high efficiency is however not attainable, as its output voltage rises close to 2 p.u., at which soft switching becomes difficult to achieve and circulating power becomes high. A new modulation method has hence been proposed, whose main idea is to introduce a dc voltage drop across the dc blocking capacitor connected in series with the transformer. Results have shown that with the simple proposed modification, a DAB converter can retain soft switching and a reduced circulating power, even when its output voltage rises close to 2 p.u. The ideal hybrid modulation is thus to use SPS when its output dc voltage is close to 1 p.u. and the proposed technique when its output dc voltage is close to 2 p.u. The resulting efficiency curve then has two peaks at output voltage equal to 1 and 2 p.u. Consequently, the hybrid scheme is suitable for interfacing DAB with, for example, a battery, whose terminal voltage may vary widely depending on its state of charge.

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