A Constant-on-Time Control DC–DC Buck Converter With the Pseudowave Tracking Technique for Regulation Accuracy and Load Transient Enhancement

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***Abstract*—Constant-on-time (COT) control with an additional current feedback path in conventional buck converters can remove the need of large equivalent series resistance (ESR) at the output capacitor but it induces degraded output voltage regulation accuracy and slow transient response owing to opposite reaction between the output voltage and the additional current feedback information. Therefore, this paper proposes the pseudowave tracking (PWT) technique to reduce the load-dependent dc offset voltage of output load regulation while keeping the fast transient response similar to conventional COT buck converter with large ESR. The PWT technique further improves the transient response instantly by extending on-time and off-time periods during light-to-heavy and heavy-to-light load changes, respectively. The test chip fabricated in 28 nm CMOS process has demonstrated the improvement of offset voltage from 42 to 4 mV, while the transient response can be improved to 4 and 5 μs with load changes from 0.3 to 1.7 A and vice versa, respectively.**

***Index Terms*—Additional current feedback path (ACFP), buck, conventional constant-on-time (COT) control, equivalent series resistance (ESR), pseudowave tracking (PWT) technique.**

I. Introduction

POWER management integrated circuit (IC) design for versatile development of the Internet of Things (IoT) needs more deliberate performance enhancement because the supplying voltage for IoT is greatly decreased due to the usage of small volume batteries. Owing to the usage of small volume batteries, the light-load efficiency becomes more critical for long-term operation, especially in sleeping mode. As we know, improvement of light-load efficiency of IoT for the extension of battery usage lifetime relies on the structure of the power converter. Therefore, it is suitable to select constant-on-time (COT) control to meet the requirements from IoT because COT control has the advantages of fast transient response and small transient voltage variation in case of any load changes while light-load efficiency is kept high due to variable switching frequency at light or no loads [1]–[13].

An ideal operation example of IoT is shown in Fig. 1. Robust and regulated supply voltage from the power converter lets the processor operate smoother. However, in a real case with a non-ideal power supply in Fig. 2, the processor of IoT usually has variable load changes in active modes and causes large disturbance on its supply voltage. If the disturbance induces too low supply voltage, the processor inserts "Idle" instructions to ensure correct operation. The processor reduces load current to maintain the performance until the power converter recovers its supply voltage back to the rated voltage. Although the operation can be maintained, it results in an extra processing time and much power loss. In conclusion, the demands for power management integrated circuit (IC) design for IoT become more stringent. It is necessary to improve some disadvantages of conventional COT control to meet the requirements including small volume, small output voltage ripple, and reliable output voltage for IoT. Even at no load condition, the power consumption of the power converter needs to be reduced to near zero for power savings [1]–[8].

Compact-size IoT applications need low supply voltage droop in case of any load change. An ideal solution is an integrated COT controlled step-down converter with a multilayer ceramic capacitor (MLCC), which provides high efficiency, simple structure, and fast transient response. Nevertheless, conventional COT control demands the product of $C_{\rm CO}$ and $R_{\rm ESR}$ larger than half of the on-time ($T_{\rm ON}$) to meet stability criteria. Low $R_{\rm ESR}$ of the MLCC causes instability of the COT control, although small output voltage variation can be ensured. Tradeoffs between stability and voltage variation are depicted in Fig. 3.

In [14] and [15], the additional current feedback path (ACFP) technique is proposed to release the stability constraint of large

Manuscript received May 29, 2017; revised July 16, 2017; accepted August 14, 2017. Date of publication August 28, 2017; date of current version March 5, 2018. Recommended for publication by Associate Editor S.-C. Tan. *(Corresponding author: Ke-Horng Chen.)*

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Digital Object Identifier 10.1109/TPEL.2017.2746659

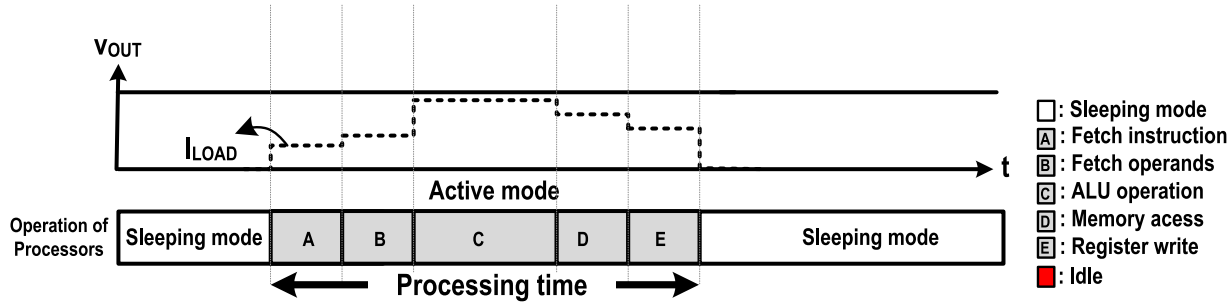


Fig. 1. Operations of the processor of IoT under ideal supply voltage ($V_{\rm OUT}$) from the power converter.

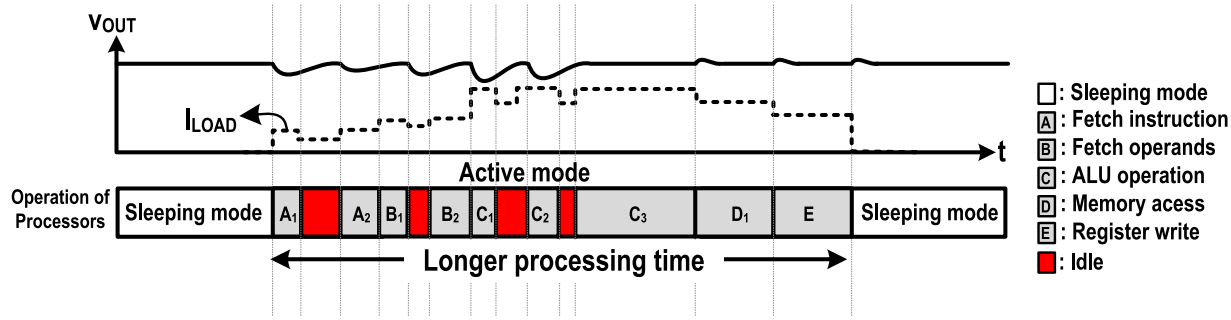


Fig. 2. Operations of the processor of IoT under nonideal supply voltage ($V_{\rm OUT}$) from the power converter.

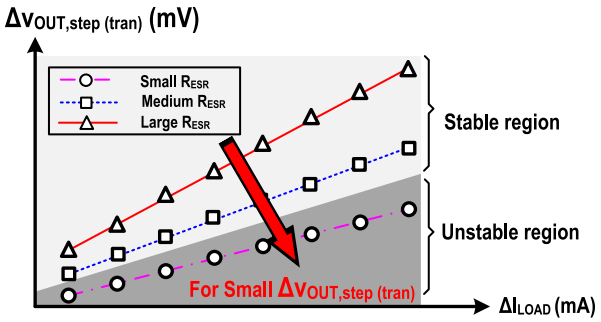


Fig. 3. Output voltage ripple versus load current change with the highlighted unstable region.

$R_{\rm ESR}$ but results in large voltage variation and longer recovery time. Therefore, when using a small $\rm R_{ESR}$, (1) fast transient response, (2) small output voltage variation, and (3) the increase of stability are required to achieve low supply voltage droop in case of load variation. Consequently, high performance of the power converter can speed up the operation of the processor of IoT with high efficiency.

This paper proposes the pseudowaveform tracking (PWT) technique to have small output voltage variation, fast transient response, and improved stability at the same time. The paper is organized as follows. Section II discusses the stability of the ACFP technique and shows how the ACFP technique causes the deterioration of accuracy due to the additional current information $v_{\rm SEN}$. Section III illustrates how the derived PWT technique effectively reflects an accurate inductor current information and improves the transient response by removing the additional current information $v_{\rm SEN}$. Section IV demonstrates the circuit implementations. Experimental results are shown in Section V. Finally, Section VI concludes the paper.

II. Stability and Offset Voltage in the ACFP Technique

ACFP technique has been proposed to reduce the COT converter's physical size and cost using the ceramic capacitor with a small $R_{\rm ESR}$. Fig. 4 shows the COT converter with an additional current feedback signal $v_{\rm SEN}$ through the $R_{\rm SEN}$ as (1) to represent the transfer function from the current signal $i_{\rm SEN}$ to the voltage signal $v_{\rm SEN}$. The $v_{\rm SEN}$ is linearly proportional to the inductor current $i_{\rm SEN}$

$$R_{\rm SEN} = \frac{v_{\rm SEN}}{i_{\rm SEN}}. \tag{1}$$

The summation signal $v_{\rm SUM}$ composed of $v_{\rm SEN}$ and $v_{\rm FB}$ is applied to regulate $v_{\rm OUT}$ by comparing with the $V_{\rm REF}$ to generate the pulse width modulation (PWM) signal $V_{\rm PWM}$. The sensed inductor current ripple information $v_{\rm SEN}$ is injected to the feedback to release the stability constraint of large $R_{\rm ESR}$ in a conventional COT converter. The switching operation point from the off-time to the on-time can be adequately determined by the $v_{\rm SUM}$ in the ACFP technique. The transfer function after applying the ACFP technique is derived in (2) as the on-time period $T_{\rm ON}$ is small [16]–[19]

$$\frac{v_{\rm OUT}}{v_{\rm REF}} \approx \frac{sR_{\rm ESR}C_{\rm OUT}+1}{1+\frac{s}{Q_s\omega_s}+\frac{s^2}{\omega_s^2}} \quad \text{where } \omega_s = \frac{\pi}{T_{sw}},$$
$$\text{and } Q_s = \frac{T_{sw}}{\left[\left(\frac{R_{\rm SEN}}{R_{\rm ESR}}+1\right)R_{\rm ESR}C_{\rm OUT}-\frac{T_{\rm ON}}{2}\right]\pi}. \tag{2}$$

To get rid of the unexpected right-half plane poles, (3) is derived since $Q_{\rm s}$ needs to be larger than zero

$$R_{\rm SEN} > \left(\frac{T_{\rm ON}}{2R_{\rm ESR}C_{\rm OUT}}-1\right)R_{\rm ESR}. \tag{3}$$

In the ACFP technique, the external current information $v_{\rm SEN}$ equivalently increases the effective value of $R_{\rm ESR}$ by the factor

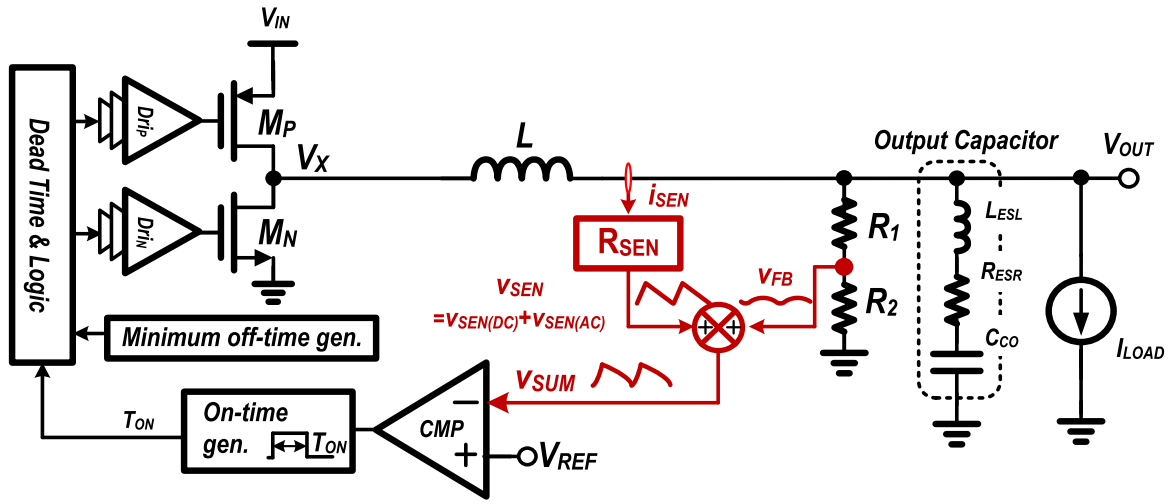


Fig. 4. COT control utilizes the ACFP technique to increase the stability when the output capacitor is MLCC.

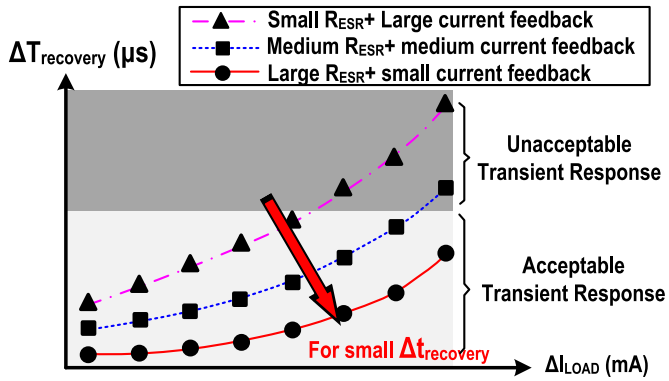


Fig. 5. Relationship between the ESR and the amount of current feedback in the ACFP technique.

of $(R_{\rm SEN}/R_{\rm ESR}+1)$ to release the stability constraint of large $R_{\rm ESR}$ in a conventional COT converter. Nevertheless, the output voltage accuracy and load regulation are seriously affected by the ACFP technique because the $v_{\rm SEN}$ is composed of $v_{\rm SEN(dc)}$ and $v_{\rm SEN(ac)}$. The $v_{\rm SUM}$ is dominated by the $v_{\rm SEN}$ to meet the requirement of (3). Unfortunately, the ACFP technique loses the $V_{\rm OUT}$ tracking ability compared to a conventional COT converter with a large $R_{\rm ESR}$. The duty is determined by comparing the $V_{\rm REF}$ with the summation signal $v_{\rm SUM}$ that is composed of $v_{\rm FB}$ and $v_{\rm SEN(ac)}$. The opposite reaction among current feedback information $v_{\rm SEN(ac)}$ and output feedback voltage $v_{\rm FB}$ slows down the transient response. That is, the controller difficultly detects the perturbation at the $v_{\rm OUT}$ caused by load transient response if much current information is injected. Overall performance becomes worse due to large voltage variation and longer recovery time. On the other hand, although reduced $v_{\rm SEN(ac)}$ has $v_{\rm FB}$ dominating the $v_{\rm SUM}$, the system needs another large $R_{\rm ESR}$ to increase stability. Fig. 5 illustrates the trade-off among the transient recovery time, the amount of additional current information, and the value of $R_{\rm ESR}$.

Conventional COT control uses large $R_{\rm ESR}$ to get the sensing signal in phase with the inductor current. When step-up load current occurs, conventional COT control increases the switching frequency due to the insertion of minimum off-time to rapidly recover the $v_{\rm OUT}$, as shown in Fig. 6(a). In contrast, Fig. 6(b) shows the converter without the minimum off-time period since the $v_{\rm SUM}$ is raised higher than the $V_{\rm REF}$ by the additional inductor current information in the ACFP technique. On the other hand, conventional COT control extends the off-time period until the $v_{\rm OUT}$ is pulled low to the $V_{\rm REF}$ by the output load current, as shown in Fig. 7(a), when step-down load current occurs. Redundant on-time periods in the ACFP technique are generated when the $v_{\rm SUM}$ in Fig. 7(b) is pulled down to approach the $V_{\rm REF}$ by the additional current formation, which is not in phase with the $v_{\rm OUT}$. It is not necessary to generate the redundant on-time periods in case of heavy-to-light load change as charges have accumulated at the $v_{\rm OUT}$. Redundant on-time periods induce extra energy being stored at the $v_{\rm OUT}$ and prolong the recovery time of the $v_{\rm OUT}$, which is a disadvantage for the ACFP technique. In conclusion, higher minimum off-time periods are required in case of light-to-heavy load change, while redundant on-time periods have to be moved in case of heavy-to-light load change.

In the ACFP technique of Fig. 4, the additional current signals including dc information $v_{\rm SEN(dc)}$ and ac information $v_{\rm SEN(ac)}$ constitute the summing signal $v_{\rm SUM}$ as expressed in (4) where $v_{\rm FB}$ is the feedback signal from the $v_{\rm OUT}$ with the feedback gain β (<1) that is equal to $R_2/(R_1+R_2)$

$$v_{\rm SUM}=v_{\rm SEN(ac)}+v_{\rm SEN(dc)}+v_{\rm FB}\ \text{where}\ v_{\rm OUT}=\frac{1}{\beta}\cdot v_{\rm FB}. \tag{4}$$

Because of the valley voltage control used in the COT control technique, the valley voltage of $v_{\rm SUM}$ is equal to the reference voltage $V_{\rm REF}$ by the comparator (CMP). Thus, the valley voltage $v_{\rm SUM(valley)}$ is shown in (5). Owing to (4) and (5), the $v_{\rm OUT}$ is derived as follows (6):

$$v_{\rm SUM(valley)}=V_{\rm REF}=v_{\rm SEN(dc)}-\frac{1}{2}v_{\rm SEN(ac)}+v_{\rm FB} \tag{5}$$

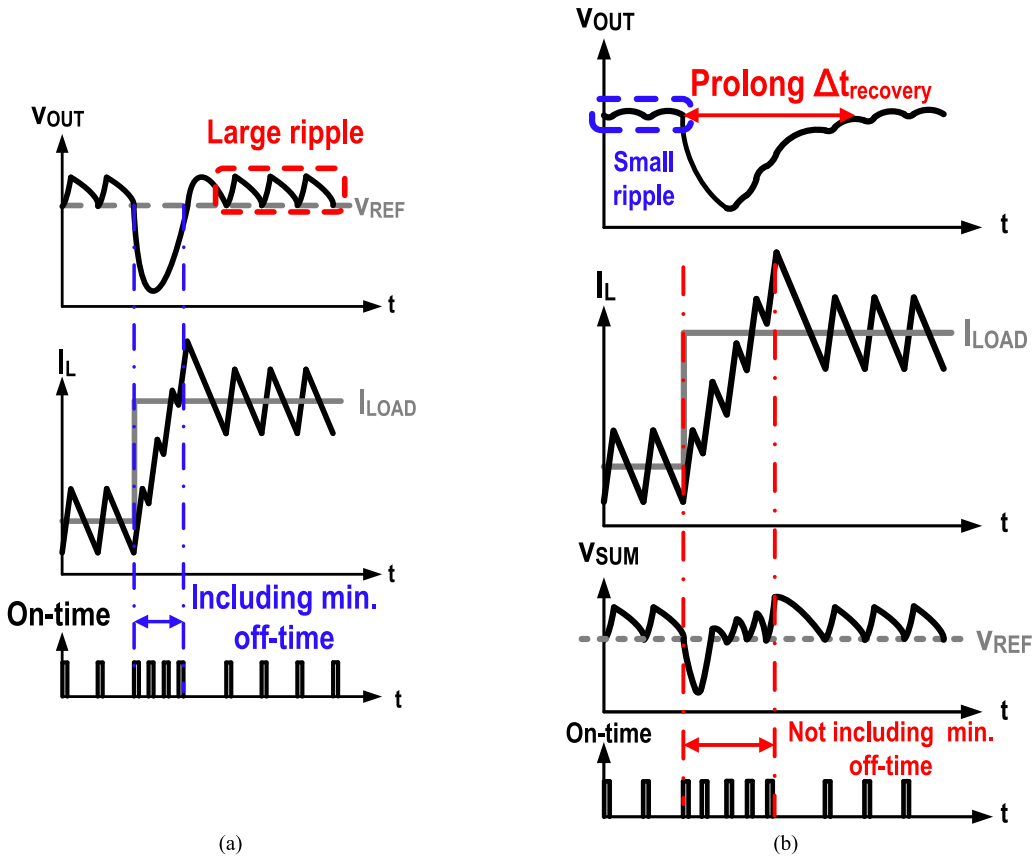


Fig. 6. Transient response waveforms when load current changes from light to heavy. (a) In conventional COT control technique. (b) In the ACFP technique.

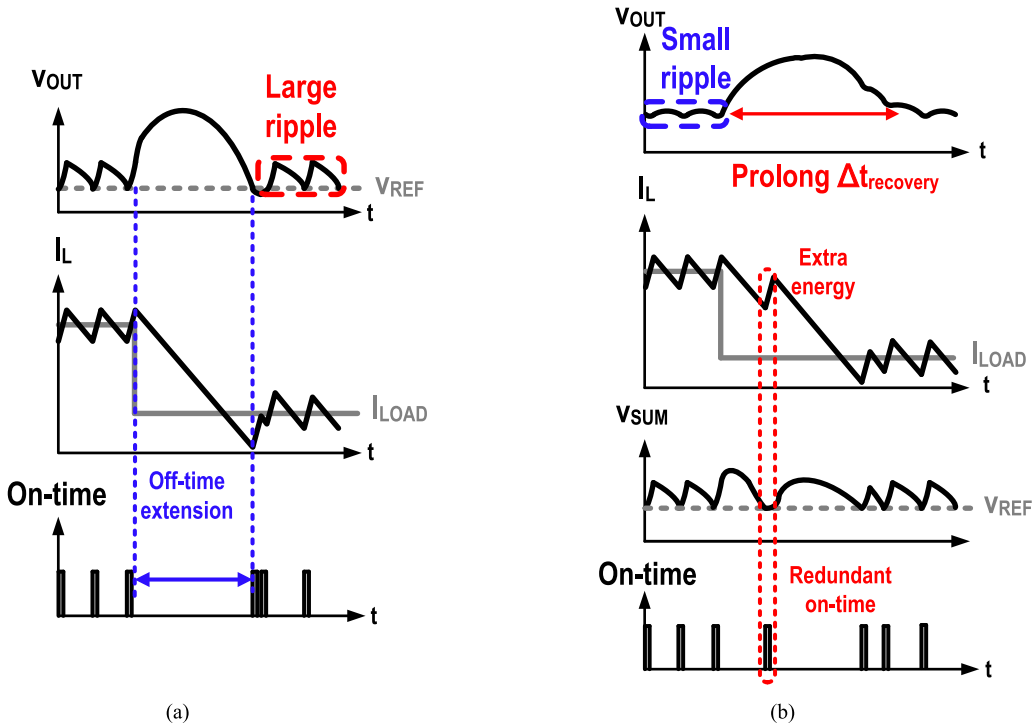


Fig. 7. Comparison of heavy-to-light transient response in conventional COT and ACFP techniques. (a) Conventional COT control uses off-time extension to reduce overshoot. (b) ACFP technique suffers from the disadvantage due to loosely tracking V_{OUT} information.

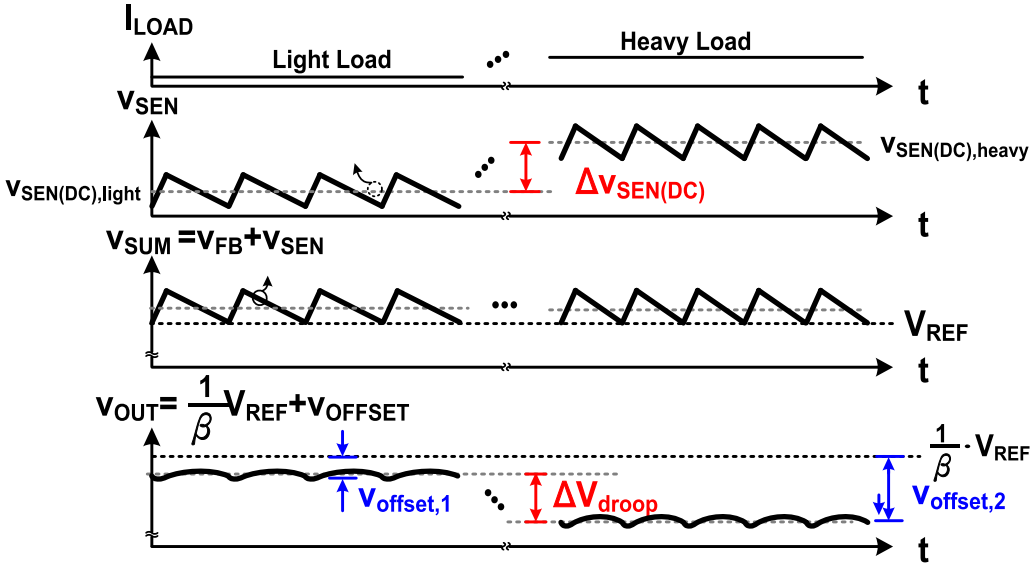


Fig. 8. v_{OUT} performs poor regulation owing to the additional inductor current information in COT control.

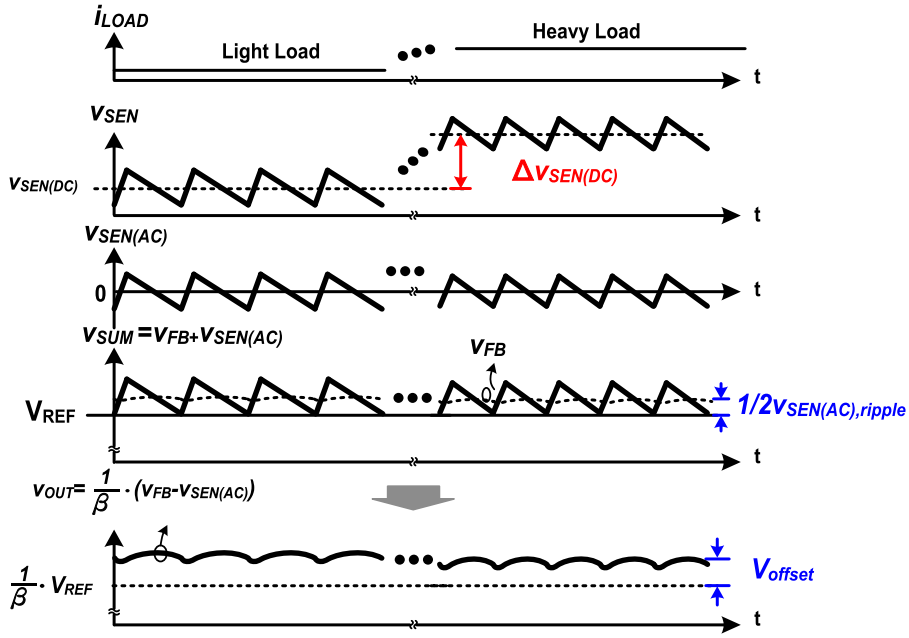


Fig. 9. v_{OUT} performs poor regulation owing to the $v_{\mathrm{SEN(ac)}}$ injected by the ACFP technique in COT control.

$$v_{\mathrm{OUT}} = \frac{1}{\beta}\left(V_{\mathrm{REF}} + \frac{1}{2}v_{\mathrm{SEN(ac)}} - v_{\mathrm{SEN(dc)}}\right). \tag{6}$$

The v_{OUT} can be further rewritten as (7) where the output offset voltage v_{OFFSET} is defined as (8) to stand for the offset voltage due to the COT control technique

$$v_{\mathrm{OUT}} \approx \frac{1}{\beta}V_{\mathrm{REF}} + v_{\mathrm{OFFSET}} \tag{7}$$

$$\text{where } v_{\mathrm{OFFSET}} = \frac{1}{\beta}\cdot\left(\frac{1}{2}v_{\mathrm{SEN(ac)}} - v_{\mathrm{SEN(dc)}}\right). \tag{8}$$

As discussed in (3), if considering the stability issue, the R_{SEN} should be sufficiently large to get an adequately large v_{SEN} but it deteriorates the voltage accuracy due to large deviation from the V_{REF}. Moreover, in consideration of v_{OUT} regulation of the ACFP technique, (8) reveals that the offset voltage v_{OFFSET} is mainly contributed by $v_{\mathrm{SEN(dc)}}$ and $v_{\mathrm{SEN(ac)}}$. Since $v_{\mathrm{SEN(dc)}}$ is load dependent, the v_{OFFSET} results in load-dependent droop voltage $\Delta V_{\mathrm{droop}}$, as shown in Fig. 8. The voltage accuracy can be improved by carefully removing the inaccurate deviation caused by $v_{\mathrm{SEN(dc)}}$ and $v_{\mathrm{SEN(ac)}}$.

Adding one extra capacitor can filter out the $v_{\mathrm{SEN(dc)}}$ from the v_{OFFSET}, but the $v_{\mathrm{SEN(ac)}}$ still causes unacceptable offset

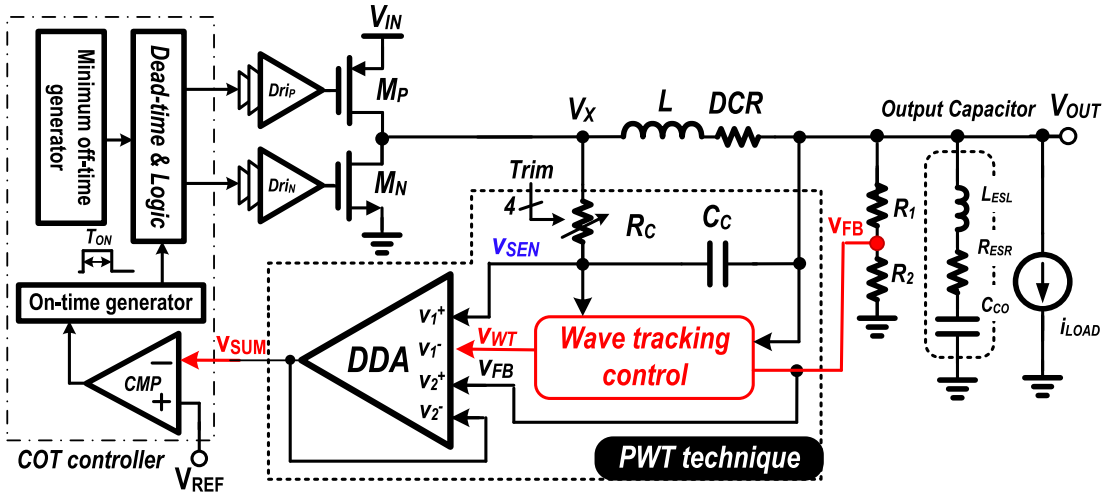


Fig. 10. COT control with the proposed PWT technique increases the stability even when the output capacitor is MLCC.

voltage, as shown in Fig. 9. The v_{OUT} in (9) with the remaining offset voltage caused by $v_{\mathrm{SEN(ac)}}$ remains load dependent, and the accuracy is affected by load current condition

$$v_{\mathrm{OUT}} \approx \frac{1}{\beta} V_{\mathrm{REF}} + \frac{1}{2\beta} v_{\mathrm{SEN(ac)}}. \tag{9}$$

III. Proposed PWT Technique

Fig. 10 illustrates the proposed PWT technique in COT control dc–dc buck converter. First, the accuracy is improved by the PWT technique, as shown in Fig. 9 and (9). The dc offset voltage is dominated by the $v_{\mathrm{SEN(ac)}}$. One half of $v_{\mathrm{SEN(ac)}}$ can be used to compensate the dc offset voltage. The sample-and-hold function senses and detects the valley voltage of the v_{SEN} as the signal V_{WT} [20]. Following the valley voltage control, the valley voltage of v_{FB} in the beginning of every on-time period is reset to V_{REF} by the CMP, so the valley of v_{SEN} is reset to zero.

As shown in Fig. 11, the v_{SEN} is the sensing signal including the ac and dc of i_{L} where v_{WT} is equal to the valley voltage of v_{SEN}. Subtracting the v_{WT} from the v_{SEN}, the $v_{\mathrm{SEN(ripple)}}$ is derived because its valley voltage is set to zero. Consequently, in comparison of Fig. 9, the $v_{\mathrm{SEN(ripple)}}$ is shifted upward the value of $1/2 * |v_{\mathrm{SEN(ac)}}|$ compared to $v_{\mathrm{SEN(ac)}}$. That is, the $v_{\mathrm{SEN(ripple)}}$ in Fig. 11 is the difference between v_{SEN} and v_{WT}, which can be viewed as a shifted signal of the $v_{\mathrm{SEN(ac)}}$ in Fig. 9. When the valley of v_{SUM} is regulated at V_{REF}, the v_{FB} is regulated at V_{REF} without any unexpected voltage deviation due to $v_{\mathrm{SEN(ac)}}$. That is, the v_{OUT} is modified from (6) to (10) as $v_{\mathrm{SEN(ac)}}$ and $v_{\mathrm{SEN(dc)}}$ are removed. Similarly, when the value of ESR is sufficiently low since MLCC is used, the v_{OUT} is approximately equal to $(1/\beta) * V_{\mathrm{REF}}$ even under any different loading conditions. In other words, load regulation is greatly improved

$$\begin{aligned} v_{\mathrm{OUT(dc)}} &= \frac{1}{\beta} \cdot V_{\mathrm{REF}} + \frac{1}{2} v_{\mathrm{OUT,ripple}} \\ &\approx \frac{1}{\beta} \cdot V_{\mathrm{REF}} \text{ if } v_{\mathrm{OUT,ripple}} \text{ is small.} \end{aligned} \tag{10}$$

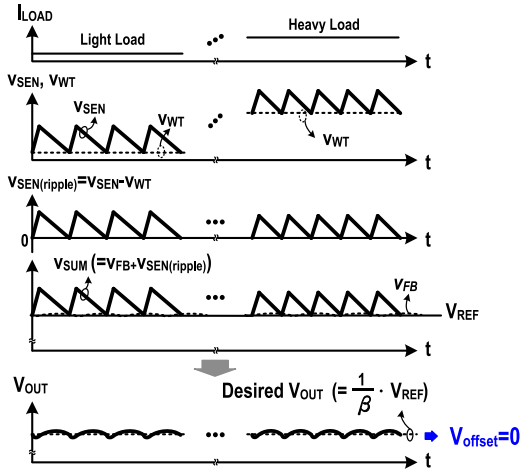


Fig. 11. Operation waveforms of the proposed PWT technique in steady state.

Although the PWT technique increases the system stability while the output offset is reduced at the same time, the PWT technique suffers from slow transient response because of the opposite trend among the inductor current and output voltage variation. Moreover, owing to large holding capacitor (a few of pico-Farads) in the S/H circuit for reducing interference, the transient response is seriously slowed down. As a result, nonzero valley voltage $V_{\mathrm{OUT,delay}}$ in Fig. 12 causes the v_{SEN} containing the dc variation of i_{L}, which performs an opposite trend compared to output voltage variation. The v_{WT} is unable to track the v_{SEN} in time because of large change at the v_{SEN}. The v_{SEN} in Fig. 12(a) is raised up forward by the additional $v_{\mathrm{OUT,delay}}$ to cause nonobvious change at the v_{SUM} even in case of large light-to-heavy load variation. That is the reason why the v_{OUT} suffers from large voltage drop. This phenomenon occurs similarly when load changes from heavy to light, as shown in Fig. 12(b), where a negative $v_{\mathrm{OUT,delay}}$ occurs. Reflecting opposite signal $v_{\mathrm{OUT,delay}}$ seriously slows down the transient response.

Therefore, the proposed PWT technique is modified to get both high accuracy and fast transient response simultaneously.

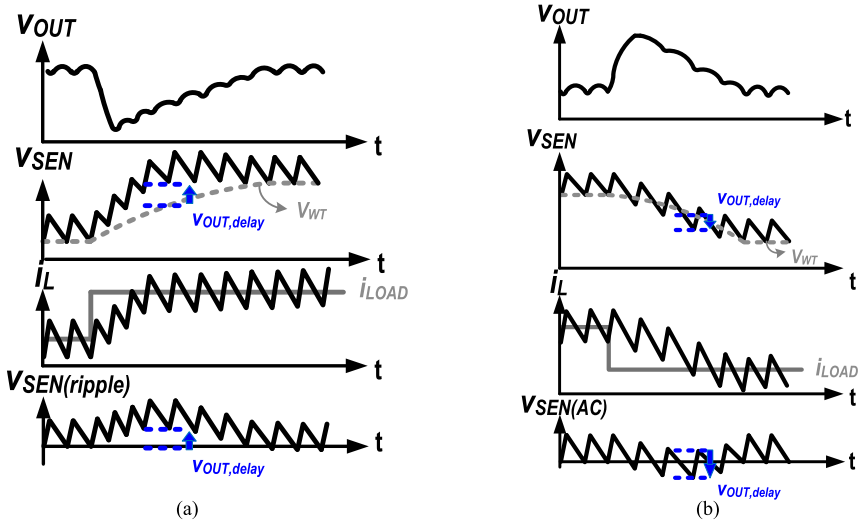


Fig. 12. Transient response in the PWT technique without transient enhancement in case of (a) light-to-heavy and (b) heavy-to-light load changes.

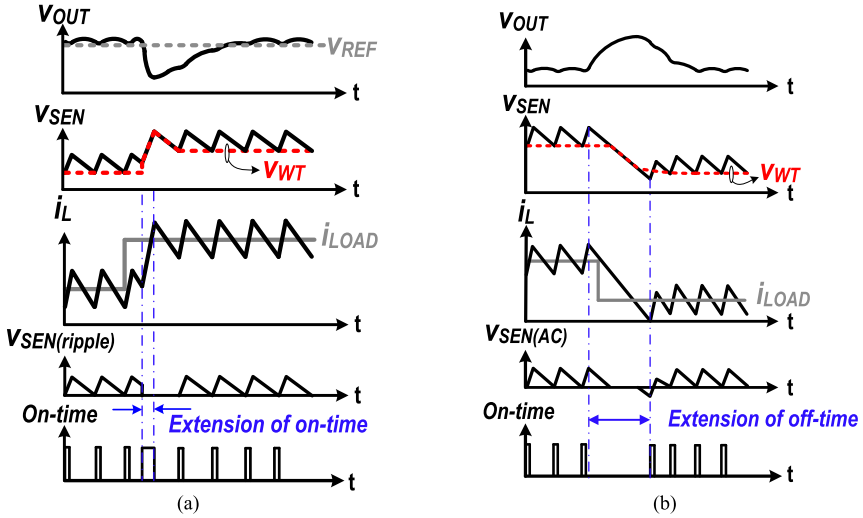


Fig. 13. Transient response in the proposed PWT technique is effectively improved in case of (a) light-to-heavy and (b) heavy-to-light load changes.

That is, improved transient response can be achieved in the PWT technique if the tracking method is changed from the valley tracking to real-time waveform tracking, as shown in Fig. 13, so the $v_{\rm WT}$ is directly connected to the $v_{\rm SEN}$ when using real-time waveform tracking. The controller is set back to the conventional COT control for fast transient response by removing opposite inductor current information in comparison of the $v_{\rm OUT}$. The $v_{\rm SUM}$ in fact reflects the real-time $v_{\rm OUT}$ information. Moreover, to further enhance the transient speed, the minimum off-time is removed to extend the duty to 100% once the controller detects twice continuous minimum off-times. Both the elimination of opposite inductor current and the extension of the duty can accelerate the overall transient response.

IV. Circuit Implementation

The proposed PWT technique in Fig. 10 includes the inductor current sensor (C_C and R_C), the wave tracking control circuit, and the dual differential amplifier (DDA).

A. Inductor Current Sensor

In Fig. 10, C_C and R_C constitute the inductor current sensor to estimate ac and dc inductor current information. Thus, the $v_{\rm SEN}$ in (11) contains the inductor current information by the direct current resistance (DCR) resistance of the inductor. However, (11) is frequency dependent because one pole ω_P and one zero ω_Z exist [21]. The relationship between ω_P and ω_Z directly affects the performance of transient response and the output voltage ripple

$$v_{\rm SEN} = v_{\rm OUT} + i_L \cdot {\rm DCR} \cdot \left(\frac{1+\frac{s}{\omega_Z}}{1+\frac{s}{\omega_P}} \right)$$
$$\text{where } \omega_P = \frac{1}{R_C C_C}, \omega_Z = \frac{\rm DCR}{L}. \tag{11}$$

If perfect pole-zero cancellation exists in (12), the $v_{\rm SEN}$ is exactly proportional to the $i_{\rm L}$. However, in reality, it is difficult

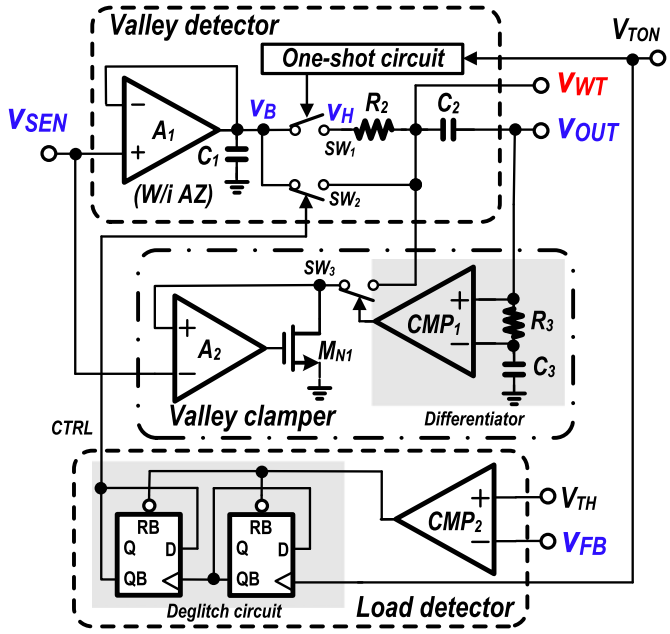


Fig. 14. Schematic of the PWT control circuit.

to have perfect pole-zero cancellation

$$\frac{1}{R_C C_C} = \frac{\mathrm{DCR}}{L}. \tag{12}$$

Phase lead or lag occurs if imperfect pole-zero cancellation is considered. Phase lead that zero is below pole causes the v_{SUM} to have more i_L information to improve system stability. In implementation, a trimming mechanism is applied to the R_C for ensuring pole-zero cancellation and achieving optimized transient and steady performance. The information from the output voltage ripple is much less than that in conventional COT control with large R_{ESR}. The advantage is low output voltage ripple at the cost of reduced v_{OUT} tracking ability at the v_{SUM}. In case of any load variation, the feedback loop loosely tracks the v_{OUT} and thus large undershoot/overshoot and long recovery time occur. In contrast, phase lag that pole is below zero causes the v_{SUM} to have less i_L information. The system stability needs large output voltage ripple information from the v_{OUT}. Better transient response including small undershoot/overshoot voltage and improved recovery time are derived because the v_{SUM} closely tracks the v_{OUT}, but the system suffers from small noise margin and the stability becomes a critical problem, which is similar to conventional COT control with small R_{ESR}.

B. PWT Control

Fig. 14 depicts the circuit implementation of the PWT technique. Mainly, it contains three blocks including the valley detector, the valley clamper, and the load detector. In the valley detector, the input signal v_{SEN} contains the v_{OUT} information and the complete i_L information as expressed in (13) where $v_{\mathrm{SEN(valley)}}$ and $v_{\mathrm{SEN(ripple)}}$ are the valley voltage and ripple value of the v_{SEN} respectively, if frequency-dependent term is small under a perfect pole-zero cancellation

$$v_{\mathrm{SEN}} = v_{\mathrm{OUT}} + i_L \cdot \mathrm{DCR} = v_{\mathrm{SEN(ripple)}} + v_{\mathrm{SEN(valley)}}. \tag{13}$$

The unit gain buffer A_1 with a sufficient driving capability and an auto zeroing mechanism [22] holds the v_{SEN} at the v_B and ensures the v_B is equal to the v_{SEN} without undesired offset voltage. In turn, the output of the one-shot circuit controls ON/OFF of the switch SW_1. Thus, the on-time signal $V_{T_{\mathrm{ON}}}$ is used to trigger the one-shot circuit and to sample and hold the valley voltage of v_B at the v_H in the beginning of every switching period. Moreover, the v_{WT} can derive the valley voltage $v_{\mathrm{SEN(valley)}}$ by the v_H after removing the $v_{\mathrm{OUT(ac)}}$ through the use of the filter R_2 and C_2. Finally, v_H and v_{WT} are expressed in (14) and (15), respectively

$$v_H = v_{\mathrm{SEN(valley)}} + v_{\mathrm{OUT(ac)}} \tag{14}$$

$$v_{\mathrm{WT}} = v_{\mathrm{SEN(valley)}}. \tag{15}$$

In case of light-to-heavy step load change in Fig. 12(a), the $v_{\mathrm{OUT,delay}}$, which is the difference voltage between the v_{SEN} and the v_{WT}, occurs at v_B due to large holding capacitor C_1 and slows down the transient response. For fast transient response, the PWT technique directly connects the v_{WT} to the v_B to closely track v_{SEN} and v_{OUT} accurately and rapidly. Owing to accurate reflection of the v_{OUT} information, the on-time period can be effectively extended. After the transient response, the v_{WT} tracks the $v_{\mathrm{SEN(valley)}}$ again to eliminate the offset voltage in steady state. The comparator CMP_2 with the deglitch function works as the load detector to determine when the v_{WT} needs to track the v_{SEN} or the $v_{\mathrm{SEN(valley)}}$. The v_{WT} tracks the v_{SEN} by the logic high signal control to turn ON SW_2 when the v_{FB} is less than the v_{TH} that is the predefined threshold voltage.

The PWT technique also provides the valley clamper to speed up the transient response in case of heavy-to-light load change. The valley clamper only has the pull-down ability by the operational amplifier A_2 and the transistor M_{N1} to ensure that v_{WT} follows the descending v_{SEN}. Owing to heavy-to-light change, any instant step-up variation at v_{SEN} may cause large overshoot at the v_{OUT} if the v_{WT} tracks the step-up v_{SEN}. Thus, the valley clamper works correctly only by turning ON SW_3 when the heavy-to-light load change occurs. Here, the differentiator, which is composed of the comparator CMP_1, R_3, and C_3, is used to determine when the heavy-to-light load change occurs. Fig. 15 shows the overall flow chart of the PWT technique.

C. DDA Design

The DDA circuit shown in Fig. 16 is a folded-cascode operational transconductance amplifier (OTA) with two input pairs, which can process the dc and ac signals to generate the v_{SUM} for effectively removing the offset voltage. Due to negative feedback, the relationship between v_1^+, v_1^-, v_2^+ and v_2^- can be derived as follows:

$$v_1{}^+ - v_1{}^- = -(v_2{}^+ - v_2{}^-). \tag{16}$$

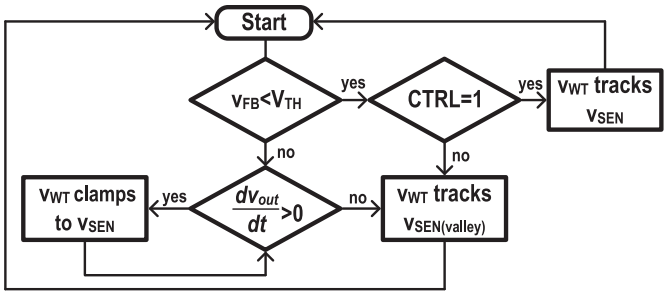


Fig. 15. Flow chart of the proposed PWT control.

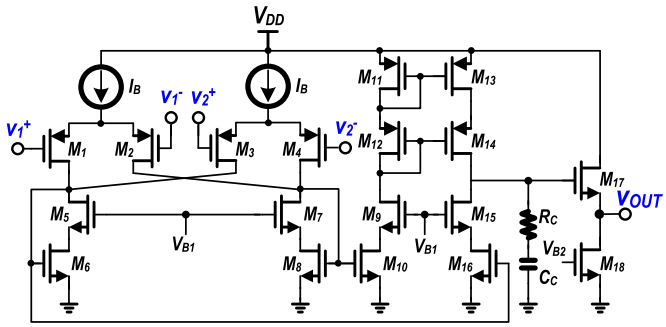


Fig. 16. Schematic of DDA.

TABLE I
PERFORMANCE OF THE COT CONVERTER

Process	United Microelectronics Corporation (UMC) 28 nm
Input voltage ($V_{\rm IN}$)	2.6–3.63 V
Output voltage ($V_{\rm OUT}$)	1.05 V
Load range ($I_{\rm LOAD}$)	300 mA–1.7 A
Inductor	1 μH
DCR	30 mΩ
Output capacitor	4.7 μF
$R_{\rm ESR}$	4 mΩ
Operation frequency	2.5 MHz
Maximum efficiency	94%

The $v_{\rm SEN}$ and the $v_{\rm WT}$ connect to v_1^+ and v_1^-, respectively, and the $v_{\rm FB}$ connects to v_2^+. Because of negative feedback, the $v_{\rm SUM}$ connects to v_2^-. As a result, (17) expresses the $v_{\rm SUM}$, and (18) can be derived by (17) due to (15)

$$v_{\rm SUM} = v_{\rm FB} + v_{\rm SEN} - v_{\rm WT} \tag{17}$$

$$v_{\rm SUM} = v_{\rm FB} + v_{\rm SEN(ripple)}. \tag{18}$$

V. EXPERIMENTAL RESULTS

The test chip of COT converter with the proposed PWT technique is fabricated in standard 28 nm CMOS process. According to the design guideline [23], the off-chip inductor and the capacitor are selected as 1 and 4.7 μF, respectively, and the specifications of the proposed converter are listed in Table I. The nominal switching frequency is near 2.5 MHz and the output voltage is 1.05 V with the input voltage ranging from 2.6 to 3.63 V. To eliminate the offset (around 20 mV) resulted from the bandgap reference and CMP, a trimming mechanism is applied. For fair comparison, the settings of bandgap reference and feedback resistor trimming are fixed under all the measurements. Fig. 17 shows the chip micrograph of the proposed COT control.

Fig. 18(a) shows that the waveforms of the proposed COT control in steady state have ripple $\Delta V_{\rm ripple}$ as small as 6 mV because of using small ESR. The output voltage is 1.05 V as $V_{\rm IN}$ is 3.3 V, the $I_{\rm LOAD}$ is 0.4 A, and the switching frequency is 2.5 MHz. The i_L is the inductor current and the L_X is the node that connects inductor high-side and low-side MOSFET. The $R_{\rm ESR}$ is about 4 mΩ and the $C_{\rm OUT}$ is 4.7 μF. According to conventional stability criteria, the switching frequency should be higher than 10 MHz, but experimental results show that the system stability is guaranteed even under the low switching frequency of 2.5 MHz since the PWT technique is able to reduce the limitation of the stability criteria. However, according to (12), the L and DCR are 1 μH and 30 mΩ, and the R_C and C_C in current sensor are 340 KΩ and 100 pF, respectively. On the other hand, the switching frequency decreases when load current becomes small, as shown in Fig. 18(b). The advantage is high efficiency at light loads due to the decrease of switching loss.

Fig. 19 shows the experimental results of a controller according to (9). In Fig. 19, the waveform of the COT control with the conventional ACFP technique in transient response is shown. There is a voltage droop $\Delta V_{\rm offset}$ as the product of DCR, and the value of load change $\Delta I_{\rm Load}$. Under this operation condition, the load range is from 300 mA to 1.7 A, so $\Delta I_{\rm Load}$ is 1.4 A and $\Delta V_{\rm offset}$ is 42 mV. Fig. 20 shows the experimental results of a controller according to (10). In Fig. 20, the waveform of the COT converter with the PWT technique in transient response is shown. The voltage droop $\Delta V_{\rm offset}$ is reduced from 42 to 4 mV. Figs. 19 and 20 compare the difference between conventional ACFP technique and the proposed PWT technique. The controller of ACFP technique and PWT technique are both implemented on the same chip, which can be selected manually by multiplexer so as to demonstrate the performance of both ACFP and proposed PWT techniques. Besides, the controller for both techniques follows the design guideline in [24] to optimize the design for COT with additional current feedback path.

Figs. 21 and 22 present the load transient responses of the PWT technique from 300 to 1700 mA and vice versa. The undershoot voltage is 75 mV and the recovery time is 4 μs in case of light-to-heavy load change, as shown in Fig. 21. The overshoot voltage is 90 mV and recovery time is 5 μs in case of heavy-to-light load change, as shown in Fig. 22. The PWT technique solves the problem of opposite trend between $v_{\rm OUT}$ and i_L because the on-time period and the off-time period are extended when load current occurs. Simultaneously, it reduces recovery time and undershoot/overshoot voltage.

Fig. 23 shows the measured efficiency of the proposed converter as the load current ranges from 200 mA to 1.8 A. The peak efficiency of the COT converter is 94% at 750 mA and the DCM load range has an acceptable efficiency as well. Two figure of merits (FoMs) are defined to compare the dynamic and overall performance, respectively. Large $\rm FoM_1$ and $\rm FoM_2$ stand for fast transient response and high accuracy, respectively. Table II lists the comparison result with the prior arts in the design of COT control dc–dc converters. The system can also operate at a lower switching frequency when using small ESR. It

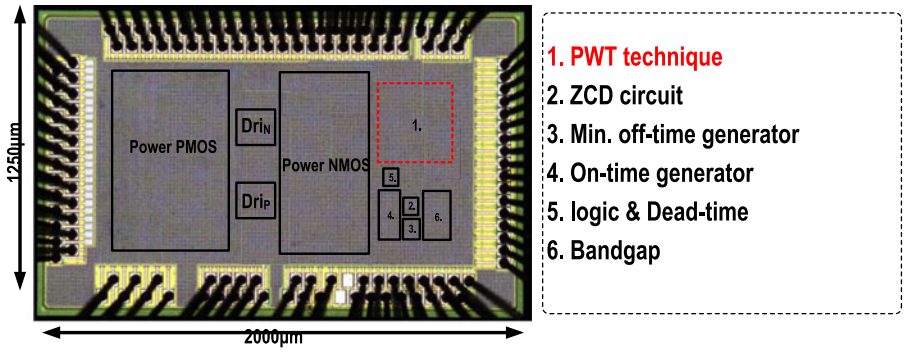
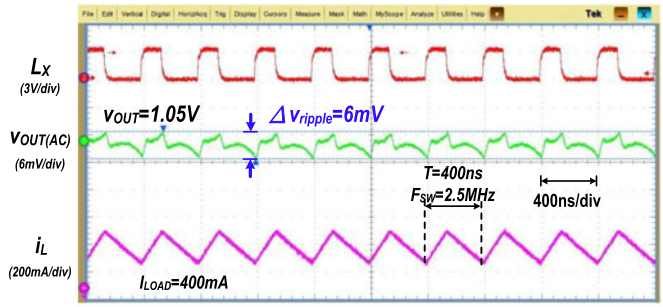
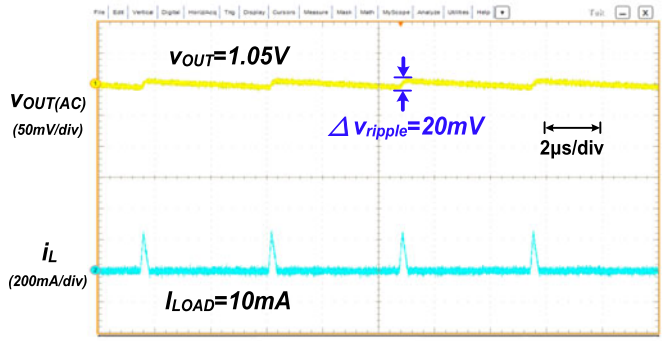


Fig. 17. Chip micrograph.



(a)



(b)

Fig. 18. Waveforms of the COT converter with the proposed PWT technique at $V_{\mathrm{IN}} = 3.3\,\mathrm{V}$ and $V_{\mathrm{OUT}} = 1.05\,\mathrm{V}$. (a) $I_{\mathrm{LOAD}} = 400\,\mathrm{mA}$. (b) $I_{\mathrm{LOAD}} = 10\,\mathrm{mA}$.

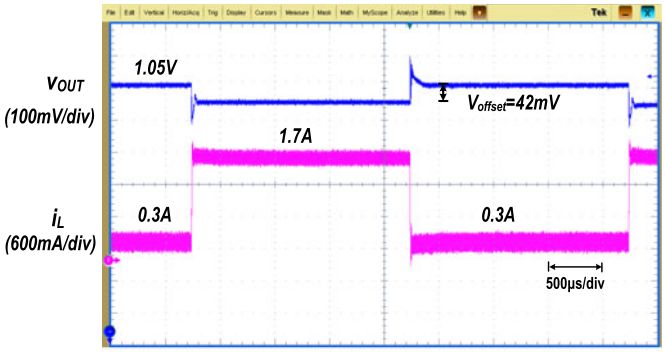


Fig. 19. Waveforms in the COT converter with the conventional ACFP technique at $V_{\mathrm{IN}} = 3.3\,\mathrm{V}$ and $V_{\mathrm{OUT}} = 1.05\ \mathrm{V}$ when the output loading current changes from 0.3 to 1.7 A and vice versa.

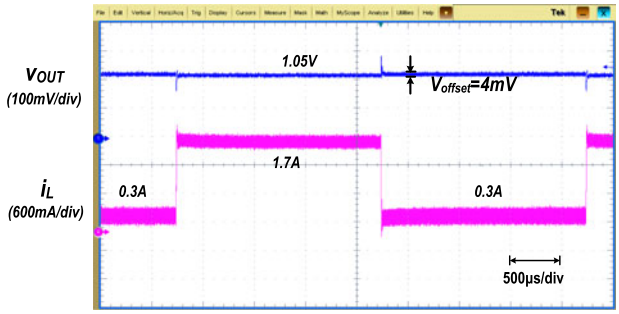


Fig. 20. Waveforms in the COT converter with the PWT technique at $V_{\mathrm{IN}} = 3.3\,\mathrm{V}$ and $V_{\mathrm{OUT}} = 1.05\,\mathrm{V}$ when the output loading current changes from 0.3 to 1.7 A and vice versa.

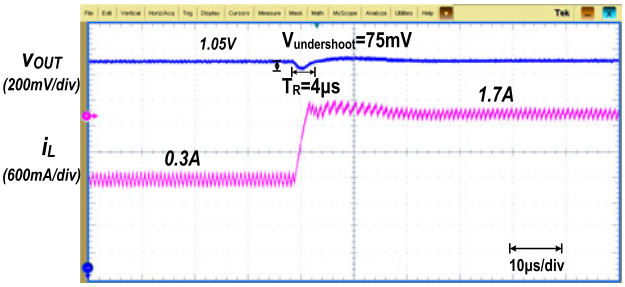


Fig. 21. Transient response in the COT converter with the PWT technique in case of light-to-heavy load change.

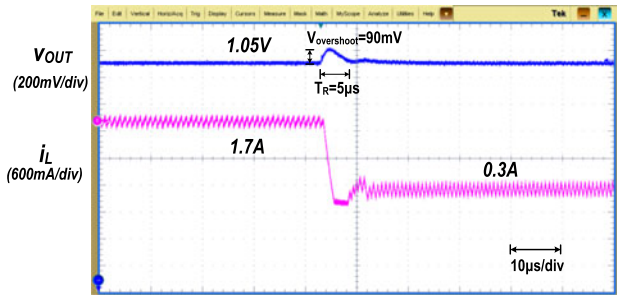


Fig. 22. Transient response in proposed COT converter with the PWT technique in case of heavy-to-light load change.

demonstrates the high performance achieved by the PWT technique. Furthermore, results show that the proposed power management scheme improves the transient response time to 4 and 5 μs.

TABLE II
COMPARISON TABLE

	This work	[1]	[2]	[3]	[4]
Control	COT	Quasi-current-mode hysteretic	COT	quasi$-V^2$ hysteretic	COT
Process	UMC 28 nm	0.35 μm	N/A	0.35 μm	0.35 μm
$V_{\rm IN}$ (V)	3.3	2.7–4.5	N/A	2.7–3.3	9
$V_{\rm OUT}$ (V)	**1.05**	2	1	0.9–2.1	4.5
$F_{\rm SW}$ (MHz)	**2.5**	3	1	3	0.33
Range of $I_{\rm LOAD}$ (A)	0.3–1.7	0–0.4	N/A	0.05–0.5	2–4
$\Delta I_{\rm LOAD}$ (A)	1.4	0.4	N/A	0.45	2
L (μH)	1	4.7	0.36	2.2	90
$C_{\rm CO}$ (μF)	4.7	10	$30 * 22$	4.4	220
$R_{\rm ESR}$ (Ω)	4 m	$<$20 m	N/A	$<$30 m	50 m
Power efficiency	94%	95.5%	N/A	93%	N/A
Offset (mV)	4	N/A	8	20	N/A
T_R, recovery time (μs) *L→H/H→L*	4/5	4.8/3	N/A	2.4/2.8	N/A
$\mathrm{FOM}_1 = \frac{L\cdot\Delta I_{\rm LOAD}\cdot 10^2}{C_{\rm CO}\cdot F_{\rm SW}\cdot T_R}$	2.956	1.31	N/A	2.67	N/A
$\mathrm{FOM}_2 = \frac{L\cdot\Delta I_{\rm LOAD}\cdot 10^3}{C_{\rm CO}\cdot F_{\rm SW}\cdot V_{\rm offset}\cdot T_R}$	5.957	N/A	N/A	1.339	N/A

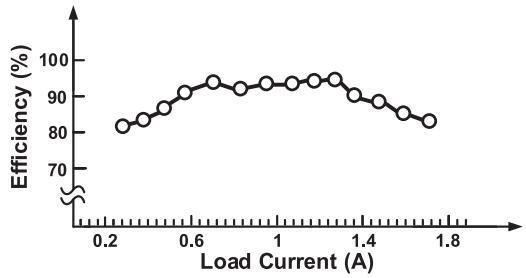


Fig. 23. Measured efficiency versus loading current of the proposed PWT technique.

VI. CONCLUSION

This paper proposes the PWT technique to remove the load-dependent dc offset voltage and to improve load regulation, since the disadvantages of conventional COT control with an additional current feedback path are the dc offset voltage and deterioration in load transient response. Moreover, the slow transient response in the ACFP technique is also improved. Because of the proposed PWT technique, test chip fabricated in 28 nm CMOS process demonstrates improvement of offset voltage from 42 to 4 mV. Furthermore, the transient response time is improved to 4 and 5 μs when load changes from 0.3 to 1.7 A and vice versa, respectively.

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