Topology and Control of a Five-Level Hybrid-Clamped Converter for Medium-Voltage High-Power Conversions

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***Abstract*—Five-level hybrid-clamped (5L-HC) converter is a newly proposed topology which is suitable for high-performance medium-voltage high-power conversions without switches directly connected in series. The critical issue of this converter is that two flying capacitor voltages of each phase and two neutral-point potentials of the dc-link need to be balanced. This paper presents a decoupled voltage balancing method for this 5L-HC converter based on modified phase-shifted pulse width modulation (PS-PWM) and optimal zero-sequence voltage injection. The voltages across the central dc-link capacitor and two flying capacitors are balanced first by adjusting the width of four PWM signals. Second, the relationship between the neutral-point currents and the output phase voltage is studied and the upper and lower dc-link capacitor voltages are balanced by zero-sequence voltage injection. Both steady-state and dynamic-state simulation and experimental results are presented to confirm the validity of this method.**

***Index Terms*—Capacitor voltage balancing, medium-voltage drive, multilevel converter, phase-shifted pulse width modulation (PS-PWM), zero-sequence voltage (ZSV).**

I. Introduction

MULTILEVEL converters have become more and more popular in high voltage high power applications these years [1]–[5]. Although multilevel converter is a mature and already proven technology, researchers all over the world are still working on developing new topologies to further improve the efficiency, reliability, power density, and cost performance of multilevel converters [6]–[29].

In order to increase the voltage levels and reduce clamping devices, many hybrid multilevel converters have been proposed. One of the earliest hybrid multilevel topologies is the stacked multicell (SMC) converter [11]–[13], which is composed of two n-level flying capacitor (FC) converters stacked together to generate a (2n-1)-level voltage waveform. By this way, the number of flying capacitors can be reduced. The five-level (5L) SMC topology is shown in Fig. 1(a).

Five-level active neutral-point clamped (5L-ANPC) converter is another attractive hybrid converter which is suitable for high performance medium-voltage motor drives [14]–[17], as shown in Fig. 1(b). It can be seen as the combination of a three-level ANPC converter and a two-level cell. A drawback of this topology is the requirement of two switches connected in series to ensure all the switches withstand the same voltage stress, which may reduce the reliability of the converter.

A new voltage source converter for medium voltage applications named four-level nested neutral-point clamped (4L-NNPC) converter is presented in [18], which can operate over a wide range of voltages without switches connected in series. The structure is very simple and the voltage balancing of flying capacitors can be achieved by redundant switching states [18]–[21]. Furthermore, a new 5L-NNPC inverter is proposed in [22] on the basis of this 4L-NNPC converter, as shown in Fig. 1(c). Only eight active switches are used per phase and hence the cost can be reduced.

Another four-level hybrid-clamped converter is proposed in [23] and [24], which is composed of only eight switches and one flying capacitor per phase. In order to increase the output voltage level, a new 5L-hybrid-clamped (5L-HC) converter is proposed in [25], as shown in Fig. 2(a). Each phase of this topology consists of ten switches and two flying capacitors, which can also be regarded as a modification of 5L-FC topology. As shown in Fig. 2(b), the high-voltage flying capacitor near the dc-link in the 5L-FC converter is replaced by two clamping switches in the 5L-HC converter.

Modular multilevel converter (MMC) is another emerging multilevel converter topology which gains increasing attentions during these years [26]–[33]. However, it suffers from the low-frequency capacitor voltage fluctuation problem in medium-voltage drive applications and it is suggested to drive fan/blower-like loads for energy savings [30]. In order to suppress the voltage fluctuation at low-frequency region, many different methods have been proposed [31]–[33]. Another drawback of this topology is too more switches and capacitors are used.

The comparison of devices in different 5L topologies is shown in Table I. The 5L-HC converter uses nearly the fewest devices among these topologies. Compared with 5L-ANPC converter, 5L-HC converter uses one more flying capacitor but two fewer

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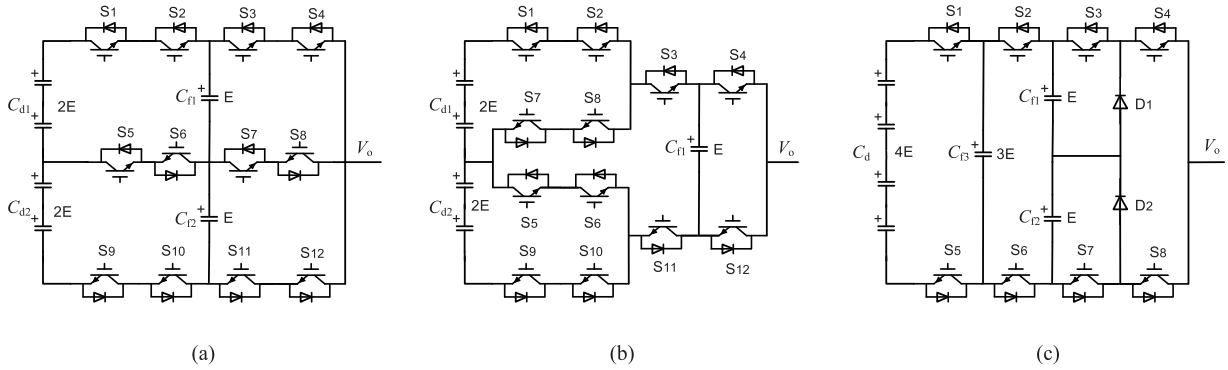

Fig. 1. Three five-level topologies: (a) 5L-SMC, (b) 5L-ANPC, and (c) 5L-NNPC.

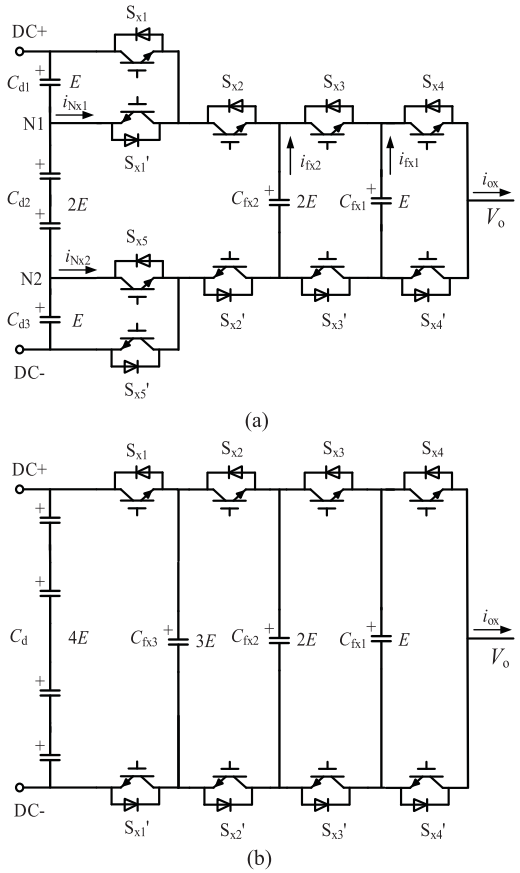

Fig. 2. (a) 5L-HC converter and (b) 5L-FC converter.

TABLE I
NUMBER OF DEVICES PER PHASE IN DIFFERENT FIVE-LEVEL TOPOLOGIES

Topology	Active switches	Diodes	Flying capacitors
5L-NPC	8	12	0
5L-FC	8	0	3
5L-SMC	12	0	2
5L-ANPC	12	0	1
5L-NNPC	8	2	3
5L-MMC	16	0	8
5L-HC	**10**	**0**	**2**

devices. Moreover, no series connected switches is required in the 5L-HC converter. Compared with 5L-FC and 5L-NNPC converters, two more active switches are used but an FC of the highest voltage is eliminated, which is beneficial to reduce the system volume and weight, particularly in high voltage high power applications. Compared with other topologies, the total number of devices is decreased obviously. So on balance, the 5L-HC converter is also a very competitive and practical solution for medium-voltage power conversions.

The major issue of this 5L-HC converter is the voltage balancing of FCs and dc-link capacitors. Most of the voltage balancing methods of other new multilevel topologies depend on the redundant switching states directly and bring extra switching transitions and losses. In order to solve this problem, this paper proposed a decoupled capacitor voltage balancing method for this 5L-HC converter, which has the following features.

1) The two neutral-point (NP) potentials of the dc-link are affected by two NP currents, which are coupled with each other. In order to decouple the two NP potentials, the two NP currents are not controlled independently. The difference of the two NP currents is used to control the central dc-link capacitor voltage, while the sum is used to control the upper and lower dc-link capacitor voltages. By this way, the central dc-link capacitor voltage is decoupled from the upper and lower dc-link capacitor voltages.
2) The central dc-link capacitor voltage and two flying capacitor voltages are controlled by modified phase-shifted pulse width modulation (PS-PWM). Four optimal duty ratios can be calculated to minimize the capacitor voltage ripples in a carrier period.
3) The upper and lower dc-link capacitor voltages are balanced by zero-sequence voltage (ZSV) injection. The relationship of total NP current and ZSV is studied and derived. A precise optimal ZSV is calculated to adjust the total NP current and then the upper and lower dc-link capacitor voltages can be balanced.

This paper is organized as follows. In Section II, the operating principle and modulation method is briefly introduced. In Section III, a switching-function model of capacitor currents and an average-value model of capacitor voltage ripples are established. And then a decoupled capacitor voltage balancing

TABLE II
SWITCHING STATES OF THE 5L-HC CONVERTER

S_{x1}	S_{x5}	S_{x2}	S_{x3}	S_{x4}	i_{fx1}	i_{fx2}	i_{N1x}	i_{N2x}	switching states	V_{ox}
0	0	0	0	0	0	0	0	0	**V0**	0
0	0	0	0	1	i_{ox}	0	0	0	**V1**	*E*
0	0	0	1	0	$-i_{ox}$	i_{ox}	0	0	**V2**	*E*
0	0	1	0	0	0	$-i_{ox}$	i_{ox}	0	**V3**	*E*
1	1	0	0	0	0	0	0	i_{ox}	**V4**	*E*
0	0	0	1	1	0	i_{ox}	0	0	**V5**	2*E*
0	0	1	0	1	i_{ox}	$-i_{ox}$	i_{ox}	0	**V6**	2*E*
0	0	1	1	0	$-i_{ox}$	0	i_{ox}	0	**V7**	2*E*
1	1	0	0	1	i_{ox}	0	0	i_{ox}	**V8**	2*E*
1	1	0	1	0	$-i_{ox}$	i_{ox}	0	i_{ox}	**V9**	2*E*
1	1	1	0	0	0	$-i_{ox}$	0	0	**V10**	2*E*
0	0	1	1	1	0	0	i_{ox}	0	**V11**	3*E*
1	1	0	1	1	0	i_{ox}	0	i_{ox}	**V12**	3*E*
1	1	1	0	1	i_{ox}	$-i_{ox}$	0	0	**V13**	3*E*
1	1	1	1	0	$-i_{ox}$	0	0	0	**V14**	3*E*
1	1	1	1	1	0	0	0	0	**V15**	4*E*

method is introduced in Section IV. Simulation and experimental results are presented in Section V and Section VI. Finally, conclusions are summarized in Section VII.

II. Operating Principles and Modulation Method

As shown in Fig. 2(a), the 5L-HC converter is composed of ten equally rated switches and two FCs C_{fx1} and C_{fx2} per phase, where x represents phase *a*, *b*, or *c*. The dc-link is split into three parts and shared for all the phases. Assume the dc-link voltage is constant and equal to 4*E*, then the nominal voltages of the upper, central, and lower dc-link capacitors C_{d1}, C_{d2}, and C_{d3} are *E*, 2*E,* and *E*, respectively. The nominal voltages of FC C_{fx1} and C_{fx2} are *E* and 2*E,* respectively. Among the ten switches, $S_{x1}-S_{x5}$ and $S_{x1}{}' - S'_{x5}$ are complementary switch pairs and S_{x1} and S_{x5} require the same switching signal. So each phase can output five voltage levels with sixteen switching states. All the switching states are summarized in Table II, where i_{ox} is the phase current. (i_{fx1}, i_{fx2}) and (i_{N1x}, i_{N2x}) are the currents flowing out of FCs (C_{fx1}, C_{fx2}) and neutral points (N1, N2). Different switching states have different effects on the FC voltages and NP potentials, which provides a high degree of freedom to balance the dc-link capacitor voltages and FC voltages.

Defining the switching functions of switches $S_{x1}-S_{x5}$ are $S_{fx1} - S_{fx5}$, then the instantaneous output voltage level V_{ox} can be written as follows:

$$V_{ox} = (S_{fx1} + S_{fx2} + S_{fx3} + S_{fx4}) \cdot E. \tag{1}$$

Equation (1) indicates that the output voltage level is determined by the sum of the switching functions $S_{fx1} - S_{fx4}$. Moreover, switches S_{x1}, S_{x2}, S_{x3}, and S_{x4} are independent of each other, so that classic PS-PWM can be used to control this converter. PS-PWM is widely used in FC-based multilevel converters for its natural capacitor voltage balancing ability [34]–[36]. For this 5L-HC topology, four triangle carriers are phase shifted by 90° and correspond to switches S_{x1}, S_{x2}, S_{x3} and S_{x4}, respectively.

III. Modeling of the Capacitor Currents and Voltages

The most important issue of this converter is the capacitor voltage balancing problem, including the voltage balancing of flying capacitors and dc-link capacitors. In order to analyze the voltage ripple characteristics of these capacitors, a switching-function model of capacitor currents and an average-value model of capacitor voltage ripples are discussed.

A. Modeling of NP and FC Currents

According to Table II, the instantaneous FC currents (i_{fx1}, i_{fx2}) can be written as

$$\begin{cases} i_{fx1} = (S_{fx4} - S_{fx3}) \cdot i_{ox} \\ i_{fx2} = (S_{fx3} - S_{fx2}) \cdot i_{ox} \end{cases}. \tag{2}$$

For the dc-link capacitors, the load current flows out of neutral point N1 when $S_{x1}{}'$ and S_{x2} are switched on and out of N2 when S_{x5} (S_{x1}) and S'_{x2} are switched on. So the instantaneous NP currents (i_{N1x}, i_{N2x}) can be written as

$$\begin{cases} i_{N1x} = S_{fx2}(1 - S_{fx1}) \cdot i_{ox} \\ i_{N2x} = S_{fx1}(1 - S_{fx2}) \cdot i_{ox} \end{cases}. \tag{3}$$

The two NP potentials are affected by i_{N1x} and i_{N2x} at the same time. In order to decouple the two NP potentials, the difference and the sum of i_{N1x} and i_{N2x} are considered, respectively

$$i_{dx} = i_{N1x} - i_{N2x} = (S_{fx2} - S_{fx1}) \cdot i_{ox} \tag{4}$$

$$i_{Nx} = i_{N1x} + i_{N2x} = |S_{fx2} - S_{fx1}| \cdot i_{ox}. \tag{5}$$

Defining the duty ratios of $S_{fx1} - S_{fx5}$ in a carrier period are $d_{x1} - d_{x5}$, based on (1), the average output phase voltage u_{ox} in a carrier period can be written as follows:

$$u_{ox} = (d_{x1} + d_{x2} + d_{x3} + d_{x4}) \cdot E. \tag{6}$$

Based on (2), the average FC currents in a carrier period can be written as follows:

$$\begin{cases} \bar{i}_{fx1} = (d_{x4} - d_{x3}) \cdot i_{ox} \\ \bar{i}_{fx2} = (d_{x3} - d_{x2}) \cdot i_{ox} \end{cases}. \tag{7}$$

Based on (4) and (5), the average values of $i_{\rm dx}$ and $i_{\rm Nx}$ in a carrier period can be written as

$$\bar{i}_{\rm dx} = (d_{x2} - d_{x1}) \cdot i_{\rm ox} \tag{8}$$

$$\bar{i}_{Nx} = d_{Nx} \cdot i_{\rm ox} \tag{9}$$

where $d_{\rm Nx}$ is the duty ratio of $|S_{\rm fx2} - S_{\rm fx1}|$.

In the conventional PS-PWM, the reference voltages for switches $\rm S_{x1}$, $\rm S_{x2}$, $\rm S_{x3}$, and $\rm S_{x4}$ are the same and can be regarded as a constant in a carrier period. If *E* is selected as the base voltage and the negative pole of the dc-link is referred as the zero potential, then the range of the output voltage $u_{\rm ox}$ is [0, 4] and the reference modulation voltage is

$$u_{\rm refx} = u_{\rm ox}/4. \tag{10}$$

Thus, the duty ratios of $S_{\rm fx1} - S_{\rm fx4}$ in a carrier period can be written as follows:

$$d_{x1} = d_{x2} = d_{x3} = d_{x4} = u_{{\rm ref}x}. \tag{11}$$

B. Modeling of Capacitor Voltage Ripples

For the FCs, the voltage ripples in a carrier period can be written as follows:

$$\begin{cases} \Delta u_{\rm fx1} = -\frac{\bar{i}_{\rm fx1} \cdot T_s}{C_{\rm fx1}} = -\frac{T_s}{C_{\rm fx1}}(d_{x4} - d_{x3}) \cdot i_{\rm ox} \\ \Delta u_{\rm fx2} = -\frac{\bar{i}_{\rm fx2} \cdot T_s}{C_{\rm fx2}} = -\frac{T_s}{C_{\rm fx2}}(d_{x3} - d_{x2}) \cdot i_{\rm ox} \end{cases} \tag{12}$$

where $\Delta u_{\rm fx1}$ and $\Delta u_{\rm fx2}$ are the voltage ripples of FCs in a carrier period, $C_{\rm fx1}$ and $C_{\rm fx2}$ are the capacitances, and $T_{\rm s}$ is the carrier period.

Assuming the dc-link capacitances are $C_{\rm d1} = 2C_{\rm d2} = C_{\rm d3} = C_{\rm d}$, then the influences of average NP currents ($\bar{i}_{N1x}$,$\bar{i}_{N2x}$) in a carrier period can be written as follows:

$$\Delta u_{d1x} = \frac{3}{4} \cdot \frac{\bar{i}_{N1x} \cdot T_s}{C_d} + \frac{1}{4} \cdot \frac{\bar{i}_{N2x} \cdot T_s}{C_d} \tag{13a}$$

$$\begin{aligned} \Delta u_{d2x} &= \frac{1}{4} \cdot \frac{\bar{i}_{N2x} \cdot T_s}{C_{d2}} - \frac{1}{4} \cdot \frac{\bar{i}_{N1x} \cdot T_s}{C_{d2}} \\ &= -\frac{1}{4} \cdot \frac{\bar{i}_{\rm dx} \cdot T_s}{C_{d2}} = -\frac{T_s}{2C_d}(d_{x2} - d_{x1}) \cdot i_{ox} \end{aligned} \tag{13b}$$

$$\Delta u_{d3x} = -\frac{1}{4} \cdot \frac{\bar{i}_{N1x} \cdot T_s}{C_d} - \frac{3}{4} \cdot \frac{\bar{i}_{N2x} \cdot T_s}{C_d}. \tag{13c}$$

Equation (13b) shows that the central dc-link capacitor voltage ripple only depends on $\bar{i}_{dx}$. Substituting (11) into (12) and (13b), it is easy to get that $\Delta u_{\rm fx1} = \Delta u_{\rm fx2} = \Delta u_{\rm d2x} = 0$, which means that the central dc-link capacitor and the FC voltages can be naturally balanced in a carrier period.

On the other hand, the unbalanced voltage of the upper and lower dc-link capacitors can be written as follows:

$$\begin{aligned} \Delta u_{Nx} &= \Delta u_{d1x} - \Delta u_{d3x} = \frac{(\bar{i}_{N1x} + \bar{i}_{N2x}) \cdot T_s}{C_d} \\ &= \frac{T_s}{C_d} \cdot d_{Nx} \cdot i_{\rm ox} \end{aligned} \tag{14}$$

which means the unbalanced voltage of the upper and lower dc-link capacitors only depends on the total NP current $\bar{i}_{Nx}$. In order to get the detailed expression of $\Delta u_{\rm Nx}$, $d_{\rm Nx}$ should be considered first. There are three cases in terms of $u_{\rm refx}$ [25].

Case I: When $0 \le u_{\rm refx} < 1/4\,(0 \le u_{\rm ox} < 1)$, $S_{\rm fx1}$ and $S_{\rm fx2}$ have no overlapped area, as shown in Fig. 3(a). Then $d_{\rm Nx}$ can be written as follows:

$$d_{Nx} = 2u_{{\rm ref}x}. \tag{15}$$

Case II: When $1/4 \le u_{\rm refx} < 3/4\,(1 \le u_{\rm ox} < 3)$, $d_{\rm Nx}$ are only determined by the phase difference of $S_{\rm fx1}$ and $S_{\rm fx2}$, as shown in Fig. 3(b) and (c). If the carrier waves of switches $\rm S_{x1}$ and $\rm S_{x2}$ are phase shifted by π/2, then $d_{\rm Nx}$ is a constant

$$d_{Nx} = 1/2. \tag{16}$$

Case III: When $3/4 \le u_{\rm refx} \le 1\,(3 \le u_{\rm ox} \le 4)$, $d_{\rm Nx}$ is determined by the pulse widths of $S_{\rm fx1}$ and $S_{\rm fx2}$, as shown in Fig. 3(d). Then $d_{\rm Nx}$ can be written as follows:

$$d_{Nx} = 2(1 - u_{{\rm ref}x}). \tag{17}$$

According to (10) and (15)–(17), the duty ratio of the total NP currents can be written as follows:

$$d_{\rm Nx} = \begin{cases} u_{\rm ox}/2, & 0 \le u_{\rm ox} < 1 \\ 1/2, & 1 \le u_{\rm ox} < 3 \\ 2 - u_{\rm ox}/2, & 3 \le u_{\rm ox} \le 4 \end{cases}. \tag{18}$$

The relationship of $d_{\rm Nx}$ and $u_{\rm ox}$ is shown in Fig. 4, which is a piecewise-linear function. The inflection points are $u_{\rm ox} = 0$, 1, 3, or 4.

IV. Capacitor Voltage Balancing Method

A. Voltage Balancing of the Central DC-Link Capacitor and FCs

Although the central dc-link capacitor and the FC voltages can be naturally balanced in a carrier period using PS-PWM, similar with classic FC multilevel converters, it also may diverge under nonideal and dynamic conditions if not controlled [35], [36]. According to (12) and (13b), a way to balance their voltages is to adjust $d_{\rm x1}$, $d_{\rm x2}$, $d_{\rm x3}$, and $d_{\rm x4}$. Therefore, the PS-PWM method should be modified slightly to achieve this goal. The following three steps are included.

Step 1: The central dc-link capacitor $C_{\rm d2}$ is considered first. If $\text{sign}(u_{\rm dc2}–2E) * \text{sign}(i_{\rm ox}) > 0$, according to (13b), the duty ratio of $S_{\rm fx1}$ should be decreased and the duty ratio of $S_{\rm fx2}$ should be increased. Since the central dc-link capacitor is shared by three phases, the central dc-link capacitor voltage ripple is affected by the three-phase currents at the same time. In order to suppress the voltage ripple in the next carrier period, the required duty ratio difference for each phase can be written as follows:

$$\Delta d_{x21} = d'_{x2} - d'_{x1} = \frac{2(u_{d2x} - 2E) \cdot C_d}{3i_{\rm ox} \cdot T_s}. \tag{19}$$

In order to not affect the average output voltage and FC voltages, the modified duty ratios of $S_{\rm fx1} - S_{\rm fx4}$ can be written as

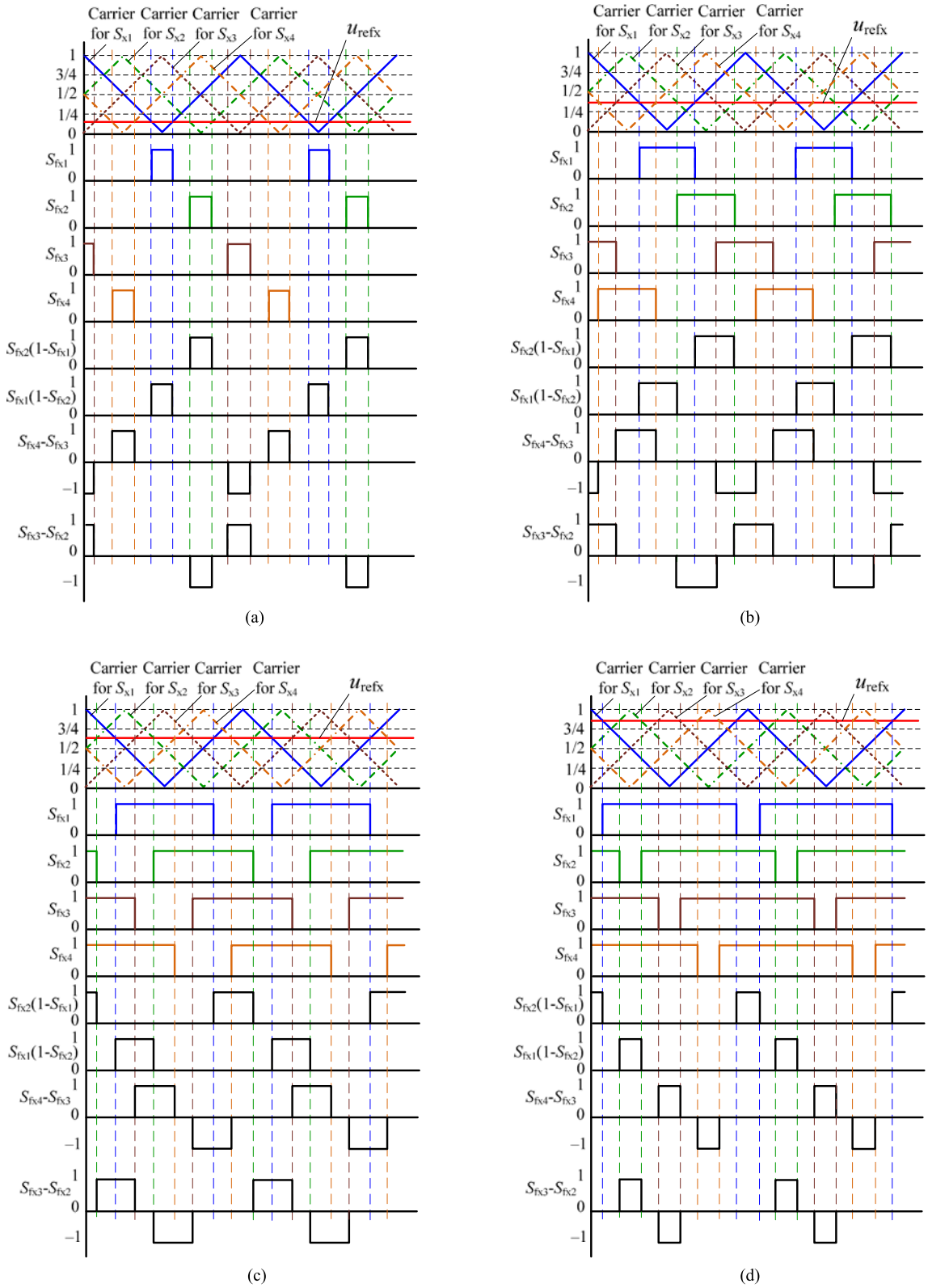

Fig. 3. Pulse patterns of PS-PWM for different reference voltage regions: (a) $0 \leq u_{\mathrm{refx}} < 1/4$, (b) $1/4 \leq u_{\mathrm{refx}} < 1/2$, (c) $1/2 \leq u_{\mathrm{refx}} < 3/4$, and (d) $3/4 \leq u_{\mathrm{refx}} \leq 1$.

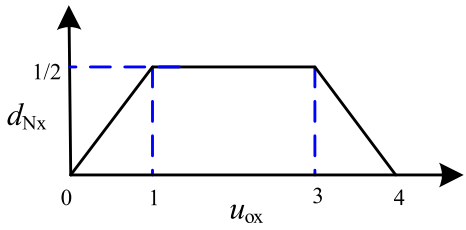

Fig. 4. Relationship of d_{Nx} and u_{ox}.

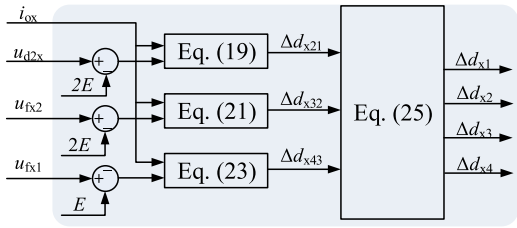

Fig. 5. Block diagram of the central dc-link capacitor and FC voltage balancing method.

follows:

$$\begin{cases} d'_{x1} = d_{x1} - \frac{3}{4}\Delta d_{x21} \\ d'_{x2} = d_{x2} + \frac{1}{4}\Delta d_{x21} \\ d'_{x3} = d_{x3} + \frac{1}{4}\Delta d_{x21} \\ d'_{x4} = d_{x4} + \frac{1}{4}\Delta d_{x21} \end{cases}. \tag{20}$$

Step 2: The FC C_{fx2} is considered second. If sign(u_{fx2}–2E) $*$ sign(i_{ox}) > 0, according to (12), the duty ratio of S_{fx2} should be decreased and the duty ratio of S_{fx3} should be increased. In order to suppress the voltage ripple in the next carrier period, the required duty ratio difference can be written as follows:

$$\Delta d_{x32} = d''_{x3} - d''_{x2} = \frac{(u_{\mathrm{fx2}} - 2E) \cdot C_{\mathrm{fx2}}}{i_{\mathrm{ox}} \cdot T_s}. \tag{21}$$

In order to not affect the average output voltage and other capacitor voltages, the modified duty ratios of $S_{\mathrm{fx1}} - S_{\mathrm{fx4}}$ can be written as follows:

$$\begin{cases} d''_{x1} = d'_{x1} - \frac{1}{2}\Delta d_{x32} \\ d''_{x2} = d'_{x2} - \frac{1}{2}\Delta d_{x32} \\ d''_{x3} = d'_{x3} + \frac{1}{2}\Delta d_{x32} \\ d''_{x4} = d'_{x4} + \frac{1}{2}\Delta d_{x32} \end{cases}. \tag{22}$$

Step 3: Finally, the FC C_{fx1} is considered. If sign($u_{\mathrm{fx1}} - E$) $*$ sign(i_{ox}) > 0, according to (12), the duty ratio of S_{fx3} should be decreased and the duty ratio of S_{fx4} should be increased. In order to suppress the voltage ripple in the next carrier period, the required duty ratio difference can be written as follows:

$$\Delta d_{x43} = d'''_{x4} - d'''_{x3} = \frac{(u_{\mathrm{fx1}} - E) \cdot C_{\mathrm{fx1}}}{i_{\mathrm{ox}} \cdot T_s}. \tag{23}$$

In order to not affect the average output voltage and other capacitor voltages, the modified duty ratios of $S_{\mathrm{fx1}} - S_{\mathrm{fx4}}$ can be written as follows:

$$\begin{cases} d'''_{x1} = d''_{x1} - \frac{1}{4}\Delta d_{x43} \\ d'''_{x2} = d''_{x2} - \frac{1}{4}\Delta d_{x43} \\ d'''_{x3} = d''_{x3} - \frac{1}{4}\Delta d_{x43} \\ d'''_{x4} = d''_{x4} + \frac{3}{4}\Delta d_{x43} \end{cases}. \tag{24}$$

Based on (20)–(24), the final duty ratio variations can be written as follows:

$$\begin{cases} \Delta d_{x1} = -\frac{3}{4}\Delta d_{x21} - \frac{1}{2}\Delta d_{x32} - \frac{1}{4}\Delta d_{x43} \\ \Delta d_{x2} = \frac{1}{4}\Delta d_{x21} - \frac{1}{2}\Delta d_{x32} - \frac{1}{4}\Delta d_{x43} \\ \Delta d_{x3} = \frac{1}{4}\Delta d_{x21} + \frac{1}{2}\Delta d_{x32} - \frac{1}{4}\Delta d_{x43} \\ \Delta d_{x4} = \frac{1}{4}\Delta d_{x21} + \frac{1}{2}\Delta d_{x32} + \frac{3}{4}\Delta d_{x43} \end{cases}. \tag{25}$$

Then the finally adjusted four duty ratios are $d_{\mathrm{x1}} + \Delta d_{\mathrm{x1}}$, $d_{\mathrm{x2}} + \Delta d_{\mathrm{x2}}$, $d_{\mathrm{x3}} + \Delta d_{\mathrm{x3}}$, and $d_{\mathrm{x4}} + \Delta d_{\mathrm{x4}}$. In order to minimize the impact of voltage balancing method to the total harmonic distortion (THD) of the output voltage, the boundary of Δd_{x1}, Δd_{x2}, Δd_{x3}, and Δd_{x4} is limited within $\pm 0.1 * u_{\mathrm{refx}}$. The block diagram of the central dc-link capacitor and FC voltage balancing method is shown in Fig. 5.

B. Voltage Balancing of the Upper and Lower DC-Link Capacitors

Assume the central dc-link capacitor voltage has already been well balanced, then according to (14), the upper and lower dc-link capacitor voltages only depend on the total NP current. For a three-phase system, the average total NP current can be written as follows:

$$\bar{i}_N = \bar{i}_{Na} + \bar{i}_{Nb} + \bar{i}_{Nc} = d_{Na} \cdot i_{oa} + d_{Nb} \cdot i_{ob} + d_{Nc} \cdot i_{oc}. \tag{26}$$

In order to balance the upper and lower dc-link capacitor voltages, an average total NP current is expected to be injected into N1 and N2. According to (14), the demanded total NP current can be written as follows:

$$i_{N,\mathrm{ref}} = -C_d \frac{(u_{d1} - u_{d3})}{T_s} \tag{27}$$

where u_{d1} and u_{d3} are the upper and lower dc-link capacitor voltages.

Classic ZSV injection method can be used to regulate the total NP current. The actual phase voltage and reference modulation voltage after ZSV injection can be written as follows:

$$\begin{cases} u'_{ox} = u_{ox} + u_z \\ u'_{\mathrm{ref}x} = u_{\mathrm{ref}x} + u_z/4 \end{cases} \tag{28}$$

where u_z is the ZSVs. The three-phase average total NP current can be rewritten as follows:

$$\bar{i}'_N = \bar{i}'_{Na} + \bar{i}'_{Nb} + \bar{i}'_{Nc} = d'_{Na} \cdot i'_{oa} + d'_{Nb} \cdot i_{ob} + d'_{Nc} \cdot i_{oc}. \tag{29}$$

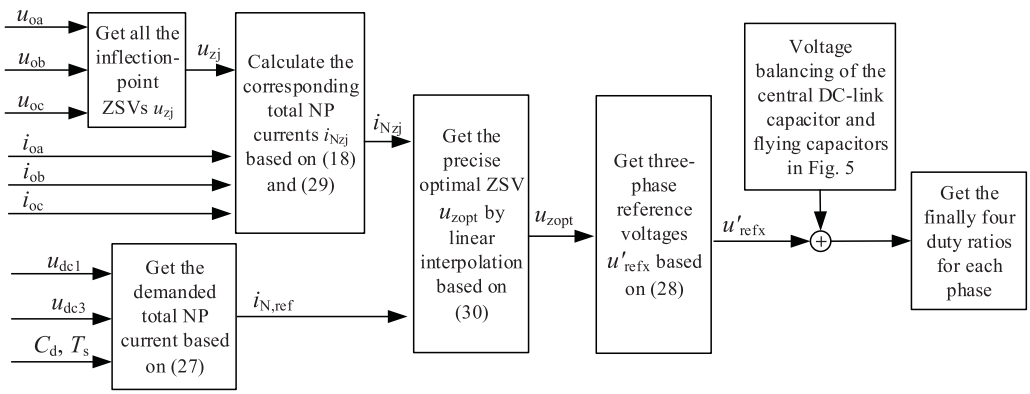

Fig. 6. Block diagram of the upper and lower dc-link capacitor voltage balancing method.

TABLE III
EXAMPLE OF THE INFLECTION POINT ZSVS

Order	ZSVs	Reference voltages		
		u_{oa}	u_{ob}	u_{oc}
0	$u_z = 0$	1.2	2.3	2.5
1	$u_{z1} = -1.2$	**0**	1.1	1.3
2	$u_{z2} = -0.2$	**1**	2.1	2.3
3	$u_{z3} = 0.5$	1.7	2.8	**3**
4	$u_{z4} = 0.7$	1.9	**3**	3.2
5	$u_{z5} = 1.5$	2.7	3.8	**4**

From (18) and (29), it can be seen that the relationship between the NP current and ZSV is nonlinear and discontinuous, it is hard to compute the expression of the precise ZSV to generate the demanded NP current directly. Fortunately, the relationship of $\bar{i}'_N$ and u_z is a piecewise-linear function. The inflection points are the ZSVs which make one of the three-phase reference voltages be one of (0, 1, 3, or 4), as illustrated in Fig. 4. Between these inflection points, $\bar{i}'_N$ is linearly proportion to u_z. So, it is possible to get the precise optimal ZSV by linear interpolation. Fig. 6 shows the block diagram of the upper and lower dc-link capacitor voltage balancing method, which can be divided into the following steps.

1) First, all the ZSVs on the inflection points are calculated and denoted by u_{zj} (j = 1, 2, 3, ...). For example, if the original three-phase reference voltages are (1.2, 2.3, 2.5), there are five inflection points. All the inflection points and the corresponding voltages after ZSV injection are listed in Table III.
2) Second, calculate the corresponding total NP currents i_{Nzj} of these inflection-point ZSVs according to (18) and (29).
3) Third, compare the demanded total NP current in (27) with i_{Nzj}. If $i_{N,ref}$ is between i_{Nzk} and $i_{Nz(k+1)}$, then the precise optimal ZSV can be obtained by linear interpolation

$$u_{zopt} = u_{zk} + \frac{u_{z(k+1)} - u_{zk}}{i_{Nz(k+1)} - i_{Nzk}} \cdot (i_{N,ref} - i_{Nzk}) \quad (30)$$

where u_{zopt} is the precise optimal ZSV which should be injected into the three-phase reference voltages.

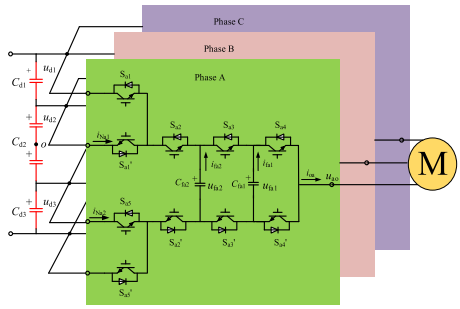

Fig. 7. Three-phase circuit of the 5L-HC inverter.

TABLE IV
CIRCUIT PARAMETERS USED FOR SIMULATION

Parameters	Value
Rated volume	1 MVA
Rated line voltage	6.6 kV
DC-link voltage	$U_{dc} = 11\ 200$ V
DC-link capacitor	$C_{d1} = C_{d3} = 500\ \mu$F, $C_{d2} = 250\ \mu$F
Flying capacitor	$C_{fx1} = 400\ \mu$F, $C_{fx2} = 200\ \mu$F
Carrier frequency	$f_c = 500$ Hz
R–L Load	$R_l = 40\ \Omega$, $L_l = 15$ mH

After the upper and lower dc-link capacitor voltages are balanced by optimal ZSV injecting, the three-phase references voltages are updated according to (28). The next step is to realize the voltage balancing of the central dc-link capacitor and FCs based on Fig. 5 for each phase. By this way, all the capacitor voltages are decoupled from each other and can be controlled solely.

V. SIMULATION VERIFICATION

In order to demonstrate the performance of the control method, a three-phase 6.6 kV/1 MVA inverter with both *R--L* load and induction motor load is simulated in MATLAB/Simulink environment. The circuit structure is shown in Fig. 7 and the parameters used for simulation are summarized in Table IV. In order to fully verify the performance of the voltage balancing method, the capacitor values are very small and the carrier frequency is as low as 500 Hz.

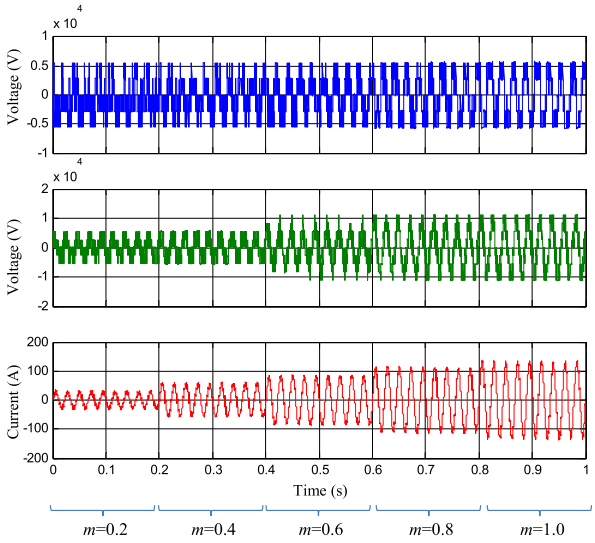

Fig. 8. Simulation result under different modulation indexes. From top to bottom are phase voltage, line voltage, and phase current.

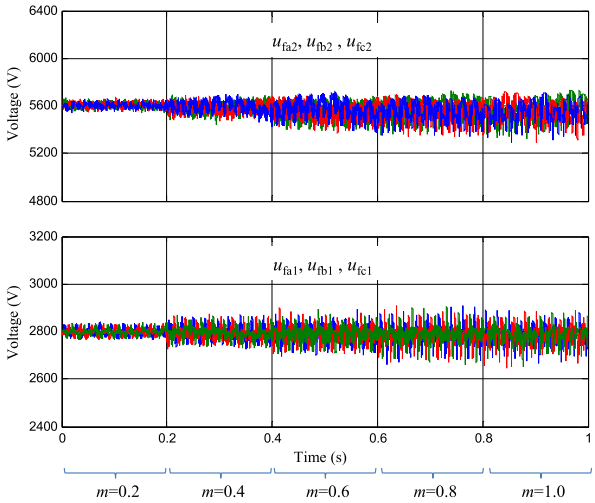

Fig. 9. Simulation result of FC voltages under different modulation indexes.

A. Steady-State Results with R–L Load

Fig. 8 shows the phase voltage, line voltage, and phase current under different modulation indexes with *R–L* load. Figs. 9 and 10 show the FC voltages and dc-link capacitor voltages. All the capacitor voltages are maintained balanced at their nominal values under different modulation indexes.

In order to verify the control performance under unbalanced load, the three-phase load resistances are adjusted to 200%, 100%, and 50% of the normal value and the modulation index is set to $m = 1.0$. The simulation results are shown in Fig. 11. It can be seen that the voltage balancing performance is not affected by the unbalanced loads at all.

B. Dynamic-State Results with R–L Load

The dynamic-state simulation results with *R--L* load are also presented. In Fig. 12, the three-phase FC voltages are controlled at their nominal values at the beginning. At $t = 0.2$ s, the reference voltages of three-phase FCs are set to 10% higher than, equal to, and 10% lower than the nominal values and all the voltages gradually stabilize at the new given values. At $t = 1.2$ s, all the voltages are controlled to the nominal values and balanced again. In Fig. 13, the central dc-link capacitor voltage is controlled to 1/2 of the dc-link voltage at the beginning. At $t = 0.2$ s, the reference voltage is set to 10% higher than the nominal value and the central dc-link capacitor voltage gradually stabilizes at the new given value. At $t = 1.2$ s, the reference voltage is set back to the nominal value and the central dc-link capacitor voltage is controlled back to the nominal value again.

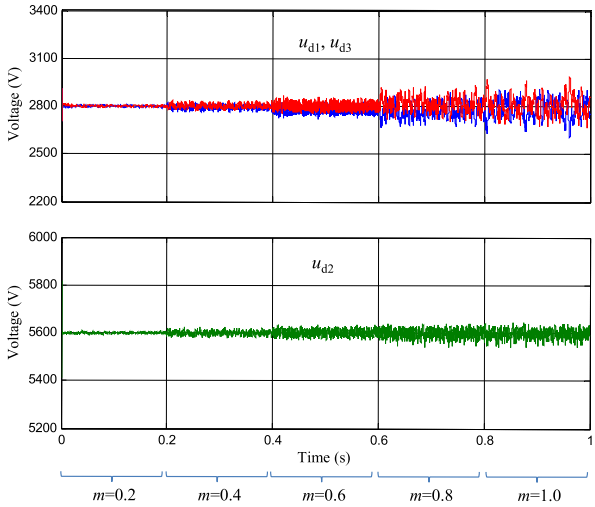

Fig. 10. Simulation result of dc-link capacitor voltages under different modulation indexes.

Fig. 14 shows the dynamic-state simulation result of the upper and lower dc-link capacitor voltage balancing control. At $t = 0.2$ s, the reference voltages of the upper and lower dc-link capacitors are set to 10% higher and 10% lower than the nominal values and gradually stabilize at the new given values. At $t = 1.2$ s, the reference voltages are set back to the nominal values and balanced again.

It is worth noticing that the upper and lower dc-link capacitor voltages remain balanced when the central dc-link capacitor voltage is controlled at different values in Fig. 13. Similarly, the central dc-link capacitor voltage remains balanced when the upper and lower dc-link capacitor voltages are controlled at different values in Fig. 14. The dynamic-state results demonstrate that the voltage balancing control for the central and upper/lower dc-link capacitors is fully decoupled.

C. Motor Drive Results

One of the most important applications of this 5L-HC converter is high-power medium-voltage motor drives. In order to demonstrate the performance of the proposed voltage balancing method in motor drive applications, an induction motor is used as load and the start-up and torque-step results are presented in Fig. 15. In Fig. 15(a) the motor is started-up and accelerated from 0 to 10 rad/s without load at first, and then a step change of 5000 Nm load torque is applied at $t = 1$ s. At t = 2 s the motor is accelerated from 10 to 100 rad/s. The corresponding capacitor

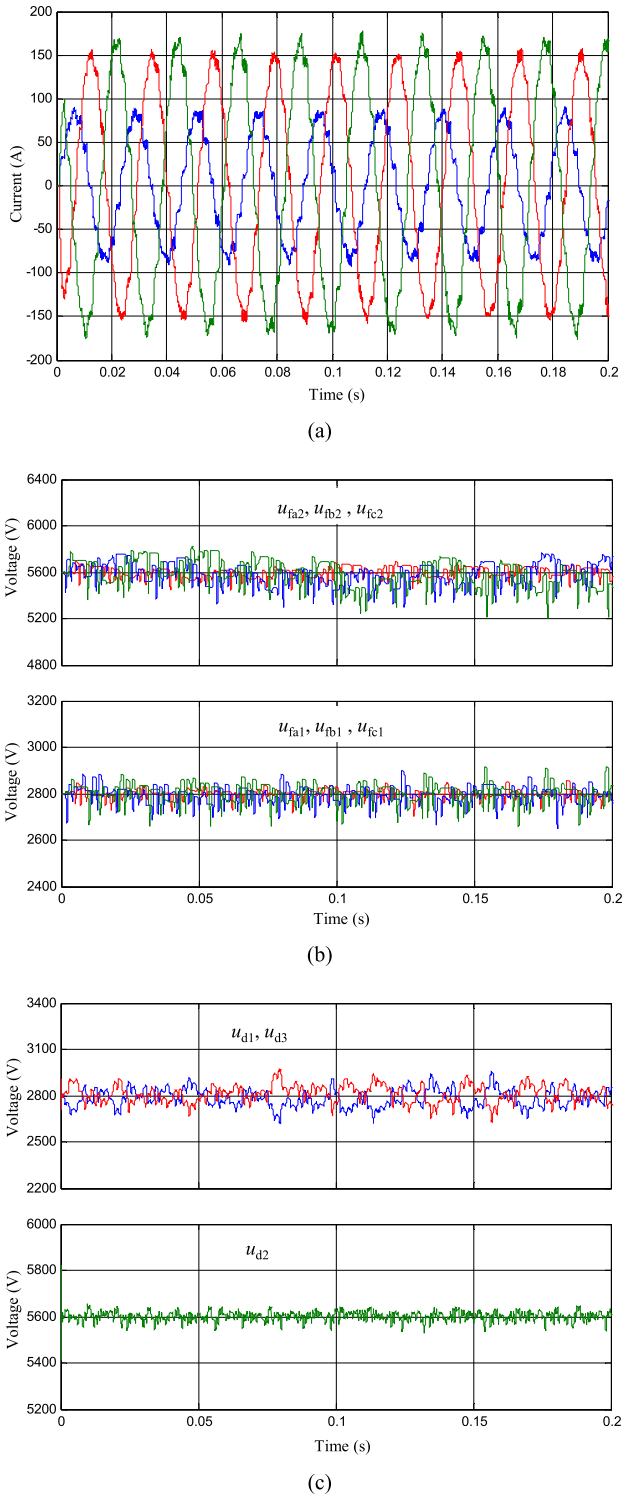

Fig. 11. Simulation result of unbalanced load: (a) Unbalanced three-phase currents, (b) FC voltages, and (c) dc-link capacitor voltages.

voltage waves are shown in Fig. 15(b) and (c). It can be seen that the capacitor voltage ripples are approximately proportional to the motor current and all the capacitor voltages are balanced very well during the whole process.

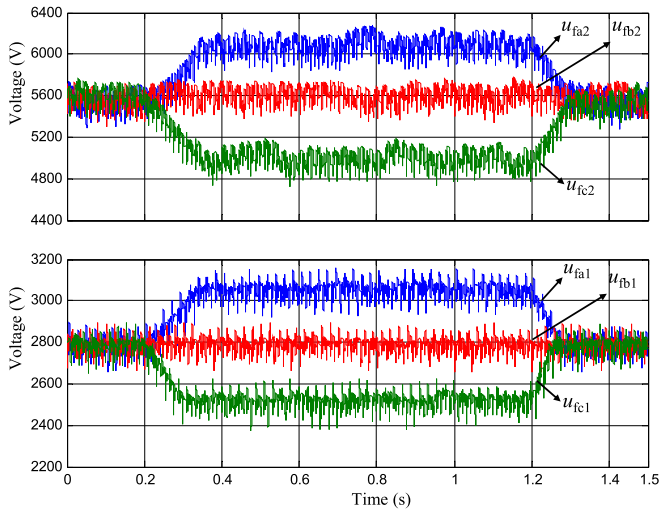

Fig. 12. Dynamic-state simulation result of three-phase FC voltages.

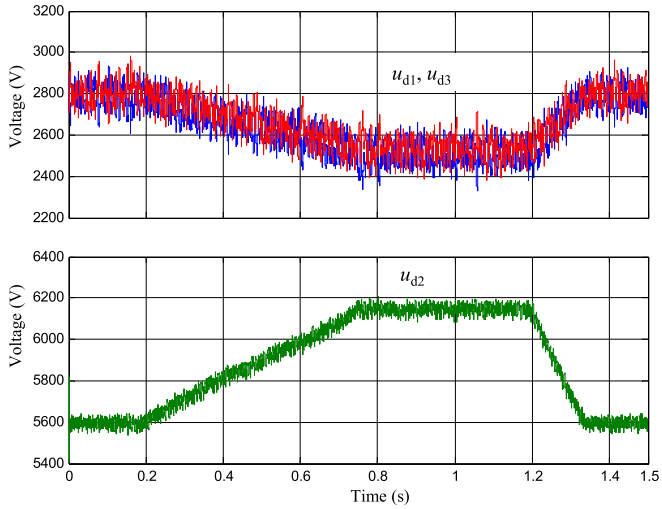

Fig. 13. Dynamic-state simulation result of the central dc-link capacitor voltage.

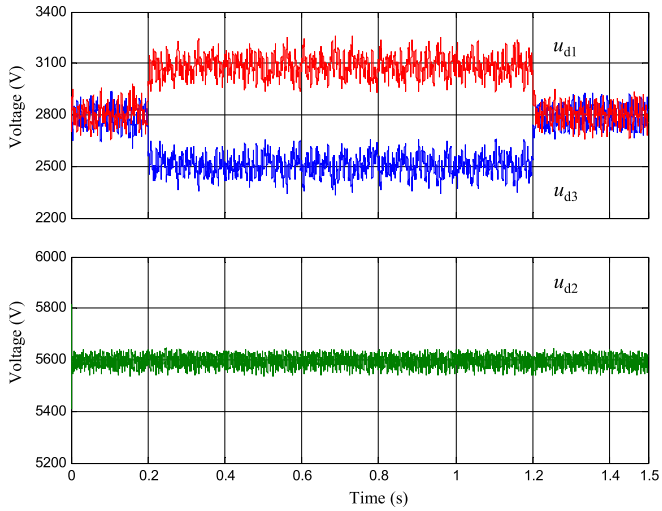

Fig. 14. Dynamic-state simulation result of the upper and lower dc-link capacitor voltages.

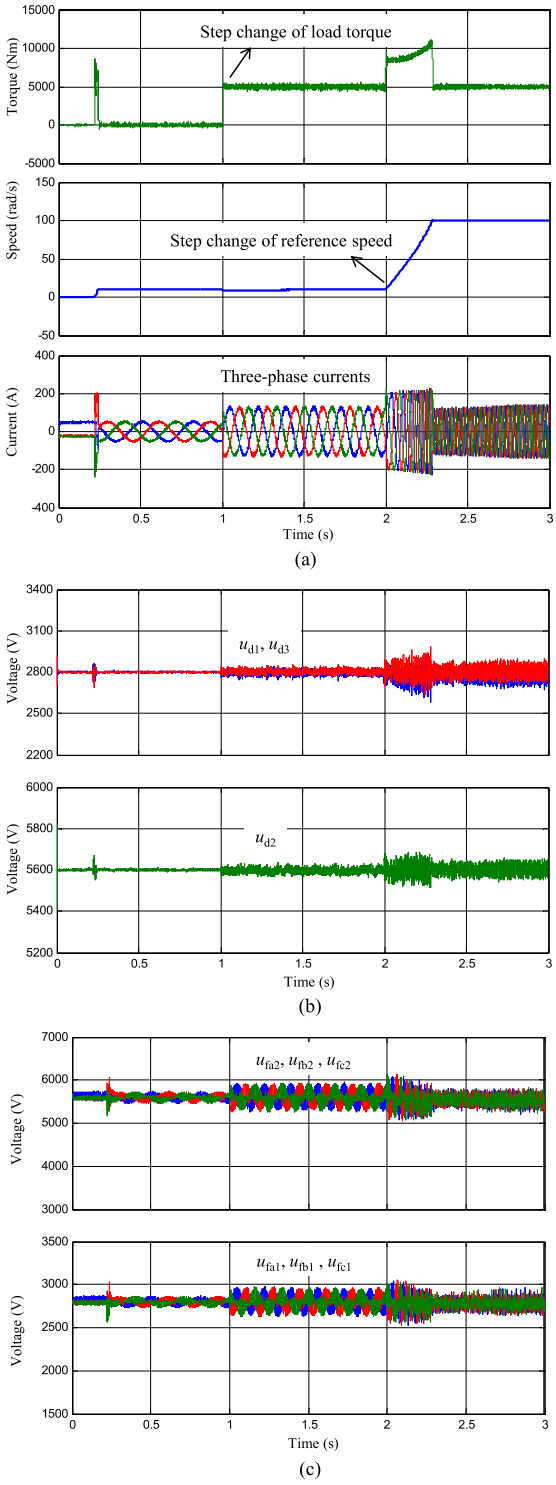

Fig. 15. Simulation result of motor drive applications: (a) motor torque, speed and currents, (b) dc-link capacitor voltages, and (c) FC voltages.

VI. Experiment Verification

A scaled-down three-phase converter prototype has been built to demonstrate the proposed topology and control method, as shown in Fig. 16. The master control board is based on a DSP chip TMS320F28335 and an field programmable gate array (FPGA) of Altera MAX 10 series. The cell control board is

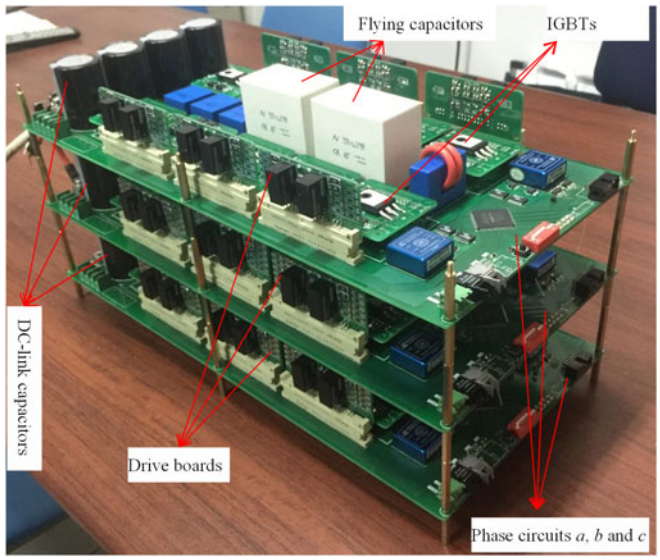

Fig. 16. Scaled-down 5L-HC converter prototype.

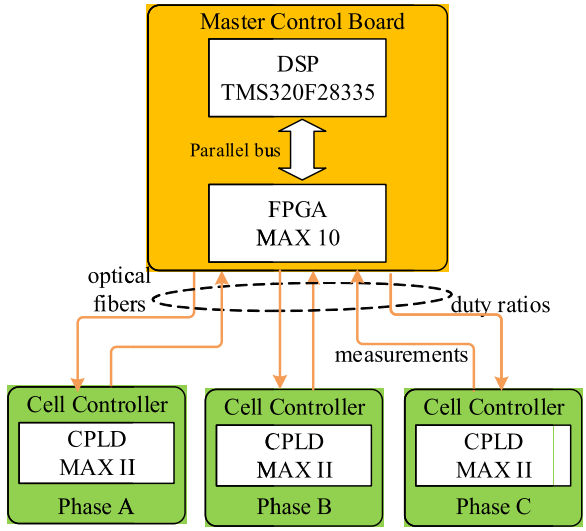

Fig. 17. Block diagram of the control system.

based on a CPLD of Altera MAX II series. The block diagram of the control system is shown in Fig. 17. The master control board and the three-phase cell control boards are communicated through three pairs of optical fibers. The downward signals are four duty ratios for each phase and the upward signals are voltage/current measurements and fault signals. The DSP on the master control board is used to execute the voltage balancing algorithm and other control algorithm such as motor control algorithm. The FPGA on the master control board is used to execute the coding and decoding of serial communication. The data exchange between DSP and FPGA is achieved through parallel data bus. The functions of CPLD on the cell control board include decoding the duty ratios, generating PWM signals and dead zones, measuring the FC voltages and phase current and communicating with master control board. The parameters used for experiments are shown in Table V.

TABLE V
CIRCUIT PARAMETERS USED FOR EXPERIMENTS

Parameters	Value
DC-link voltage	$U_{\rm dc} = 200$ V
DC-link capacitor	$C_{\rm d1} = C_{\rm d3} = 2460\ \mu$F, $C_{\rm d2} = 1230\ \mu$F
Flying capacitor	$C_{\rm fx1} = C_{\rm fx2} = 100\ \mu$F
Carrier frequency	$f_{\rm c} = 8$ kHz
R–L Load	$R_{\rm l} = 25\ \Omega$, $L_{\rm l} = 5$ mH

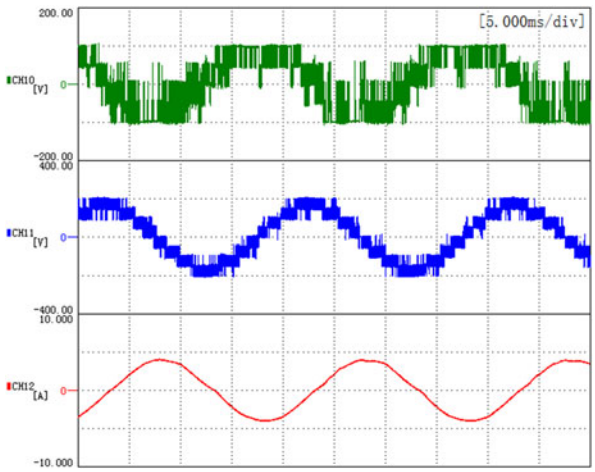

Fig. 18. Detailed phase voltage (100 V/div), line voltage (200 V/div), and phase current (5 A/div) with $m = 1.0$.

A. Steady-State Results with R–L Load

Fig. 18 shows the experimental results of phase voltage, line voltage, and phase current with modulation index $m = 1.0$ and Fig. 19 shows the flying capacitor voltages and dc-link capacitor voltages under different modulation indexes. The performance under unbalanced load is also tested in Fig. 20. A 50 Ω resistor is inserted into the circuit and the load current of phase ***a*** is decreased to 1/3 of the other two phases. However, the dc-link capacitor voltages and FC voltages are still balanced very well.

B. Dynamic-State Results with R–L Load

Fig. 21 shows the dynamic-state performance of the flying capacitor voltage balancing method. The voltages of flying capacitors $C_{\rm fx1}$ and $C_{\rm fx2}$ are balanced at the beginning. At about $t = 4$ s, the three-phase flying capacitor voltages are set to 20% higher than, equal to, and 20% lower than the nominal values, respectively. All the capacitor voltages stabilize at the new given values quickly. At about $t = 14$ s, all the capacitor voltages are set back to the nominal values and balanced soon.

Fig. 22 shows the dynamic-state performance of the central dc-link capacitor voltage balancing method. The dc-link capacitor voltages are controlled balanced at the beginning. At about $t = 4$ s, the central dc-link capacitor voltage is set to 20% higher than the nominal value and then gradually stabilizes at the new given value. At $t = 14$ s, the central dc-link capacitor voltage is set back to the nominal value and balanced again.

Fig. 23 shows the dynamic-state performance of the upper and lower dc-link capacitor voltage balancing method. The dc-link capacitor voltages are controlled balanced at the beginning. At about $t = 2$ s, the upper and lower dc-link capacitor voltages are set to 10% higher and 10% lower than the nominal values. The two capacitor voltages gradually stabilize at the new given values. At about $t = 6$ s, the upper and lower dc-link capacitor voltages are set back to the nominal values and balanced again.

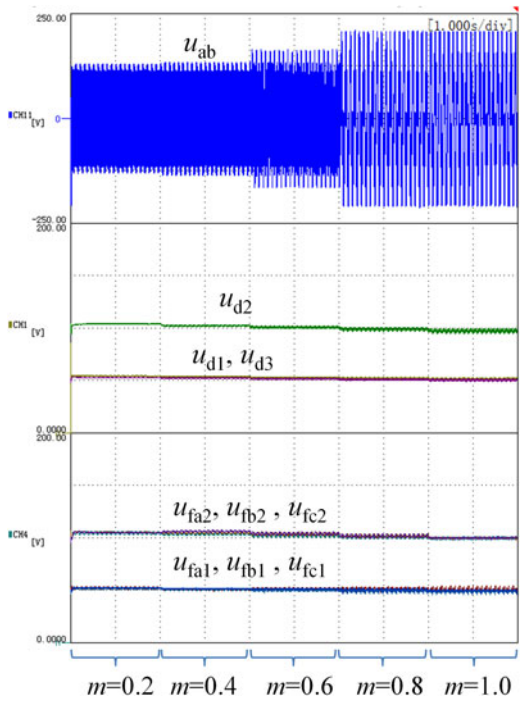

Fig. 19. Flying capacitor and dc-link capacitor voltages under different modulation indexes.

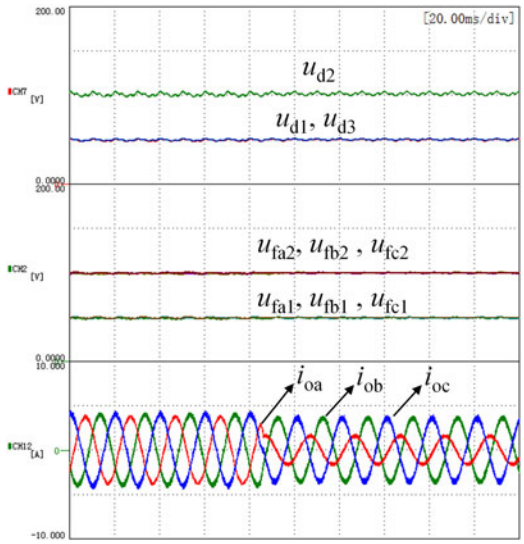

Fig. 20. Experimental result of unbalanced load: (a) DC-link capacitor voltages (50 V/div), (b) FC voltages (50 V/div), and (c) unbalanced three-phase currents (5 A/div).

C. Motor Drive Results

In order to verify the performance of 5L-HC converter in motor drive applications, a 2 kW induction motor is used as

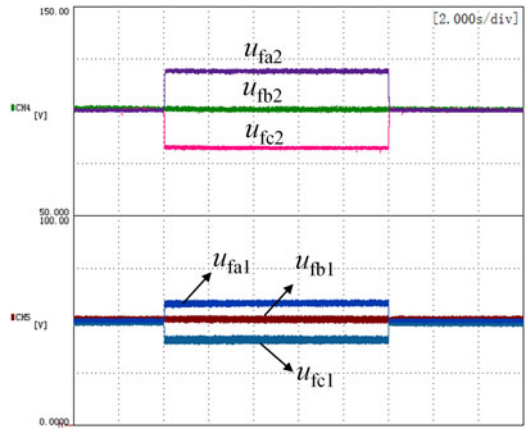

Fig. 21. Dynamic-state experimental result of three-phase FC voltages (25 V/div).

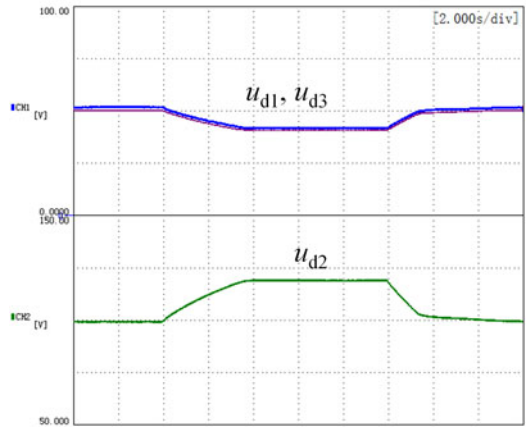

Fig. 22. Dynamic-state experimental result of the central dc-link capacitor voltage (25 V/div).

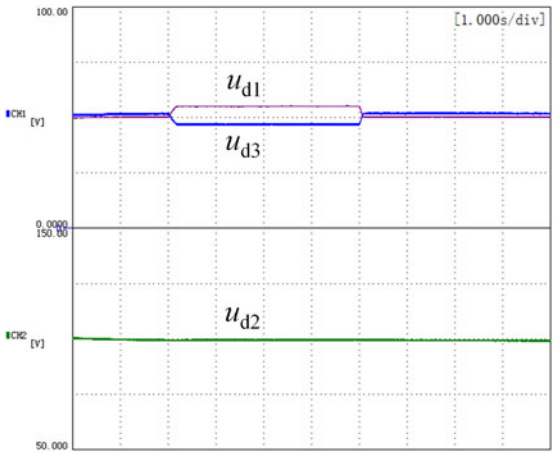

Fig. 23. Dynamic-state experimental result of the upper and lower dc-link capacitor voltages (25 V/div).

load. Fig. 24 shows the experimental result of motor acceleration from 1 to 30 Hz using VVVF control. During the whole process, the dc-link and FC voltages are maintained at their nominal voltages stably. The above simulation and experimental results demonstrate that the proposed voltage balancing method has an effective and powerful control to the dc-link and FC voltages.

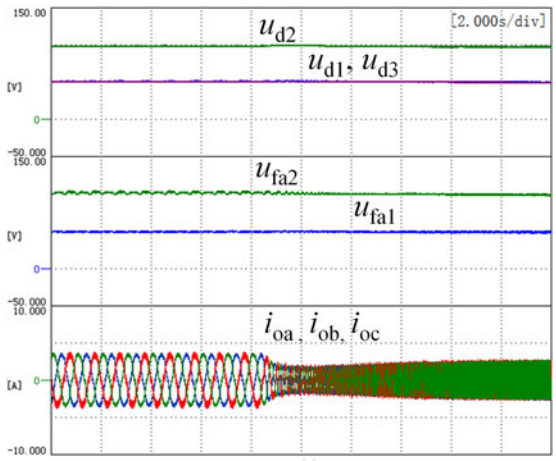

Fig. 24. Experimental result of driving an induction motor. From top to bottom are dc-link capacitor voltages (50 V/div), FC voltages of phase ***a*** (50 V/div), and three-phase motor currents (5 A/div).

VII. Conclusion

5L-HC converter is a competitive and practical multilevel topology for medium-voltage high-power conversions without the need of switches connected in series. This paper focuses on the capacitor voltage balancing problem of this converter, including the voltage balancing of dc-link capacitors and FCs. The switching function model of the NP currents and FC currents is analyzed first and then an average-value model for capacitor voltage ripples is derived. It is found that the central dc-link capacitor voltage ripple only depends on the difference of the two NP currents while the upper and lower dc-link capacitor voltage imbalance only depends on the sum of the two NP currents. Based on this model, a decoupled voltage balancing method is proposed. The central dc-link capacitor and the FC voltages are balanced using modified PS-PWM and four precise duty ratios can be calculated. The upper and lower dc-link capacitor voltages can be balanced by optimal ZSV injection. Simulation and experimental results demonstrate the validity of this method.

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