

# Single-Phase Converter With Shared Leg and Generalizations

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**Abstract**—In this paper, a single-phase shared leg converter is proposed along with two generalizations. The basic configuration has three two-level insulated gate bipolar transistor (IGBT) legs and is cascaded on the main power system by means of two injection transformers, such that one of these legs is shared between the transformers. The generalizations are expanded cases in which the converter has  $N_{\text{leg}}$  legs. The first generalization is the cascaded shared leg (CSL), where the converter is cascaded by  $N_{\text{leg}} - 1$  transformers, and one of the  $N_{\text{leg}}$  legs is shared between all transformers. The second is the modular CSL, where  $N_{\text{mod}}$  modules, each one similar to the basic configuration, are cascaded by  $2N_{\text{mod}}$  transformers. The conventional configurations considered for general comparisons are the cascaded h-bridge (CHB) and the cascaded half-bridge (CHfB). In this paper, we show that proposed configurations provide multilevel ac voltages with greater levels-per-switch ratio compared to the CHB. We also show that proposed CSL generalization has practically the same levels-per-switch than conventional CHfB and saves one transformer. Simulations and experimental results are shown to demonstrate proposed configurations performance and feasibility.

**Index Terms**—Cascaded systems, dc–ac power conversion, harmonic distortion, insulated gate bipolar transistor (IGBT) switches, level-shifted pulse width modulation, multilevel systems, transformers.

## I. INTRODUCTION

MULTILEVEL voltage source converters (VSC) have been developed by researchers and engineers in order to supply the industry demand for devices with better power quality, lower operational costs, and greater power and voltage capabilities [1], [2]. These converters are traditionally classified in the literature in three main topology groups:

- 1) the neutral point clamped [3], [4];
- 2) the flying capacitor [5];
- 3) the cascaded multilevel [6], [7].

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DC–AC VSC have many applications, which can range from uninterruptible power supplies (UPS) [8], photovoltaic power conditioning [9], [10] and ac motor drivers [11], to dynamic voltage restorers (DVR) [12] and active power filters in general [13], [14].

Converter topologies with shared legs have been studied for quite some time. Early topologies of three-legged single-phase ac–dc–ac converters with one shared leg can be found in [15], where an UPS with a diode leg on the rectifier side is proposed, and in [16], where a voltage regulator composed only of controlled switches was proposed. These configurations employ a T-topology that has been utilized not only for ac–dc–ac conversion, but also for dc–ac applications [17].

The conventional cascaded h-bridge (CHB) [10], [18]–[20] provides a good cost effective solution between multilevel voltage source inverters, but lacks flexibility when it comes to increasing the number of levels generated at the output voltage. Transformer-less CHB are relatively convenient because they may save the cost, space, and weight of injection transformers, but require multiple isolated dc-links, demanding greater number of dc-link capacitors and sources. There are cases in which this is a good solution because the isolated dc-sources are naturally available, such as in photovoltaic systems [10]. Nevertheless, if the number of levels supplied in the output ac voltage needs to be increased while keeping the same number of devices, the converter has to use asymmetric h-bridges [21], which is inconvenient for photovoltaic systems, for example, since panels with different dc-voltage and power ratings would have to be designed. Moreover, if the primary electrical power source is a single ac-voltage source, such as the electrical grid, multiple transformers must be employed to generate isolated rectifiers in order to supply each h-bridge with a dc-link.

In these cases, it becomes more attractive to utilize a single dc-source for all bridges and cascade them by means of injection transformers [20]. Inverters cascaded by transformers are solutions that have been observed quite frequently in the literature [20], [22]–[25]. They provide enhanced system reliability by saving dc-link sources and capacitors, which are more susceptible to failure than transformers [26]. They also demand a simpler control system for the dc-link voltage, when required [24], [25], and permit to improve the output voltage by setting proper turns ratios for the transformers [20], [25].

CHB can provide  $N_{\text{leg}} + 1$  levels for the multilevel output voltage in the symmetric case, or up to  $3^{N_{\text{leg}}/2}$  levels in the asymmetric one, where  $N_{\text{leg}}$  is the total number of legs of the

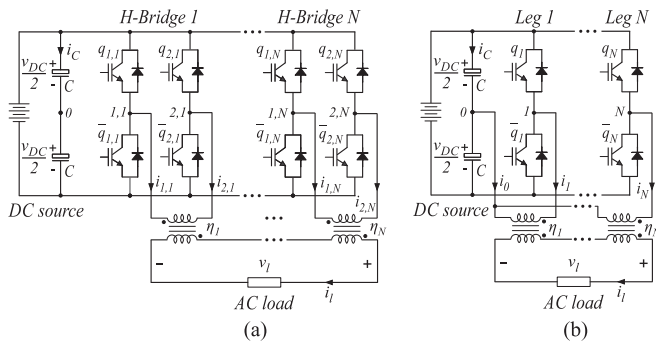


Fig. 1. Generalization of the conventional configurations applied as inverters. (a) Single-phase CHB, where  $N = N_{\text{leg}}/2$ . (b) Single-phase CHfB, where  $N = N_{\text{leg}}$ .

CHB structure. For the option with injection transformers [see Fig. 1(a)],  $N_{\text{leg}}/2$  transformers are needed to connect the converter to the load.

If performance is of great concern and more levels-per-switch are required, another conventional option is the cascaded half-bridge (CHfB) [27]. Its transformer-less version requires two times the number of dc-links and capacitors compared to the CHB. Its version with injection transformer, shown in Fig. 1(b), can provide up to  $2^{N_{\text{leg}}}$  levels. Nevertheless, it requires  $N_{\text{leg}}$  transformers on the load side (twice as the CHB) and access to the dc-link midpoint, which makes it use two capacitors of capacitance  $2C$  instead of one of capacitance  $C$ . This adds complexity to the control system because these capacitors need to be regulated so they have equal voltages.

In this paper, alternatives to the conventional CHB and CHfB with injection transformers are presented. As it will be shown, proposed configurations present greater performance in comparison to the CHB, providing more levels-per-switch, and utilize less transformers than the CHfB with equivalent performance. They can be generalized for cases with  $N_{\text{leg}}$  legs, and have modular options that have the flexibility of producing more or less levels-per-switch at the cost of greater number of transformers for greater number of levels.

The basic proposed configuration is the shared leg converter, which is a three-leg single-phase converter with one shared leg and two injection transformers, shown in Fig. 2(a). Its generalizations are 1) the cascaded shared leg (CSL), shown in Fig. 2(b), and 2) the modular CSL (MCSL), shown in Fig. 2(c). The first one produces more levels-per-switch with more transformers, whereas the last one produces less levels (but even so more than conventional CHB) with less transformers.

The MCSL generalization shown in Fig. 2(c) is in fact one of many possible cases. By utilizing the proposed law of formation, modules with any quantity of insulated gate bipolar transistor (IGBT) legs can be constructed, but for illustration and analysis purposes the one considered has minimum number of legs per module, which is 3. The proposed configuration and its generalizations are suited for both ac–dc and dc–ac conversion, which yields applications such as rectifiers, inverters, DVR, and series filters. However, in this paper, they are analyzed in the dc–ac perspective, more specifically applied as inverters feeding a generic ac load.

In order to evaluate proposed inverters, proposed generalizations with  $N_{\text{leg}} = 6$  legs are compared by means of simulations with the conventional CHB inverter composed of three h-bridges, so that the better performance of proposed systems can be demonstrated. Experimental results are also provided with  $N_{\text{leg}} = 4$  legs for the CSL generalization and conventional CHB.

## II. PROPOSED CONFIGURATION AND GENERALIZATIONS

An usual technique to increase the number of levels in the output ac voltage of multilevel static converters based on cascaded cells is to operate with asymmetric cells [20], [21]. While symmetric operation allows to distribute the power evenly between the cells, the asymmetric operation tends to concentrate the power processed on some cells because the voltage contribution of each cell is different, causing an increase in the levels-per-switch ratio.

The CHB and the CHfB are conventional configurations of cascaded multilevel converters whose versions with injection transformers are shown in Fig. 1. Since all legs are connected to the same dc-link, the symmetrical and asymmetrical operations are defined by the transformers turns ratios, which apportion the voltage contribution of each cell. In our paper, we focus on the asymmetrical operation, such that the turns ratios of the transformers are different and must be set in order to increase the number of levels generated with relation to the symmetrical cases.

Considering this, the motivation for proposing the generalizations of the shared leg topology introduced in this paper reside in some problems found in these asymmetrical conventional configurations, which are 1) for the CHB, the levels-per-switch produced are not optimized because the cells are composed by pairs of two level legs connected to a single transformer, forcing that the legs within a pair have the same voltage contribution to the load, and 2) for the CHfB, even though the levels-per-switch is optimal because each leg is connected to its own transformer, it requires access to the dc-link midpoint, requiring a specific control loop to balance the voltages of the two dc-link capacitors. In comparison, proposed configurations provide many more levels-per-switch than the CHB, and do not require the dc-link midpoint connection of the CHfB.

Henceforward, we consider that  $\eta$  denotes a transformer turns ratio, which is the factor to which the voltage applied to the primary side is multiplied to generate the voltage on the secondary side. Additionally, each turns ratio has an index that addresses it to the correspondent transformer. Taking Figs. 1 and 2 for reference, each transformer has its corresponding turns ratio  $\eta$  shown near it. Hence, the transformers are named after the index of their respective turns ratios. For example, if a transformer has turns ratio denoted by  $\eta_{2,1}$ , it is then labeled as transformer  $T_{2,1}$ . Also, each converter leg is named after its midpoint node from which it is connected to the corresponding transformer. For example, leg 2,1 is the one whose midpoint is node 2,1, which in turn is connected to transformer  $T_{2,1}$ .

In the proposed shared leg configuration [see Fig. 2(a)], legs 1 and 2 are connected to the primary positive terminals of

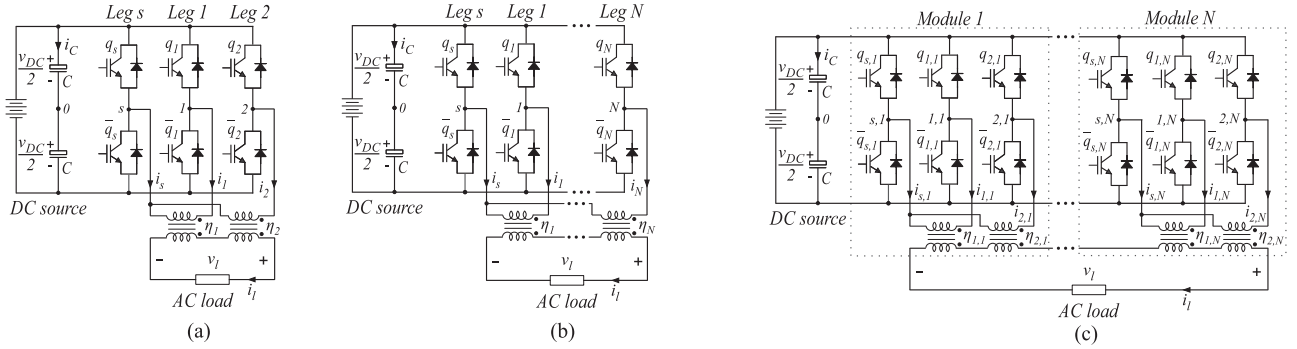


Fig. 2. Proposed single-phase converters and generalizations applied as inverters. (a) Proposed shared leg converter, with three legs. (b) CSL generalization, where  $N = N_{leg} - 1$ . (c) MCSL generalization, where  $N = N_{leg}/3$ .

transformers  $T_1$  and  $T_2$ , respectively. Leg  $s$ , which is the shared leg, is connected to the primary negative terminal of both transformers. The output voltage  $v_l$  is produced by cascading the secondaries of the injection transformers. Following this logic, we introduce two generalizations.

Proposed CSL generalization [see Fig. 2(b)] consists of adding new legs by replicating the configuration of these transformers, such that every new leg is connected to the primary side positive terminal of its respective transformer, and the shared leg  $s$  is connected to negative terminal of all transformers primaries.

The second proposed generalization is the MCSL [see Fig. 2(c)], that is produced by simply defining the proposed shared leg converter as a modular unity. Then, it is replicated such that  $N_{mod}$  modules are cascaded by means of  $2N_{mod}$  transformers to produce the multilevel voltage  $v_l$ , composing a resultant converter with  $N_{leg} = 3N_{mod}$  legs. Other possibilities of MCSL generalizations can be generated by adding new legs to each module in the same way done to the CSL generalization. In this paper, we address only the MCSL generalization with three legs per module.

The conventional CHB [see Fig. 1(a)] is the main conventional configuration considered for comparisons, where  $N_{hb}$  h-bridges are cascaded by means of  $N_{hb}$  transformers, in which case the resultant converter has  $N_{leg} = 2N_{hb}$  legs. The conventional CHfB [see Fig. 1(b)] is shown as a conventional option with optimal levels-per-switch output voltage, requiring  $N_{leg}$  transformers, but is not effectively considered in simulation and experimental comparisons because it needs access to the dc-link midpoint, requiring double the number of capacitors, and a control system to balance the dc-link capacitors voltage, all this to generate one more level than the proposed CSL generalization, requiring also one additional transformer.

### III. VOLTAGE EQUATIONS

In the next topics, important voltage equations for the systems understanding are shown for proposed CSL and MCSL generalizations, and for conventional CHB.

#### A. Proposed CSL Generalization

For proposed CSL, it is considered from now on that the subscript  $k$  relates to the variables from the nonshared legs, such that  $k = \{1, 2, \dots, K\}$ , where  $K = N_{leg} - 1$ . On the other

hand, the subscript  $s$  relates to the variables from the shared leg. Also, the turns ratio of the transformer linked to leg  $k$  is  $\eta_k$ . Then, if  $v_{k,0}$  is the pole voltage produced by leg  $k$ , or  $v_{s,0}$  for leg  $s$ , the resultant voltage  $v_l$  produced is given by

$$v_l = \sum_{k=1}^K \eta_k v_{k,0} - \eta_s v_{s,0} \quad \eta_s = \sum_{k=1}^K \eta_k \quad (1)$$

where  $\eta_s$  is the virtual turns ratio that multiplies the pole voltage  $v_{s,0}$ . Observe that, since the contribution of each pole voltage to the multilevel voltage  $v_l$  is apportioned by the turns ratios  $\eta_k$ , it is possible to calculate these turns ratios to maximize the number of levels. This is valid for all configurations, and the calculation method is going to be shown in the following section.

#### B. Proposed MCSL Generalization

For proposed MCSL, it is considered that the subscript  $k$  relates a variable to a specific nonshared leg within a module, such that  $k = \{1, 2\}$ , and the subscript  $s$  relates the variable to the shared leg. In turn, the subscript  $k_m$  relates a variable to a specific module  $k_m$ , such that  $k_m = \{1, 2, \dots, K_m\}$ , where  $K_m = N_{mod}$ . Then, the resultant subscript that addresses a variable to a specific leg of a specific module is denoted by  $k, k_m$  for the nonshared legs, and  $s, k_m$  for the shared legs. For example, the current  $i_{k,k_m}$  is the current flowing out of leg  $k$  of module  $k_m$ .

Then, the turns ratio of the transformer linked to leg  $k$  of converter  $k_m$  is  $\eta_{k,k_m}$ . If the pole voltage produced by the leg  $k$  of converter  $k_m$  is  $v_{k,k_m,0}$ , and  $v_{s,k_m,0}$  for leg  $s$ , the resultant output voltage  $v_l$  is given by

$$v_l = \sum_{k_m=1}^{K_m} \left( \sum_{k=1}^2 \eta_{k,k_m} v_{k,k_m,0} - \eta_{s,k_m} v_{s,k_m,0} \right) \quad \eta_{s,k_m} = \sum_{k=1}^2 \eta_{k,k_m} \quad (2)$$

where  $\eta_{s,k_m}$  are virtual turns ratios that multiplies the pole voltages  $v_{s,k_m,0}$ .

#### C. Conventional CHB Generalization

For conventional CHB, we consider that the subscript  $k$  relates to the variables of each leg within an h-bridge, such that  $k =$

$\{1, 2\}$ , and that the subscript  $k_h$  denotes the variables of the h-bridge  $k_h$  as a hole, such that  $k_h = \{1, 2, \dots, K_h\}$ , where  $K_h = N_{hb}$ . Then, the resultant subscript that addresses a variable to a specific leg of a specific h-bridge is denoted by  $k, k_h$ . For example, the current  $i_{k,k_h}$  is the current flowing out of the leg  $k$  of the h-bridge  $k_h$ .

Then, the turns ratio of the transformer linked to the h-bridge  $k_h$  is  $\eta_{k_h}$ . If the pole voltage produced by the leg  $k$  of the h-bridge  $k_h$  is  $v_{k,k_h 0}$ , the resultant output voltage  $v_l$  is given by

$$v_l = \sum_{k_h=1}^{K_h} \eta_{k_h} (v_{1,k_h 0} - v_{2,k_h 0}). \quad (3)$$

#### IV. TURNS RATIO CALCULATION

The criterion chosen in order to calculate the transformers turns ratios is the optimization of the output voltage  $v_l$  waveform. This means that turns ratios are calculated to generate the maximum equally spaced number of levels for  $v_l$ . When turns ratios are calculated with this purpose, we say that they are *optimal turns ratios*.

Nevertheless, it is possible to establish other criteria. One of them is generating less levels than the maximum, so that some levels are produced by more than one possible switches states. In this case, we say that these levels have *redundancies*, which can be utilized to reduce the switching frequency. Turns ratios calculated for this case are labeled *nonoptimal*.

Because optimal turns ratios calculations are unique for each configuration (though variations are possible, they are basically equivalent to the ones presented here), it is possible to cover them all. But nonoptimal cases are very vast in possibilities, such that their design must be done case by case. Hence, in this section, we will show how to calculate optimal turns ratios, and at the end an example of nonoptimal calculation is going to be given.

##### A. Proposed CSL Generalization

Here, we define turns ratios  $\eta_k$  in terms of two components:  $\eta_p$  and  $\eta_{k_s}$ . They are, respectively, the turns ratios of the primary and the secondary sides of transformer  $T_k$ . By standard, it is considered that  $\eta_p$  is the primary side turns ratio for all transformers. Then, the value that differ from one transformer to another is  $\eta_{k_s}$ , such that  $\eta_k$  is given by

$$\eta_k = \eta_{k_s} / \eta_p. \quad (4)$$

In order to maximize the number of levels  $N_{|v_l|}$  generated for  $v_l$ , for a converter with  $N_{leg}$  legs,  $\eta_{k_s}$  and  $\eta_p$  are calculated by (5). The number of levels  $N_{|v_l|}$  generated is given by (6)

$$\eta_{k_s} = 2^{(K-k)} \quad \eta_p = \sum_{k=1}^K \eta_{k_s} \quad (5)$$

$$N_{|v_l|} = 2^{N_{leg}} - 1 \quad (6)$$

where  $K = N_{leg} - 1$ .

If all that has been stated in order to calculate  $\eta_k$  is followed, the maximum voltage level of  $v_l$  produced by the converter, labeled  $v_{DCm}$ , is given by (7) in function of the dc-link voltage

$v_{DC}$  and turns ratios  $\eta_k$

$$v_{DCm} = \sum_{k=1}^K \eta_k v_{DC} = v_{DC}. \quad (7)$$

Because  $\eta_p$  is common to all transformers, it does not influence the number of levels  $N_{|v_l|}$  generated. In fact,  $\eta_p$  is a degree of freedom that has influence over  $v_{DCm}$ , along with  $v_{DC}$ . Observe that, if  $\eta_p$  is calculated accordingly to (5), we have that  $\sum_{k=1}^K \eta_k = 1$ , which leads to  $v_{DCm} = v_{DC}$ , as stated in (7). Then, even though  $\eta_p$  could assume any value from the standpoint of levels maximization, we establish as standard that it is calculated such that  $v_{DCm} = v_{DC}$ , in this configuration and in all others (even in nonoptimal cases). In this way, we grant the same values of dc-link voltage  $v_{DC}$  and maximum voltage  $v_{DCm}$  to each converter. This is important in order to normalize the semiconductor losses comparison, which are going to be analyzed further because if we establish the same  $v_{DCm}$  for all configurations, we also want them to have the same dc-link voltage  $v_{DC}$ , so that we make fair switching losses comparison. Moreover, different values of  $\eta_p$  yields different current ratings in each converter leg, affecting conduction losses. In other words, because  $\eta_p$  has indirect influence over semiconductor losses, it is calculated so that it does not benefit any configuration.

##### B. Proposed MCSL Generalization

Like the CSL generalization, for the MCSL the turns ratios  $\eta_{k,k_m}$  are also given in terms of two components:  $\eta_p$  and  $\eta_{k_s,k_m}$ . Likewise, they are, respectively, the turns ratios of the primary and the secondary sides of transformer  $T_{k,k_m}$ . Since  $\eta_p$  is also considered the same for all transformers,  $\eta_{k,k_m}$  is given by (8) in function of  $\eta_{k_s,k_m}$  and  $\eta_p$

$$\eta_{k,k_m} = \eta_{k_s,k_m} / \eta_p. \quad (8)$$

For  $N_{mod}$  modules, the turns ratios  $\eta_{k_s,k_m}$  and  $\eta_p$  are calculated by (9) in order to maximize the number of levels generated at the output voltage  $v_l$ , such that  $N_{|v_l|}$  is calculated by (10)

$$\eta_{k_s,k_m} = 2^{(2-k)} \times 7^{(K_m - k_m)} \quad \eta_p = \sum_{k_m=1}^{K_m} \sum_{k=1}^2 \eta_{k_s,k_m} \quad (9)$$

$$N_{|v_l|} = 7^{N_{mod}} \quad (10)$$

where  $K_m = N_{mod}$ .

Following the equations so far, voltage  $v_{DCm}$ , which is the maximum value of  $v_l$ , can be calculated by (11) in function of the dc-link voltage  $v_{DC}$  and turns ratios  $\eta_{k,k_m}$

$$v_{DCm} = \sum_{k_m=1}^{K_m} \sum_{k=1}^2 \eta_{k,k_m} v_{DC} = v_{DC} \quad (11)$$

##### C. Conventional CHB Generalization

Similarly to the proposed generalizations (CSL and MCSL), in the CHB the turns ratio  $\eta_{k_h}$  is given in terms of two components,  $\eta_p$  and  $\eta_{k_h s}$ , which are, respectively, the turns ratios of the primary and the secondary sides of transformer  $T_{k_h}$ . Since  $\eta_p$  is

the same for all transformers,  $\eta_{k_h}$  is given by (12) in function of  $\eta_{k_h s}$  and  $\eta_p$

$$\eta_{k_h} = \eta_{k_h s} / \eta_p. \quad (12)$$

For  $N_{hb}$  h-bridges, the turns ratios  $\eta_{k_h s}$  and  $\eta_p$  are calculated by (13) in order to maximize the number of levels  $N_{lv1}$ , which is given by (14)

$$\eta_{k_h s} = 3^{(K_h - k_h)} \quad \eta_p = \sum_{k_h=1}^{K_h} \eta_{k_h s} \quad (13)$$

$$N_{lv1} = 3^{N_{hb}} \quad (14)$$

where  $K_h = N_{hb}$ .

The voltage  $v_{DCm}$ , which is the maximum value of  $v_l$ , is calculated by (15) in function of the dc-link voltage  $v_{DC}$  and turns ratios  $\eta_{k_h}$

$$v_{DCm} = \sum_{k_h=1}^{K_h} \eta_{k_h} v_{DC} = v_{DC}. \quad (15)$$

#### D. Nonoptimal Turns Ratio for CSL Configuration

As mentioned, even though the optimal turns ratios calculation is our standard, nonoptimal cases are also possible. These cases have less levels than the maximum calculated by (6), (10), and (14), but are still evenly spaced. Also, by this method, some levels have redundancies that can be utilized in the Level-Shifted (LS)-PWM technique to reduce the switching frequency. Here, we show one nonoptimal example for proposed CSL, which is analyzed further in the simulation results. Some other cases not covered here are also shown in the experimental results.

In our example case,  $\eta_k$  is also given by (4), but the way in which the  $\eta_{k_s}$  are calculated is different. The principle of this design is that  $\eta_{N_s} = 1$  and  $\eta_{N-1_s} = 2$  ( $N = N_{leg} - 1$ ), and all other  $\eta_{k_s}$  are the sum of all  $\eta_{k'_s}$ , where  $k' > k$ . As in previous cases,  $\eta_p$  is the sum of all  $\eta_{k_s}$ . If we put this into equations, for  $N_{leg}$  legs, the turns ratios  $\eta_p$  and  $\eta_{k_s}$  are calculated by (16) to produce  $N_{lv1}$  levels given by (17). As in the optimal case, voltage  $v_{DCm}$  is calculated by (7)

$$\eta_{k_s} = \begin{cases} 3 \times 2^{(K-2-k)}, & \text{if } k < N_{leg} - 2 \\ 2^{(K-k)}, & \text{if } k \geq N_{leg} - 2 \end{cases} \quad \eta_p = \sum_{k=1}^K \eta_{k_s} \quad (16)$$

$$N_{lv1} = 3 \times 2^{(N_{leg}-2)} + 1 \quad (17)$$

where  $K = N_{leg} - 1$ .

#### V. LS-PWM TECHNIQUE

From now on, the superscript \* is an indication of a reference variable. For example,  $v_i^*$  is the reference of voltage  $v_l$ . Also, when an example is needed, the configuration considered in this section is the basic proposed shared leg converter, shown in Fig. 2(a). Nevertheless, the method described here is general and its principle can be extended for any configuration, proposed or conventional.

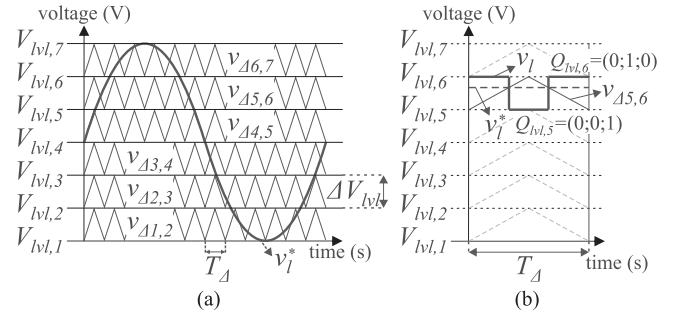


Fig. 3. Illustration of the LS-WPM technique for  $N_{lv1} = 7$ . (a) Carriers set with reference signal  $v_i^*$ . (b) Generation of the actual voltage  $v_l$  by comparing  $v_i^*$  with  $v_{\Delta d,u}$ .

Given that voltage  $v_i^*$  is set accordingly to the load voltage requirement, such that  $-v_{DCm} \leq v_i^* \leq v_{DCm}$  at any given time, the LS-PWM is responsible for generating the switching states for the IGBT legs in function of  $v_i^*$ , so that the proper multilevel voltage  $v_l$  is applied to the load. Then, assuming that the topology can generate  $N_{lv1}$  voltage levels equally spaced ranging from  $-v_{DCm}$  to  $v_{DCm}$ ,  $v_i^*$  must be compared with a certain level-shifted triangular carrier  $v_\Delta$ , chosen among a set of  $N_{lv1} - 1$  carriers, such that the maximum and the minimum values of the carrier stand between the two levels closest to  $v_i^*$ , within a carrier period  $T_\Delta$ . This way, if the proper switches are associated to the true and false results of the comparison,  $v_l$  assumes only the values of the two levels closest to  $v_i^*$ , such that the voltage variation of  $v_l$  is minimized, optimizing its profile, and reducing harmonic distortion.

Hence, for  $N_{lv1}$  levels, there must be  $N_{lv1} - 1$  level-shifted carriers, such that the comparison of  $v_i^*$  with these carriers gives  $v_l$  accordingly to (18), where each voltage level is denoted by  $V_{lv1,n_l}$ , such that  $n_l = \{1, 2, \dots, N_{lv1}\}$ , where  $V_{lv1,1} < V_{lv1,2} < \dots < V_{lv1,N_{lv1}}$ , and each level-shifted carrier is denoted by  $v_{\Delta d,u}$ , such that  $d = \{1, 2, \dots, N_{lv1} - 1\}$ ,  $u = d + 1$ , and  $V_{lv1,d} \leq v_{\Delta d,u} \leq V_{lv1,u}$

$$v_l = \begin{cases} V_{lv1,u}, & \text{if } v_i^* > v_{\Delta d,u} \\ V_{lv1,d}, & \text{if } v_i^* \leq v_{\Delta d,u} \end{cases} \quad \begin{matrix} V_{lv1,d} \leq v_i^* < V_{lv1,u} \\ u = d + 1. \end{matrix} \quad (18)$$

In this way, two levels  $V_{lv1,d}$  and  $V_{lv1,u}$  define a region  $d, u$ , which contains both carrier  $v_{\Delta d,u}$  and the current value of  $v_i^*$ . What has been described so far is illustrated in Fig. 3 for the particular case where  $N_{lv1} = 7$ , which corresponds to the basic proposed shared leg converter. In order to generate  $N_{lv1} = 7$ , it is set  $\eta_1 = 2/3$  and  $\eta_2 = 1/3$ .

In Fig. 3(a), it can be seen the complete set of level-shifted carriers  $v_{\Delta d,u}$ , the dc voltage levels  $V_{lv1,n_l}$ , and the reference signal  $v_i^*$ . It is also highlighted the carriers period  $T_\Delta$  and the voltage variation  $\Delta V_{lv1}$  between the dc levels. Fig. 3(b) illustrates the comparison mechanism. Each voltage level  $V_{lv1,n_l}$  can be calculated in function of  $n_l$  by (19), such that  $\Delta V_{lv1}$  is also given in

$$V_{lv1,n_l} = -v_{DCm} + (n_l - 1)\Delta V_{lv1}, \quad \Delta V_{lv1} = \frac{2v_{DCm}}{N_{lv1} - 1}. \quad (19)$$

TABLE I  
SWITCHES STATES MAPPING FOR  $N_{lv1} = 7$

$Q_{lv1,1}$	$Q_{lv1,2}$	$Q_{lv1,3}$	$Q_{lv1,4}$	$Q_{lv1,5}$	$Q_{lv1,6}$	$Q_{lv1,7}$
(1; 0; 0)	(1; 0; 1)	(1; 1; 0)	(1; 1; 1)	(0; 0; 1)	(0; 1; 0)	(0; 1; 1)
			(0; 0; 0)			

The legs switching itself is realized by the comparison logic described so far, considering that to each voltage level  $V_{lv1,n_l}$  corresponds a proper set of switches states  $Q_{lv1,n_l}$ . For example, for the CSL generalization this set is given by (20). For the basic shared leg converter, where  $N_{lv1} = 7$  and  $Q_{lv1,n_l} = (q_s; q_1; q_2)$ , this comparison logic is shown in Fig. 3(b) with correspondent switches states

$$Q_{lv1,n_l} = (q_s; q_1; q_2; \dots; q_N)_{N=N_{leg}-1}. \quad (20)$$

Switches states  $Q_{lv1,n_l}$  must be mapped to the correspondent voltage levels  $V_{lv1,n_l}$  by means of tables, and the PWM system sets appropriate values for  $Q_{lv1,n_l}$  such that (18) is true. For our example case, the corresponding mapping table is Table I. When redundancies occur, as in  $Q_{lv1,4}$ , the PWM designer must use them to favor the topology in some predefined aspect. For example, if a criterion of switching frequency minimization is chosen, then  $Q_{lv1,4} = (1; 1; 1)$  if it switches with  $Q_{lv1,3}$ , and  $Q_{lv1,4} = (0; 0; 0)$  if it switches with  $Q_{lv1,5}$ .

## VI. SIMULATION RESULTS

Simulation results were obtained for both proposed CSL and MCSL generalizations, and conventional CHB, considering  $N_{leg} = 6$  and  $v_{DCm} = 170$  V. For the MCSL, this means  $N_{mod} = 2$  modules, and for CHB configuration, it means  $N_{hb} = 3$  h-bridges. In each case, the results were taken for turns ratios calculated to produce maximum number of levels. For the CSL, additional results were acquired for nonoptimal turns ratio, calculated accordingly to (16).

Then, the specific configurations of simulated cases are labeled as follows: 1) CSL<sub>6l</sub>: CSL configuration with  $N_{leg} = 6$  legs and optimal turns ratios, 2) CSL<sub>6l</sub><sup>nop</sup>: CSL configuration with  $N_{leg} = 6$  legs and nonoptimal turns ratios, 3) MCSL<sub>2m</sub>: MCSL configuration with  $N_{mod} = 2$  modules, 4) CHB<sub>3h</sub>: conventional CHB with  $N_{hb} = 3$  h-bridges. For each configuration, the following turns ratios were calculated:

- 1) CSL<sub>6l</sub>:  $(\eta_1; \eta_2; \eta_3; \eta_4; \eta_5) = (\frac{16}{31}; \frac{8}{31}; \frac{4}{31}; \frac{2}{31}; \frac{1}{31})$ ;
- 2) CSL<sub>6l</sub><sup>nop</sup>:  $(\eta_1; \eta_2; \eta_3; \eta_4; \eta_5) = (\frac{12}{24}; \frac{6}{24}; \frac{3}{24}; \frac{2}{24}; \frac{1}{24})$ ;
- 3) MCSL<sub>2m</sub>:  $(\eta_{1,1}; \eta_{2,1}; \eta_{1,2}; \eta_{2,2}) = (\frac{14}{24}; \frac{7}{24}; \frac{2}{24}; \frac{1}{24})$ ;
- 4) CHB<sub>3h</sub>:  $(\eta_1; \eta_2; \eta_3) = (\frac{9}{13}; \frac{3}{13}; \frac{1}{13})$ .

In every case, it was considered  $f_{\Delta} = 10$  kHz as the standard level-shifted carriers frequency,  $V_l = 110$  V as the nominal rms load voltage, and a resistive-inductive load of resistance  $R_l = 20$   $\Omega$  and inductance  $L_l = 7$  mH, implying in a load power of  $P_l = 600$  W approximately with power factor p.f. = 0.99.

In the following sections, different aspects of simulated proposed configurations CSL<sub>6l</sub>, CSL<sub>6l</sub><sup>nop</sup> and MCSL<sub>2m</sub>, and conventional CHB<sub>3h</sub>, are going to be analyzed.

### A. Load Voltage Harmonic Spectrum and THD Analysis

Fig. 4 depicts the output load voltage  $v_l$  and the load current  $i_l$  for every case considered (the current is amplified by a gain of ten times for better visualization). It was observed that proposed configuration CSL<sub>6l</sub> produced the greatest amount of levels for  $v_l$ , followed by CSL<sub>6l</sub><sup>nop</sup> and MCSL<sub>2m</sub>. Conventional CHB<sub>3h</sub> produced the lowest quantity. The levels are more clearly distinguishable by observing the zoomed views given in each graphic. This was expected because, for the turns ratios established, we had  $N_{lv1} = 63$  levels for configuration CSL<sub>6l</sub>,  $N_{lv1} = 49$  levels for CSL<sub>6l</sub><sup>nop</sup>,  $N_{lv1} = 49$  levels for MCSL<sub>2m</sub>, and  $N_{lv1} = 27$  levels for CHB<sub>3h</sub>. Configuration CSL<sub>6l</sub><sup>nop</sup> produced the same amount of levels than MCSL<sub>2m</sub>. From these graphics, it is possible to conclude that proposed configurations provided better voltage profiles, since more levels were produced with relation to conventional CHB<sub>3h</sub>. Also, by comparing Fig. 4(a) and (b), it becomes clear that the nonoptimal turns ratios reduced the amount of levels provided.

The consequence of the different number of levels produced by each configuration is seen in Fig. 5, which shows their harmonic spectrum from 5 to 55 kHz. The magnitudes are normalized with relation to the magnitude of their respective fundamental components at 60 Hz. It can be seen that all configurations have a main harmonic component in 10 kHz, since the level-shifted carrier frequency is  $f_{\Delta} = 10$  kHz. They also have other minor components around every frequency multiple of 10 kHz. Some values are highlighted in the graphics, and it can be seen that proposed configuration CSL<sub>6l</sub> presented the harmonic components with lowest amplitudes, followed by configurations CSL<sub>6l</sub><sup>nop</sup> and MCSL<sub>2m</sub>, which had very close spectrum profiles. The configuration with greatest harmonic content was conventional CHB<sub>3h</sub>.

Table II shows the total harmonic distortion (THD) values for  $f_{\Delta} = 10$  kHz, calculated for the output voltage  $v_l$  in order to support what has been stated by observing graphical results. The THD obtained confirm the spectrum profiles, it can be seen that proposed configurations provided voltages with lower THD (lower harmonic content). The lowest THD was that of configuration CSL<sub>6l</sub>, followed by CSL<sub>6l</sub><sup>nop</sup>, which had the same THD as configuration MCSL<sub>2m</sub>. Conventional CHB<sub>3h</sub> had the highest THD.

### B. Semiconductors Losses Analysis

Since proposed configurations provided considerably lower voltage THD for  $f_{\Delta} = 10$  kHz, it was possible to lower their LS-PWM carriers frequency  $f_{\Delta}$  in order to rise their THD to make semiconductor losses comparison. By lowering  $f_{\Delta}$ , we expected to lower their switching losses to the point that they provided lower total semiconductor losses than conventional configuration, but kept lower THD. Then, the losses were calculated by lowering proposed configurations  $f_{\Delta}$  to match their THD at 3.2%. Conventional CHB<sub>3h</sub> was maintained with THD = 5% at  $f_{\Delta} = 10$  kHz. The losses results are shown in Table III.

As seen, conduction losses were the same for all configurations, since they all had the same number of semiconductors, but both THD and switching losses of proposed configurations

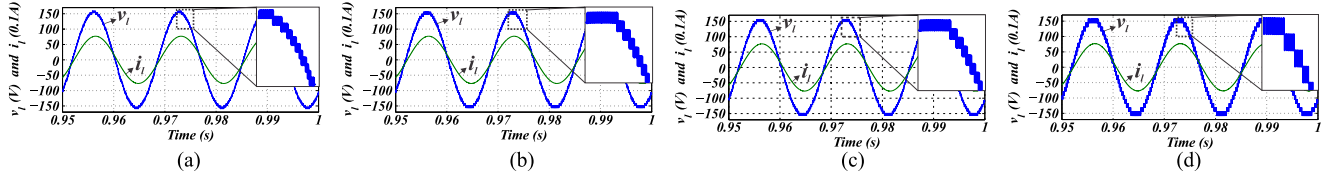


Fig. 4. Simulation results of output voltage  $v_l$  and load current  $i_l$  for all configurations with  $N_{leg} = 6$ . (a) For proposed  $CSL_{6l}$  ( $N_{lv1} = 63$ ). (b) For proposed  $CSL_{6l}^{nop}$  ( $N_{lv1} = 49$ ). (c) For proposed  $MCSL_{2m}$  ( $N_{lv1} = 49$ ). (d) For conventional  $CHB_{3h}$  ( $N_{lv1} = 27$ ).

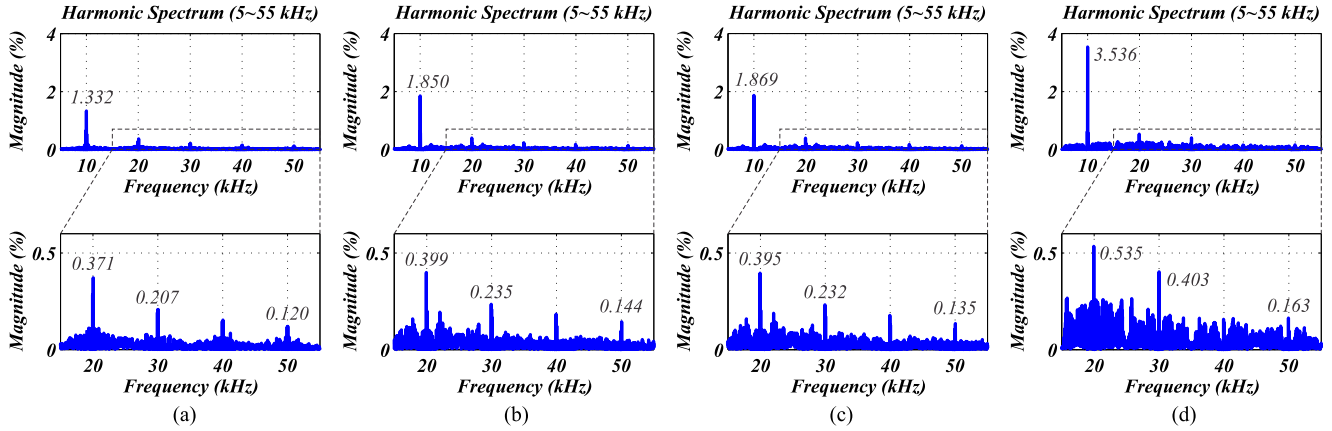


Fig. 5. Normalized harmonic spectrum of output voltage  $v_l$ , from 5 to 55 kHz, obtained from simulation data with  $N_{leg} = 6$  and  $f_{\Delta} = 10$  kHz. The magnitudes are normalized with relation to the fundamental amplitude in each case. (a) For proposed  $CSL_{6l}$ . (b) For proposed  $CSL_{6l}^{nop}$ . (c) For proposed  $MCSL_{2m}$ . (d) For conventional  $CHB_{3h}$ .

TABLE II  
VOLTAGE  $v_l$  THD WITH FIXED CARRIERS FREQUENCY  $f_{\Delta} = 10$  kHz FOR ALL CONFIGURATIONS

	$CSL_{6l}$	$CSL_{6l}^{nop}$	$MCSL_{2m}$	$CHB_{3h}$
$v_l$ THD (%)	2.31	2.90	2.91	5.05

TABLE III  
SEMICONDUCTORS LOSSES WITH VOLTAGE  $v_l$  THD = 3.2% FOR PROPOSED CONFIGURATIONS AND 5% FOR CONVENTIONAL CHB

	$CSL_{6l}$	$CSL_{6l}^{nop}$	$MCSL_{2m}$	$CHB_{3h}$
$f_{\Delta}$ (kHz)	4.5	5.5	5.5	10.0
$v_l$ THD (%)	3.2	3.2	3.2	5.0
Cd. losses (%)	2.23	2.23	2.23	2.23
Sw. losses (%)	0.52	0.44	0.53	0.89
Total (%)	2.75	2.67	2.76	3.12

Losses are normalized with relation to load power  $P_l = 600$  W.

were considerably lower than that of the conventional CHB, which shows their better performance. Proposed configurations  $CSL_{6l}$  and  $MCSL_{2m}$  showed practically the same losses, but  $CSL_{6l}^{nop}$  had them slightly lower because of its lower switching losses. This shows that nonoptimal turns ratios can be used to provide good results by reducing switching losses, even though they cannot give as much levels as the optimal case.

The switching losses results can be further justified by observing Table IV, which shows the switching frequency calculated for the legs of each configuration. In Table IV, it was estab-

TABLE IV  
SWITCHING FREQUENCY FOR THE SWITCHES OF EACH LEG OF EACH CONFIGURATION WITH VOLTAGE  $v_l$  THD = 3.2% FOR PROPOSED CONFIGURATIONS AND 5% FOR CONVENTIONAL CHB

Switch. Freq.	$CSL_{6l}$	$CSL_{6l}^{nop}$	$MCSL_{2m}$	$CHB_{3h}$
$f_{\Delta}$ (kHz)	4.5	5.5	5.5	10.0
$v_l$ THD (%)	3.2	3.2	3.2	5.0
Leg s / s,1 / 1,1 (Hz)	120	120	120	120
Leg 1 / 1,1 / 2,1 (Hz)	600	360	720	1440
Leg 2 / 2,1 / 1,2 (Hz)	1800	840	2040	3120
Leg 3 / s,2 / 2,2 (Hz)	4440	1800	2760	5400
Leg 4 / 1,2 / 1,3 (Hz)	7800	6240	6640	16 520
Leg 5 / 2,2 / 2,3 (Hz)	10 640	13 520	13 840	13 200
Mean value (Hz)	4233	3813	4353	6633

TABLE V  
CURRENT RATING  $\left| \frac{i_{sc}}{i_l} \right|$  FOR THE SWITCHERS OF EACH LEG, NORMALIZED WITH RESPECT TO THE LOAD CURRENT  $i_l$

Current rating	$CSL_{6l}$	$CSL_{6l}^{nop}$	$MCSL_{2m}$	$CHB_{3h}$
Leg s / s,1 / 1,1	100%	100%	87.5%	69.2%
Leg 1 / 1,1 / 2,1	51.6%	50.0%	58.3%	69.2%
Leg 2 / 2,1 / 1,2	25.8%	25.0%	29.2%	23.1%
Leg 3 / s,2 / 2,2	12.9%	12.5%	12.5%	23.1%
Leg 4 / 1,2 / 1,3	6.5%	8.3%	8.3%	7.7%
Leg 5 / 2,2 / 2,3	3.2%	4.2%	4.2%	7.7%

lished THD = 3.2% for proposed configurations and 5% for conventional  $CHB_{3h}$ , as in Table III. The switching frequencies of proposed configurations were considerably lower compared

TABLE VI  
MEAN ABSOLUTE POWER TRANSFERRED BY EACH TRANSFORMER,  
NORMALIZED WITH RELATION TO LOAD POWER  $P_l = 600$  W

Abs. Power	CSL <sub>6l</sub>	CSL <sub>6l</sub> <sup>nop</sup>	MCSL <sub>2m</sub>	CHB <sub>3h</sub>
$T_1$ or $T_{1,1}$	44.1%	42.8%	56.4%	80.7%
$T_2$ or $T_{2,1}$	25.8%	25.0%	38.0%	35.8%
$T_3$ or $T_{1,2}$	14.9%	14.8%	12.4%	15.2%
$T_4$ or $T_{2,2}$	9.3%	10.2%	8.1%	–
$T_5$	5.9%	7.2%	–	–
Total	100.0%	100.0%	114.9 %	131.7 %

to CHB<sub>3h</sub>. The fact that configuration CSL<sub>6l</sub><sup>nop</sup> had lower mean switching frequency shows why it also had lower switching losses. This is also an example of how nonoptimal turns ratio can be used to reduce the number of levels and increase the number of switches states redundancies, decreasing the switching stress. Moreover, the fact that proposed configurations could provide lower THD with lower losses yields not only better performance, but potentially cheaper devices with lower frequency rating.

### C. Switches Current and Transformers Power Rating Analysis

In order to compare the IGBT switches and injection transformers from one configuration to the other, along with Table IV that gives the switching frequencies, the current rating for the IGBTs from each leg and the power rating for each transformer are shown in Tables V and VI, respectively.

By observing Table V, it can be seen that, except for the legs in the first line (Legs  $s / s, 1 / 1, 1$ ), in general the legs from proposed configurations had lower current rating compared to the conventional CHB<sub>3h</sub>, with some legs having slightly higher rating. Configurations CSL<sub>6l</sub> and CSL<sub>6l</sub><sup>nop</sup> had the lowest ratings, except for leg  $s$ . Moreover, by relating Table V to Table IV, it can be noticed that the legs with higher current ratings also had the lowest switching frequencies, and that the ones with highest switching frequencies had lower current ratings. In this matter, proposed configurations had advantage because most of their switches had not only lower current rating, but for THD = 3.2% they also had lower switching frequency, making the total cost of the switches potentially lower.

Table VI shows the mean absolute power rating for each transformer of each configuration. The absolute power transfer accounts positively for negative power transfer, which is the amount of power that flows back to the dc power source. It can be noticed that even though the proposed configurations had more transformers than the conventional CHB<sub>3h</sub>, the power rating of each transformer was in general lower. Conventional CHB<sub>3h</sub> naturally concentrated most power transfer in transformer  $T_1$ , while in the proposed configurations the contribution of other transformers was more significant. This means that, even though proposed configurations require more transformers, these additional transformers are of much lower power rating and, thus, can be lighter and smaller. Moreover, the transformers with greatest absolute power rating in proposed configurations was almost half the rating of that of conventional CHB<sub>3h</sub>.

By observing the total power transferred by all transformers in each case, it can be noticed that in configurations CSL<sub>6l</sub> and CSL<sub>6l</sub><sup>nop</sup> the total absolute power rating was 100%, i.e., there was no negative power transfer. On the other hand, in configuration MCSL<sub>2m</sub> this power exceeded the load power in about 15%, and in the conventional CHB<sub>3h</sub> the excess power was over 30% of load power. These negative power ends up rising the power rating of individual transformers, reducing the efficiency of transformers and associated IGBT legs.

Though it is not trivial to say which option is most cost effective in terms of transformers, one can say that proposed configurations should not be that much expensive. More transformers, indeed, may translate into higher weigh and more space, but in terms of costs there might not be a great difference. Because proposed configurations may also provide better power quality with potentially cheaper switches and lower semiconductor losses, they are an interesting option.

## VII. EXPERIMENTAL RESULTS

The experimental setup is shown in Fig. 6. The inverters where assembled in a workbench composed of 16 IGBT legs and associated drive boards, with independent dc-link capacitors for each leg, which can be connected in parallel to form a common dc-link. Fig. 6(a) shows the front view of the workbench, and only the elements utilized in our setup have been highlighted. The dc source was a single-phase rectifier composed by a diode bridge, and the inverters have been assembled utilizing the four IGBT legs from one module. The injection transformers are shown at the bottom along with the  $RL$  load. Also, a DSP board with an F28335 device is connected to the workbench at its back, as shown in Fig. 6(b). The workbench protection system is also located at its back. Other elements not highlight are signal conditioning boards for the sensors-DSP interfacing and ICs with logic gates that generate the complementary signals for the IGBT legs.

Experimental results are shown in Fig. 7 for proposed configuration CSL with  $N_{leg} = 4$  legs, and for the conventional CHB with  $N_{hb} = 2$  h-bridges. Two situations were also considered, the first where optimal turns ratios were calculated such that the maximum number of levels where produced for  $v_l$ , and the second where nonoptimal turns ratios where established in order to produce intermediate number of levels. For each graphic, the top curve is the output load voltage  $v_l$  and the bottom curve is the load current  $i_l$ . The converters were applied as inverters and, similarly to the simulations results, it was established  $v_{DC} = v_{DCm} = 170$  V. An  $RL$  load of resistance  $R_l = 25 \Omega$  and inductance  $L_l = 7$  mH was fed with a voltage equal to  $V_l = 110$  V rms. This way, a nominal load power of approximately  $P_l = 500$  W with power factor p.f. = 0.99 was established.

Since experiments were made for four different configurations, they are labeled henceforward as follows: 1) CSL<sub>4l</sub>: CSL configuration with  $N_{leg} = 4$  legs and quasi-optimal turns ratios, 2) CHB<sub>2h</sub>: conventional CHB with  $N_{hb} = 2$  h-bridges and optimal turns ratios. Each configuration described also had correspondent nonoptimal turns ratios cases, labeled the same

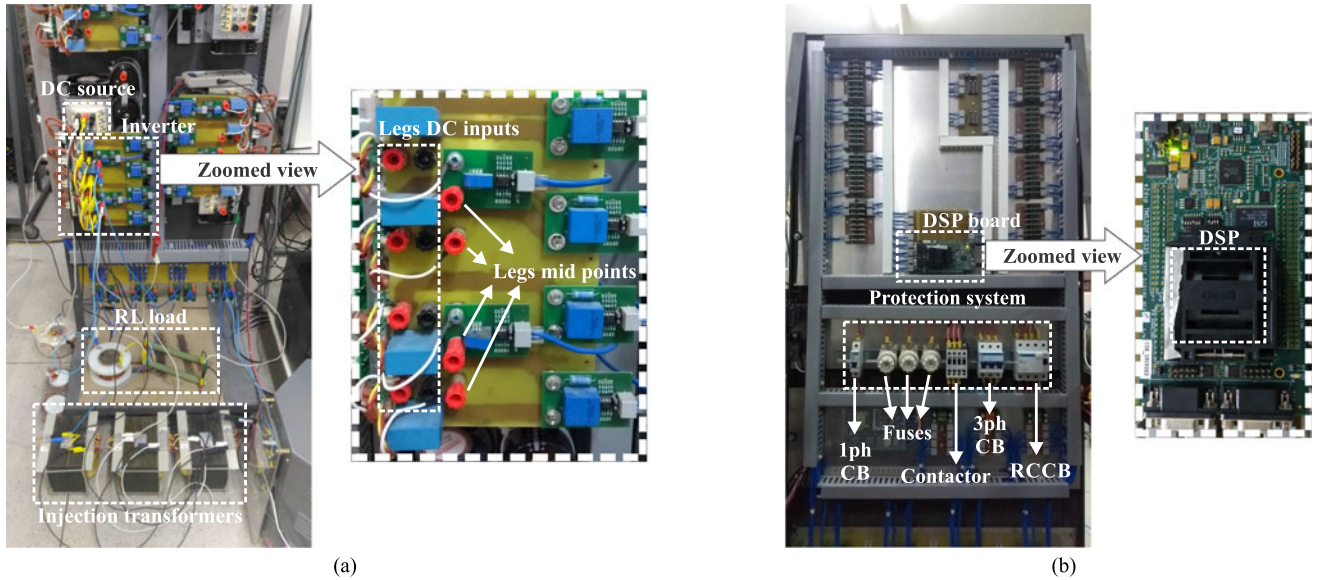


Fig. 6. Workbench utilized for the experimental setup. (a) Front view showing the dc-link source, the inverter, the load, and injection transformers. (b) Back view showing the DSP board and protection system.

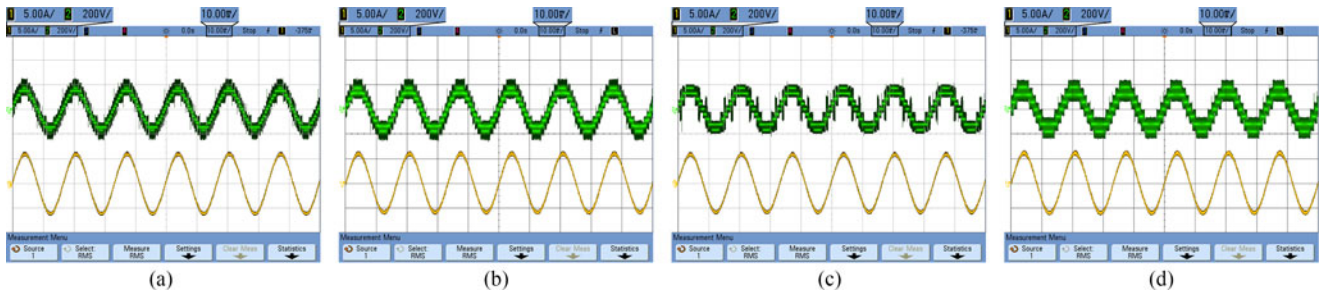


Fig. 7. Experimental results with optimal and nonoptimal turns ratio. Load voltage  $v_l$  is the top curve, and current  $i_l$  is the bottom curve. (a) Proposed  $CSL_{4l}$  ( $N_{lv1} = 13$ ). (b) Proposed  $CSL_{4l}^{nop}$  ( $N_{lv1} = 9$ ). (c) Conventional  $CHB_{2h}$  ( $N_{lv1} = 9$ ). (d) Conventional  $CHB_{2h}^{nop}$  ( $N_{lv1} = 7$ ).

way as the optimal ones, but with the superscript<sup>nop</sup>. For example,  $CSL_{4l}^{nop}$  is configuration  $CSL_{4l}$  with nonoptimal turns ratio. Then, for each configuration the turns ratios calculated were as follows.

- 1) For  $CSL_{4l}$  ( $N_{lv1} = 13$ ):  $(\eta_1; \eta_2; \eta_3) = (\frac{3}{6}; \frac{2}{6}; \frac{1}{6})$ .
- 2) For  $CSL_{4l}^{nop}$  ( $N_{lv1} = 9$ ):  $(\eta_1; \eta_2; \eta_3) = (\frac{2}{4}; \frac{1}{4}; \frac{1}{4})$ .
- 3) For  $CHB_{2h}$  ( $N_{lv1} = 9$ ):  $(\eta_1; \eta_2) = (\frac{3}{4}; \frac{1}{4})$ .
- 4) For  $CHB_{2h}^{nop}$  ( $N_{lv1} = 7$ ):  $(\eta_1; \eta_2) = (\frac{2}{3}; \frac{1}{3})$ .

Notice that the turns ratios set for configuration  $CSL_{4l}$  was not exactly the optimal one. In fact, the optimal number of levels for  $CSL_{4l}$  would be  $N_{lv1} = 15$ , but it was required to approximate the ideal turns ratio by a nonoptimal relation in order to perform the experiment with the transformers available in laboratory. This relation is referred henceforward as quasi-optimal.

The experimental results were obtained in order to demonstrate the feasibility and performance of proposed configuration CSL, and to show the influence in the choice of the transformers turns ratios. Then, while Fig. 7(a) and (c) shows results with optimal turns ratios for configurations  $CSL_{4l}$  and  $CHB_{2h}$ , respectively, Fig. 7(b) and (d) shows results for nonoptimal turns ratios, i.e., configurations  $CSL_{4l}^{nop}$  and  $CHB_{2h}^{nop}$ , respectively.

As seen, for optimal/quasi-optimal turns ratios cases, voltage  $v_l$  presented  $N_{lv1} = 13$  for  $CSL_{4l}$  and  $N_{lv1} = 9$  for  $CHB_{2h}$ . Configuration  $CSL_{4l}$  provided four more levels than  $CHB_{2h}$ , with the same number of legs. Nonoptimal turns ratios cases produced less levels than their correspondent optimal cases, as expected, but kept an even distribution of levels, showing correctness in the turns ratio design. For configuration  $CSL_{4l}^{nop}$ , it could be observed  $N_{lv1} = 9$  levels, four less levels compared to  $CSL_{4l}$ , which was already nonoptimal. Finally, for the conventional conf.  $CHB_{2h}^{nop}$ , it could be observed  $N_{lv1} = 7$  levels, two less levels compared to  $CHB_{2h}$ .

As analyzed in the simulation results, the number of levels produced by the converter in the output voltage  $v_l$  reflects in its harmonic spectrum, as seen in Fig. 8, which shows the spectra from 5 to 55 kHz, for voltages of all experimental cases. The magnitudes are normalized with respect to the fundamental components, in 60 Hz. It can be seen that, similarly to the simulation cases, all configurations had a main harmonic component at 10 kHz, which is the level-shifted carrier frequency, and minor components around frequencies multiple of 10 kHz. Proposed configuration  $CSL_{4l}$  had the lowest harmonic magnitudes,

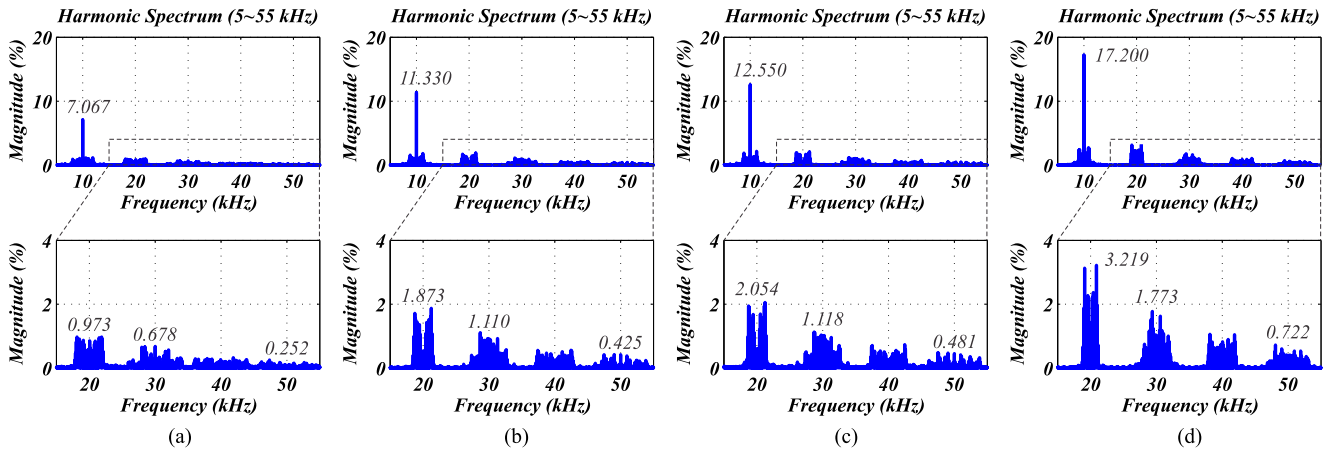


Fig. 8. Normalized harmonic spectrum of output voltage  $v_l$ , from 5 to 55 kHz, obtained from experimental data with  $N_{leg} = 4$  and  $f_{\Delta} = 10$  kHz. The magnitudes are normalized with relation to the fundamental amplitude in each case. (a) For proposed  $CSL_{4l}$ . (b) For proposed  $CSL_{4l}^{nop}$ . (c) For conventional  $CHB_{2h}$ . (d) For conventional  $CHB_{2h}^{nop}$ .

TABLE VII  
VOLTAGE  $v_l$  THD OBTAINED IN WITH EXPERIMENTAL DATA, WITH FIXED  
CARRIERS FREQUENCY  $f_{\Delta} = 10$  KHZ

	$CSL_{4l}$	$CSL_{4l}^{nop}$	$CHB_{2h}$	$CHB_{2h}^{nop}$
$v_l$ THD (%)	9.80	14.42	16.20	21.76

followed by  $CSL_{4l}^{nop}$  and conventional  $CHB_{2h}$ , which had similar spectrum profiles. The greatest magnitudes were observed in conventional  $CHB_{2h}^{nop}$ . Table VII shows the THD calculated for each case, and confirm numerically what has been observed graphically in Fig. 8.

Even though the nonoptimal calculation of the turns ratio produced less levels, it is a useful resource that allows us to adapt the topologies to be utilized when transformers with ideal turns ratios are not available, as was the case shown in Fig. 7(a). Moreover, they allow the design of an LS-PWM with redundant states. As shown in the simulation results, these states can be properly used to reduce the switching frequency of the converter, especially in legs with higher current rating. This enables the reduction of switching losses and stress, keeping good performance with a number of voltage levels still greater than the conventional configuration.

### VIII. GENERAL ANALYSIS

By analyzing simulation results, it could be verified that for the same number of legs ( $N_{leg} = 6$ ), proposed configurations provided more levels in the output voltage than the conventional CHB, such that their harmonic spectrum had lower magnitudes (see Fig. 5), granting them lower voltage THD. As seen in Table II, proposed configuration  $CSL_{6l}$  provided the greatest number of levels ( $N_{lv1} = 63$ ) and the lowest THD, followed by proposed configuration  $MCSL_{2m}$  ( $N_{lv1} = 49$ ). Conventional  $CHB_{3h}$  provided the minor number of levels ( $N_{lv1} = 27$ ) and the highest THD.

It could also be verified from the data in Table III that proposed configurations could provide both lower semiconductor losses and voltage THD (THD = 3.2%) than the conventional  $CHB_{3h}$  (THD = 5%), showing that proposed configurations could provide better voltage quality without prejudice to the power losses. Particularly, for configuration  $CSL_{6l}^{nop}$ , it has been observed an intermediate number of levels ( $N_{lv1} = 49$ ), lower than the optimal case ( $CSL_{6l}$ ). Nevertheless,  $CSL_{6l}^{nop}$  had the lowest semiconductor losses among all configurations, showing that nonoptimal turns ratio can be used to decrease not only the number of levels, but also the switching frequency by properly utilizing the switches states redundancies in the LS-PWM. Moreover, in general proposed configurations had lower current rating in higher switching frequency IGBTs, and lower switching frequency on high current rating ones, as verified by comparing the data on Tables IV and V, yielding possibly cheaper devices.

By the data provided in Table VI, it has been shown that even though proposed configurations required additional transformers, they are of lower power rating compared to the ones of conventional configuration. Particularly, CSL generalization had the transformers with lowest power ratings. Hence, even though the utilization of more transformers means greater weight and more space, in terms of cost they would not be that much expensive in proposed configurations because they are of lower power rating. Then, the tradeoff of more but individually cheaper transformers for better voltage quality with less semiconductors losses is attractive.

In the experimental results, it could be verified the feasibility and the better performance of proposed CSL configuration, already indicated by the simulation results. Cases with optimal and nonoptimal turns ratios have been analyzed, and what was stated based on simulations was confirmed in the experiments.

Moreover, Table VIII shows some general data on proposed (CSL and MCSL) and conventional (CHB and CHfB) configurations. In the table,  $k$  is the number of switches employed,  $n$  is any integer such that  $n \geq 1$ ,  $N_{lv1}$  is the number of levels produced, and  $N_{trf}$  the number of transformers utilized. It can

TABLE VIII  
GENERAL DATA ON PROPOSED AND CONVENTIONAL CONFIGURATIONS, WHERE  $k$  IS THE NUMBER OF SWITCHES,  $n$  IS ANY INTEGER SUCH THAT  $n \geq 1$ ,  $N_{lv1}$  THE NUMBER OF LEVELS PRODUCED, AND  $N_{trf}$  THE NUMBER OF TRANSFORMERS

	Proposed		Conventional		
	CSL	MCSL	CHB	CHfB	
$k$	$k \geq 4 + 2n$	$k \geq 6n$	$k \geq 4n$	$k \geq 2n$	
$N_{lv1}$	$2^{k/2} - 1$	$7^{k/6}$	$3^{k/4}$	$2^{k/2}$	
$N_{trf}$	$k/2 - 1$	$k/3$	$k/4$	$k/2$	
$k = 8$	$N_{lv1}/k$	1.875	–	1.125	2
	$N_{trf}$	3	–	2	4
$k = 12$	$N_{lv1}/k$	5.250	4.083	2.250	5.333
	$N_{trf}$	5	4	3	6

be verified that for  $k = 8$  switches, which is the case of experimental configurations, proposed CSL generalization has almost twice the levels-per-switch ( $N_{lv1}/k$ ) than the conventional CHB, and is very close to the CHfB. For  $k = 12$  switches, which is the case of simulated configurations, the levels-per-switch of proposed CSL is over twice than that of the conventional CHB, and even closer to that of CHfB. Proposed MCSL generalization also present high levels-per-switch ratio, almost twice than the conventional CHB.

Considering that proposed CSL generalization provides almost the same levels-per-switch ratio than conventional CHfB for increasing values of  $k$ , and that it utilizes one less transformer and does not need dc-link midpoint connection, it becomes a very good alternative. However, proposed CSL utilizes considerably more transformers than conventional CHB (almost twice for  $k = 12$ ). Hence, if an economy in the number of transformers is desired, proposed MCSL generalization rises as an interesting choice. It still utilizes more transformers than conventional CHB, but has considerably higher levels-per-switch ratio and uses less transformers than proposed CSL and conventional CHfB. As a general rule, the cost for higher levels-per-switch is more transformers, and the designer must reason about this implication. Nevertheless, one must remind that more transformers do not mean necessarily a more expensive device, since transformers are of different current and power ratings in each case.

## IX. CONCLUSION

In this paper, we have proposed a new single-phase shared-leg multilevel converter utilizing two injection transformers connected to three two-level IGBT legs, along with two generalizations for devices with  $N_{leg}$  legs. This converter and its generalizations have been proposed as alternatives to the conventional CHB and the CHfB, providing higher levels-per-switch ratio. It has been shown that proposed configurations can provide practically equivalent levels-per-switch than the CHfB, with less transformers and without requiring connection to the dc-link midpoint. Moreover, simulation and experimental results have been provided to show that proposed configurations have better performance than the conventional CHB, with considerably

more levels-per-switch and lower semiconductor losses, at the cost of requiring more transformers. Nevertheless, we have verified that the additional transformers of proposed configurations are of lower current and power rating than those of conventional CHB, which implies that they are not necessarily more expensive, making proposed configurations a viable alternative with improved voltage waveform quality.

## REFERENCES

- [1] R. A. Krishna and L. P. Suresh, "A brief review on multi level inverter topologies," in *Proc. 2016 Int. Conf. Circuit, Power Comput. Technol.*, Mar. 2016, pp. 1–6.
- [2] F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," in *Proc. 2010 Int. Power Electron. Conf.*, Jun. 2010, pp. 492–501.
- [3] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep. 1981.
- [4] N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," in *Proc. 22nd Annu. IEEE Power Electron. Spec. Conf.*, Jun. 1991, pp. 96–103.
- [5] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proc. 23rd Annu. IEEE Power Electron. Spec. Conf.*, vol. 1, Jun. 1992, pp. 397–403.
- [6] F. Z. Peng, J.-S. Lai, J. W. McKeever, and J. VanCoeveering, "A multilevel voltage-source inverter with separate DC sources for static VAR generation," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130–1138, Sep. 1996.
- [7] P. W. Hammond, "A new approach to enhance power quality for medium voltage AC drives," *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202–208, Jan. 1997.
- [8] H. Deng, R. Oruganti, and D. Srinivasan, "Modeling and control of single-phase ups inverters: A survey," in *Proc. 2005 Int. Conf. Power Electron. Drives Syst.*, vol. 2, Nov. 2005, pp. 848–853.
- [9] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "Power inverter topologies for photovoltaic modules—A review," in *Proc. 37th IAS Annu. Meeting Conf. Rec. IEEE Ind. Appl. Conf.*, vol. 2, Oct. 2002, pp. 782–788.
- [10] O. Alonso, P. Sanchis, E. Gubia, and L. Marroyo, "Cascaded H-bridge multilevel converter for grid connected photovoltaic generators with independent maximum power point tracking of each solar array," in *Proc. 2003 IEEE 34th Annu. Power Electron. Spec. Conf.*, vol. 2, Jun. 2003, pp. 731–735.
- [11] M. Swamy and T. Kume, "Present state and a futuristic vision of motor drive technology," in *Proc. 11th Int. Conf. Optim. Elect. Electron. Equip.*, May 2008, pp. XLV–LVI.
- [12] J. Praveen, B. P. Muni, S. Venkateshwarlu, and H. V. Makthal, "Review of dynamic voltage restorer for power quality improvement," in *Proc. 30th Annu. Conf. IEEE Ind. Electron. Soc.*, vol. 1, Nov. 2004, pp. 749–754.
- [13] K. Steela and B. S. Rajpurohit, "A survey on active power filters control strategies," in *Proc. 2014 IEEE 6th India Int. Conf. Power Electron.*, Dec 2014, pp. 1–6.
- [14] M. El-Habrouk, M. K. Darwish, and P. Mehta, "A survey of active filters and reactive power compensation techniques," in *Proc. 8th Int. Conf. Power Electron. Variable Speed Drives (IEE Conf. Publ. No. 475)*, 2000, pp. 7–12.
- [15] D. M. Divan, "A new topology for single phase UPS systems," in *Proc. Conf. Rec. IEEE Ind. Appl. Soc. Annu. Meeting*, vol. 1, Oct. 1989, pp. 931–936.
- [16] S.-J. Park, H.-W. Park, J.-I. Bae, M.-H. Lee, and C.-U Kim, "Development of a high performance single-phase voltage regulator composed of 3 arms bridge," in *Proc. IEEE Int. Symp. Ind. Electron.*, vol. 2, 1999, pp. 700–705.
- [17] W. R. N. Santos, E. M. Fernandes, E. R. C. da Silva, C. B. Jacobina, A. C. Oliveira, and P. M. Santos, "New single-phase universal active power filter topology with ups features and reduced number of components," in *Proc. 2015 IEEE 13th Brazilian Power Electron. Conf. 1st Southern Power Electron. Conf.*, Nov. 2015, pp. 1–8.
- [18] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel inverters for electric vehicle applications," in *Proc. Power Electron. Transp. (Cat. No. 98TH8349)*, Oct. 1998, pp. 79–84.
- [19] A. Marquez *et al.*, "Variable-angle phase-shifted PWM for multilevel three-cell cascaded H-bridge converters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 5, pp. 3619–3628, May 2017.

- [20] A. Ajami, A. Farakhor, and H. Ardi, "Minimisations of total harmonic distortion in cascaded transformers multilevel inverter by modifying turn ratios of the transformers and input voltage regulation," *IET Power Electron.*, vol. 7, no. 11, pp. 2687–2694, 2014.
- [21] J. Muoz *et al.*, "A 27-level asymmetric multilevel converter for harmonic currents compensation," in *Proc. 2017 11th IEEE Int. Conf. Compat. Power Electron. Power Eng.*, Apr. 2017, pp. 538–543.
- [22] F.-s. Kang, S.-J. Park, C.-U Kim, and S. E. Cho, "Half-bridge and full-bridge cell based multilevel PWM inverter with cascaded transformers," in *Proc. 2004 47th Midwest Symp. Circuits Syst.*, vol. 2, Jul. 2004, pp. II-273–II-276.
- [23] M. R. Banaei, H. Khounjahan, and E. Salary, "Single-source cascaded transformers multilevel inverter with reduced number of switches," *IET Power Electron.*, vol. 5, no. 9, pp. 1748–1753, Nov. 2012.
- [24] H. K. Jahan, M. R. Banaei, and S. T. Mobaraki, "Combined H-bridge cells cascaded transformers multilevel inverter," in *Proc. 5th Annu. Int. Power Electron., Drive Syst. Technol. Conf.*, Feb. 2014, pp. 524–528.
- [25] G. A. d. A. Carlos and C. B. Jacobina, "Series compensator based on cascaded transformers coupled with three-phase bridge converters," *IEEE Trans. Ind. Appl.*, vol. 53, no. 2, pp. 1271–1279, Mar. 2017.
- [26] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters—An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep. 2014.
- [27] K. M. Kotb, A. E. W. Hassan, and E. M. Rashad, "Simplified sinusoidal pulse width modulation for cascaded half-bridge multilevel inverter," in *Proc. 2016 18th Int. Middle East Power Syst. Conf.*, 2016, pp. 907–913.



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