New Modulated Carrier Controlled PFC Boost Converter

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***Abstract*—A new modulated carrier control (MCC) method is proposed in this paper for a power factor correction (PFC) boost converter, which provides high power factor (PF) and low total harmonic distortion (THD) in wide input voltage and load range. The proposed MCC method employs a zero current duration (ZCD) demodulator that detects ZCD in each switching cycle to estimate current conduction duration of the boost inductor. Using the estimated signal of the ZCD demodulator, the proposed controller generates a compensated duty signal with a PFC converter to properly operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). Unlike the conventional MCC PFC converter where the line current is distorted in DCM resulting in poor PF and high THD, the proposed MCC method can provide higher PFC performance regardless of CCM and DCM while maintaining the simple control loop of conventional MCC control method that does not require inner current loop and using relatively small inductance. In this paper, the operational principle of the proposed method has been discussed. To verify the proposed method, it has been tested on a 400-W PFC boost converter.**

***Index Terms*—AC–DC power converters, boost converter, modulated carrier control (MCC), nonlinear carrier (NLC) control, power conversion, power factor correction (PFC).**

I. Introduction

As POWER grid harmonic pollution has attracted growing attention, standards such as IEC/EN61000-3-2 and IEC/EN61000-3-12 regulating the line current harmonic contents have become more stringent. Even a power factor (PF) have been included into the regulation conditions as well, such as 80 Plus developed by Ecos Consulting. These conditions have resulted in power factor correction (PFC) to be indispensable for offline power supplies and have increased the necessity of developing a high-performance PFC. For the low- to high-power applications, PFC converters with various control methods have been researched and developed.

For the low to middle power range, discontinuous conduction mode (DCM) or critical conduction mode (CRM) PFC converters have been studied and widely employed [1]–[5].

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For the middle to high power range, continuous conduction mode (CCM) PFC converters usually have been employed, in which the root mean square (rms) current is smaller than one of the CRM or DCM PFC converters using relatively low inductance. This smaller rms current results in low current ripple stress on devices, facilitating physically small size of an input filter [5]–[15]. However, the control methods generally used for the CCM PFC converter are more complicated; for example, the average current mode boost PFC converter requires two control loops of the outer voltage error amplifier and inner current error amplifier, which should sense an output voltage, a sinusoidal shape, and amplitude of an ac input line, and an inductor current to regulate the input current. Generally, the CCM PFC offers high performance when it operates in CCM. But, when it enters DCM operation as the load decreases or the line input increases, the input current can be distorted resulting in low PF and high THD. This may lead to employing physically large inductance considering tolerance of inductance in order to guarantee CCM operation under as much of load condition. Alternatively, it can result in the need to relinquish good THD at a lower than certain load condition to avoid using large inductance. This obstacle of the operation mode may be a problem, which has been discussed in [9]–[11]. Accordingly, new control methods have been actively researched to overcome this problem and obtain high performance in the PFC operation regardless of the operation modes [12]–[15].

Among various control methods for CCM PFC converters, the modulated carrier control (MCC) method (also referred to as the nonlinear carrier (NLC) control method) has attracted considerable attention due to its simple control loop that does not require sensing line input voltage and current loop; hence, it provides fast dynamic response compared to the conventional CCM PFC boost converter [16]–[27]. Fig. 1 illustrates THD comparison simulation results at 400 and 200 W of the load condition in the conventional MCC PFC boost converter introduced in [16]. At the simulation, key parameters are 220 Vrms/60 Hz of ac input line, 80 kHz of the switching frequency, and 520 μH of the boost inductance.

Fig. 1 (a) shows that the conventional MCC boost converter operates in the CCM operation during the entire cycle of the ac line and results in low THD of 2.4%. In contrast, if it partially enters the DCM operation, its PFC performance deteriorates to THD of 13.7%, as shown in Fig. 1 (b), because its control method is also based on the CCM operation equation. The distortion of the conventional MCC in DCM has been researched in [19] and [20].

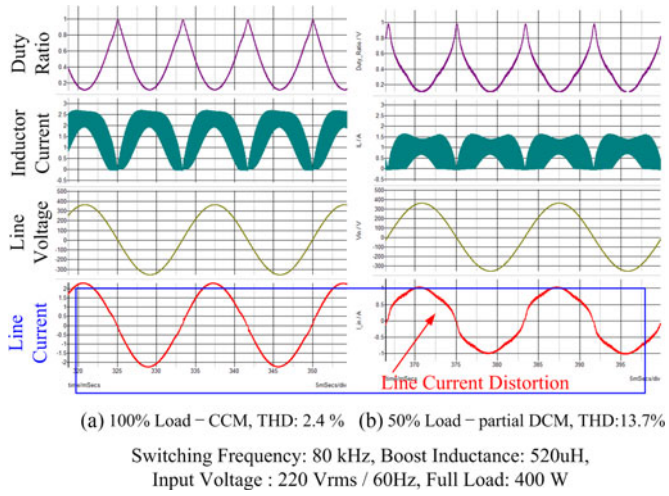

Fig. 1. Simulation results THD comparison depending on load variation at the conventional MCC PFC boost converter. (a) 100% Load—CCM, THD: 2.4% (b) 50% Load—Partial DCM, THD:13.7%

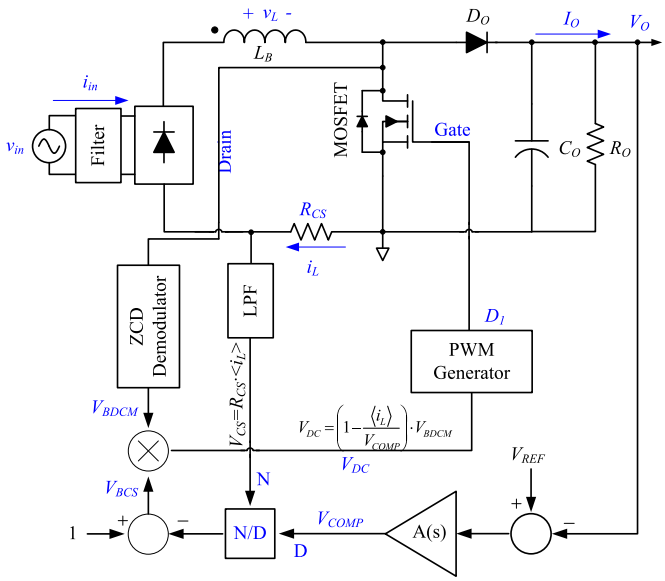

Fig. 2. Block diagram of the proposed MCC method.

To overcome the problems of the operation mode while maintaining the advantages of the conventional MCC method, this paper proposes new MCC method for PFC. The proposed MCC method employs a zero current duration (ZCD) demodulator that detects a ZCD in each switching cycle to estimate the current conduction duration of the boost inductor. The ZCD demodulator converts the measured duration to a compensation signal. With the compensation signal from the ZCD demodulator, a new controller generates appropriate duty cycles in either CCM or DCM operation. Therefore, the proposed MCC method no longer requires relatively large boost inductance compared to the conventional MCC boost converter and thus can offer high flexibility in designing a boost inductance and high PFC performance of low THD and high PF in a wide input voltage and load range. Additionally, the proposed control method uses a resistive and capacitive (RC) low-pass filter to detect average inductor current for better noise immunity, as suggested in [16].

This paper is organized as follows. Section II-A describes the basic operating principle of the proposed MCC method whereas Section II-B explains the detailed operation of the added circuits compared to the conventional MCC. Section III describes linear analysis of the proposed method including RC low-pass filter circuits and an output voltage error amplifier. Section IV presents the experimental results that validate the proposed MCC method implemented in a 400-W PFC boost converter. Finally, Section V concludes this paper.

II. Description of The Proposed Method

Fig. 2 shows a boost converter and the proposed control block diagram comprised of a ZCD demodulator, an inductor current sensing resistor with an RC low-pass filter, an output voltage error amplifier, a new control circuit revised from [16] and [21], and a pulse width modulation (PWM) generator. ZCD demodulator detects the duration of zero inductor current in each switching cycle at the DCM operation and converts the duration to a compensation signal V_{BDCM}. The control circuit generates a duty control signal $\mathrm{V_{DC}}$ using V_{BDCM} from the ZCD demodulator and an average inductor current $< i_L >$ and the output signal of output voltage error amplifier V_{COMP}. At the PWM generator, $\mathrm{V_{DC}}$ is compared with a saw-tooth waveform and generates an appropriate ratio duty D_1 able to cover CCM and DCM operations.

A. Operating Principle

The fundamental operating principle of the conventional MCC was introduced in [21]–[25]. Based on these accounts, the operating principle of the proposed MCC can be described as follows.

Basically, the PFC controller maintains an input current i_{in} in proportion with following an ac input voltage v_{in} while keeping an output voltage V_o as a specified reference V_{REF}. With this assumption, an input impedance of the PFC converter can be expressed as

$$R_e = \frac{v_{\mathrm{in}}}{i_{\mathrm{in}}} \tag{1}$$

where R_e is an emulated resistance.

The input current i_{in} can be expressed with a function of the average current of the boost inductor $< i_L >$and can be expressed as

$$i_{\mathrm{in}} = \langle i_L \rangle = \frac{1}{T_s}\int_0^{T_s} i_L(t)dt \tag{2}$$

where T_S is the switching period of the controller and i_L is the instantaneous inductor current, which can be detected through a sensing resistor R_{CS}.

Meanwhile, assuming negligible power losses between the input and output, and slowly varying v_{in}, a voltage conversion ratio of the boost converter can be obtained as (3) by applying

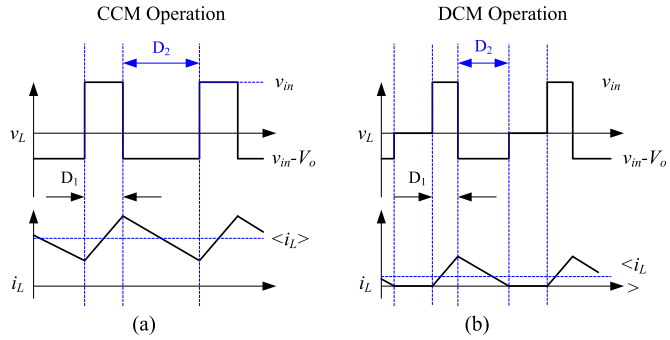

Fig. 3. Operating waveforms of the boost converter in CCM and DCM. (a) CCM operation. (b) DCM operation.

the volt-second balance as shown in Fig. 3

$$v_{\text{in}} \cdot D_1 = (V_o - v_{\text{in}}) \cdot D_2$$

$$v_{\text{in}} = \frac{D_2}{D_1 + D_2} V_o \tag{3}$$

where D_1 is the duty ratio of the MOSFET and D_2 is the time interval ratio of the discharging inductor current.

Substituting (1) and (2) into (3), a relationship between the output voltage V_o and the average inductor current $< i_L >$can be rearranged as

$$R_e \cdot \langle i_L \rangle = \frac{D_2}{D_1 + D_2} \cdot V_o. \tag{4}$$

Then, the control equation can be expressed as

$$\left(1 - \frac{\langle i_L \rangle}{V_{\text{COMP}}}\right) \cdot (D_1 + D_2) = D_1 \tag{5}$$

where V_{COMP} is equal to V_O / R_e and represents the control signal from the output voltage error amplifier.

As previously mentioned, the average inductor current gradually changes in proportion to the ac input voltage in a line frequency and the other parameters R_e and V_o are constant. Accordingly, if the amount of time of D_1 and D_2 is measured properly and can be input to (5), the appropriate duty ratio D_1 can be naturally generated by the sensed average inductor current $< i_L >$, which makes sinusoidal input current waveforms in proportion to the input voltage regardless of the CCM and DCM operation.

B. ZCD Demodulator

To solve the left term in (5), the control circuit requires information on amounts of time of D_1 and D_2. Because of different unit between the duty and others, the ZCD demodulator detects the amounts of time of D_1 and D_2 and converts them to a compensation voltage signal V_{BDCM}. In the mean time, each D_1 of left and right side in (5) becomes different since the left side D_1 is measured by the ZCD demodulator. And the right D_1 will be a gate signal. Fig. 4 shows the ZCD demodulator and operating waveforms. The ZCD demodulator simply consists of a detecting capacitor C_D, current-to-voltage converter comprising a current source I_B and a Zener diode Z_D, rising edge triggered D-FF (flip flop) and RC low-pass filter.

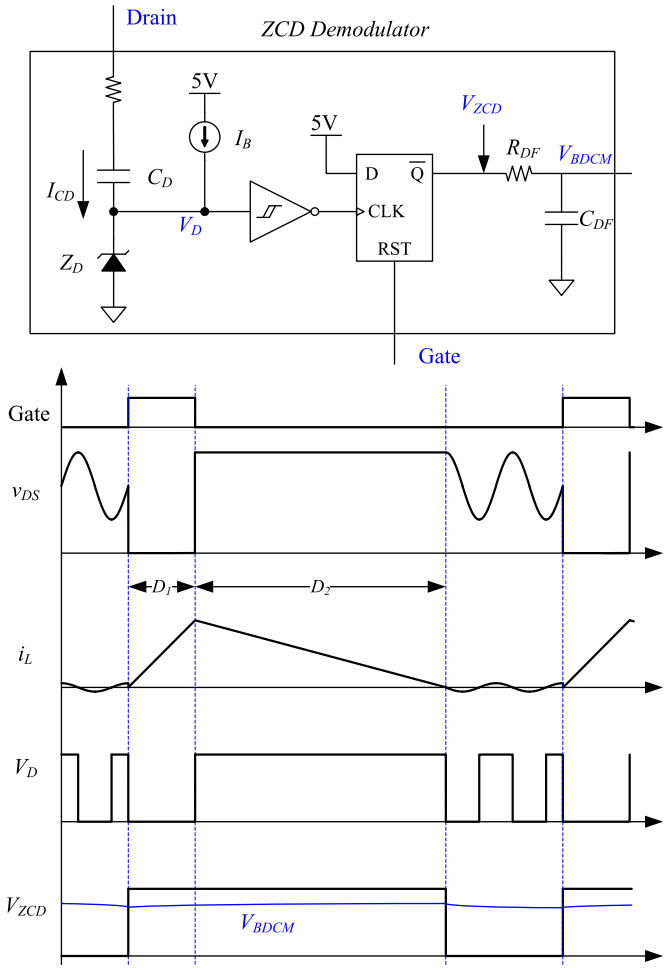

Fig. 4. ZCD demodulator circuit and operating waveforms.

The following steps are the procedures of the ZCD demodulator circuit operation.

1) During a high gate signal, the D-FF stays in the reset state so that the Q-bar output remains high regardless of the inverted V_D signal input to CLK of D-FF.
2) After a gate signal switches from high to low, D-FF is enabled and a drain-to-source voltage v_{DS} increases up to V_o by the MOSFET turn-off as well. Accordingly, I_{CD} flowing through C_D increases as v_{ds} increases and makes a detecting voltage V_D, which is clamped by Z_D. And V_D is input to CLK of the D-FF through the inverter logic. However, the Q-bar output of D-FF still remains high.
3) While the MOSFET is turned OFF, an inductor current is gradually discharged. As soon as it is fully discharged, resonance is initiated by the boost inductor and parasitic capacitance of MOSFET. This causes fluctuation of v_{ds} and C_D is repeatedly charged and discharged by I_{CD}. During the discharging, when I_{CD} is lower than $' - I_B,'$ V_D is changed to zero. At the transition of V_D, a rising edge signal occurs at CLK of D-FF. Then, the Q-bar output of D-FF is changed but is kept low until the next high gate signal resets the D-FF. The pulse V_{ZCD} generated from D-FF is flattened by the RC-filter R_{DF} and C_{DF}.

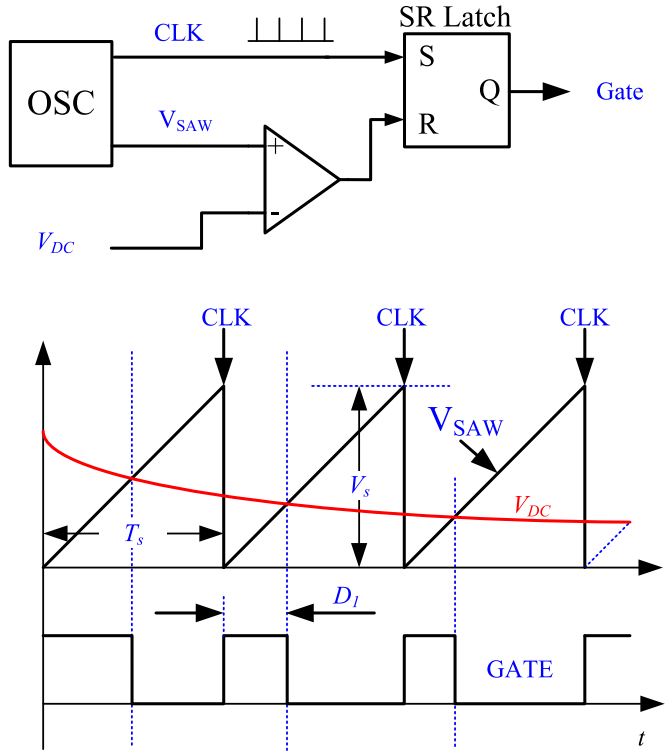

Fig. 5. PWM generator and operating waveforms.

Finally, V_{ZCD} becomes a compensation signal V_{BDCM} in the proposed control method. At CCM operation, the Q-bar of D-FF is constantly high so that V_{BDCM} is a maximum output voltage of D-FF. On the other hand, as discontinuous conduction duration increases, V_{BDCM} gradually decreases from the maximum output voltage.

C. PWM Generator

Finally, in this method, a duty ratio D_1 to satisfy (5) can be simply obtained by comparing a duty control signal V_{DC} with a periodic saw-tooth waveform having constant slope as follows:

$$V_{\mathrm{DC}} = \left(1 - \frac{\langle i_L \rangle}{V_{\mathrm{COMP}}}\right) \cdot V_{\mathrm{BDCM}} = V_s \cdot \left(\frac{t_{\mathrm{on}}}{T_s}\right) = D_1 \quad (6)$$

where V_s is the peak voltage of the saw-tooth waveform, and t_{on} is the MOSFET turn-on time.

In addition, (6) can be realized as a PWM circuit as can be seen in Fig. 5.

III. Current Distortion Analysis in DCM

The conventional MCC method is derived based on the assumption that the boost converter operates in CCM. As mentioned in Section I, a line input current can be distorted when the conventional MCC PFC boost converter operates in DCM. In this section, a condition for operation in DCM is confirmed and current distortion in DCM is analyzed.

The control equation of conventional MCC can be also derived from (4) as

$$R_e \cdot \langle i_L \rangle = (1 - D_1) \cdot V_o. \quad (7)$$

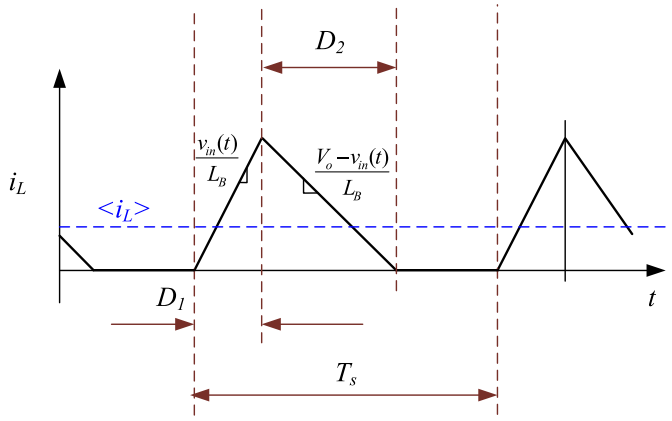

Fig. 6. Inductor current waveform in DCM operation of the boost converter.

The average inductor current $\langle i_L \rangle$ is the amount of two average currents flowing through a MOSFET and output diode. Accordingly, (7) can be expressed with the average MOSFET current $\langle i_S \rangle$ as follows:

$$R_e \cdot \langle i_S \rangle = D_1 (1 - D_1) \cdot V_o. \quad (8)$$

Fig. 6 shows an inductor current waveform of the boost converter operating in DCM. Substituting (8) with $\langle i_S \rangle$ derived from Fig. 6 gives a relationship between a line input voltage $v_{\mathrm{in}}(t)$ and the output voltage V_o as follows:

$$\langle i_S \rangle = \frac{|v_{\mathrm{in}}(t)|}{2 \cdot L_B} {D_1}^2 T_s = D_1 (1 - D_1) \cdot \frac{V_o}{R_e} \quad (9)$$

where $v_{\mathrm{in}}(t)$ is the line input voltage $V_{\mathrm{inpk}} \sin(\omega t)$.

And a duty ratio D_1 can be derived using (9) as

$$D_1 = \frac{1}{1 + \frac{R_e}{R_o} \frac{|v_{\mathrm{in}}(t)|}{K \cdot V_o}} \quad (10)$$

where R_o is V_o / I_o, and K is $2 L_B f_s / R_o$ that is the load parameter commonly used in the DCM analysis.

When the boost converter operates in DCM, D_1 meets the following condition:

$$D_1 < \left(1 - \frac{|v_{\mathrm{in}}(t)|}{V_o}\right). \quad (11)$$

On the other hand, D_1 is equal or higher than the right term in (11) while the boost converter operates in CCM.

Substituting (10) into (11) gives DCM operating condition as

$$K < \left(1 - \frac{|v_{\mathrm{in}}(t)|}{V_o}\right) \cdot \frac{v_{\mathrm{inpk}}}{2 \cdot V_o}. \quad (12)$$

In addition, during DCM operation of the conventional MCC, (7) can be replaced to the expression for the input current using (10) as follows:

$$i_{\mathrm{in}} = \langle i_L \rangle = \frac{|v_{\mathrm{in}}(t)|}{K \cdot R_o} \frac{V_o}{V_o - |v_{\mathrm{in}}(t)|} {D_1}^2. \quad (13)$$

Fig. 7 shows a waveform of normalized line input current distortion calculated based on (13). The electrical specifications and parameters introduced in Fig. 1 are equally applied to this simulation. Among the normalized line input current waveforms, "SIN_REF" is a sinusoidal waveform for a reference, K

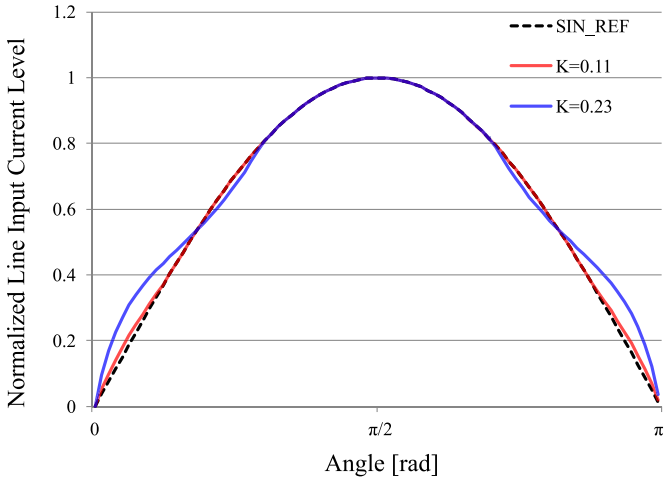

Fig. 7. Normalized line input current depending on the load parameter *K*.

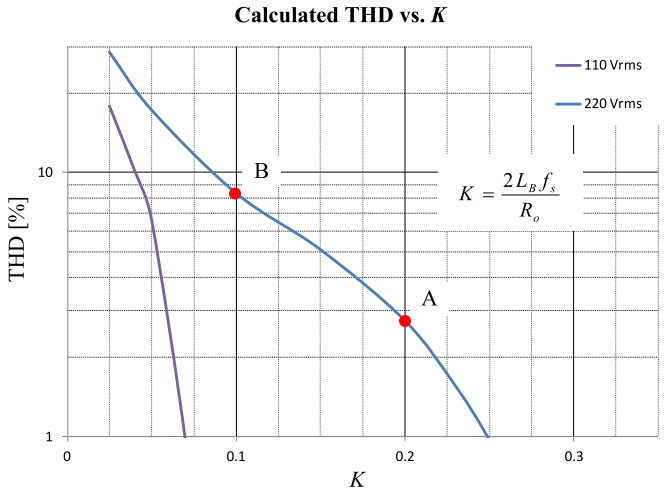

Fig. 8. THD of the line input current versus the load parameter *K*.

of 0.11 is a calculated result at full-load condition whose THD is 1.55%, and *K* of 0.23 is a result at the load condition of 200 W whose THD is 7.2%.

Fig. 8 shows THD of the line input current depending on the load parameter *K*. As a result, THD variation can be estimated depending on a load, frequency, and inductance. Assume that THD at "A" point is at full-load condition. If the load is reduced to the half, THD increases up to 8% depicted as "B" point. If THD at "B" point cannot meet a requirement, then inductance should be double. This is one of the disadvantages of the conventional MCC where the boost inductance should be designed big enough, considering a line input voltage and load condition.

Therefore, the proposed MCC method introduced in this paper is expected to provide high PFC performance regardless of the line input voltage and load condition unlike this conventional MCC method.

IV. Linear Analysis of the Proposed Control Method

A linear analysis of the system is carried out in this section for the design of the control loop of the proposed MCC boost PFC converter. The method of modeling used with the conventional MCC method has been explained in [24], [28], and [29] on which the approach of the proposed method is based.

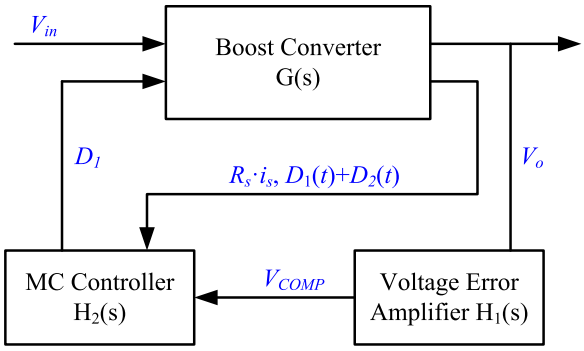

Fig. 9. Linear model of the proposed MCC PFC boost converter.

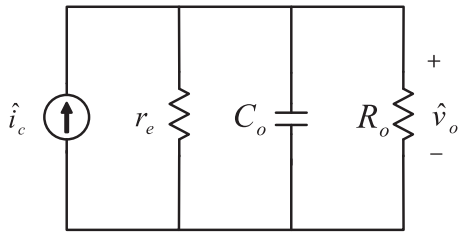

Fig. 10. Small signal of the boost converter.

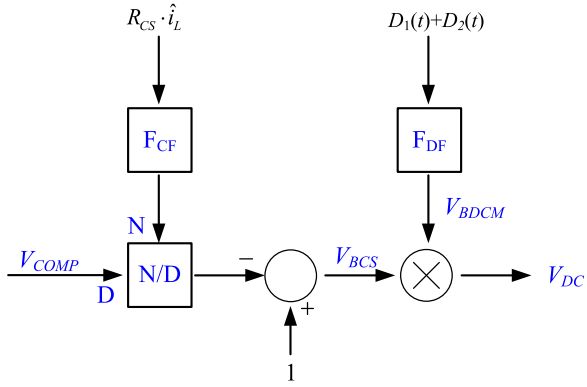

Fig. 11. Modulated carrier controller.

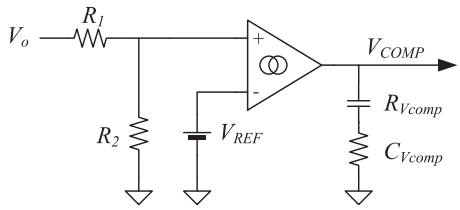

Fig. 12. Output voltage error amplifier.

Fig. 9 shows a linear model of the proposed MCC PFC boost converter. A loop gain can be obtained by the product as

$$T(s) = G(s) \cdot H_1(s) \cdot H_2(s) \tag{14}$$

where $G(s)$ is the transfer function of the boost converter, and $H_1(s)$ and $H_2(s)$ are the transfer functions of the output voltage

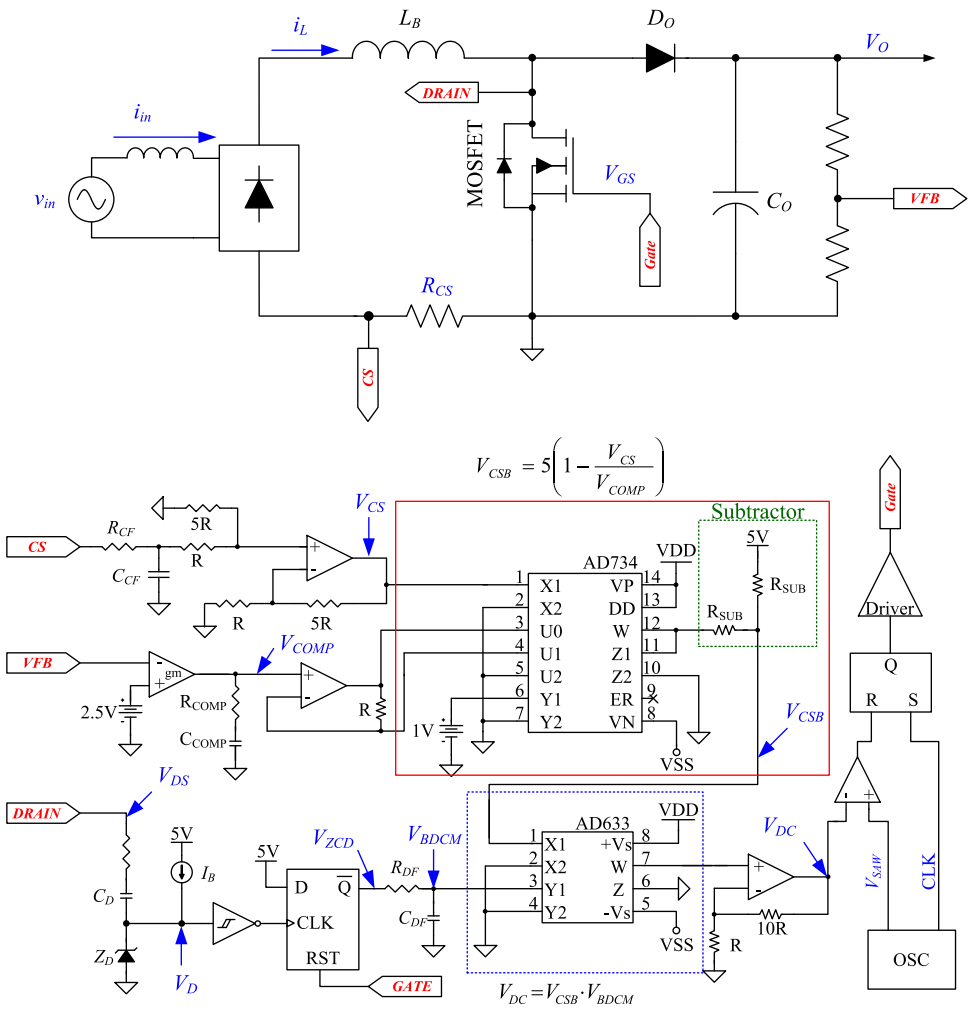

Fig. 13. Feasible implementation circuit schematic of the proposed control method.

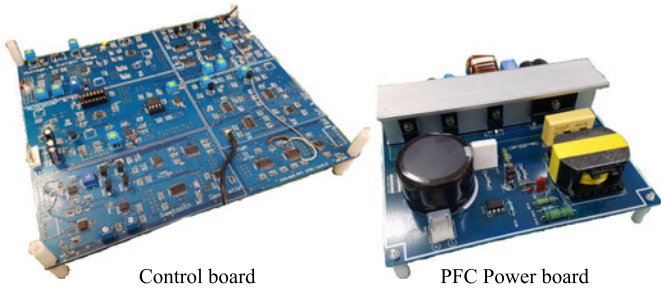

Fig. 14. Photographs of the implemented control board and PFC power board.

error amplifier including the voltage divide resistors and the proposed MC control part, respectively.

Fig. 10 shows a small-signal model of the boost converter, where r_e is equal to the load resistance R_o because an application of resistive load is assumed in this paper. Therefore, the transfer function can be derived as

$$G(s) = \frac{\hat{v}_o}{\hat{i}_c} = \frac{1/2 \cdot R_o}{1 + 1/2sC_o \cdot R_o} \tag{15}$$

where $\hat{i}_c$ is the output average current.

TABLE I
ELECTRICAL SPECIFICATIONS AND KEY PARAMETERS OF THE BOOST CONVERTER

Parameter	Values
Input voltage	85–265 Vrms
Line frequency	60 Hz
Output voltage	380 V_{dc}
Output power	400 W
Switching frequency	80 kHz
Boost inductance	520 μH
Current sensing filter	R_{CF}: 2.2 kΩ, C_{CF}: 47 nF
ZCD filter	R_{DF}: 1.1 kΩ, C_{DF}: 47 nF

In addition, the relationship between the inductor current $\hat{i}_L$ and $\hat{i}_c$ is

$$\hat{i}_L = \frac{\hat{p}_{\text{in}}}{V_{\text{in}}} = \frac{\hat{i}_c \cdot V_o}{V_{\text{in}}}. \tag{16}$$

By substituting (16) into (15), the control to output transfer function of the input current and output voltage shown in Fig. 11 is as follows:

$$\frac{\hat{v}_o}{\hat{i}_L} = \frac{V_{\text{in}}}{V_o} \cdot \frac{1/2 \cdot R_o}{1 + 1/2sC_o \cdot R_o}. \tag{17}$$

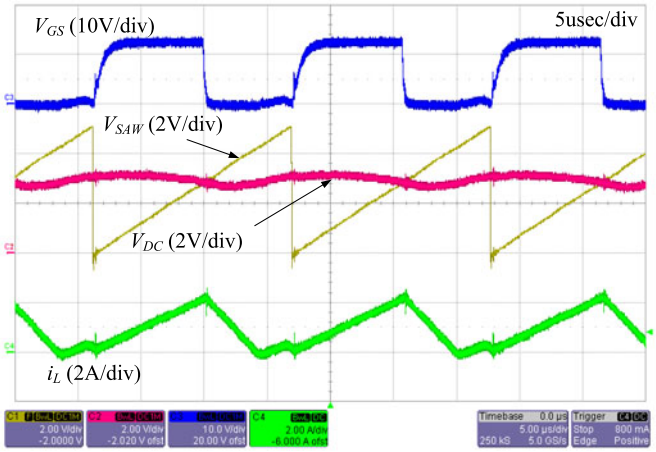

Fig. 15. Experimental waveforms of the PWM generator.

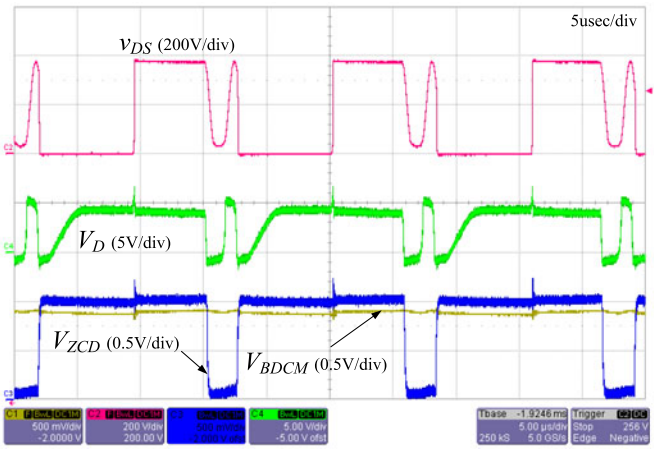

Fig. 16. Experimental waveforms of the ZCD demodulator.

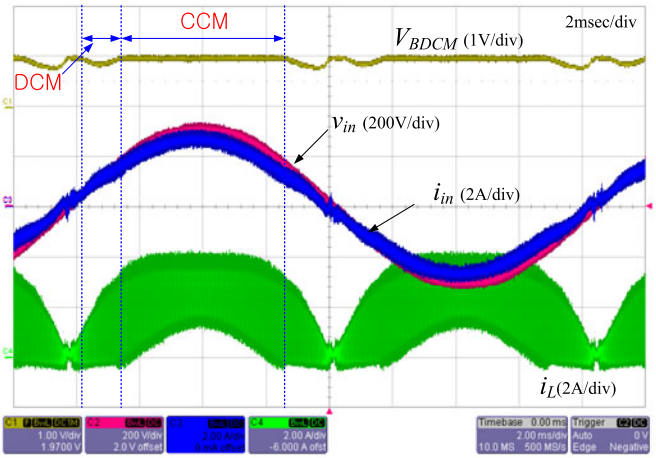

Fig. 17. Experimental waveforms at 220 Vrms and 100% load.

The control equation of MCC discussed previously in (5) of Section II can be rearranged as

$$R_{\rm CS}\cdot i_L\cdot F_{\rm CF}=\frac{V_{\rm COMP}}{\left(1+\frac{D_1}{D_2}\right)F_{\rm DF}}$$
$$F_{\rm CF}=\frac{1}{sR_{\rm CF}C_{\rm CF}},\ F_{\rm DF}=\frac{1}{sR_{\rm DF}C_{\rm DF}} \tag{18}$$

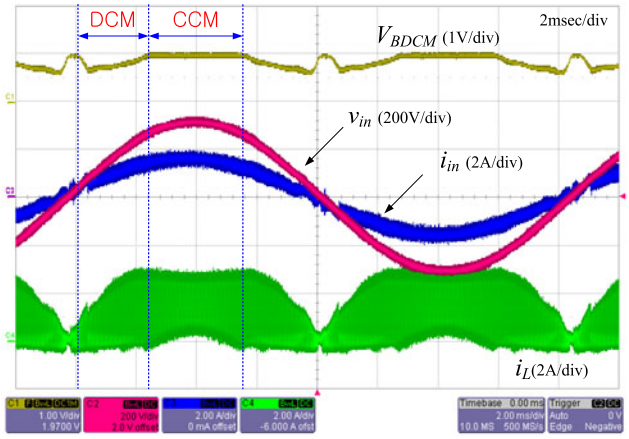

Fig. 18. Experimental waveforms at 220 Vrms and 50% load.

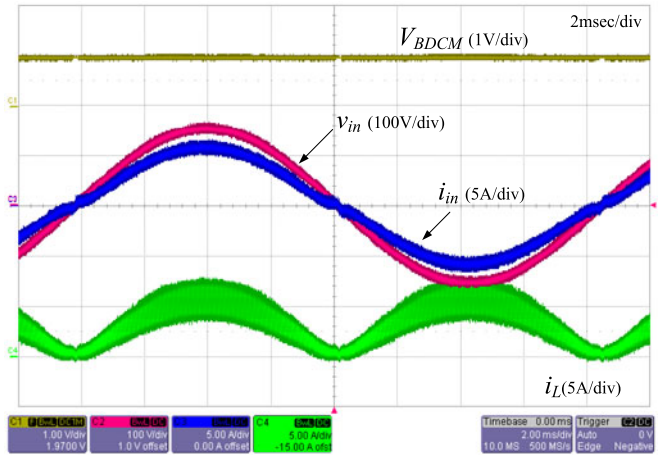

Fig. 19. Experimental waveforms at 110 Vrms and 100% load.

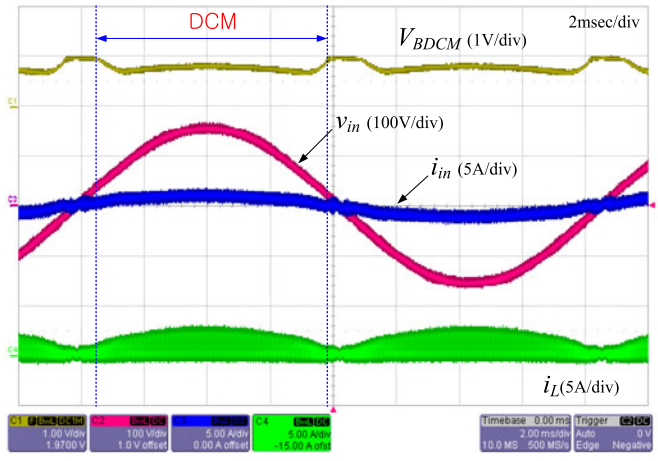

Fig. 20. Experimental waveforms at 110 Vrms and 20% load.

where $F_{\rm CF}$ and $F_{\rm DF}$ are the gain of current sensing filter and the filter for the ZCD pulse signal $V_{\rm ZCD}$ shown in Fig. 4.

By applying perturbation in (18), a control to output transfer function can be derived as

$$H_2=\frac{\hat{i}_L}{\hat{v}_{\rm COMP}}=\frac{V_{\rm in}}{R_{\rm CS}\cdot F_{\rm CF}\cdot F_{\rm DF}\cdot(V_{\rm in}-V_o)} \tag{19}$$

TABLE II
MEASURED HARMONICS CONTENTS OF THE CONVENTIONAL MCC (NOTATED AS CON) AND PROPOSED MCC (NEW) PFC BOOST CONVERTER AT 110-VRMS INPUT VOLTAGE

Measured Harmonics Contents @ 110Vrms										Unit: [mA/W]
Harmonic Order	3		5		7		9		11	
IEC61000-3-2 Limit Level	3.4 mA/W		1.9 mA/W		1 mA/W		0.5 mA/W		0.35 mA/W	
Load [W] \ Type	CON	NEW	CON	NEW	CON	NEW	CON	NEW	CON	NEW
400	0.485	0.498	0.215	0.223	0.105	0.110	0.050	0.050	0.020	0.020
320	0.466	0.525	0.197	0.225	0.088	0.103	0.034	0.044	0.013	0.016
240	0.467	0.475	0.179	0.188	0.025	0.071	0.025	0.025	0.029	0.021
160	0.438	0.463	0.144	0.156	0.044	0.044	0.025	0.025	0.044	0.044
80	0.850	0.254	0.249	0.086	0.456	0.206	0.231	0.255	0.021	0.146
40	1.485	0.635	0.225	0.033	0.103	0.060	0.055	0.283	0.315	0.120

TABLE III
MEASURED HARMONICS CONTENTS OF THE CONVENTIONAL MCC (NOTATED AS CON) AND PROPOSED MCC (NEW) PFC BOOST CONVERTER AT 220-VRMS INPUT VOLTAGE

Measured Harmonics Contents @ 220Vrms										Unit: [mA/W]
Harmonic Order	3		5		7		9		11	
IEC61000-3-2 Limit Level	3.4 mA/W		1.9 mA/W		1 mA/W		0.5 mA/W		0.35 mA/W	
Load [W] \ Type	CON	NEW	CON	NEW	CON	NEW	CON	NEW	CON	NEW
400	0.053	0.066	0.031	0.017	0.033	0.030	0.011	0.013	0.035	0.033
320	0.200	0.013	0.198	0.056	0.039	0.031	0.079	0.004	0.076	0.008
240	0.391	0.024	0.254	0.020	0.081	0.043	0.046	0.059	0.010	0.040
160	0.646	0.043	0.261	0.062	0.109	0.092	0.053	0.058	0.046	0.016
80	0.846	0.093	0.386	0.143	0.216	0.130	0.115	0.079	0.050	0.003
40	1.138	0.220	0.505	0.163	0.290	0.155	0.195	0.068	0.123	0.030

where D_1/D_2 is $(V_{\rm in} - V_o)/(V_{\rm in})$.

Fig. 12 shows the output voltage error amplifier circuit in this paper. The control to output transfer function of the error amplifier by applying perturbation can be obtained as

$$H_1 = \frac{\hat{v}_{\rm COMP}}{\hat{v}_o} = g_m \frac{V_{\rm REF}}{V_o} \frac{sR_{V\rm comp} \cdot C_{V\rm comp} + 1}{sC_{V\rm comp}} \quad (20)$$

where g_m is the gain of the transconductance amplifier used for the output voltage error amplifier.

Substituting (17), (19), and (20) into (14), the overall loop gain can be calculated as

$$T(s) = \frac{V_{\rm in}^2}{V_o} \cdot \frac{R_o}{2 + sC_o \cdot R_o} \cdot \frac{1}{R_{\rm CS} \cdot F_{\rm CF} \cdot F_{\rm DF} \cdot (V_{\rm in} - V_o)} \cdot g_m \frac{V_{\rm REF}}{V_o} \frac{sR_{V\rm comp} \cdot C_{V\rm comp} + 1}{sC_{V\rm comp}}. \quad (21)$$

V. IMPLEMENTATION AND EXPERIMENTAL RESULTS

A. Implementation Control Circuit

The proposed control method needs a divider and multiplier, which can be realized as the digital circuit base, e.g., a micro control unit or an analog circuit. For this paper, the proposed method has been simply realized based on the analog circuits. Figs. 13 and 14 show a schematic of the feasible implementation circuit, and the photographs of the proposed MCC PFC boost converter, respectively.

To simply implement the calculations to generate $V_{\rm DC}$, analog device's ICs were employed. The remaining circuit blocks were constructed with discrete components, operational amplifiers and gate logics, such as a current sensing circuit, an output voltage feedback circuit, a ZCD demodulator, and a PWM circuit. A negative current was sensed through a sensing resistor, $R_{\rm CS}$ so that the output of AD734 had negative polarity. Thus, subtraction arithmetic expressed at the left term in (6) is easily conducted by applying two same resistors $\rm R_{SUB}$ with both the output voltage of AD734 and the bias voltage of 5 V.

In addition, to verify the proposed MCC method based on the analog circuits, in this paper, a 400-W boost PFC converter was designed with electric specifications and key parameters shown in Table I.

Fig. 15 shows the experimental operating waveforms of the PWM generator. As can be seen i_L stands for a current waveform flowing to the boost inductor that is sensed by $R_{\rm CS}$, and $V_{\rm DC}$ is the current control signal generated by (14) where a small ripple voltage is observed because the inductor current was sensed

by the low-pass filter of $R_{\rm CF}$ and $C_{\rm CF}$. $V_{\rm GS}$ is a gate signal waveform for the MOSFET generated from the PWM generator comparing $V_{\rm DC}$ and saw-tooth waveforms $V_{\rm SAW}$.

Fig. 16 shows the experimental operating waveforms of the ZCD demodulator, which consists of a drain-to-source voltage $V_{\rm DS}$, ZCD detecting voltage V_D, ZCD pulse $V_{\rm ZCD}$, and the average voltage of ZCD pulse $V_{\rm BDCM}$ shown in Fig. 13. These results are in good agreement with those discussed previously in Section II-B

Figs. 17 and 18 show the experimental results of the proposed PFC converter with 220-Vrms line input at 100% and 50% load condition, where $V_{\rm BDCM}$ is a compensation signal generated from ZCD demodulator, i_L is the current flowing through the boost inductor, and $v_{\rm in}$ and $i_{\rm in}$ are the line input voltage and current, respectively.

The results show that CCM and DCM are mixed during a half cycle of the ac line, where $V_{\rm BDCM}$ of 1 V indicates PFC converter entering CCM and $\rm V_{BDCM}$ lower than 1 V indicates DCM operation. By referring to $\rm V_{BDCM}$, CCM operation is observed only in the vicinity of the peak and zero crossing of ac line, whereas DCM operation is observed at the side band. Any distorted current such as glitch or spike does not occur while the operation mode switches from DCM to CCM and vice versa because during the transitions between DCM and CCM, $V_{\rm BDCM}$ has continuous changes.

Figs. 19 and 20 show the experimental results of the proposed PFC converter with 110-Vrms line input and 100% and 20% load conditions, respectively. As can be seen in Fig. 19, the proposed converter operates with full CCM operation during the cycle by referring to $V_{\rm BDCM}$. However, it can enter DCM operation as the load decreases. At the test board with a boost inductance of 520 μH, the DCM operation was first observed from a load condition of less than 30%. The operation then continued with full DCM during the entire cycle at 20% load condition as shown in Fig. 20.

Tables II and III show the measured harmonic current levels of the proposed MCC and conventional MCC in each order depending on the load conditions and input voltages, and the harmonic limit levels corresponding to IEC6100-3-2 Class-D as well.

In addition, the measured harmonic current levels of full load at 20% and 10% load condition are plotted in Fig. 21 in order to clearly compare between the proposed MCC and conventional MCC. All of the measured harmonic levels of the proposed MCC at 110 and 220 Vrms can satisfy the international standard of IEC61000-3-2 Class-D, respectively. In particular, the harmonic levels at 10% load condition and 110 Vrms could meet the standard with sufficient margin unlike the conventional MCC. Those figures were measured using a PZ4000 power analyzer.

Fig. 22 shows comparison results of THD of the proposed MCC boost converter and the conventional MCC boost converter depending on the load and line input voltage. The conventional MCC boost converter was implemented at the same by disabling the ZCD demodulator for an exact comparison regardless of the effect of various parameters, such as boost inductance, MOSFET, controller's gain, etc., in the test board.

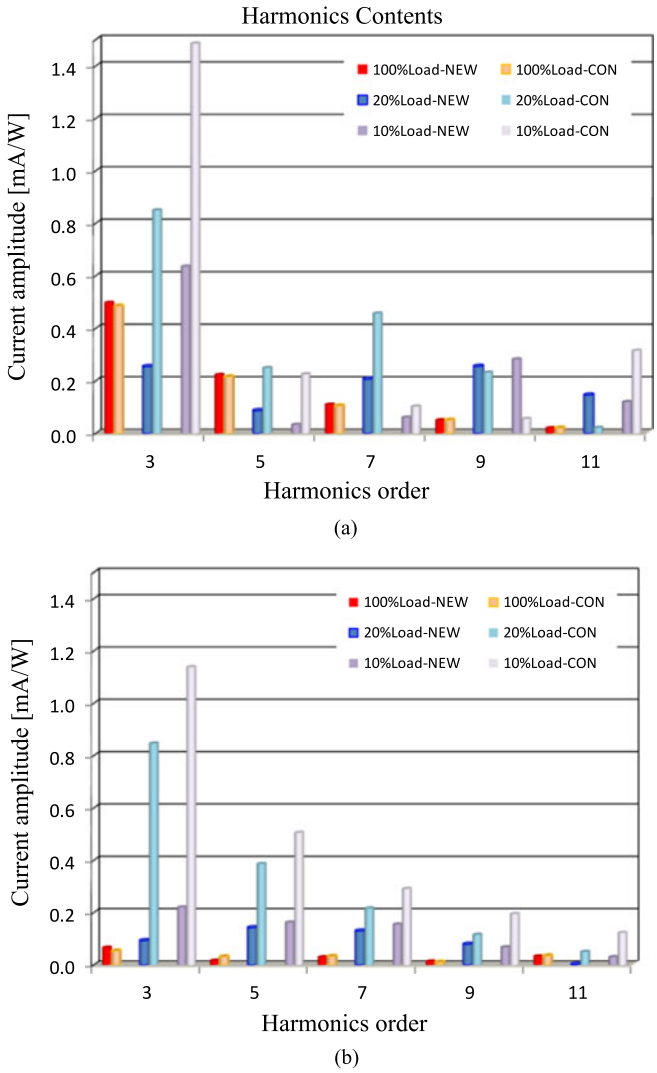

Fig. 21. Comparison graph of the measured harmonics of the conventional MCC (marked as CON) and proposed MCC (NEW) depending on the load variation and line input voltage. (a) Measured harmonic current at 110 Vrms. (b) Measured harmonic current at 220 Vrms.

At 220 Vrms line input and full-load condition, DCM region of both the converters is small at the half of the input line cycle, as can be seen in Fig. 17. Accordingly, the figure shows that almost the same THD result was obtained in both MCC methods, with 2.39% for the proposed method and 2.21% for the conventional MCC method.

Meanwhile, with the conventional MCC method, as the load decreases, THD performance deteriorates gradually reaching up to 21.81% at 10% load condition. On the other hand, the proposed method shows that THD performance dramatically improves over the entire load range and THD performance of 8.59% was recorded at 10% load condition, as can be seen in Fig. 22.

At the low line input of 110 Vrms, THD values with the conventional MCC method start to deteriorate because it starts to enter the DCM operation at 30% load condition. But, the proposed method shows a continued low THD value of less than 11% at 10% load condition.

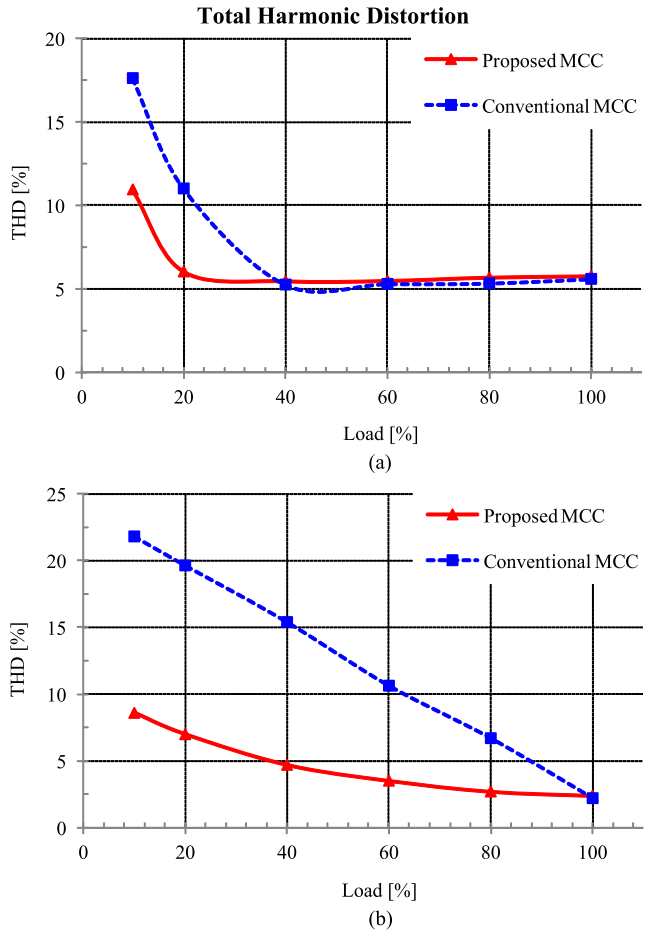

Fig. 22. Comparison results of THD of the proposed MCC converter versus conventional MCC converter. (a) Total harmonic distortion at 110 Vrms input. (b) Total harmonic distortion at 220 Vrms input.

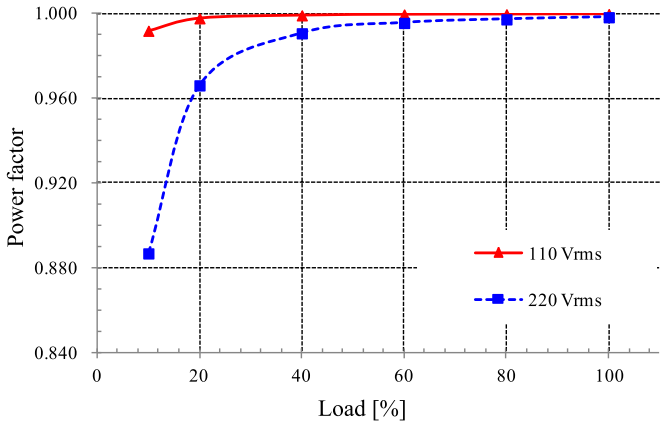

Fig. 23. PF performance of the proposed MCC converter.

Fig. 23 shows PF performance of the proposed MCC converter. At 20% load condition, 0.998 of PF was measured in 110 Vrms and 0.966 of PF is measured in 220 Vrms.

VI. Conclusion

This paper proposed new MCC method for PFC boost converter to provide a high PF and low THD in a wide line input voltage and load range while maintaining the simple control structure and fast dynamic response of the conventional MCC method. In addition, the proposed MCC method provides more flexibility in designing a boost inductor so that it does not consider using a big inductor to guarantee CCM under as much load range as possible to meet the harmonic regulation.

The proposed control method and feasibility were verified using a 400-W PFC boost converter. The proposed method showed outstanding performance of THD of 2.39% and 5.76% under each input voltage of 220 and 110 Vrms with a full-load condition, respectively. Moreover, THD of less than 7% was maintained even though the load was decreased up to 20%. Therefore, the proposed control method could be a good candidate as a controller for high performance PFC boost converter that covers wide line input voltage and load range.

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