Investigation of the Active Ripple Compensation Technique to Reduce Bulk Capacitance in Offline Flyback-Based LED Drivers

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***Abstract*—This paper presents the study of an offline flyback-based light-emitting diode (LED) driver with reduced storage capacitance. An approach called active ripple compensation was used for minimizing the converter bulk capacitance. This technique is oriented to voltage-controlled pulse width modulation converters and is based on the modulation of the duty cycle, which allows for the reduction of the filtering capacitance by increasing the harmonic content of the input current up to the limits established by the standards. By means of the design procedure presented in this paper, the amount of capacitance reduction and input current distortion can be fully controlled and theoretically predicted. In addition, no extra sensors are required to implement the proposed technique, apart from the LED current sensor already available in most LED drivers. Experimental results from a 50-W laboratory prototype supplied from a 220-V 60-Hz grid were carried out. The results were compared with the conventional approach, attesting the superior performance of the proposed methodology.**

***Index Terms*—Active ripple compensation (ARC), capacitance reduction, flyback converter, light-emitting diode (LED) drivers, offline operation, power factor correction, power supplies.**

I. Introduction

ARTIFICIAL lighting represents a significant portion of the global energy consumption, attaining nowadays a share of about 19% [1]. This scenario encourages researchers to work toward more efficient lighting systems. In this context, the solid-state lighting concept can be highlighted as one of the more efficient, durable, and environmental friendly lighting technology commercially available nowadays [2], [3].

In order to ensure the maximum performance of the light-emitting diodes (LEDs), they must be driven by an electronic circuit, i.e., a driver. The main function of this device is to stabilize the current through the load, controlling its average value and ripple level, which can affect significantly the photometric performance of the LEDs [4], [5]. Furthermore, the current ripple can cause stroboscopic and flickering effects, which could be noticeable to the human eye in some circumstances [6].

Therefore, the correct design of the LED driver is essential to the success of the solid-state lighting system. This design must ensure not only the photometric performance of the LEDs, but also the long lifespan of the system and a good power density of the electronic circuit. In offline applications, the achievement of the latter characteristics could be difficult, since usually a large low-frequency ripple must be filtered to compensate the input-to-output instantaneous power imbalance [7].

The low-frequency ripple filtering is normally performed by electrolytic capacitors, which are known to reduce the circuit lifespan, or alternatively by using a bank of metalized film capacitors, which have better lifespan, but decrease the power density of the drivers [8].

Some researchers have proposed techniques to deal with these problems [7], [9]–[16]. Some of these approaches are based on the reduction of the instantaneous power unbalance between the input and the output of the converter, which causes a reduction of the output current ripple [13]–[16]. On the other hand, the works presented in [7], [9]–[12] all focus on alternative topologies or design procedures to reduce the required filtering capacitances.

The alternative presented in [16], called active ripple compensation technique (ARCT), proposed a method for capacitance minimization in pulse width modulation converters, in which it is possible to reduce the required filtering capacitance just by adding a branch to the conventional control scheme. However, this paper proposed the application of the aforementioned scheme to an integrated, two-stage converter, which is normally required for high power levels.

This paper evaluates the application of the ARCT to a single-stage converter, suitable for low-to-medium power applications. The flyback-based ac–dc converter topology has been chosen in this study, since it is widely used as LED driver nowadays.

The remainder of this paper is organized as follows. Section II describes the basic operation of the flyback-based LED driver associated to the active ripple compensation (ARC) approach. Section III presents the design strategy using such technique in order to minimize the bulk capacitance while fulfilling the standard requirements. Section IV presents experimental results from a laboratory prototype. Finally, the conclusions of this paper are detailed in Section V.

Manuscript received June 26, 2017; accepted August 7, 2017. Date of publication August 11, 2017; date of current version February 22, 2018. This work was supported by PPEE/UFJF, FAPEMIG, CAPES (process no. 88881.132529/2016-01) and by the Spanish Government under research Grant ENE2013-41491-R. Recommended for publication by Associate Editor M. Ponce-Silva. *(Corresponding author: Guilherme Marcio Soares.)*

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Digital Object Identifier 10.1109/TPEL.2017.2738779

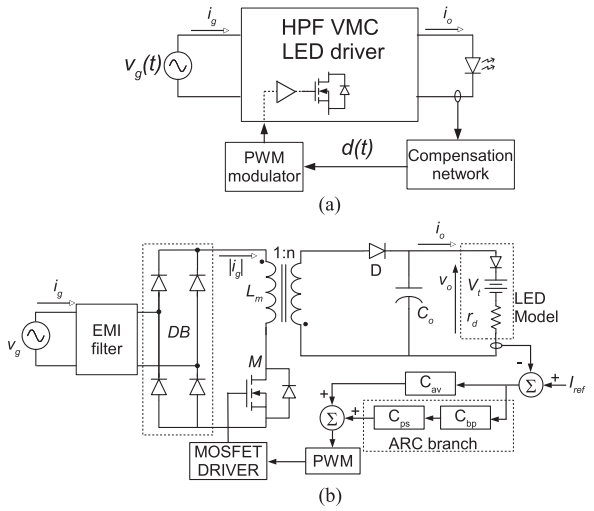

Fig. 1. (a) Basic diagram of an offline VMC LED driver. (b) Offline flyback-based LED driver with ARC.

II. Flyback-Based LED Driver With ARC

This section gives the mathematical description of the flyback-based LED driver with the ARCT. The converter was devised to operate in the discontinuous conduction mode (DCM), since in this operating mode, the circuit behaves like a voltage follower and achieves a high-power factor at the driver ac input.

Fig. 1(a) presents the simplified diagram of a voltage-mode controlled (VMC) LED driver. In such circuits, there is a single compensation network for controlling the converter, which is responsible for generating the duty cycle $d(t)$ from measurements of the output current. In conventional approaches, the compensation network is designed only to ensure null steady-state error of the average output current. On the other hand, the ARCT proposed the large-signal modulation of $d(t)$, so that this signal was also used to compensate the low-frequency ripple of the output current.

Fig. 1(b) depicts a schematic including the main driver components as well as the compensation network block diagram assuming the flyback-based topology, which is the one considered in this paper. As can be seen, the ARCT requires an additional branch for its proper operation as compared to a typical VMC technique. However, no additional sensors are required, since all the modulation process is generated from the output current signal.

The design of the flyback driver with ARC must meet the requirements regarding the input current, so that it complies with the IEC-61000-3-2 standard, and the output current, which must ensure that its average value and ripple stay within the desired values in order to assure the lighting quality [6]. Therefore, the mathematical analysis presented in this paper focuses on these two aspects.

According to [17], the input current of the flyback converter operating in DCM can be written as (1) in terms of the mains voltage $v_g(t)$, the duty-cycle function $d(t)$, the flyback transformer magnetizing inductance of the flyback transformer L_m, and the converter switching frequency f_s

$$|i_g(t)| = \frac{|v_g(t)|\, d(t)^2}{2L_m f_s}. \tag{1}$$

On the other hand, the mains voltage can be defined by its rms value V_G and frequency f_L

$$v_g(t) = \sqrt{2}V_G \sin(2\pi f_L t). \tag{2}$$

Owing to the instantaneous power imbalance between the converter input and output, its main variables will oscillate at twice the line frequency. Therefore, as presented in [16], a duty cycle modulating at twice the line frequency has been selected, thus allowing it to influence the large-signal behavior of the converter. In this way, the duty cycle can be expressed as (3). Note that the modulation function is composed by three parameters: a dc component D_0, the duty-cycle modulation amplitude D_2, and the modulation phase ϕ_c. The implementation of the duty-cycle function is accomplished by the two branches in the control loop shown in Fig. 1(b): the compensator $C_{\rm av}$ is used to synthesize the value of D_0, whereas the blocks $C_{\rm bp}$ and $C_{\rm ps}$ generates the oscillating portion of $d(t)$ from the output signal. The design of these blocks are discussed in Section III-B

$$d(t) = D_0 + D_2 \sin(2\omega_L t + \phi_c). \tag{3}$$

By using (3) in (1), the converter input current under the proposed modulation strategy can be derived as follows:

$$\begin{aligned} i_g(t) = {} & I_1 \sin(\omega_L t + \phi_1) + I_3 \sin(3\omega_L t + \phi_3) \\ & + I_5 \sin(5\omega_L t + \phi_5) \end{aligned} \tag{4}$$

in which the magnitudes and phases of the harmonic components are given by the following equations:

$$I_1 = \frac{\sqrt{2}V_G}{2L_m f_s}\left[\left(D_0{}^2 + \frac{D_2{}^2}{2} - D_0 D_2 \sin(\phi_c)\right)^2 + (D_0 D_2 \cos(\phi_c))^2\right]^{\frac{1}{2}} \tag{5}$$

$$\phi_1 = tg^{-1}\left(\frac{2D_0 D_2 \cos(\phi_c)}{2D_0{}^2 + D_2{}^2 - 2D_0 D_2 \sin(\phi_c)}\right) \tag{6}$$

$$I_3 = \frac{\sqrt{2}V_G}{4L_m f_s}\left[\left(2D_0 D_2 \sin(\phi_c) + \frac{D_2{}^2}{2}\cos(2\phi_c)\right)^2 + \left(\frac{D_2{}^2}{2}\sin(2\phi_c) - 2D_0 D_2 \cos(\phi_c)\right)^2\right]^{\frac{1}{2}} \tag{7}$$

$$\phi_3 = tg^{-1}\left(\frac{\frac{D_2{}^2}{2}\sin(2\phi_c) - 2D_0 D_2 \cos(\phi_c)}{2D_0 D_2 \sin(\phi_c) + \frac{D_2{}^2}{2}\cos(2\phi_c)}\right) \tag{8}$$

$$I_5 = \frac{\sqrt{2}V_G D_2{}^2}{8L_m f_s} \tag{9}$$

$$\phi_5 = 2\phi_c + \pi. \tag{10}$$

As can be seen, with the proposed duty-cycle signal, given by (3), the input current of the converter is composed only by the first, third, and fifth harmonics. For the sake of simplicity, the analysis presented in this paper will consider that the electromagnetic interference (EMI) input filter is designed to eliminate all the harmonics above the fifth harmonics.

It is also important to note that in order to have good accuracy in the converter design, the converter input power must be analyzed taking into account the superposed modulation

TABLE I
DESIGN PARAMETERS

Symbol	Description	Value
V_G	Mains voltage	220 V ±10%
f_L	Line frequency	60 Hz
V_{t0}	Nominal threshold voltage of the LED lamp	128.27 V at 25 °C
k_v	Temperature coefficient of the threshold voltage	− 0.0816 V/°C
ΔT_j	LED junction temperature range	0 °C–100 °C
T_{j0}	Nominal LED junction temperature	25 °C
r_d	Dynamic resistance of the LED lamp	44.38 Ω
η	Estimated efficiency	90%
I_o	Average output current	350 mA
V_o	Average output voltage	143.81 V
P_o	Output power	50 W
$\Delta I_{o\%}$	Maximum current ripple	10%
f_s	Switching frequency	50 kHz

(D_2, ϕ_c) and not only the dc value (D_0). This analysis will be shown in Section III.

With regard to the converter output current, this variable can be calculated by means of

$$i_o(t) = \frac{v_o(t) - V_t}{r_d} \tag{11}$$

in which V_t and r_d are the threshold voltage and the dynamic resistance of the LED string. The instantaneous output voltage $v_o(t)$ can be calculated by means of (12) in terms of the diode current, which is given by (13). In (12), η represents the estimated efficiency of the circuit, whereas C_o is the output capacitance

$$\frac{dv_o(t)}{dt} = \frac{1}{C_o}\left(\eta i_D(t) - \frac{v_o(t) - V_t}{r_d}\right) \tag{12}$$

$$i_D(t) = \frac{v_g(t)^2 d(t)^2}{2 f_s L_m v_o(t)}. \tag{13}$$

In order to obtain the average value and the ripple of the output current, the numerical method shown in [16] was used to solve the equation system composed by (12) and (13).

III. DESIGN EXAMPLE

The design of the flyback-based LED driver with ARC must be performed in two steps. First, the passive elements (L_m and C_o) and the parameters of the duty-cycle function (D_0, D_2, and ϕ_c) must be obtained. Thereafter, the control loop is designed so that $d(t)$ assumes the form defined in the previous step.

A. Design of the Passive Elements and the Parameters of the Duty-Cycle Function

According to [16], the passive elements must be designed simultaneously with the definition of the duty-cycle function when the ARCT is employed, since the values of D_0, D_2, and ϕ_c affect the large signal behavior of the circuit.

Table I summarizes the design parameters. The load, whose equivalent model presented in Table I is described in terms of V_{t0}, r_d, and k_v, comprises 16 LED modules connected in series. Each module consists of the parallel association of four branches, which are composed by the series connection of three Nichia NFSL757DT-V devices.

The criterion for choosing the current ripple level was based on the directives presented in [6], which showed that a ripple level of 10% has a low risk to cause human biological effects if the light modulation is at 120 Hz (typical in offline LED drivers supplied by a 60-Hz mains voltage).

The first step is to define the maximum duty cycle, which ensures the DCM operation. As shown in [17], this parameter can be calculated by the following equation:

$$D_{\text{crit}}(V_o, V_G, n) = \frac{V_o}{V_o + n\sqrt{2}V_G}. \tag{14}$$

According to [5], the output voltage of the circuit can be estimated by means of

$$V_o = V_t + r_d \times I_o \tag{15}$$

in which V_t is the threshold voltage, defined in the following equation as a function of the LED p-n junction temperature T_j:

$$V_t = V_{t0} + k_v \times (T_j - T_{j0}). \tag{16}$$

Since the output voltage varies according to the temperature, D_{crit} must be calculated for the operating condition in which V_o is maximum. According to (15) and (16), this situation occurs when the junction temperature is the lowest and can be calculated using the data presented in Table I, yielding $V_{o\_\max} = 145.9$ V. Therefore, the constraint for ensuring the DCM when the converter is operating with the ARCT is given by

$$D_0 + D_2 \leq D_{\text{crit}}(V_{o\_\max}, V_G, n). \tag{17}$$

As long as the condition for the DCM operation is defined, the design of the main parameters of the driver can be done. This task can be accomplished by adopting a graphical evaluation of the input and output current behaviors according to variations of the output capacitance and the parameters of the duty-cycle function.

The design of the driver presented in the following will consider the nominal operating point, i.e., $V_G = 220$ V and $T_j = T_{j0}$. Furthermore, the chosen transformation relationship was $n = 1$, which results in a critical duty cycle of $D_{\text{crit}}(V_{o\_\max}, 220, 1) = 0.319$ for this operating condition. Therefore, in order to ensure the DCM operation and allow for the large-signal modulation of the duty-cycle signal, a value of $D_0 = 0.225$ was defined.

Fig. 2 shows the behavior of the third and the fifth harmonic components of the input current as a function of the modulation angle ϕ_c for different values of the modulation amplitude D_2.

In Fig. 2(a), one can see that for $D_2 \leq 0.05$, the third harmonic component of the input current is within the limits established by the IEC 61000-3-2 standard regardless the value of ϕ_c. Nevertheless, if $D_2 = 0.07$, the aforementioned standard is not met when the angle ϕ_c is larger than $-8°$. On the other hand, the fifth harmonic component [see Fig. 2(b)] remained within the limits of the IEC 61000-3-2 standard regardless the values of the duty-cycle parameters.

As can be noted from (5), the fundamental harmonic of the input current is also affected by D_2 and ϕ_c, so that the power processed by the converter is also modified according to the values of such parameters. Therefore, in order to ensure the

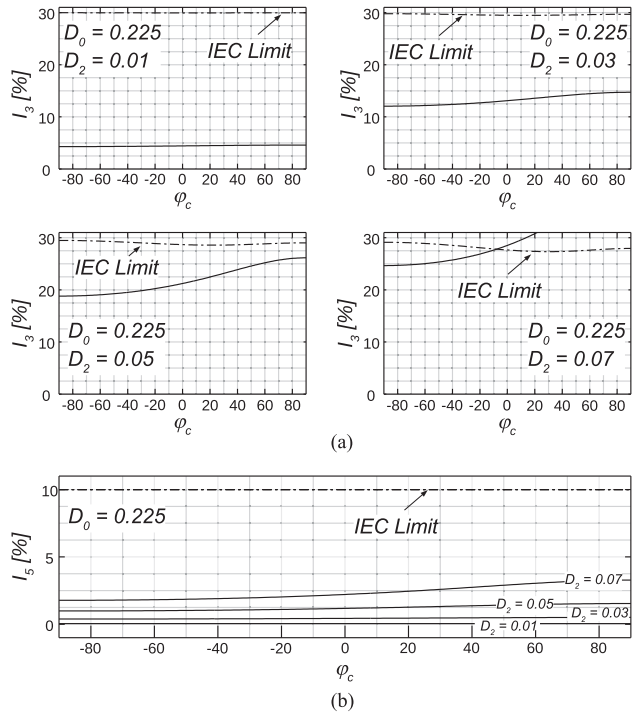

Fig. 2. Behavior of the input current according to variations on the duty-cycle parameters. (a) Third harmonic component. (b) Fifth harmonic component.

power balance of the converter, for each pair (D_2, ϕ_c) a new value of the magnetizing inductance must be calculated so that the power delivered to the load remains constant.

Inductance L_m can be designed by means of power balance between the input and the output of the converter, as stated in (18) and (19). Thus, the flyback transformer magnetizing inductance can be obtained by using (1) and (19), which yields (20)

$$P_{\text{in}} = \frac{P_o}{\eta}. \tag{18}$$

$$\frac{1}{T}\int_0^T v_g(t) i_g(t) dt = \frac{P_o}{\eta}. \tag{19}$$

$$L_m = \frac{1}{T}\frac{\eta \int_0^T v_g(t)^2 d(t)^2 dt}{2 P_o f_s} \tag{20}$$

in which T is the line period ($T = 1/f_L$).

Fig. 3 shows the behavior of the relative output current ripple for some typical commercial values of C_o. For each capacitance, a set of curves was generated, being each one characterized by a certain value of D_2, ranging from $D_2 = 0$ up to $D_2 = 0.07$, and plotted for several values of ϕ_c. The graphs were obtained by solving (11)–(13) using the values of D_2, ϕ_c, and C_o as well as the parameters presented in Table I.

As can be noted in Fig. 3, if $\phi_c \geq 0$, the large-signal modulation of $d(t)$ decreases the output current ripple, achieving the maximum reduction when ϕ_c is around 90°. The graphs also show that if ϕ_c is positive, the output current ripple decreases as D_2 increases. Nevertheless, if $D_2 \geq 0.05$, the driver lost the compliance with the IEC-61000-3-2 standard, so that this represents the limit for the parameter D_2, as already addressed in Fig. 2(a).

Therefore, by choosing $D_2 = 0.05$ and $\phi_c = 90°$, the desired ripple criterion is achieved for an output capacitance of $C_o = 470\ \mu$F, which yields an output current ripple of 9.8% (34.3 mA).

In Fig. 3, it can be noted that if the ARCT was not used (i.e., $D_2 = 0$), this capacitance would be insufficient for meeting the design requirements. In such case, a capacitance of ca. 620 μF must be used for achieving a similar ripple level. Therefore, the modulation of the duty cycle provided a capacitance reduction of 150 μF (24.2%) when compared to the conventional approach without modulation.

Analogously to Fig. 2, for each point of Fig. 3, a magnetizing inductance L_m must be obtained to ensure the average power balance. Thus, Fig. 4 shows the behavior of the magnetizing inductance as a function of ϕ_c for several values of D_2. In Fig. 4, it can be seen that for positive values of ϕ_c, the required value of the inductance L_m decreases as the amplitude of the ac portion of $d(t)$ increases. Furthermore, the graph also shows that for the chosen operating point (i.e., $D_2 = 0.05$ and $\phi_c = 90°$), the value of the inductance L_m must be 352 μH.

B. Design of the Control Loop

Since the passive elements and the duty-cycle function have been defined, the control circuit can be designed in a similar way as presented in [16].

One of the advantages of such approach is that both control branches operate independently so that they can also be designed separately. As already mentioned, the compensator C_{av} is responsible for synthesizing the dc component (D_0) of the duty cycle while the ARC branch generates its ac portion ($D_2 \sin(2\omega_L t + \phi_c)$) from the error signal in two steps. The first one consists of isolating the $2\omega_L$ component of the error signal by means of the bandpass filter C_{bp}. Thereafter, the C_{ps} block gives the correct gain and phase shifting to the output of C_{bp} in order to produce the desired oscillating portion of $d(t)$.

The transfer function of C_{av} is shown in (21). As can be noted, this compensator is an integrator, which ensures that the system have null steady-state error [18]. Furthermore, the crossover frequency of this transfer function must be tuned so that the output of the C_{av} block does not present any ac component in steady state, i.e., C_{av} must attenuate all the oscillating components of the error signal

$$C_{\text{av}}(s) = K_a \frac{1}{s}. \tag{21}$$

In order to ensure a good attenuation at 120 Hz, a $K_a = 30$ was chosen, resulting in a crossover frequency of ca. 5 Hz, which is nearly two decades below $2f_L$.

The expression for $C_{\text{bp}}(s)$ was designed based on a narrow-band second-order bandpass filter [19]. This element was tuned with a center angular frequency of $2\omega_L$ ($4\pi f_L$), which ensures that the oscillating component of the duty cycle presents the desired frequency. Thus, the transfer function of C_{bp} is given by (22), in which K_{bp} is the gain at center frequency and B is the filter bandwidth

$$C_{\text{bp}}(s) = K_{\text{bp}} \frac{Bs}{s^2 + Bs + 4{\omega_L}^2}. \tag{22}$$

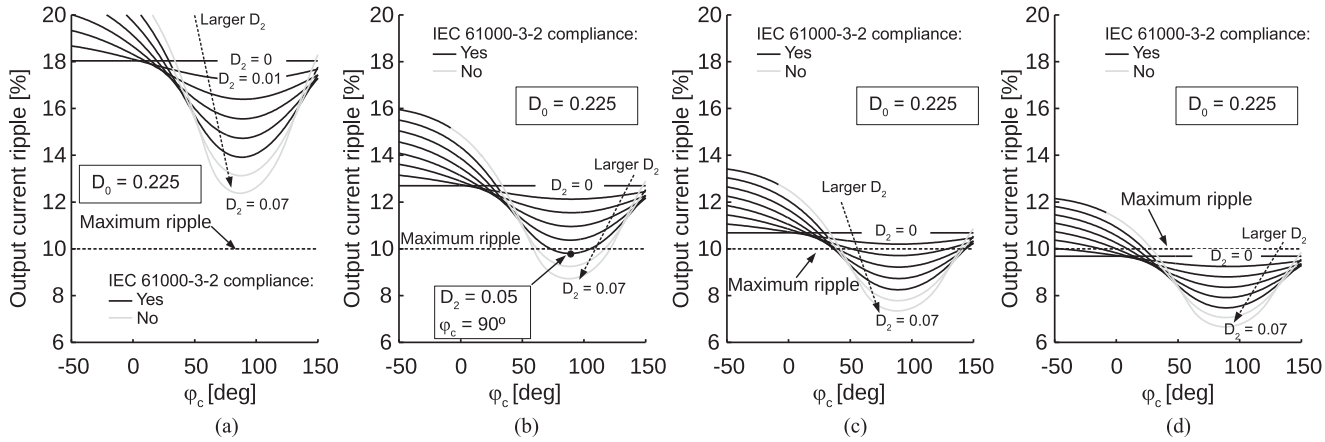

Fig. 3. Behavior of the peak-to-peak output current ripple according to D_2 and ϕ_c for several values of C_o. (a) $C_o = 330$ μF. (b) $C_o = 470$ μF. (c) $C_o = 560$ μF. (d) $C_o = 620$ μF.

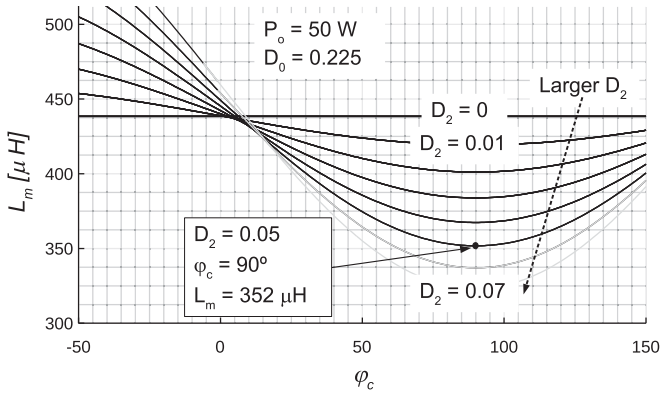

Fig. 4. Variation of the magnetizing inductance according to the duty-cycle parameters.

Finally, the design of the phase-shifting filter $C_{\rm ps}$ was based on the lead-lag compensator [18]. It must be calculated by considering the amplitude and phase of the output current at the frequency of interest ($2\omega_L$). These values can be obtained from (11) by using the Fourier series. Thus, the transfer function of $C_{\rm ps}(s)$ is shown in (23) and its parameters must be chosen so that the output waveform of this filter is the desired oscillating component of the duty-cycle signal. This condition is fulfilled by equations (24) and (25), which were derived from the analysis of the control diagram of Fig. 1. It is important to highlight that in this paper, the current sensor circuit was based on the HCPL-7840 IC, tuned with a cutoff frequency of 2.5 kHz and a gain of 1 V/A. Therefore, the measured value presents a negligible phase shift at $2\omega_L$

$$C_{\rm ps}\left(s\right) = K_{\rm ps}\frac{s+z_{\rm ps}}{s+p_{\rm ps}} \tag{23}$$

$$\left|C_{\rm ps}\left(2\omega_L\right)\right| = \frac{D_2}{I_{o\_2\omega L}K_{\rm bp}} \tag{24}$$

$$\angle C_{\rm ps}\left(2\omega_L\right) = \phi_c - \phi_{io\_2\omega L} - 180^\circ \tag{25}$$

in which $I_{o\_2\omega L}$ and $\phi_{io\_2\omega L}$ are the amplitude and phase of the $2\omega_L$ component of the output current, respectively.

TABLE II
CONTROL CIRCUIT PARAMETERS

Parameter	Value
K_a	30 Hz
$K_{\rm bp}$	1
B	125.66 rad/s
$K_{\rm ps}$	27.88
$z_{\rm ps}$	27.04 rad/s
$p_{\rm ps}$	$21.02 \cdot 10^3$ rad/s

By using the design results obtained in Section III-A in (11)–(13) for calculating the output current $i_o(t)$ and thereafter performing the Fourier series, the amplitude and phase of the $2\omega_L$ component of the output current is found as 17.2 mA and -175.9°, respectively. Therefore, those values can be used in (24) and (25) to find the parameters of $C_{\rm ps}$.

Table II summarizes the design results of the control loop.

In this paper, the control system was implemented digitally by means of a TIVAC-Series microcontroller. The discretization of elements of the control loop was performed using the bilinear transformation [20] in a similar way to [16]. The difference equations that represent the compensator $C_{\rm av}(s)$, the bandpass filter $C_{\rm bp}(s)$, and the phase-shifting filter $C_{\rm ps}(s)$ are given by (26)–(28), respectively. Finally, the duty cycle of the discrete-time system at the kth instant is calculated by (29)

$$y_{\rm avg}\left(k\right) = N_{a1}\varepsilon\left(k\right) + N_{a2}\varepsilon\left(k\ +\ 1\right) - N_{a3}y_a\left(k\ +\ 1\right) \tag{26}$$

$$y_{\rm bp}\left(k\right) = N_{\rm bp1}\varepsilon\left(k\right) + N_{\rm bp2}\varepsilon\left(k\ +\ 2\right) - N_{\rm bp3}y_{\rm bp}\left(k\ +\ 1\right) - N_{\rm bp4}y_{\rm bp}\left(k\ +\ 2\right) \tag{27}$$

$$y_{\rm ps}\left(k\right) = N_{\rm ps1}y_{\rm bp}\left(k\right) + N_{\rm ps2}y_{\rm bp}\left(k\ +\ 1\right) - N_{\rm ps3}y_{\rm ps}\left(k\ +\ 1\right) \tag{28}$$

$$d_k\left(k\right) = y_a(k) + y_{\rm ps}(k) \tag{29}$$

where $y_{\rm avg}$, ϵ, $y_{\rm bp}$, $y_{\rm ps}$, and d_k are the discrete variables representing the output of the average current compensator, the error signal, the bandpass filter, the phase-shifting filter, and the duty

TABLE III
COEFFICIENTS USED IN THE DISCRETE IMPLEMENTATION

Coefficient	Definition	Value
N_{a1}	$\frac{K_a}{2f_{sam}}$	0.003003
N_{a2}	$\frac{K_a}{2f_{sam}}$	0.003003
N_{a3}	-1	-1
N_{bp1}	$\frac{K_{\text{bp}} \cdot B \cdot f_{sam}}{2f_{sam}{}^2 + B \cdot f_{sam} + 2\omega_L{}^2}$	0.012341
N_{bp2}	$-\frac{K_{\text{bp}} \cdot B \cdot f_{sam}}{2f_{sam}{}^2 + B \cdot f_{sam} + 2\omega_L{}^2}$	-0.012341
N_{bp3}	$\frac{4\omega_L{}^2 - 4f_{sam}{}^2}{2f_{sam}{}^2 + B \cdot f_{sam} + 2\omega_L{}^2}$	-1.953
N_{bp4}	$\frac{2f_{sam}{}^2 + 2\omega_L{}^2 - B \cdot f_{sam}}{2f_{sam}{}^2 + B \cdot f_{sam} + 2\omega_L{}^2}$	0.97532
N_{ps1}	$\frac{K_{\text{ps}}(2f_{sam} + z_{ps})}{2f_{sam} + p_{\text{ps}}}$	26.2043
N_{ps2}	$\frac{K_{\text{ps}}(z_{ps} - 2f_{sam})}{2f_{sam} + p_{\text{ps}}}$	-26.063
N_{ps3}	$\frac{p_{\text{ps}} - 2f_{sam}}{2f_{sam} + p_{\text{ps}}}$	0.35528

TABLE IV
MAIN PROTOTYPE COMPONENTS

Item	Value
Diode bridge DB	$4 \times$ HER156G
MOSFET M	IRF840 (500V/0.85 Ω)
Diode D	HFA04SD60S
Capacitor C_o	470 μF/tanδ = 0.12/2000h@105 °C (Electrolytic)
Flyback transformer	L_m = 355 μH/Leakage inductance = 15.4 μH/ ETD34 3C90/Primary: 43T/Secondary: 43T/ gap = 0.315 mm /Litz wire 66 $\times$ 38AWG
EMI Filter	CM:5.2 mH/DM: 3 mH/2 $\times$ 220 nF
MOSFET RCD snubber	R: 180 kΩ/C: 2.2nF/D: MUR160
Microcontroller	TI TM4C123G

cycle, respectively. The integer k is the index of the kth sample of the discrete system.

In order to calculate the coefficients in (26)–(28), a sampling frequency f_{sam} of 5 kHz was considered. According to [21], this choice ensures that the discretization error for the bilinear transformation is lower than 3%, since the largest noticeable frequency in the output current is below one-tenth of the sampling frequency. Moreover, since the cutoff frequency of the current sensor was tuned at 2.5 kHz, the aliasing errors in the digital system are mitigated because any noise with frequencies larger than the half of the sampling frequency will be attenuated.

The definition and values for each coefficient in (26)–(28) are gathered in Table III.

It is important to highlight that owing to the simplicity of the control structure used in the ARCT (see Fig. 1), its implementation could be performed by using a simpler microcontroller or even by means of analog circuits.

IV. EXPERIMENTAL RESULTS

In order to verify the theoretical analysis, a laboratory prototype was built. Table IV presents the main elements used in the experiment. Fig. 5 shows a photograph of the prototype boards.

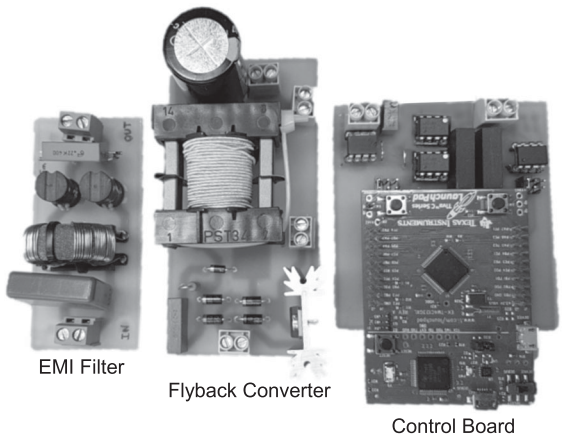

Fig. 5. Photograph of the prototype.

Fig. 6 depicts some experimental waveforms from the flyback-based LED driver employing ARCT [see Fig. 6(a)] compared with the same circuit without the large-signal modulation of the duty cycle [see Fig. 6(b)], and also with the conventional approach with an additional output capacitance of 150 μF, i.e., $C_o = 620$ μF [see Fig. 6(c)]. As can be seen, these experimental results are in agreement with the theoretical analysis, since the ripple of 36 mA found in the experiment is close to the 34.3 mA predicted theoretically. Furthermore, Fig. 6(b) shows that when the ARCT is not used, the capacitance of 470 μF results in a larger ripple, an additional value of 150 μF [see Fig. 6(c)] being necessary to decrease the output current ripple to a similar level to that in which the ARC is employed.

The results presented in Fig. 6 show that the output current ripple of the circuit with duty-cycle large-signal modulation is lower than the conventional approach (i.e., without ARC) at the cost of an increase of the input current distortion. Nevertheless, this distortion was predicted during the design procedure so that the harmonic content of the input current remains in compliance with the IEC-61000-3-2 standard, as shown in Fig. 7. The other harmonics were not depicted in Fig. 7 because their values were negligible. As can be noted, the experimental results of the input current are also close to the values obtained in the theoretical analysis.

The measured efficiency of the prototype with ARCT was 90.1% and 90.2% with the conventional approach (i.e., without ARC). This means that the effect of the large-signal modulation of the duty cycle upon the efficiency of the converter is negligible. Table V shows the measured loss distribution in the prototype, which was obtained at nominal input voltage and rated load. Those measurements did not take into account the consumption of the control board.

The modulated duty-cycle signal at steady-state operation can be seen in Fig. 8. The measurement of this signal was carried out from the MOSFET gate-to-source voltage by using an infinite impulse response (IIR) low-pass filter tuned at 1 kHz, which was embedded in the digital oscilloscope. The results show that the ARC branch is operating properly, since the ac portion of the duty-cycle function is similar to the calculated value (i.e., $D_2 = 5\%$ and $\phi_c = 90°$).

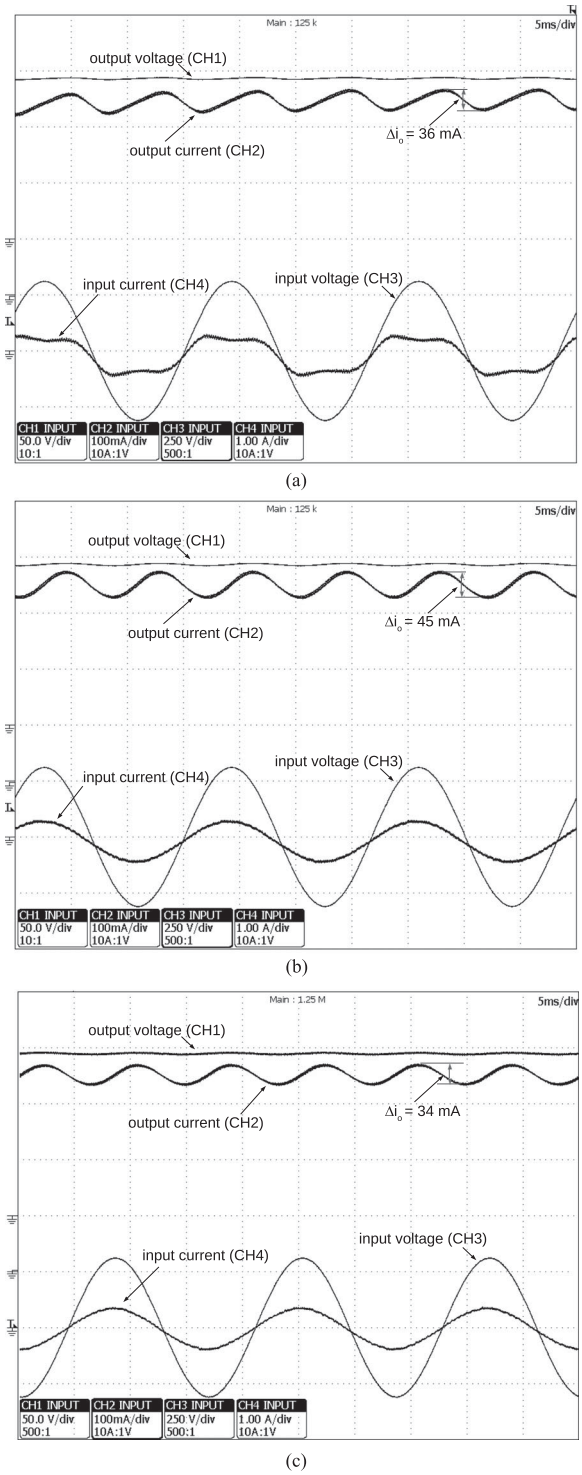

Fig. 6. Experimental waveforms obtained with ARC (a) and without ARC (b). (c) Results without ARC with $C_o = 620\ \mu$F. Output voltage (CH1—50 V/div), output current (CH2—100 mA/div), input voltage (CH3—250 V/div), and input current (1 A/div). Horizontal scale: 5 ms/div.

The waveforms obtained from the MOSFET *M* and diode *D* can be observed in Fig. 9. As can be seen, the active switch is turned ON with zero current, thus proving the DCM operation of the converter. One can note that during the turn-off of the active switch, the MOSFET entered in the avalanche mode. However, owing to the small leakage inductance of the flyback transformer (4.3%), the duration of the voltage spike was short and did not affect the circuit operation.

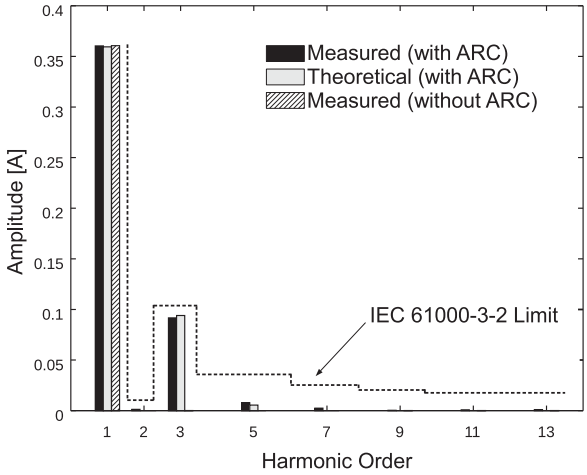

Fig. 7. Harmonic content of the input current.

TABLE V
MEASURED LOSS DISTRIBUITION

Component	Value
EMI filter	0.24 W
Diode bridge	1.03 W
Flyback transformer	0.79 W
MOSFET *M*	2.75 W
MOSFET snubber	0.20 W
Diode *D*	0.37 W
Output capacitor	0.23 W
Total	5.61 W

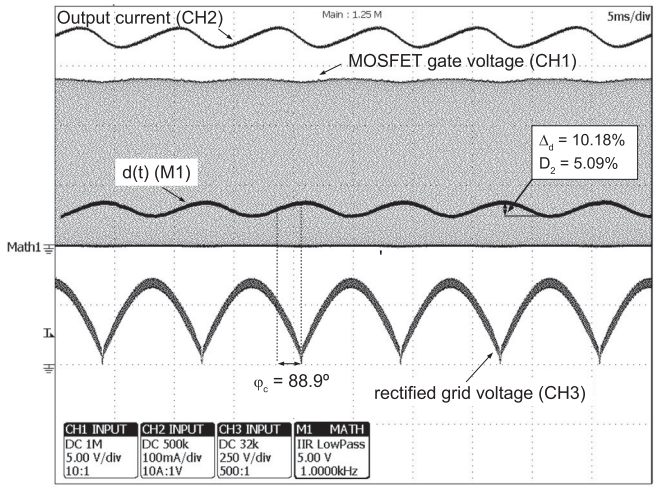

Fig. 8. Behavior of the duty cycle in steady state. MOSFET gate voltage (CH1–5 V/div); duty cycle (M1—IIR low-pass filter with a cutoff frequency of 1 kHz—5 V/div) output current (CH2—100 mA/div); rectified grid voltage (CH3—250 V/div). Horizontal scale: 5 ms/div.

Fig. 10 shows some results related to the closed-loop operation of the converter against input voltage and load variations. Fig. 10(a) and (b) demonstrates that the control loop was able to ensure a good output current regulation. In both the cases, the output current remained very close to its nominal value for

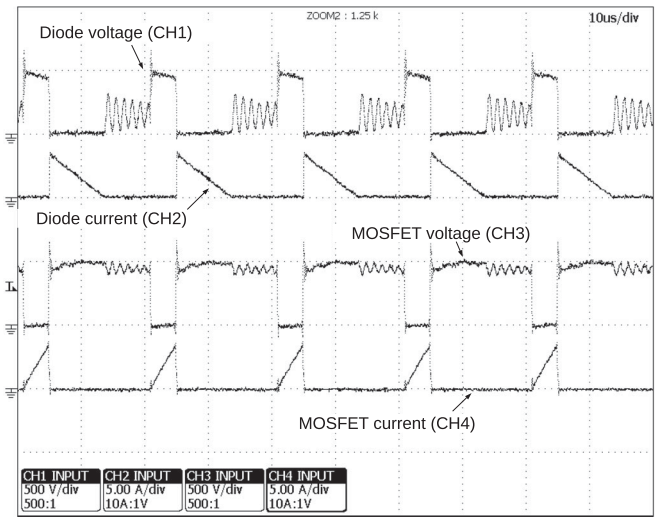

Fig. 9. MOSFET voltage (CH3—500 V/div) and current (CH4—5 A/div). Diode D voltage (CH1—500 V/div) and current (CH2—5 A/div). Waveforms measured at the peak of the rectified voltage. Horizontal scale: 10 μs/div.

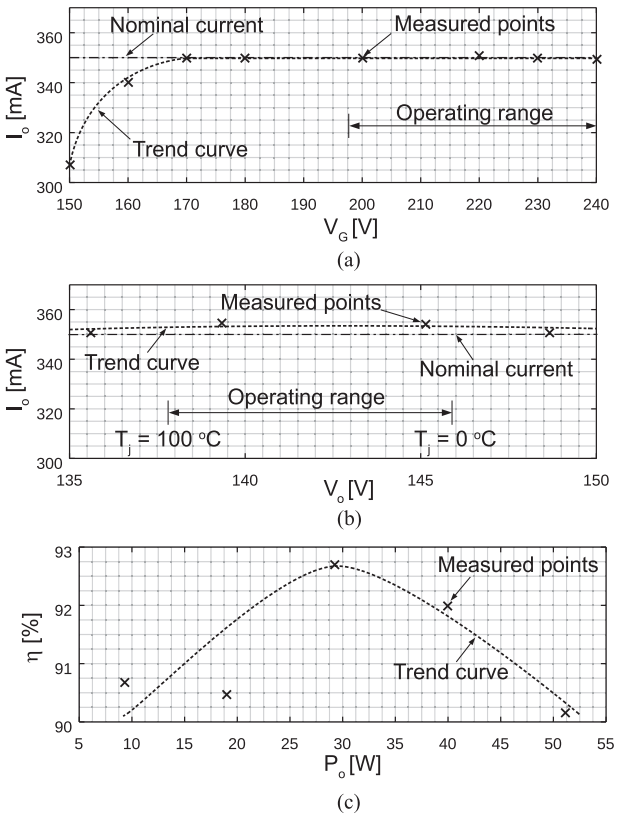

Fig. 10. Behavior of the converter owing to variations of the input voltage, lamp voltage, and output power. (a) Output current regulation against input voltage. (b) Output current regulation against output voltage. (c) Efficiency with respect to output power (dimming levels).

the whole operating range, so that the system was able to deal with variations in the input voltage, and also for changes in the output voltage, which can occur owing to alterations in the LED junction temperature, as explained in Section III.

Fig. 10(c) presents the efficiency of the converter owing to load variations. As can be seen, the maximum efficiency occurs

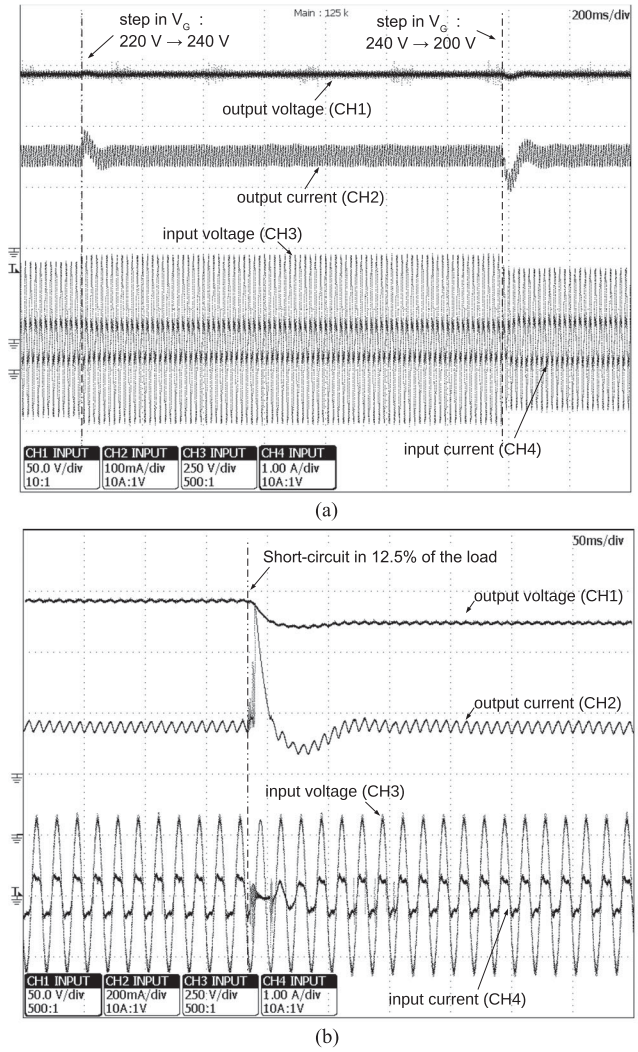

Fig. 11. Dynamic behavior of the converter upon steps of the input voltage (a) and the load (b). Output voltage (CH1: 50 V/div), output current [CH2: 100 mA/div in (a)—200 mA/div in (b)], input voltage (CH3: 250 V/div), and input current (1 A/div). Horizontal scale: 200 ms/div in (a) and 50 ms/div in (b).

when the load is about 60% reaching 92.7% and decreases for higher power levels.

Finally, Fig. 11 shows the dynamic performance of the converter during steps of the input voltage and the load. In Fig. 11(a), two steps in the input voltage were carried out: from $V_G = 220$ V to $V_G = 240$ V and after from $V_G = 240$ V to $V_G = 200$ V. As can be seen, in both the cases the steady-state error of the average output current was approximately null, indicating the proper operation of the compensator $C_{\rm av}$. On the other hand, the dynamic behavior of the converter for a short circuit of two modules (12.5% of the load) can be observed in Fig. 11(b). In this case, the control system also was able to deal with the load variation and ensured null-steady state error. It is important to highlight that when part of the load was short circuited, the excess of energy stored in the output capacitor caused a current overshoot. Nevertheless, it is possible to see in Fig. 11(b) that the input current decreases to zero in less than a half line cycle, indicating the quick action of the control system.

V. Conclusion

This paper presented the investigation of the ARCT applied to an offline flyback-based LED driver. The theoretical analysis described the circuit operation under the modulation of the duty cycle. Furthermore, an application example was also detailed, highlighting the sizing of the passive elements based on design abacuses and the calculation of the control system. Experimental results verified the theoretical analysis, showing that the ARCT allowed for a capacitance reduction of 24.2% when compared with the conventional approach. The experiments also showed that the circuit presents a good performance in terms of current regulation and dynamic response.

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