Digital Implementation of Adaptive Synchronous Rectifier (SR) Driving Scheme for High-Frequency *LLC* Converters With Microcontroller

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***Abstract*—Synchronous rectifiers (SRs) are important for high-output-current *LLC* converters in order to reduce the secondary conduction loss. Conventional SR driving schemes are not suitable for high-frequency *LLC* converters: the analog driving schemes will lose a large portion of duty cycle due to SR parasitic inductance; and the digital driving schemes will require a much higher cost digital controllers in high-frequency operation. In this paper, a digital implementation of adaptive SR driving scheme for high-frequency *LLC* converters with cost-effective microcontroller is proposed. The proposed SR driving scheme senses SR drain–source voltage in order to detect body diode conduction, and tune the SR on-time every several switching cycles using ripple (asynchronous) counter to minimize body diode conduction. The proposed digital implementation has a simple control scheme, requires only low-cost digital controllers and minimizes controller resources utilization. More importantly, to cooperate with the closed-loop control, adaptive SR driving and closed-loop control are executed synchronously and SR on-time is modified accordingly during fast transient response to guarantee safe operation. With these techniques, the proposed adaptive SR driving can be embedded into the digital controllers with little extra cost. Experimental results are demonstrated on a 500-kHz 1-kW 400 V/12 V *LLC* converter with a 60-MHz microcontroller and a ripple counter.**

***Index Terms*—Digital control, *LLC* converter, synchronous rectification, transient response.**

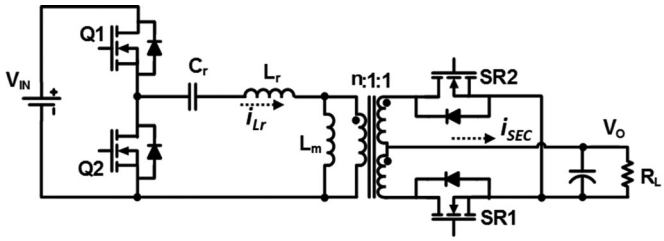

Fig. 1. Topology of the *LLC* converters.

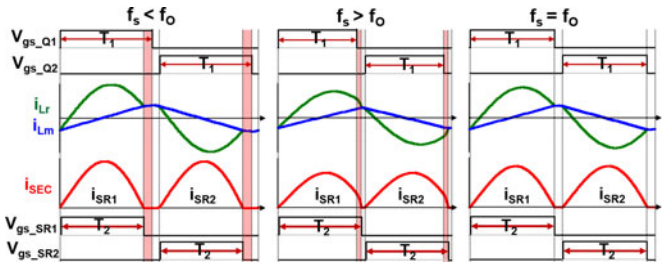

Fig. 2. Key waveforms of desired SR driving signal under different f_S with a heavy load.

I. Introduction

THE *LLC* resonant converter, as shown in Fig. 1, has been widely used as a dc–dc converter due to its high efficiency and hold-up capability [1], [2]. With the property of zero-voltage switching (ZVS) for the primary switches and zero-current switching (ZCS) for the secondary synchronous rectifiers (SRs), using *LLC* converters can also reduce electromagnetic interference [3]. With the fast development of the information technology (IT), the demand for higher efficiency keeps growing [4], [5]. Since most of the IT applications require the dc–dc converters to provide a low-voltage high-current output, the diode rectifiers will induce very large conduction loss. The SRs are critical for the *LLC* converters to improve the efficiency by tremendously reducing the conduction loss of the diode rectifiers. High-frequency *LLC* converters have become more popular in recent years due to their high-power density and integrated magnetics, which reduces the total cost [6], [7]. With the fast development of wideband gap devices and novel magnetic materials, the trend of raising the switching frequency f_S will continue. *LLC* converters capable of MHz-level operation with gallium nitride (GaN) devices have been designed for different applications [8]–[12], and these demonstrate significantly improved power density.

However, the SR driving scheme is quite challenging due to the discrepancy between the primary driving signal and the SR driving signal, especially under high f_S. Key waveforms of desired SR driving signal under different f_S with a heavy load are shown in Fig. 2, including Q1 gate signal $V_{\text{gs\_Q1}}$, Q2 gate signal $V_{\text{gs\_Q2}}$, resonant current i_{Lr}, magnetizing current i_{Lm}, transformer secondary current i_{SEC}, SR1 gate signal $V_{\text{gs\_SR1}}$, and SR2 gate signal $V_{\text{gs\_SR2}}$. If f_S is below the resonant frequency f_O, the SR is turned OFF earlier than the primary switch; if f_S is above f_O, the SR is turned OFF slightly later than the primary switch; and if f_S is equal to f_O, the SR is turned

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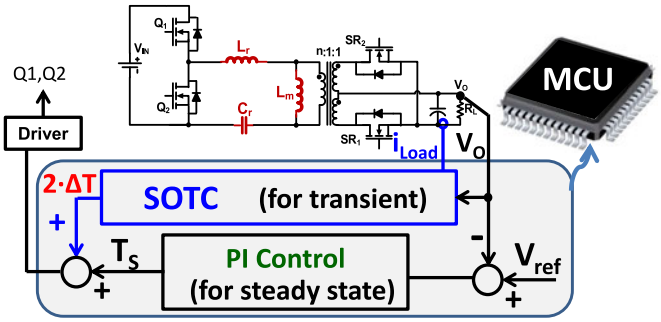

Fig. 3. Control scheme of SOTC with MCU implementation.

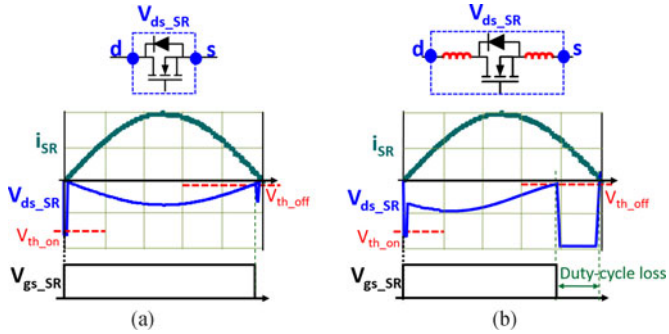

Fig. 4. Waveforms of smart IC based SR driving. (a) Without parasitic inductance. (b) With parasitic inductance.

OFF same as the primary switch. Besides, T_2 is also dependent on the load condition. So, the primary driving signal cannot be applied directly to the SRs. In addition, deviation from the desired SR driving will cause efficiency drop due to a large forward conduction voltage in the body diode. This problem becomes more severe at high f_S since a small deviation occupies a large portion of the duty cycle.

Many efforts have been made on the SR driving schemes. Current sensing-based SR driving schemes, although accurate, require additional current sensing components and induce large loss [13]–[15]. Most of the SR driving schemes nowadays are based on sensing the SR drain–source voltage V_{ds_SR}. Some of these SR driving schemes use an independent driving circuit [16]–[18], but the accuracy of these SR driving schemes is highly affected by the SR package, which becomes extremely severe for high-frequency *LLC* converters [19]. Other SR driving schemes employ the adaptive control concept to tune the SR driving signal adaptively to the desired situation. Cheng *et al.* [20] propose to use a linear compensator to generate the SR on-time, which is expensive and has a maximum on-time limitation. Feng *et al.* [21] propose to detect the body diode conduction just at the SR turn-off moment, and tune the SR on-time step-by-step to the vicinity of the desired situation, which requires expensive field-programmable gate array (FPGA) implementation. Recently, a commercial SR driving integrated circuit (IC) [22] was released, which communicates with the digital controller to optimize the SR on-time, and further improvements on this method have been made to prevent negative current in SRs [23], but this device is only dedicated to a specified digital controller [24].

Digital controllers are gradually taking the place of analog controllers in the control of *LLC* converters. Among the digital controllers, the cost-effective microcontrollers (MCUs) are preferred in industrial applications [25]–[27]. Since high-frequency *LLC* converters are gaining more popularity, it is meaningful to investigate the control of high-frequency *LLC* converters with low-cost MCUs. Recently, a lot of effort has been made on the control of the *LLC* converters with low-cost MCUs based on the concept of the simplified optimal trajectory control (SOTC) [28]–[34]. Different SOTC control functions have been integrated in a low-cost MCU and demonstrated on a 130-kHz *LLC* converter [29] with the control scheme shown in Fig. 3. Then, digital implementation of SOTC control for high-frequency *LLC* converters has been analyzed, including soft start-up and short-circuit protection [30], fast load transient response [31], and light load efficiency improvement with burst mode [32]. The adaptive SR driving, as an individual function, has been discussed in [33], but how to minimize controller resource utilization and handle the SR driving under fast transient response have not been investigated for high-frequency *LLC* converters.

In commercial power supply products, the SR driving function can be further integrated into the digital controller to reduce the system cost. The conventional SR driving schemes, requiring either additional circuitry or expensive smart IC, are not preferred due to the extra components and increased cost. There are several challenges to integrate the SR driving within the low-cost MCU for high-frequency *LLC* converters. First, the controller resources and CPU utilization for the SR driving must be minimized to spare space for the other control functions. Second, the SR driving must cooperate with the closed-loop control to guarantee safe operation during a fast transient response. Third, the additional component should be minimized to reduce the extra cost.

In this paper, Section II investigates the limitation of the previous adaptive SR driving schemes. Section III proposes the adaptive SR driving scheme for high-frequency *LLC* converters. Section IV analyzes how to combine the proposed adaptive SR driving scheme with the closed-loop control, specifically, integrating the SR driving with SOTC control into low-cost MCU. Section V presents the experimental results on a 500-kHz 1-kW 400 V/12 V *LLC* converter with a 60-MHz MCU. The conclusions are given in Section VI.

II. Investigation of SR Driving Schemes for *LLC* Converters

To figure out an SR driving scheme suitable for digital implementation, different SR driving schemes are investigated in this section. Most of the SR driving schemes nowadays are based on sensing V_{ds_SR}. The commercialized SR driving smart ICs can work as independent driving circuit at the secondary side and do not require primary control signals [16]–[18]. These smart ICs work in the following principle as shown in Fig. 4(a): at the beginning, the SR is in the off-state; when there is a body diode conduction, it results in a large forward voltage drop in V_{ds_SR}, which is compared with the turn-on threshold voltage V_{th_on}; if the V_{ds_SR} is larger than V_{th_on}, the SR driving IC turns ON the

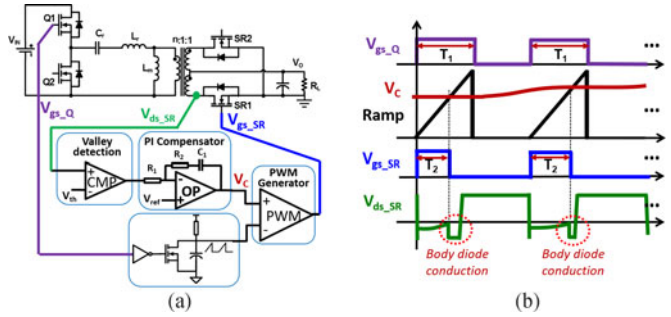

Fig. 5. Adaptive SR driving scheme using a linear compensator. (a) Control scheme. (b) Waveforms.

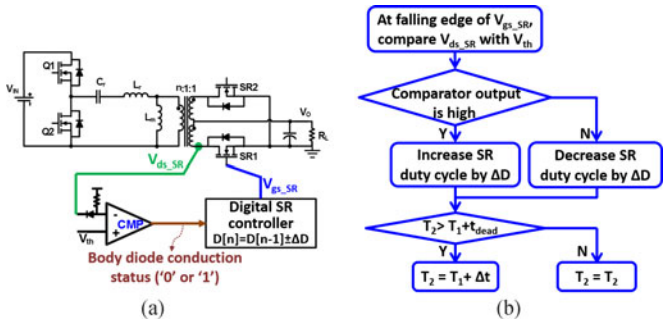

Fig. 6. Adaptive SR driving scheme using digital tuning. (a) Control scheme. (b) Control flowchart.

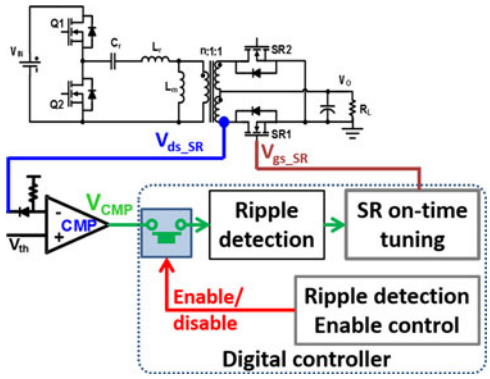

Fig. 7. Integrating adaptive SR driving in the low-cost digital controller.

SR; in the *LLC* converters, during the SR on-time, the current in SR i_{SR} will first increase and then decrease to zero; and as the current approaches zero, V_{ds_SR} also becomes very small, which is compared with the turn-off threshold voltage V_{th_off} to determine when to turn OFF the SR. However, the actual SR on-time is shorter than the expected value and there is a duty-cycle loss due to the inevitable package inductance of the SRs, as shown in Fig. 4(b). This problem is extremely severe in high-frequency applications since even a very small package inductance can induce a large phase leading in V_{ds_SR}. A compensation network can be connected to the sensed terminals to solve this problem [19], but it is very complex and also impacted by the tolerance of the compensation network.

Adaptive SR driving can solve the issue of an extra body diode conduction in a smart IC based SR driving when operating at high f_S by detecting the body diode conduction after SR turn-off [20]–[22]. The turn-on of the SR can be synchronized with the primary driving signal by adding a small constant delay, as shown in Fig. 2, however, the turn-off tuning mechanisms are different.

The control scheme and waveforms of the adaptive SR driving [20] are shown in Fig. 5. The V_{ds_SR} is detected and compared with a threshold voltage V_{th}. The output of the comparator is connected to the input of a linear compensator, whose output is then compared with a sawtooth waveform generated from primary driving signal to get the SR driving signal. If the body diode conduction is detected, the compensator output will increase, so as the SR on-time T_2. If no body diode conduction is detected, the compensator will decrease T_2 accordingly. There would be two major limitations if this SR driving scheme is integrated within the cost-effective digital controllers. The first limitation is that it requires a linear compensator, which would either require the additional circuit or occupy a lot of CPU resources. The second limitation is that since the negative input of the pulse width modulation (PWM) generator is the primary driving signal, T_2 cannot be large than the corresponding T_1, which is not suitable when f_S is above f_O under a heavy load condition.

The control scheme and flowchart of the adaptive SR driving using digital tuning [21] are shown in Fig. 6. V_{ds_SR} is sensed just at the falling edge of V_{gs_SR} and compared to V_{th}. The output of the comparator indicates if there is a body diode conduction, and the digital controller would increase or decrease the SR duty cycle by ΔD accordingly for the next switching cycle. Texas Instruments [22] uses similar adaptive SR driving concepts and integrates this function into an IC chip, but this IC is dedicated to digital controller UCD3138A and requires complex communication protocol between the digital controller and SR driving IC.

The limitation with these SR driving schemes is that they require complex algorithm and compare the V_{ds_SR} to V_{th} just at the falling edge of V_{gs_SR}; thus, the implementation of this function requires either an FPGA controller [21] or additional logic circuitry [22], which cannot be integrated within the cost-effective digital controllers. More importantly, how to integrate SR driving with a fast transient response has also not been addressed yet. Further efforts need to be spent on integrating adaptive SR driving into low-cost digital controllers. Furthermore, when applied to high-frequency *LLC* converters, tuning the SR on-time every switching cycle in the digital controller will greatly increase the CPU utilization and consume more auxiliary power. The following sections present how to solve these issues with a low-cost digital controller.

III. Proposed Adaptive SR Driving Scheme for High-Frequency *LLC* Converters

A. Integrating Adaptive SR Driving Into Low-Cost Digital Controllers

The adaptive SR driving scheme can be integrated within the digital controllers by using ripple detection, whose control scheme is shown in Fig. 7. The V_{ds_SR} is sensed and compared

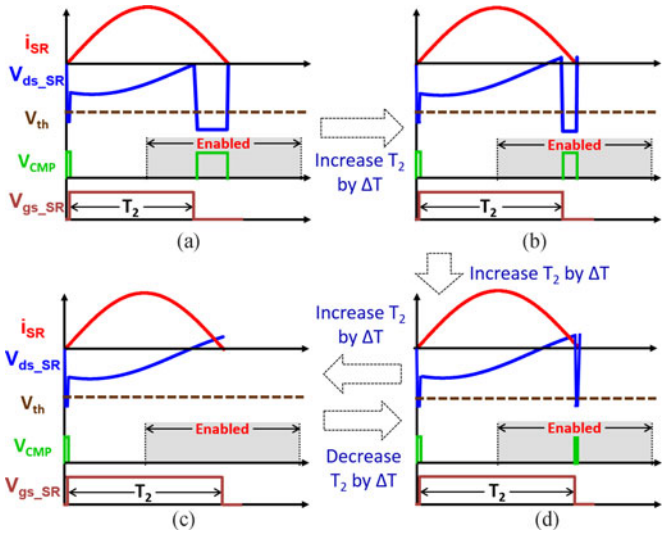

Fig. 8. Control mechanism of integrated adaptive SR driving schemes.

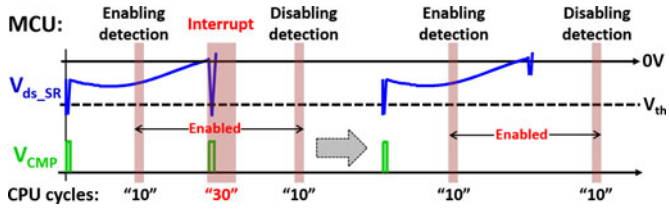

Fig. 9. CPU utilization with the integrated adaptive SR driving scheme.

with V_{th} to detect body diode conduction, and the output of the comparator V_{CMP} is connected to the ripple detection function of the digital controller, i.e., the external interrupt of the MCU, based on which the on-time of SR is tuned accordingly. Since the adaptive SR driving scheme is integrated within the digital controller, the primary driving signal can be used to synchronize the turn-on of SR and control the enable/disable of the ripple detection.

The control mechanism of the integrated adaptive SR driving is shown in Fig. 8. Since there is a small body diode conduction period at the SR turn-on moment, only the ripple at V_{CMP} in the shaded area will be detected by controlling the enable/disable of the ripple detection based on the primary driving signal. The ripple detection is enabled at the middle of the primary switch on-time, and disabled at the middle of the primary switch off-time, so that if there is body diode conduction, the ripple at comparator output can be detected. In Fig. 8, at the beginning, as shown in Fig. 8(a), there is large body diode conduction; the controller continues to increase T_2 by ΔT, which is the minimum resolution of the digital controller, as shown in Fig. 8(b) and (c); this process continues until no ripple at V_{CMP} in the shaded area is detected, as shown in Fig. 8(d); then, the controller decreases T_2 by ΔT and comes back to Fig. 8(c). In the steady state, the SR on-time will jitter between the condition with no body diode conduction in Fig. 8(d) and that with a very small body diode conduction in Fig. 8(c). It is optimal for the adaptive SR driving to jitter between these two conditions; otherwise, if the SR on-time stays in the condition with no body diode conduction, when f_S increases, the adaptive SR driving cannot reduce the SR on-time accordingly.

The CPU utilization can be estimated when integrating the adaptive SR driving into the digital controller. Take a 60-MHz MCU TMS320F28027 as an example for the following analysis, which is a popular low-cost MCU and widely used in telecom and server power supplies [26], [27]. It takes ten CPU cycles to enable or disable the ripple detection, and around 30 CPU cycles to modify SR on-time for the next switching cycle when there is ripple detected and the interrupt in the MCU is triggered, as shown in Fig. 9. So the total adds up to a maximum of 50 CPU cycles within one switching cycle to implement such an adaptive SR driving scheme. The CPU utilization for SR driving η_{SR} is calculated as follows:

$$m_{\text{total}} = \frac{f_{\text{clock}}}{f_s} \tag{1}$$

$$\eta_{\text{SR}} = \frac{m_{\text{SR}}}{m_{\text{total}}} \tag{2}$$

where f_{clock} is the clock frequency of the digital controller, m_{total} is the total CPU cycles within one switching cycle, and m_{SR} is the required CPU cycles for adaptive SR driving within one switching cycle, specifically, $m_{\text{SR}} \approx 50$ when integrating the SR driving scheme into TMS320F28027. To control a 100-kHz *LLC* converter with a 60-MHz MCU ($m_{\text{total}} = 600$), the adaptive SR driving takes around 8.3% CPU utilization. When using 8.3% CPU utilization for the SR driving, the digital controller still has enough resources for the closed-loop control and auxiliary functions.

However, when this method is applied to high-frequency *LLC* converters, the CPU utilization for the SR driving would increase dramatically. For example, if the SR driving is applied to a 500-kHz *LLC* converter with a 60-MHz MCU ($m_{\text{total}} = 120$), it would take 42% CPU utilization, which means that most of the time, the CPU is occupied by SR driving and has little spare time for the closed-loop control and auxiliary functions.

B. Proposed Adaptive SR Driving for High-Frequency LLC Converters

To achieve effective control performance for high-frequency *LLC* converters with the cost-effective digital controller, the control loop can be executed every several switching cycles. A similar concept has already been implemented for soft start-up and fast transient response [30], [31]. Specifically, to solve the challenge of the SR driving for high-frequency *LLC* converters, an adaptive SR driving scheme using a ripple counter is proposed in this paper. The control scheme is shown in Fig. 10. Compared with the method in Fig. 7, a ripple counter is added between the comparator and the digital controller, which can help the digital controller to tune the SR on-time every several switching cycles.

By using the ripple counter, the proposed method can tune the SR on-time every Nth switching cycle ($N = 2, 3, 4\ldots$). The turn-on time of the SRs is still synchronized with the primary switches, so there is always a very small duration of body diode conduction at the turn-on moment. The proposed method counts the ripples at V_{CMP} to determine if there is extra body diode

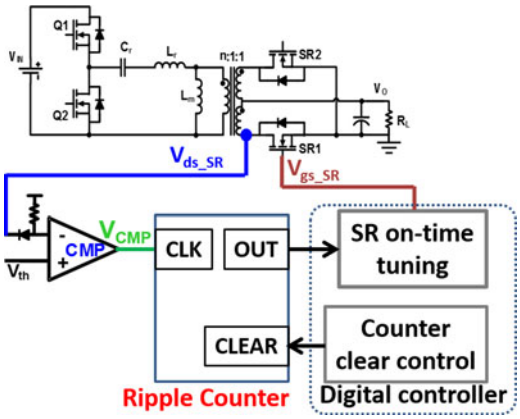

Fig. 10. Proposed integrated adaptive SR driving for high-frequency *LLC* converters.

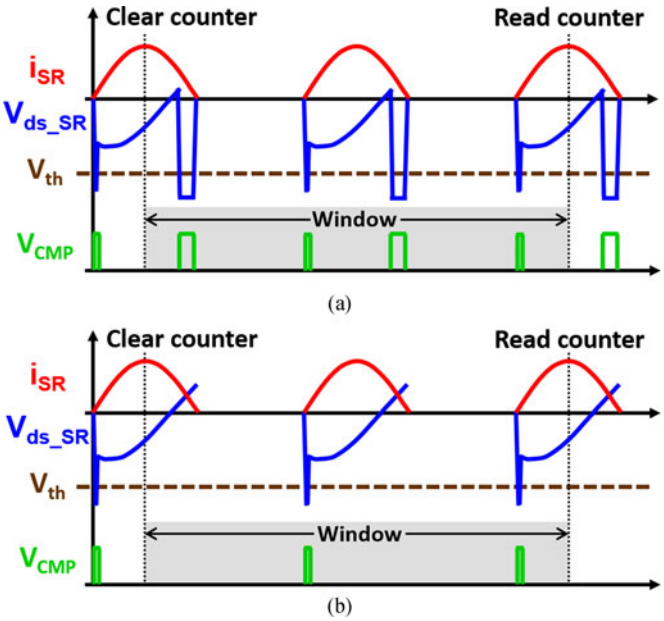

Fig. 11. Detecting body diode conduction every third switching cycle. (a) There is body diode conduction after SR turn-off. (b) No body diode conduction after SR turn-off.

conduction after the SR turn-off in the following principles: the controller clears the ripple counter in the first switching cycle after SR turn-on; then, the controller reads the ripple counter in the Nth switching cycle after SR turn-on. If the output is "$2 \cdot (N-1)$," it means that there is the body diode conduction after the SR turn-off. Otherwise, there is no body diode conduction. Fig. 11 is an example in which the SR on-time is tuned every third switching cycle.

An example of a tuning process for the proposed adaptive SR driving is shown in Fig. 12, in which the SR on-time is tuned every second switching cycle. At the beginning, there is a large body diode conduction after the SR turn-off, and the ripple counter indicates two ripples in the detection window. So, the controller keeps increasing the SR on-time. Every two switching cycles, the SR on-time is increased by ΔT, which continues until when the ripple counter indicates that there is only one ripple. Then, the controller decreases the SR on-time by ΔT. In the

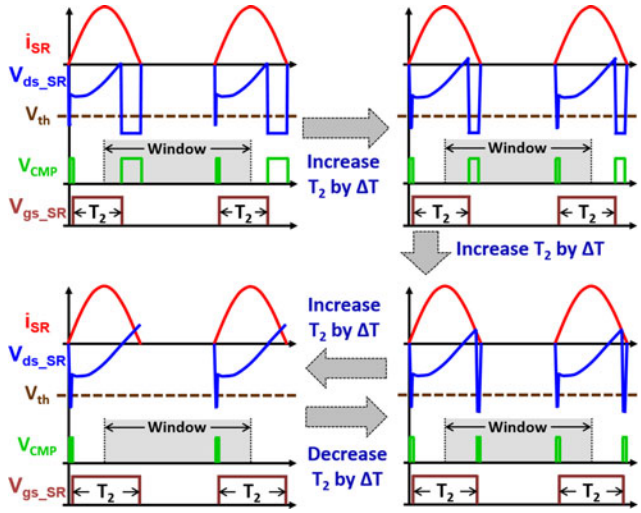

Fig. 12. Control mechanism of integrated adaptive SR driving scheme for high-frequency *LLC* converter.

next two switching cycles, there are two ripples again. Thus, the SR on-time is tuned step-by-step to eliminate the body diode conduction, and finally it is around the optimal point.

On the one hand, with the proposed adaptive SR driving method, the CPU utilization for high-frequency *LLC* converters can be reduced effectively by reducing the SR on-time tuning speed with minimum auxiliary circuits and components. On the other hand, by eliminating the external interrupt in the MCU with the ripple counter, it takes less than 20 CPU cycles to execute the proposed adaptive SR driving every digital control cycle, meaning $m_{\mathrm{SR}} < 20$ in this case. Reducing the control speed is quite a common practice when using low-cost digital controllers to control high-frequency converters. When tuning the SR on-time every Nth switching cycle ($N = 2, 3, 4 \ldots$), the total CPU cycles within one digital control cycle m_{total} become as follows:

$$m_{\mathrm{total}} = N \cdot \frac{f_{\mathrm{clock}}}{f_s}. \tag{3}$$

Compared with the method in Fig. 7, the proposed method for high-frequency *LLC* converters can increase m_{total} by N times and reduce m_{SR} from 50 to 20. When applying the proposed SR driving scheme to a 500-kHz *LLC* converter with a 60-MHz MCU by tuning the SR on-time every third switching cycle ($m_{\mathrm{total}} = 360$), the CPU utilization for SR driving is reduced to less than 6%, compared to 42% CPU utilization with the method in Fig. 7 by tuning the SR on-time every switching cycle. Furthermore, by reducing the SR on-time tuning speed, the SR driving control and the closed-loop control can be updated synchronously, and the SR on-time can be modified accordingly during fast transient response to guarantee safe operation. These transient response issues will be discussed in the next section.

IV. Integrating the Proposed Adaptive SR Driving With Fast Transient Response

In most *LLC* converters, the output voltage V_O regulation is obtained by frequency control. To achieve a high efficiency, the

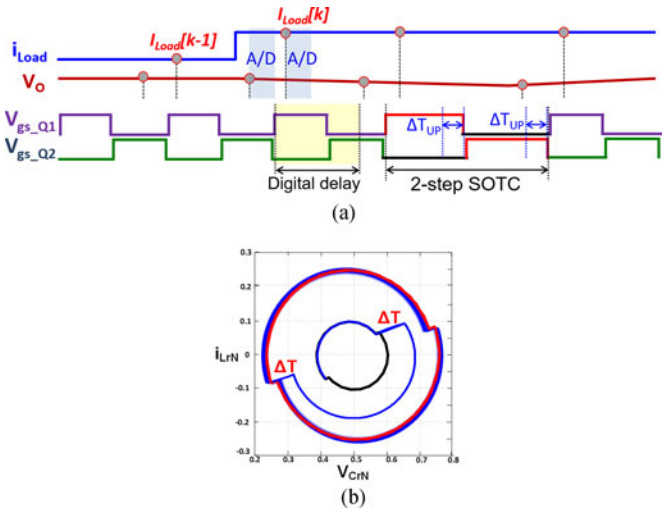

Fig. 13. Two-step SOTC for load step-up. (a) Time-domain response. (b) Trajectory.

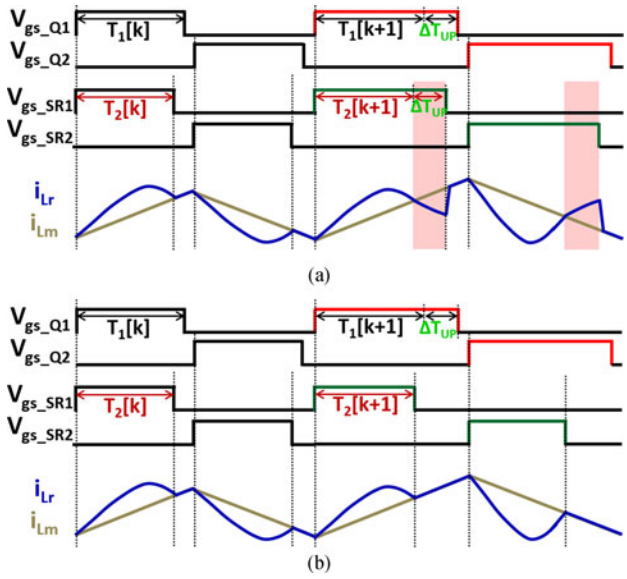

Fig. 14. Comparison of SR driving signals during load step-up. (a) SR on-time increases with primary on-time causing negative current in SR. (b) SR on-time remains the same (proposed method).

input voltage $V_{\rm IN}/V_O$ ratio is maintained in a small range so that the corresponding f_S is in the vicinity of f_O. Specifically for server applications, the input for the *LLC* converter is the output of power factor correction circuit, which is normally 380 V with less than 5% variation, and V_O for the *LLC* converter is fixed to 12 V. While during fast load transient, the f_S of the *LLC* converter is changed rapidly to reduce the overshoot/undershoot in V_O. Special attention needs to be paid to the SR driving control in these fast transient conditions to guarantee that the SR driving signals are proper. Among the control methods for *LLC* converters, SOTC in Fig. 3 can achieve nearly one-cycle response by sensing the load transient directly. Due to this fast transient response mechanism, the step response of f_S in the SOTC makes it the most difficult to handle the SR driving when combined with the SOTC control.

A. Adaptive SR Driving Executed Every Switching Cycle

The time-domain response of a two-step SOTC under load step-up is illustrated in Fig. 13(a) [31]. The controller requires at least one switching cycle digital delay to process the SOTC control after sensing the load transient. For the load step-up, the controller will increase the on-time of the primary switches by $\Delta T_{\rm UP}$ for the next switching cycle; and for the load step-down, the controller will decrease that by ΔT_D as expressed in the following:

$$\Delta T_{\rm UP} = \frac{L_M \cdot (I_{\rm Load}[k] - I_{\rm Load}[k-1])}{n \cdot V_{\rm IN}} \tag{4}$$

$$\Delta T_D = \left(1 - \sqrt{\frac{I_{\rm Load}[k]}{I_{\rm Load}[k-1]}}\right) \cdot \frac{T_O}{4} \tag{5}$$

where L_M is the magnetizing inductance, n is transformer primary to secondary turn ratio, T_O is the *LLC* resonant period, and $I_{\rm Load}[k]$ and $I_{\rm Load}[k-1]$ are sensed load currents in this switching cycle and previous switching cycle, respectively. For the following analysis of a two-step SOTC, the number k indicates the switching cycle immediately after the load transient, the numbers $k-1$ and $k+1$ indicate the switching cycle before and after that, respectively. The state trajectory during load step-up with SOTC is shown in Fig. 13(b) with the x-axis of the normalized resonant voltage $V_{\rm CrN}$ and the y-axis of the normalized resonant current $i_{\rm LrN}$. Initially, the converter runs at the light load condition, corresponding to the inner trajectory in the state plane. After the load step-up, SOTC will increase the width of the primary driving signal by $\Delta T_{\rm UP}$ to boost the resonant tank energy. Then, the linear regulator in the SOTC will eliminate the steady-state error for heavy load, corresponding to the outer trajectory in the state plane.

Under fast load transient, f_S may change very fast and the SR driving needs to be handled properly. When f_S suddenly decreases under load step-up, as shown in Fig. 14, the primary on-time increases from $T_1[k]$ to $T_1[k+1] + \Delta T_{\rm UP}$, where the change from $T_1[k]$ to $T_1[k+1]$ is determined by linear regulator based on V_O regulation and $\Delta T_{\rm UP}$ is determined by SOTC calculation based on sensed load current, as expressed in (4) and (5). In such a case, if the SR on-time is also increased from $T_2[k]$ to $T_2[k+1] + \Delta T_{\rm UP}$, as shown in Fig. 14(a), i_{Lr} would cross i_{Lm} as the shaded area and there would be a negative current going through SRs, inducing extra losses. Furthermore, if the SR conducts too much longer than it is supposed to, there would be ringing caused by resonance between Lr and parasitic, causing SR body diode to conduct again after SR turn-off [23]. To solve this issue, the SR on-time will not increase with the primary on-time in the propose method; instead, it will be determined only by the tuning process when the on-time of primary switches is increasing, as shown in Fig. 14(b). The proposed SR on-time T_2 after load step-up will be increased by ΔT if there is body diode conduction in current switching cycle and will be decreased by ΔT if not. T_2 is expressed as follows:

$$T_2 = T_2\ [k+1] = \begin{cases} T_2[k] + \Delta T, & \text{if } V_{\rm CMP} = 1 \\ T_2[k] - \Delta T, & \text{if } V_{\rm CMP} = 0 \end{cases}. \tag{6}$$

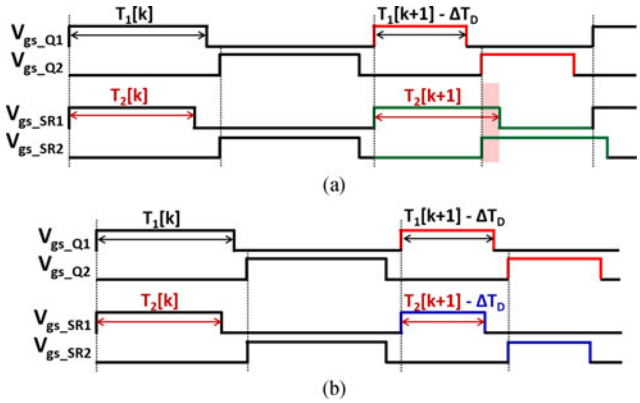

Fig. 15. Comparison of SR driving signals during load step-down. (a) SR on-time remains the same under the risk of potential shoot through. (b) SR on-time decreases with primary on-time (proposed method).

When f_S suddenly increases under load step-down, as shown in Fig. 15, the primary on-time increases from $T_1[k]$ to $T_1[k+1]-\Delta T_D$, in which the change from $T_1[k]$ to $T_1[k+1]$ is also determined by linear regulator based on V_O regulation and ΔT_D is determined by SOTC calculation based on load transient. In addition, the change of the SR on-time from $T_2[k]$ to $T_2[k+1]$ is determined by the tuning process and explained in (6). If there is no further modification and protection mechanism of SR on-time, there is a potential shoot-through condition, as shown in Fig. 15(a), and the shoot-through conditions are highlighted in the shaded area. To prevent shoot through, the proposed SR on-time T_2 is modified accordingly, as shown in Fig. 15(b), following the principle

$$T_2 = \begin{cases} T_2[k+1]-\Delta T_D, & \text{if load step-down} \\ T_2[k+1], & \text{if load step-up} \end{cases}. \quad (7)$$

B. Adaptive SR Driving Executed Every Several Switching Cycles

For a two-step SOTC implemented by MCU, there is a maximum f_S limitation caused by the digital delay. To increase the converter f_S while using a low-cost controller, multistep SOTC is proposed in [31] to accommodate the digital delay in several switching cycles. For the following analysis of a multistep SOTC, the number k indicates the digital control cycle immediately after the load transient; the numbers $k-1$ and $k+1$ indicate the digital control cycle before and after that, respectively. An example of a four-step SOTC under load step-up is shown in Fig. 16, in which the SOTC control loop is executed every second switching cycle, and the transition from light load to heavy load in state-trajectory is achieved in four steps, as shown in Fig. 16(b). The $\Delta T_{\rm UP}$ for load step-up and ΔT_D for load step-down in a multistep SOTC are expressed below, assuming the SOTC control loop is executed every Nth switching cycle ($N = 2, 3, 4\ldots$)

$$\Delta T_{\rm UP} = \frac{L_M \cdot (I_{\rm Load}[k] - I_{\rm Load}[k-1])}{N \cdot n \cdot V_{\rm IN}} \quad (8)$$

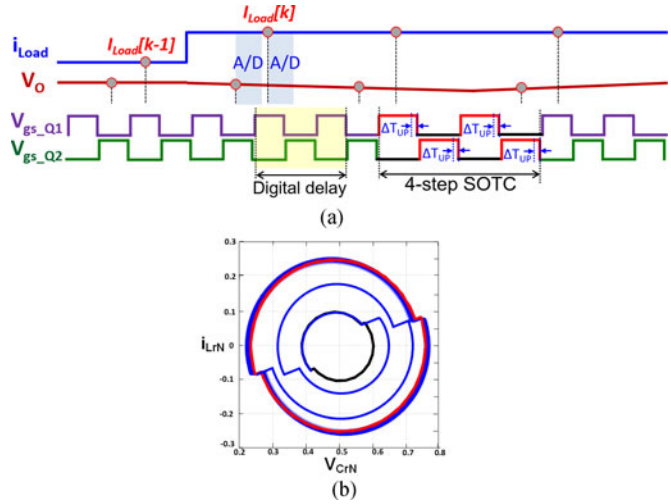

Fig. 16. Four-step SOTC for load step-up. (a) Time-domain response. (b) Trajectory.

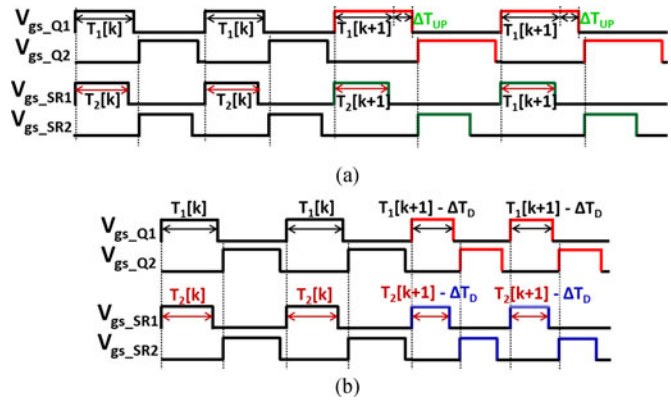

Fig. 17. Integrating SR driving with four-step SOTC. (a) Load step-up. (b) Load step-down.

$$\Delta T_D = \left(1 - \sqrt[2N]{\frac{I_{\rm Load}[k]}{I_{\rm Load}[k-1]}}\right) \cdot \frac{T_O}{4}. \quad (9)$$

The proposed adaptive SR driving can be integrated with a multistep SOTC by synchronizing the adaptive SR driving with the SOTC control, meaning that the SR on-time and primary f_S are updated simultaneously. During load transient response, the SR on-time is modified according to (6) and (7). An example is shown in Fig. 17, in which the SR on-time and primary f_S are updated every second switching cycle.

Based on the aforementioned techniques, the proposed adaptive SR driving can be integrated with closed-loop control for high-frequency *LLC* converters. For a given MCU, the number of required CPU cycles for closed-loop control $m_{\rm Control}$ and that for adaptive SR driving $m_{\rm SR}$ is given. Take TI's MCUs as an example, to include the control and protection functions, $m_{\rm Control} \approx 200$ in this case. As analyzed in Section III, $m_{\rm SR} \approx 50$ without ripple counter when PWM is updated every switching cycle, and $m_{\rm SR} \approx 20$ with ripple counter when

TABLE I
COMPARISON OF MCUS FOR 500-KHZ *LLC* CONVERTER

MICROCONTROLLER	F28027	F28069	F28345
Clock frequency	60 MHz	90 MHz	200 MHz
Price	$3.05 | 1 ku	$8.69 | 1 ku	$14.45 | 1 ku
PWM update speed	Every 3rd cycle	Every 2nd cycle	Every cycle
Total CPU utilization	61%	61%	63%
SR CPU utilization	5.6%	5.6%	13%

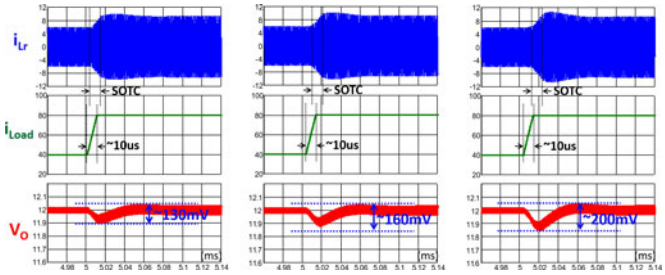

Fig. 18. Simulation of SOTC for load transient under different PWM update speed. (a) Two-step SOTC. (b) Four-step SOTC. (c) Six-step SOTC.

PWM is updated second switching cycle or slower. The total CPU utilization η_{Total} can be calculated as follows:

$$\eta_{\text{Total}} = \frac{m_{\text{Control}} + m_{\text{SR}}}{m_{\text{total}}} = \frac{m_{\text{Control}} + m_{\text{SR}}}{N \cdot f_{\text{clock}}/f_s}. \quad (10)$$

Although there are options to execute the control loop every Nth switching cycle ($N = 1, 2, 3\ldots$), N should be minimized to improve the transient response under the restriction of $\eta_{\text{Total}} < 1$ for all steady-state conditions. It is worth noting that η_{Total} should have enough margins since *LLC* converter is variable frequency control. Taking 500-kHz *LLC* converter as an example, three MCUs from TI are compared in Table I.

Increasing the PWM update speed will of course increase the transient response performance, but how far we can increase this is limited by the digital controller. Using a higher performance controller can overcome this limitation, but the cost increases significantly with a higher clock frequency, as summarized in Table I. Most server power supplies still use the low-cost MCU [26], [27] due to the concern of cost. Fig. 18 provides a simulation comparison of transient response among two-step SOTC, four-step SOTC, and six-step SOTC under 50%–100% load step-up within 10 μs. This is mostly considered to be a tradeoff between the cost and transient performance, and if cost is the highest priority, six-step SOTC should be chosen so that the controller cost remains the same as the traditional designs while the switching frequency for power stage is increased a lot to get the benefit of higher power density and lower cost for magnetic components.

V. EXPERIMENTAL RESULTS

The proposed adaptive SR driving scheme is verified on a 1-kW 400 V/12 V 500-kHz *LLC* converter, whose specifications are shown in Table II. The 500-kHz *LLC* converter is designed based on the matrix transformers for the *LLC* converters [9] and

TABLE II
SPECIFICATIONS OF 1-KW 500-KHZ *LLC* CONVERTER

COMPONENT	PARAMETERS
Resonant frequency f_O	500 kHz
Dead time	180 ns
Transformer turns ratio	16:1
Primary devices	IPW60R099P6
Secondary devices	BSC010N04LS
Primary driver	ADuM4223
Secondary drivers	FAN3122
Resonant capacitor *Cr*	22 nF
Resonant inductance *Lr*	4.5 μH
Magnetizing inductance *Lm*	21.6 μH
Output capacitance	3 mF
Comparator for SR driving	MAX9140

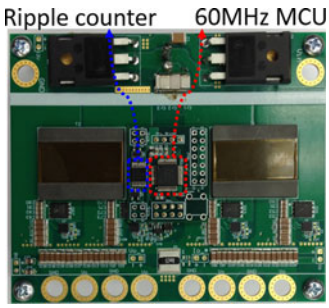

Fig. 19. 1-kW 500-kHz *LLC* converter with 60-MHz MCU.

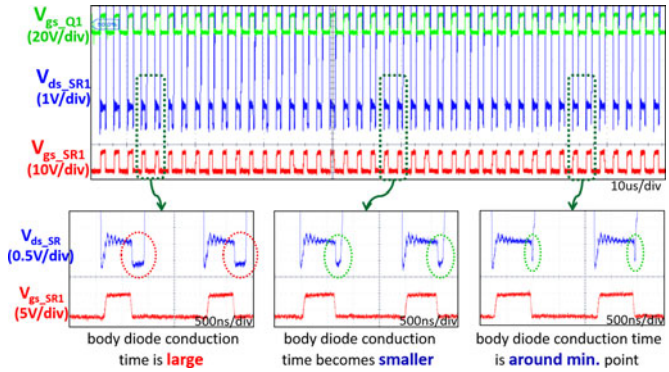

Fig. 20. Tuning process of proposed SR driving.

has a power density of 200 W/in^3. The prototype of the *LLC* converter is shown in Fig. 19, with a ripple counter SN74LV393A and a 60-MHz MCU TMS320F28027, which offers a resolution ΔT of 16.7 ns for SR on-time. The PWM for the primary switches and SRs is updated every third switching cycle.

The tuning process of the proposed adaptive SR driving scheme on the 500-kHz *LLC* converter is shown in Fig. 20. The initial SR on-time is relatively small, and the body diode conduction time is large. The proposed adaptive SR driving tunes the SR on-time step-by-step until finally the body diode conduction is around the minimum point.

Experimental results of the proposed adaptive SR driving under load step-up from 40 to 70 A are shown in Fig. 21. The envelop of i_{Lr} increases from light load condition to heavy

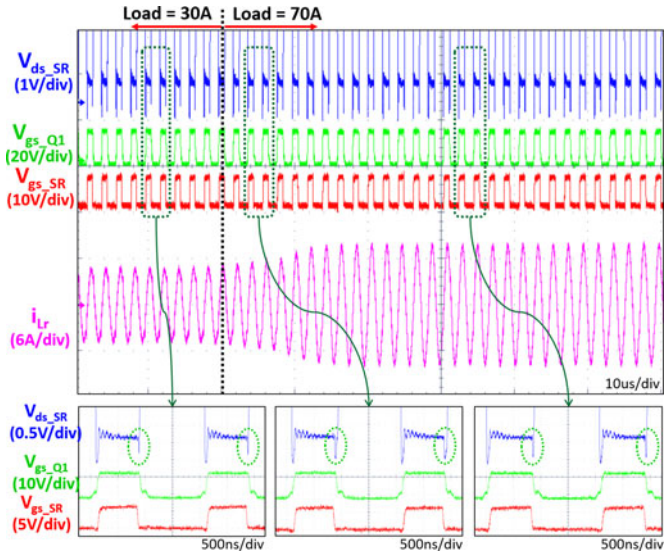

Fig. 21. Proposed SR driving during load step-up.

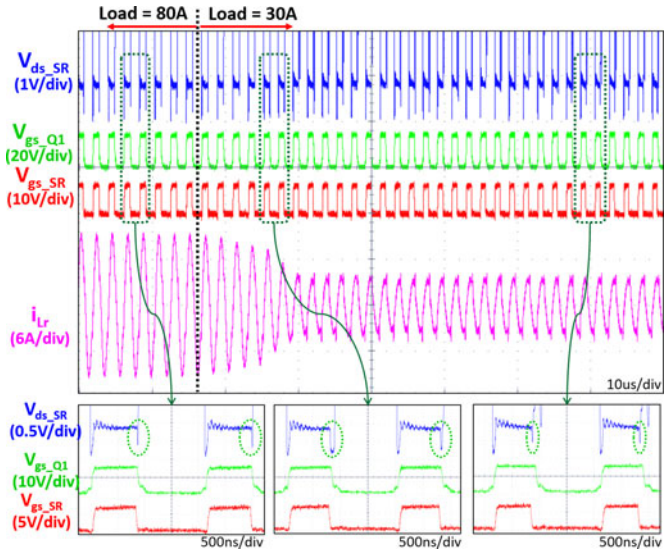

Fig. 22. Proposed SR driving during load step-down.

load condition very fast with SOTC control; the SR body-diode conduction before the load transient is around the minimum, increases slightly during the transient, and converges to the minimum immediately after the transient.

Experimental results of the proposed adaptive SR driving under load step-down from 80 to 30 A are shown in Fig. 22. The envelop of i_{Lr} decreases from heavy load condition to light load condition very fast with SOTC control, and the SR on-time approaches the optimal very fast after the transient.

The efficiency curve of the 500-kHz *LLC* converter with and without the proposed adaptive SR driving scheme is shown in Fig. 23. The proposed adaptive SR driving can improve efficiency by around 0.3%. The utilization of MCU resources is shown in Fig. 24. All the control functions, including closed-loop control [31], start-up and short-circuit protection [30], burst mode [32], and proposed SR driving, take around 3.5 k RAM

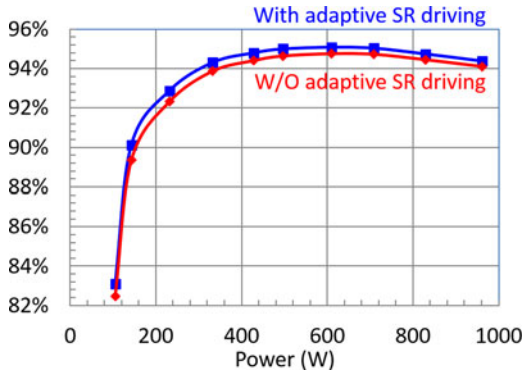

Fig. 23. Efficiency.

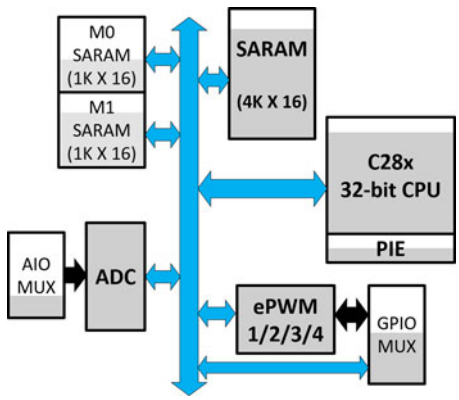

Fig. 24. Utilization of MCU resources.

space. The control loop is executed every third switching cycle and the maximum CPU utilization is around 90%, which happens during start-up and burst mode. The controller only needs to sense V_O and the load current. The ePWM1 module is used to drive the primary switches. The ePWM2 module is used for the start of conversion of the analog-to-digital converter and the ePWM3/4 modules are used to drive the SRs. Four general-purpose input/outputs are needed for the proposed adaptive SR driving control, two of which are used to clear the ripple counter and the other two are used to read the output of the ripple counter.

Achieving soft start-up has always been challenging for *LLC* converters due to severe stresses in the resonant tank. To limit these stresses, f_S has to be increased a lot, which increases CPU utilization to a very high level that the controller does not have enough resources for adaptive SR driving. But on the other hand, it is not necessary to enable adaptive SR driving during start-up since start-up is a short period of time and losing some duty cycle in the SR gate signals does not cause thermal issues. When integrating the proposed adaptive SR with the soft start-up method in [30], the SR on-time is kept slightly larger than that of the primary switches at the beginning of start-up, and kept the same as that of the primary switches during the latter part of start-up, while adaptive SR driving is enabled immediately after the start-up. Detailed waveforms of SRs during start-up are shown in Fig. 25.

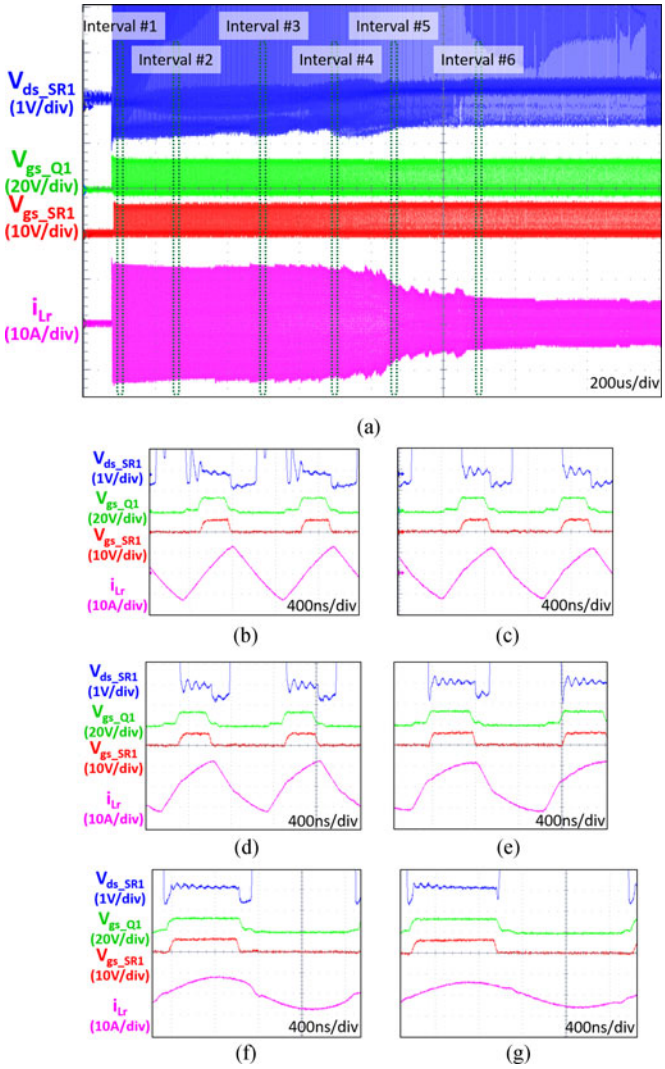

Fig. 25. Controlling SR on-time same as primary switches during soft start-up. (a) Whole start-up waveforms. (b) Interval #1: $f_S = 1.07$ MHz. (c) Interval #2: $f_S = 1.03$ MHz. (d) Interval #3: $f_S = 1.00$ MHz. (e) Interval #4: $f_S = 806$ kHz. (f) Interval #5: $f_S = 568$ kHz. (g) Interval #6: $f_S = 492$ kHz.

VI. Conclusion

SRs are important for high-output-current *LLC* converters in order to reduce the secondary conduction loss. Different SR driving schemes are investigated, and their limitations and digital implementation are discussed in detail in this paper. The adaptive SR driving is suitable to be integrated with a closed-loop control into a digital controller, but it will require a much higher cost digital controllers when applied to high-frequency *LLC* converters. To solve this challenge, the adaptive SR driving based on the ripple detection is proposed to integrate the SR driving into a low-cost digital controller without auxiliary circuits; then it is proposed to extend this method to high-frequency *LLC* converters by adding a ripple counter. By tuning the SR on-time every several switching cycles, the proposed method can effectively reduce the cost of auxiliary circuit and reduce the CPU utilization for SR driving, and thus be implemented by the low-cost digital controllers. Different adaptive SR driving methods are summarized and compared in Table III to demonstrate the benefit with the proposed adaptive SR driving method. Furthermore, since some MCUs have internal ripple counters function, the ripple counter may be eliminated to further reduce the cost.

TABLE III
Comparison of Adaptive SR Driving Methods

Methods	Major components	Requirement for controller
Smart SR driving IC [16]–[18]	Driving IC	None
SR driving using compensator [20]	Operational amplifier, comparator ×2	General-purpose MCU, low CPU utilization
SR driving for FPGA controller [21]	Comparator	High-performance FPGA
SR driving for UCD3138A [22]	UCD7138	Dedicated to Controller UCD3138A
Proposed SR driving for MCU	Comparator, counter (optional)	General-purpose MCU, low CPU utilization

A very important issue for adaptive SR driving is how to cooperate with the closed-loop control during fast transient response to guarantee that the SR driving signals are in safe conditions. This paper discusses the proper response of SR driving when embedded into a closed-loop control during a fast transient response. By synchronizing the PWM update of an adaptive SR and the closed-loop control, guidelines on how to modify the SR on-time accordingly are provided in this paper. The proposed method is verified on a 1-kW 500-kHz 400 V/12 V *LLC* converter with a 60-MHz MCU and a ripple counter. Compared with the other SR driving schemes, the proposed method is suitable to be embedded into digital controller, while at the same time, minimizing the CPU utilization and extra components.

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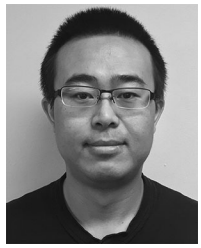

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