Development of DC to Single-Phase AC Voltage Source Inverter With Active Power Decoupling Based on Flying Capacitor DC/DC Converter

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***Abstract*—In the present, a power decoupling method without additional component is proposed for a dc to single-phase ac converter, which consists of a flying capacitor dc/dc converter (FCC) and the voltage source inverter (VSI). In particular, a small flying capacitor in the FCC is used for both a boost operation and a double-line-frequency power ripple reduction. Thus, the dc-link capacitor value can be minimized in order to avoid the use of a large electrolytic capacitor. In addition, component design, of, e.g., the boost inductor and the flying capacitor, is clarified when the proposed control is applied. Experiments were carried out using a 1.5-kW prototype in order to verify the validity of the proposed control. The experimental results revealed that the use of the proposed control reduced the dc-link voltage ripple by 74.5%, and the total harmonic distortion (THD) of the inverter output current was less than 5%. Moreover, a maximum system efficiency of 95.4% was achieved at a load of 1.1 kW. Finally, the high power density design is evaluated by the Pareto front optimization. The power densities of three power decoupling topologies, such as a boost topology, a buck topology, and the proposed topology are compared. As a result, the proposed topology achieves the highest power density (5.3 kW/dm^3) among the topologies considered herein.**

***Index Terms*—Active power decoupling, flying capacitor dc/dc converter (FCC), photovoltaic (PV) system, power density design.**

I. Introduction

In RECENT years, photovoltaic (PV) systems have been actively researched as a sustainable power solution. As a result, the world global market installation reached a record high of 228 GW in 2015 [1]. In order to use the generated power by PV panels, power converter systems (PCSs) are used to connect the PV system to the single-phase ac grid. These PCSs require the following capabilities: high efficiency power conversion; "plug and play" operation; maintenance free; and small packaging design.

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In order to fulfill these capabilities, two-stage power conversion using a dc/dc converter and a voltage source inverter (VSI) is generally used due to its simple configuration. Furthermore, multilevel converters, such as neutral point clamped converters or flying-capacitor dc/dc converters (FCCs), have been used in two-stage power conversion due to advantages such as high efficiency and high power density. These advantages are obtained by using a low on-resistance switching power device owing to the use of low-voltage-rating devices in the multilevel topology. Meanwhile, the inductor volume can also be minimized because the harmonic components of the inductor voltage can be reduced. In the FCC converter topology, the switched capacitor converter (SCC) is the popular configuration [2]–[3]. SCC can achieve the boost-up operation without large inductor. However, the inrush current on dc side occurs due to the flying capacitor. In order to solve this problem, the SCC with the small inductor is considered in [4]. The SCC with small inductor can reduce the inrush current in comparison with the conventional SCC. In addition, a high boost ratio can be achieved by small inductor and flying capacitor.

On the other hand, double-line-frequency power ripple occurs in the dc side due to the single-phase ac grid. This power ripple leads to a decrease in a performance of the maximum power point tracking (MPPT). Therefore, a bulky electrolytic capacitor is usually required in the dc-link in order to absorb the power ripple: i.e., a passive power decoupling method is used. However, the electrolytic capacitor limits the life-time of the power converter according to the Arrhenius law.

In order to solve this problem, active power decoupling methods have been energetically studied [5]–[15]. The active power decoupling is realized through the addition of switching devices and small passive energy buffer. Active power decoupling methods can reduce the capacitance required for power ripple compensation, which enables the use of film capacitors or ceramic capacitors instead of an electrolytic capacitor. Generally, the active power decoupling technique can be categorized into two types: the power decoupling technique based on parallel connection and series connection, where an auxiliary power decoupling circuit is connected to the dc link or ac side. A topological review of these power decoupling techniques has been presented in [16]. In [16], these conventional techniques can reduce the capacitance for power decoupling. However, it is also reported that the active power decoupling methods based on

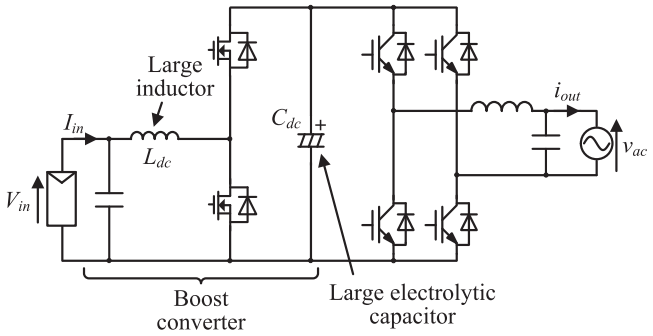

Fig. 1. DC to single-phase ac grid-connected converter with typical boost converter.

series or parallel connection worsens the converter efficiency due to the loss from the additional component [17]. Therefore, the achievement of active power decoupling capability without the need for an additional component is a key technique in realizing high efficiency and high power density [18].

This paper proposes a novel active power decoupling method based on the FCC. The original contribution of the present paper is that the active power decoupling control is achieved using a typical dc/dc converter without any additional components in order to reduce the volume, cost, and converter loss. In the paper, a multilevel dc/dc converter that has capacitive storage is focused. Originally, the FCC has a small flying capacitor in order to achieve a high boost ratio. The proposed control uses this capacitor for both boost operation and double-line-frequency power ripple compensation, i.e., active power decoupling. As a result, the dc-link capacitor value can be minimized. In addition, the advantages of the multi-level converter is also utilized in the proposed converter. Thus, the conduction losses and the inductor volume are reduced in comparison with the typical boost converter. However, the active power decoupling control decays the PV input current control performance because the voltage fluctuation of the flying capacitor disturbs the input current control. Therefore, this disturbance is compensated by the proposed input current control.

The remainder of the paper is organized as follows. In Section II, the configuration of the proposed converter is explained. In Section III, the proposed active power decoupling control is described. In Section IV, the component design of the proposed converter is explained, and the fundamental operation is then demonstrated experimentally. In this section, high efficiency design is discussed based on converter loss analysis. In Section V, the high power density condition is evaluated with the Pareto front optimization when the switching frequency is changed.

II. Circuit Configuration

A. Two-Stage DC to Single-Phase AC Grid-Connected Converter With Typical Boost Converter

Fig. 1 shows the dc to single-phase ac grid-connected converter with a typical boost converter. The boost converter boosts the PV input voltage above the peak value of the grid voltage,

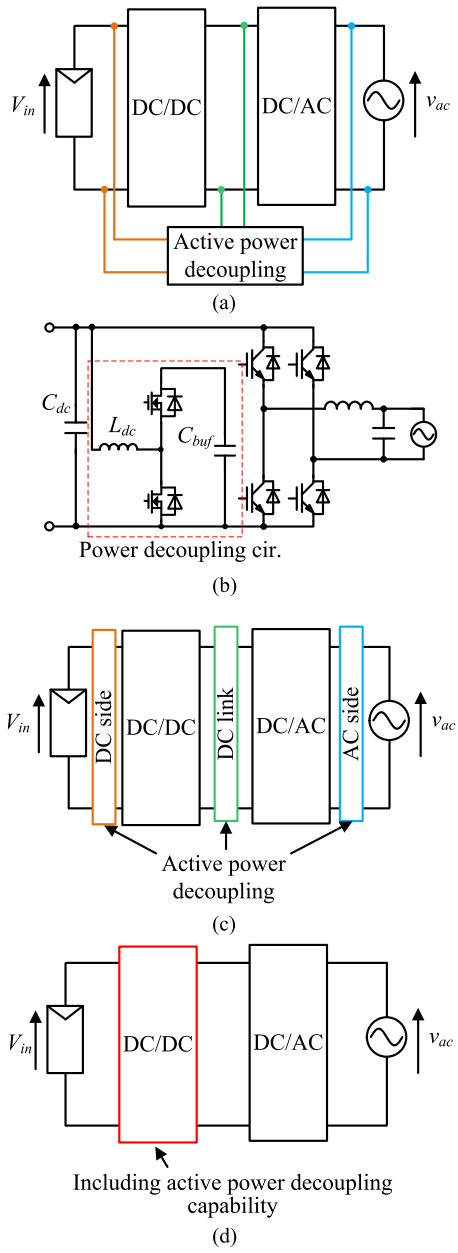

Fig. 2. Active power decoupling approaches. (a) Parallel-connected topology. (b) Conventional power decoupling circuit in parallel connection. (c) Series-connected topology. (d) Proposed approach.

and the generated power is supplied to the single-phase grid by the VSI. In this case, a bulky electrolytic capacitor $C_{\rm dc}$ is required in the dc-link due to the double-line-frequency power ripple of the single-phase grid. In addition, a large dc inductor $L_{\rm dc}$ is used for the boost operation of the PV input voltage Vin. In addition, the electrolytic capacitor limits the life-time of a converter.

B. Electrolytic Capacitor-Less Converter With Active Power Decoupling Circuit

Fig. 2 shows the active power decoupling configuration for the electrolytic capacitor-less converter and the conventional

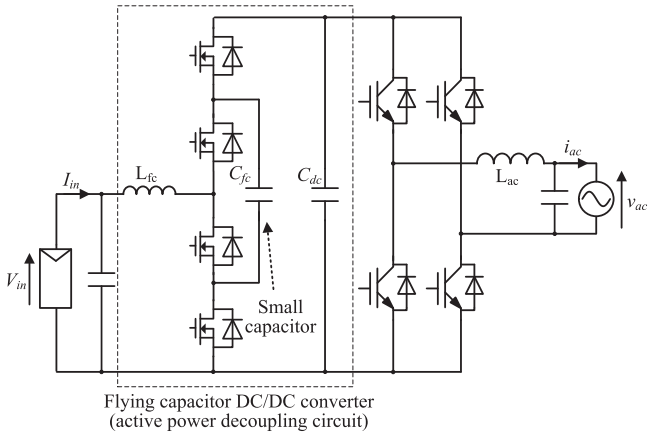

Fig. 3. DC to single-phase ac grid-connected converter with FCC. The proposed active power decoupling approach does not require additional component.

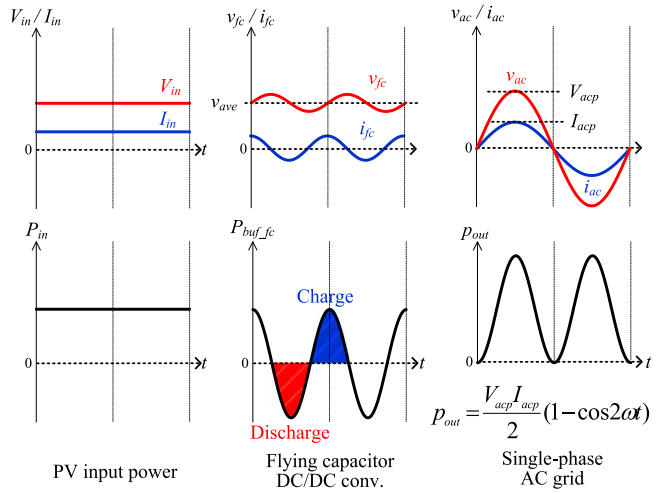

Fig. 4. Principle of the active power decoupling. Buffer power $P_{\mathrm{buf\_fc}}$ is charge and discharge by the flying capacitor C_{fc}. The $P_{\mathrm{buf\_fc}}$ is given by the mismatch in instantaneous power between input power P_{in} and output power P_{out}.

active power decoupling topologies considered herein [19]–[22]. Topologies can be categorized into two basic types, parallel-connected topologies and series-connected topologies, as shown in Fig. 2(a)–(c), respectively. In particular, the active power decoupling circuit is implemented in series or in parallel from the main power path. Consequently, the dc-link capacitance is drastically reduced, and a small film or ceramic capacitor can be used instead of the bulky electrolytic capacitor. However, the additional component increases the converter loss. In addition, the circuit configuration becomes complex, as shown in Fig. 2(b), and the control for the additional circuit must be modified for each conventional topology in order to achieve active power decoupling. In order to solve these problems, an approach in which the active power decoupling capability is implemented through the dc/dc converter is proposed, as shown in Fig. 2(d).

C. Proposed Active Power Decoupling Scheme for DC/AC Conversion

Fig. 3 describes the dc to single-phase ac grid-connected converter with the FCC, which is used in the proposed active power decoupling. In the proposed method, the small flying capacitor C_{fc} is used for both the boost operation of the PV input voltage V_{in} and the power decoupling capability. The FCC has many advantages compared to the typical boost converter.

First, the low voltage rating devices, which have low on-resistance, can be used because the drain-source voltage of each MOSFET can be reduced due to the increase in the number of levels, i.e., the characteristic of the multilevel topology. Therefore, low conduction loss can be achieved. In addition, the volume of the boost inductor L_{fc} is small compared to that of the typical boost converter. In the typical boost converter, the inductor voltage alternates between zero voltage and the dc-link voltage. On the other hand, the maximum inductor voltage of FCC converter can be reduced in comparison with typical boost converter because the inductor voltage is clamped to the flying capacitor voltage and the difference value between the dc-link voltage and the flying capacitor voltage. In other words, in the typical boost converter, the boost operation is achieved by only the boost inductor, whereas in the FCC converters (even when the proposed method is applied) the boost operation is achieved by both the boost inductor and the flying capacitor. As a result, the inductor current ripple in the FCC converters becomes low in comparison with the typical boost converter. Therefore, the inductance in the FCC converters can be minimized compared with the typical boost converter.

In the conventional control for the FCC, the flying capacitor voltage is maintained constant at the half of the dc-link voltage. In this paper, this flying capacitor voltage is fluctuated in order to realize active power decoupling. Consequently, when active power decoupling is achieved by the FCC, the dc-link capacitance can be reduced, and the bulky electrolytic capacitor is not required. The contribution of the proposed converter has a simple configuration and requires no additional components.

Note that, the decrease in the converter efficiency is an important technical issue in active power decoupling methods. The proposed active power decoupling approach has the potential to achieve low efficiency degradation as compared to conventional active power decoupling topologies. On the other hand, in the paper, a two-level VSI is used for grid connection. In order to achieve high efficiency and to reduce the use of the grid-connected inductor, a multilevel inverter topology can also be used. In this paper, only the FCC is focused.

III. Control Strategy of Proposed Converter

A. Principle of Active Power Decoupling

Fig. 4 shows the principle of power ripple compensation by fluctuating the flying capacitor voltage. When both the output voltage and current waveforms are sinusoidal, the instantaneous output power pout is expressed as

$$p_{\mathrm{out}} = \frac{V_{\mathrm{acp}} I_{\mathrm{acp}}}{2}(1 - \cos 2\omega t) \tag{1}$$

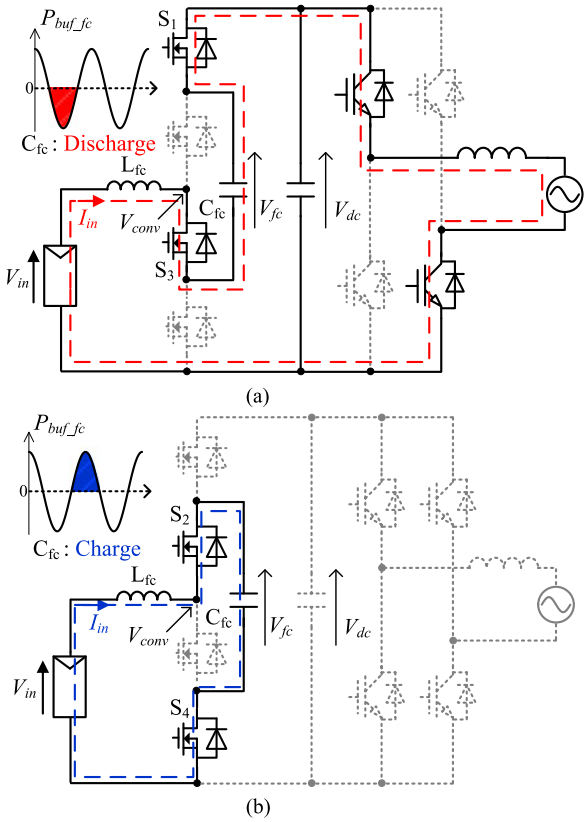

Fig. 5. Operation mode of the flying capacitor dc/dc converter for achieving active power decoupling. (a) Discharge mode (mode 1). (b) Charge mode (mode 2).

where, $V_{\rm acp}$ is the peak voltage, $I_{\rm acp}$ is the peak current, and ω is the angular frequency of the output voltage [23]. As shown in (1), the power ripple at twice the frequency of the single-phase power grid appears at the dc-link.

In order to absorb this power fluctuation, the instantaneous buffer power $p_{\rm buf}$ should be controlled by

$$p_{\rm buf} = \frac{1}{2} V_{\rm acp} I_{\rm acp} \cos 2\omega t \tag{2}$$

where, the polarity of $p_{\rm buf}$ is defined as positive when the flying capacitor $C_{\rm fc}$ discharges. Note that the active power of $C_{\rm fc}$ is zero. As a result of the power decoupling, the input power is matched to the output power. Thus, the relationship between the input and output power is expressed as follows:

$$p_{\rm in} = \frac{1}{2} V_{\rm acp} I_{\rm acp} = V_{\rm IN} I_{\rm IN}. \tag{3}$$

Fig. 5 shows the operation modes of the FCC. The proposed converter is operated in two modes. In mode 1, the flying capacitor $C_{\rm fc}$ is discharged to the single-phase grid, whereas, in mode 2, the flying capacitor $C_{\rm fc}$ is charged. Each mode is switched at twice the grid frequency. Through these modes, the flying capacitor voltage is fluctuated at twice the grid frequency in order to compensate the mismatch power between the PV side and the single-phase grid, and to maintain a constant PV input power.

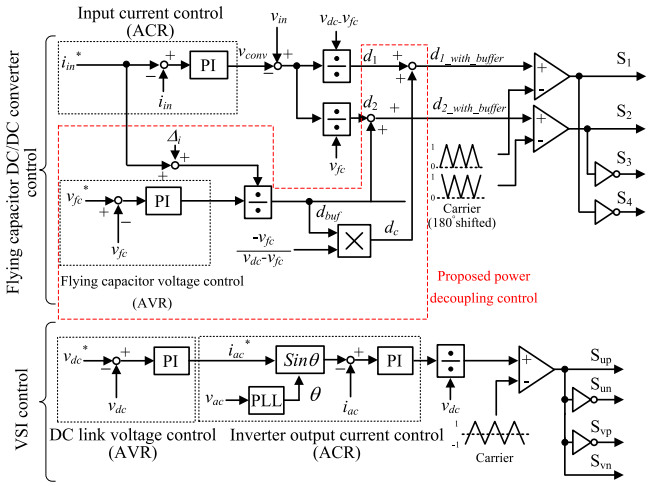

Fig. 6. Control block diagram of proposed converter.

B. Control Block Diagram of Proposed Converter

Fig. 6 shows the control block diagram of the FCC and the VSI. In the proposed control, an automatic current regulator and an automatic voltage regulator (AVR) are implemented in order to control the generated power, and the active power decoupling.

First, the duty references for the input current control are expressed as

$$d_1 = \frac{v_{\rm in} - v_{\rm conv}}{v_{\rm dc} - v_{\rm fc}} \tag{4}$$

$$d_2 = \frac{v_{\rm in} - v_{\rm conv}}{v_{\rm fc}} \tag{5}$$

where $v_{\rm in}$ is the PV input voltage, $v_{\rm conv}$ is the terminal voltage, $v_{\rm fc}$ is the flying capacitor voltage, and $v_{\rm dc}$ is the dc-link voltage. Conventionally, $v_{\rm fc}$ is constant, and is clamped to $v_{\rm dc}/2$. Thus, the duty references in (4) and (5) become equal to each other, and each switching mode, as shown in Fig. 5, is employed equally. On the other hand, the proposed control fluctuates the flying capacitor voltage in order to achieve the power decoupling. As a result, the duty reference of the discharge mode (mode 2) is different than that without the power decoupling.

In addition, in the flying capacitor voltage control, the flying capacitor voltage $v_{\rm fc}$ is fluctuated at twice the grid frequency in order to compensate the single-phase power fluctuation. The voltage reference $v_{\rm fc}^*$ is expressed as

$$v_{\rm fc}^* = \sqrt{\left(\frac{v_{\rm dc}}{2} - \frac{p_{\rm out}}{\omega C_{\rm fc} V_{\rm dc}}\right)^2 - \frac{p_{\rm out}}{\omega C} \{\sin(2\omega t) - 1\}} \tag{6}$$

where $p_{\rm out}$ is the output power, and ω is the angular frequency of the single-phase grid voltage. Following (6), the flying capacitor voltage includes the second-order harmonics of the single-phase grid frequency, and the voltage amplitude value is inversely proportional to the flying capacitor value $C_{\rm fc}$. In other words, when the flying capacitor voltage is fluctuated largely, $C_{\rm fc}$ can be minimized.

In order to ensure the stability between the input current control and the flying capacitor voltage control, it is necessary

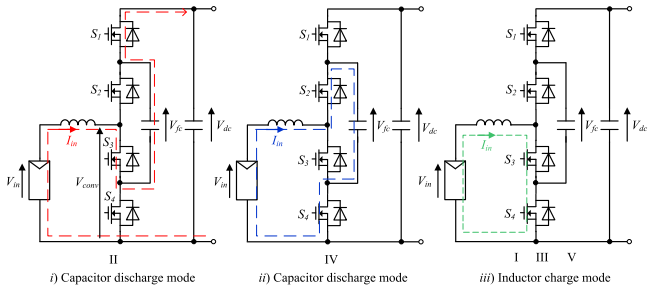

Fig. 7. Operation mode of FCC.

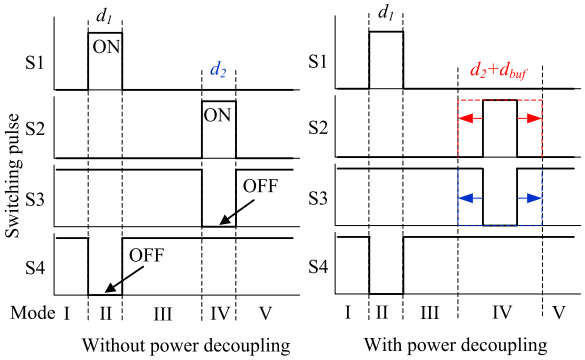

Fig. 8. Switching state of the FCC.

to consider the nonlinearity of the duty reference because the power decoupling duty reference given by the flying capacitor voltage control is added to the input current duty reference.

Fig. 7 shows the operation mode when the boost ratio is more than two. In this case, the FCC has three modes. Fig. 8 shows the switching state on each operation mode both with and without power decoupling. Note that, the duty reference d_1 is the duty ratio of the discharge mode (Mode II), the duty reference d_2 is the duty ratio of the charge mode (Mode IV), the other state is defined the by inductor charge mode (Mode I, III, V).

First, the inductor voltage V_L is expressed as

$$V_L = V_{\rm in} - V_{\rm conv} \tag{7}$$

where $V_{\rm conv}$ is the voltage across $\rm S_3$ and $\rm S_4$. Generally, the flying capacitor voltage is clamped to half of the dc-link voltage $V_{\rm dc}$. In state II, $V_{\rm conv}$ equals to the difference value between the dc-link voltage and the flying capacitor voltage. In state IV, $V_{\rm conv}$ equals to the flying capacitor voltage. Finally, in the state I, III, and V, the inductor voltage equals to the input voltage.

According to these conditions, when the active power decoupling is not applied, $V_{\rm conv}$ is expressed as

$$V_{\rm conv} = d_1 \frac{V_{\rm dc}}{2} + d_2 \frac{V_{\rm dc}}{2} = dV_{\rm dc}. \tag{8}$$

On the other hand, when the power decoupling is applied, d_2 depends on the power decoupling control because the flying capacitor should be charged by the double-line frequency, as shown in Fig. 2(b). In addition, the flying capacitor voltage fluctuates around the half value of the dc-link voltage due to the power decoupling control. Following these reasons, when the active power decoupling is applied, $V_{\rm conv\_with\_buffer}$ is expressed as

$$\begin{aligned} V_{\rm conv\_with\_buffer} &= d_1 \left(V_{\rm dc} - V_{\rm fc}\right) + \left(d_2 + d_{\rm buf}\right) V_{\rm fc} \\ &= dV_{\rm dc} + d_{\rm buf} V_{\rm fc} \end{aligned} \tag{9}$$

where $d_{\rm bud}$ is the duty ratio of the power decoupling mode. Comparing (8) and (9), $V_{\rm conv}$ does not match, and $d_{\rm bud}$ behaves as a disturbance to the input current control. Consequently, the input current is fluctuated at the double-line frequency.

In order to obtain the constant input current, the disturbance compensation is considered. In order to compensate the disturbance introduced by the power decoupling, $V_{\rm conv}$ has to be matched in both case with or without power decoupling. Thus, the disturbance compensation duty d_c is added to d_1. In this case, $V_{\rm conv\_with\_buffer}$ is expressed as

$$\begin{aligned} V_{\rm conv\_with\_buffer} &= \left(d_1 + d_c\right) \left(V_{\rm dc} - V_{\rm fc}\right) + \left(d_2 + d_{\rm buf}\right) V_{\rm fc} \\ &= dV_{\rm dc} + d_c \left(V_{\rm dc} - V_{\rm fc}\right) + d_{\rm buf} V_{\rm fc}. \end{aligned} \tag{10}$$

According to (10), when the second and three terms become zero, $V_{\rm conv}$ is matched in both (8) and (10). Thus, d_c is decided from (10), and it is expressed as

$$d_c(v_{\rm dc} - v_{\rm fc}) = v_{\rm fc} d_{\rm buf} \tag{11}$$

$$d_c = \frac{v_{\rm fc}}{v_{\rm dc} - v_{\rm fc}} d_{\rm buf}. \tag{12}$$

The proposed converter is operated by the typical PWM, which means that the switching frequency is constant. The controller operation is synchronized with the sampling frequency, and the control performance depends on the design of PI controller. The flying capacitor voltage control is based on the input current control, which adjusts the duty for active power decoupling. However, when the input current has negative or zero periods, the flying capacitor cannot charge. It means the flying capacitor voltage cannot control in these modes. Thus, the proposed converter has to be always operated in continuous current mode. In addition, the over modulation limits the flying capacitor control because the duty reference from the power decoupling control is added to the input current control.

When the MPPT is implemented, the input current reference $i_{\rm in}^*$ is decided from the maximum power point. For example, when the perturbation and observation method is applied, the input power is calculated from the detected values of the input voltage and the input current. When the value of the input power at the previous sampling period is less than the value, the input current reference $i_{\rm in}^*$ is increased. On the other hand, when the previous value of the input power at the previous sampling period is higher than the present value, $i_{\rm in}^*$ is decreased. In the other words, the typical MPPT control can be simply applied into the proposed control.

On the ac side, the dc-link voltage control and the inverter output current control are implemented in the VSI control. The dc-link voltage is regulated to be higher than the single-phase peak grid voltage $V_{\rm acp}$, and the inverter output current is controlled to sinusoidal waveforms. Note that, the phase reference is given by the grid voltage $v_{\rm ac}$ and the phased looked loop. As a result, the power factor becomes unity.

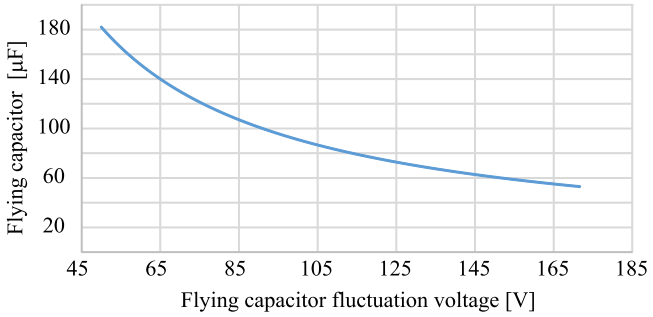

Fig. 9. Relationship between flying capacitor fluctuation voltage and flying capacitor.

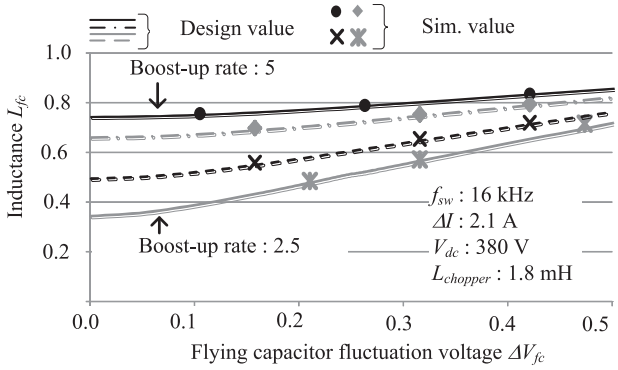

Fig. 10. Relationship between boost inductor value and ripple voltage of flying capacitor $C_{\rm fc}$.

IV. Component Design

A. Flying Capacitor $C_{\rm fc}$

The flying capacitor $C_{\rm fc}$ is designed from the buffer energy $W_{\rm buffer}$, which is the electric storage energy compensating the power fluctuation. Then, $C_{\rm fc}$ is expressed as

$$C_{\rm fc} = \frac{2W_{\rm buffer}}{\omega({V_{c\max}}^2 - {V_{c\min}}^2)} \tag{13}$$

where $V_{c\max}$ is the maximum value of the flying capacitor voltage, $V_{c\min}$ is the minimum value of the flying capacitor voltage, and ω is the angular frequency of the single-phase grid. In the proposed FCC converter, the flying capacitor becomes large in comparison with typical FCC converter because the flying capacitor is utilized for both the boost-up operation and the power decoupling. In order to reduce $C_{\rm fc}$, the voltage amplitude of the flying capacitor voltage should be designed to be high.

Fig. 9 shows the relationship between the flying capacitor fluctuation voltage and the flying capacitor with 1 kW. For example, when the fluctuation voltage is set to 87 V, the flying capacitor is reduced to 100 μF. However, the over modulation limits the flying capacitor control, as explained in Section III. In the future work, the limitation of the proposed control will be considered for optimization.

B. Boost Inductor $L_{\rm fc}$

The boost inductor L_{fc} is designed based on the current ripple Δi_{Lfc} of the inductor current. When the active power decoupling is not applied, the flying capacitor voltage is clamped to the half of the dc-link voltage. On the other hand, the proposed control fluctuates the flying capacitor voltage at twice the grid frequency. As a result, the inductor voltage is similar to that without the active power decoupling. Thus, the boost-up inductor design of the proposed converter is considered from the maximum inductor ripple condition.

First, $L_{\rm fc}$ is designed from the inductor voltage and the current ripple, and expressed as

$$L_{\rm fc} = \alpha \frac{V_L}{4 f_{\rm sw} \Delta I} \tag{14}$$

where α is the duty ratio, V_L is the inductor voltage, $f_{\rm sw}$ is the switching frequency, and ΔI is the ripple ratio of the inductor current. In comparison with the typical boost converter, the inductance of the FCC can be reduced to one quarter because the ripple current frequency becomes the twice the switching frequency, and the voltage applied to the inductor V_{Lfc} is only half the dc-link voltage $V_{\rm dc}$ because of the flying capacitor voltage $V_{\rm fc}$. However, in the proposed circuit, the duty ratio and V_L are continuously changed due to the power decoupling control. Thus, the boost inductor of the proposed circuit is designed based on duty references $d_{1\_\rm with\_buffer}$ and $d_{2\_\rm with\_buffer}$.

In the proposed control, the duty references $d_{1\_\rm with\_buffer}$ and $d_{2\_\rm with\_buffer}$ are expressed as

$$d_{1\_\rm with\_buffer} = \frac{V_{\rm in}}{V_{\rm dc}} \{1 - \cos(2\omega t)\} \tag{15}$$

$$d_{2\_\rm with\_buffer} = \frac{V_{\rm in}}{V_{\rm dc}} \left\{1 + \left(\frac{V_{\rm dc}}{v_{\rm fc}} - 1\right) \cos(2\omega t)\right\} \tag{16}$$

where $d_{1\_\rm with\_buffer}$ and $d_{2\_\rm with\_buffer}$ include the frequency component, which is dependent on the power decoupling duty $d_{\rm buf}$ and the control decoupling reference d_c. Using (15) and (16), the boost inductor of the proposed circuit is expressed as

$$L_{\rm fc} = \frac{\max\{(v_{\rm dc} - v_{\rm fc} - v_{\rm in}) d_{1\_\rm with\_buffer}, (v_{\rm fc} - v_{in}) d_{2\_\rm with\_buffer}\}}{f_{\rm sw} \Delta I_{Lfc}}. \tag{17}$$

Fig. 10 shows the relationship between the boost inductor value and the ripple voltage of the flying capacitor in the FCC. The switching frequency $f_{\rm sw}$ is 16 kHz, and the dc-link voltage $V_{\rm dc}$ is 380 V. The ripple current ΔI_{Lfc} is 2.1 A, and the inductance of the typical boost converter is 1.8 mH. Note that, the inductance of the typical boost converter is constant with respect to the ripple voltage of the flying capacitor. In order to consider the validity of the inductor design (17), the design value and the simulation results are compared. In addition, the boost-up rate is changed from 2.5 to 5. The boost inductor value $L_{\rm fc}$ in the FCC is normalized by the inductance of the typical boost converter $L_{\rm chopper}$. As shown in Fig. 9, the simulation results agree with the design values, thereby confirming the validity of the boost inductor design. In addition, the inductance ratio is less than

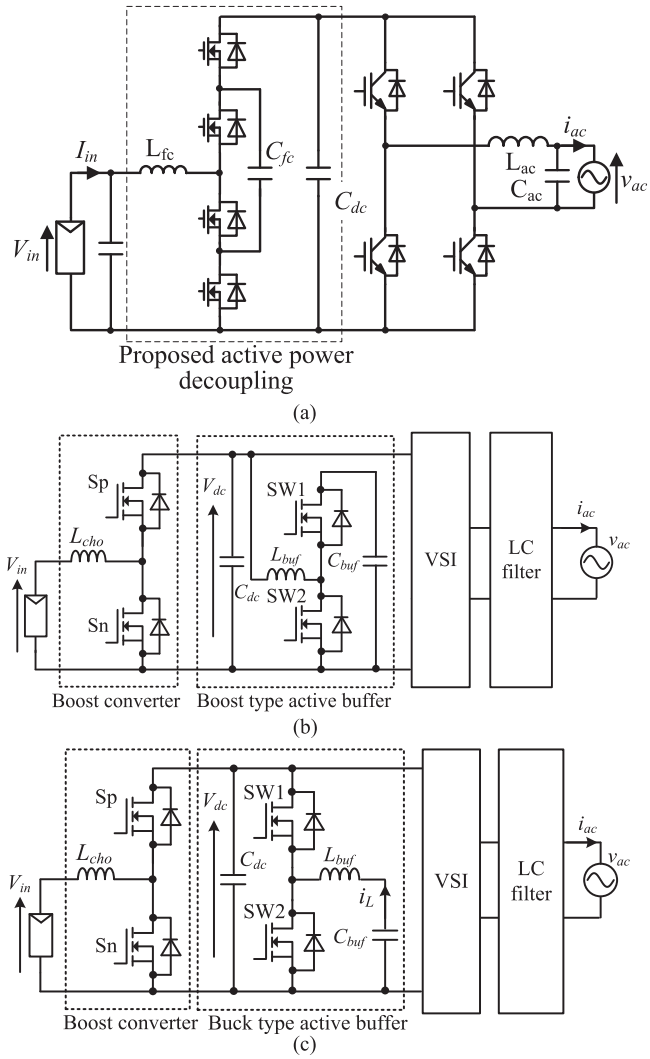

Fig. 11. Comparison of power decoupling topology. (a) Proposed active power decoupling. (b) Conventional boost-type active power decoupling. (c) Conventional buck-type active power decoupling.

1 p.u. for all conditions, which implies that the inductance of the FCC is smaller than that of the typical boost converter.

V. Power Density Comparison With Pareto Optimization

In this section, the design method for achieving high power density and high efficiency in the dc to single-phase ac grid-connected system is discussed. In particular, several active power decoupling topologies are compared in the terms of the power density [24]–[25].

Fig. 11 shows the three topologies considered in this paper, the proposed active power decoupling, conventional boost-type active power decoupling, and conventional buck-type active power decoupling. In order to achieve high power density and higher efficiency, the design flows for the active power decoupling using the ceramic capacitor are introduced. Then, from the design flowchart and the specifications of commercially available products, the power density and efficiency of the active power decoupling circuit are evaluated by Pareto optimization. Finally, the total loss and a total volume at the maximum power density are compared.

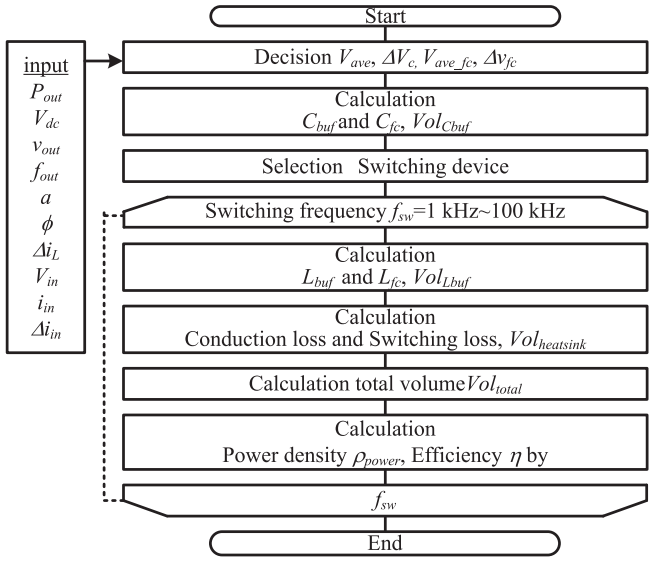

Fig. 12. Designing flow for boost-up and buck-type power decoupling circuit.

A. Conventional Boost-Type Power Decoupling Design

As shown in Fig. 11(b), conventional boost-type active power decoupling uses a typical boost converter and a buffer capacitor $C_{\rm buf}$ to absorb the power ripple in the dc-link.

Fig. 12 shows the design flowchart for optimizing the design of the boost-type active power decoupling. First, the capacitance of the buffer capacitor is calculated based on the average voltage and the voltage fluctuation range of the buffer capacitor. Then, the capacitor volume $\rm Vol_{Cbuf}$ is determined using commercially available products. The switching device is decided based on the maximum voltage of the buffer capacitor. In this paper, a switching device having a rating voltage of 1200 V is used. The boost inductor is designed based on the switching frequency $f_{\rm sw}$ and the inductor ripple current. The volume of the boost inductor is estimated according to the area product method [26]. The heatsink volume is then calculated from the thermal resistance, which depends on the conduction loss $P_{\rm loss\_cond}$ and the switching loss $P_{\rm loss\_sw}$ of the switching devices. Finally, the Pareto optimization is obtained by varying the switching frequency in order to obtain the maximum power density point.

The buffer capacitor $C_{\rm buf}$ is decided based on the relationship between the storage energy and the capacitor voltage and can be designed in a manner similar to that used to design the proposed FCC, as expressed in (13). When the buffer capacitor amplitude voltage $\Delta V_{C\_\rm buf}$ is increased, a switching device with a high rating voltage is required. Thus, a switching device, which has the rating voltage of 1200 V is selected because the peak capacitor voltage is 800 V.

The buffer inductor is designed based on the allowable ripple current ΔI_{Lf}. The inductance becomes the maximum value when the difference between the DC-link voltage and the buffer

capacitor voltage reaches the maximum. Thus, the inductance of the buffer inductor is obtained as

$$L_{\mathrm{buf}} = \frac{V_{\mathrm{dc}}}{\Delta i_L f_{\mathrm{sw}}} \frac{\left(V_{\mathrm{ave}} + \frac{\Delta V_c}{2}\right) - V_{\mathrm{dc}}}{V_{\mathrm{ave}} + \frac{\Delta V_c}{2}}. \tag{18}$$

The inductor volume depends on several parameters of the components. Moreover, there are several ways to select the core for the inductor. Thus, the buffer inductor is designed by the area product method using the window area and the cross-sectional area. Hence, the volume of the boost inductor $\mathrm{Vol}_{L\mathrm{buf}}$ is calculated as

$$\mathrm{Vol}_{L\mathrm{buf}} = K_v \left(\frac{L_{\mathrm{buf}} I_{\mathrm{max}}^2}{K_u B_{\mathrm{max}} J} \right)^{\frac{3}{4}} \tag{19}$$

where K_v is the volume coefficient depending on the shape of cores, I_{max} is the maximum current flowing to the inductor, K_u is the fill factor of the window, B_{max} is the maximum flux density of the core, and J is the current density of the windings.

The switching devices require a cooling system, e.g., heatsinks and fans. In general, the cooling system is designed based on the thermal resistance. The cooling system performance index (CSPI) is introduced in order to estimate the volume of the cooling system. The CSPI is an indication of the cooling performance per unit volume of the cooling system. The cooling system is small when CSPI becomes higher. The volume of the cooling system $\mathrm{Vol}_{\mathrm{heatsink}}$ is given by

$$\mathrm{Vol}_{\mathrm{heat\,sin}\,k} = \frac{1}{R_{\mathrm{th}(f-a)} \mathrm{CSPI}} \tag{20}$$

where $R_{\mathrm{th(f-a)}}$ is the thermal resistance of the cooling system which is given by

$$R_{\mathrm{th}(f-a)} = \frac{T_j - T_a}{P_{\mathrm{loss}}} - \left(R_{\mathrm{th}(j-c)} + R_{\mathrm{th}(c-f)} \right) \tag{21}$$

where T_j is the junction temperature of the switching device, T_a is the ambient temperature, $R_{\mathrm{th}(j-c)}$ is the junction-to-case thermal resistance, and $R_{\mathrm{th}(j-c)}$ is the case-to-fin thermal resistance. The total loss P_{loss}, which is composed of the conduction loss $P_{\mathrm{loss\_cond}}$ and the switching loss $P_{\mathrm{loss\_sw}}$ of the switching devices, is calculated as

$$P_{\mathrm{loss}} = P_{\mathrm{loss\_cond\_buffer}} + P_{\mathrm{loss\_sw\_buffer}} \tag{22}$$

where $P_{\mathrm{loss\_cond}}$ and $P_{\mathrm{loss\_sw}}$ are given by

$$P_{\mathrm{loss\_cond\_buffer}} = \frac{1}{T_{\mathrm{out}}} \int_0^{T_{\mathrm{out}}} i_L^2 r_{\mathrm{on\_buffer}} dt \tag{23}$$

$$P_{\mathrm{loss\_sw\_buffer}} = \frac{1}{E_{\mathrm{dcd}} I_{\mathrm{md}}} \left(e_{\mathrm{on}} + e_{\mathrm{off}} \right) f_{\mathrm{sw}} \frac{1}{T_{\mathrm{out}}} \int_0^{T_{\mathrm{out}}} v_c i_L dt \tag{24}$$

in which, T_{out} is the period of the single-phase grid, r_{on} is the on-resistance of the switching device, f_{sw} is the switching frequency of the active power decoupling circuit, e_{on} and e_{off} are the turn-ON and turn-OFF energy per switching referred from a datasheet, and E_{dcd} and I_{md} are the voltage and current under the measurement condition of the switching loss described in the datasheet. The buffer capacitor voltage v_c and the boost inductor current i_L are expressed as

$$v_c = V_{\mathrm{ave}} - \frac{\Delta V_c}{2} \sin\left(2\omega_{\mathrm{out}} t\right) \tag{25}$$

$$i_L = \frac{V_{\mathrm{ave}}}{V_{\mathrm{dc}}} C_{\mathrm{buf}} \frac{dv_c}{dt}. \tag{26}$$

According to (25), an increase in the switching frequency leads to an increase in the switching loss. The cooling performance can be improved by fans in order to minimize the use of heatsinks. However, the system lifetime is limited by these fans. Thus, the cooling system is designed based on the assumption that the natural cooling is used.

B. Conventional Buck-Type Power Decoupling Design

The buck-type active power decoupling can reduce the buffer capacitor voltage, as compared to the boost-up-type active power decoupling, and it can still be designed based on the flowchart shown in Fig. 12.

The buffer capacitor is designed by (13). However, the dc-link voltage limits the peak voltage of the buffer capacitor. As a result, the buffer capacitance must be larger than the capacitance of the boost-up-type active power decoupling.

The inductance of the buffer inductor reaches the maximum value when the capacitor voltage is half the input voltage. Thus, the inductance is designed by

$$L_{\mathrm{buf}} = \frac{V_{\mathrm{dc}}}{4\Delta i_L f_{\mathrm{sw}}} \tag{27}$$

where i_L is the current that flows to the smoothing inductor, which is given by

$$i_L = C_{\mathrm{buf}} \frac{dv_c}{dt} = -\frac{P_{\mathrm{out}}}{V_{\mathrm{ave}}} \cos\left(2\omega_{\mathrm{out}} t\right). \tag{28}$$

C. Boost Converter Design

In order to compare between the volumes of the FCC and the conventionalactive power decoupling circuit, the volume design of the boost converter must be determined.

First, the boost inductor is determined by

$$L_{\mathrm{cho}} = \frac{V_{\mathrm{in}}}{\Delta I_{\mathrm{in}} f_{\mathrm{sw}}} \frac{V_{\mathrm{dc}} - V_{\mathrm{in}}}{V_{\mathrm{dc}}} \tag{29}$$

where ΔI_{in} is the inductor current ripple, which is 30% of the rated input current.

The total loss of the switching devices is expressed as

$$P_{\mathrm{loss\_chopper}} = P_{\mathrm{loss\_cond\_chopper}} + P_{\mathrm{loss\_swi\_chopper}} \tag{30}$$

where the conduction loss $P_{\mathrm{loss\_cond\_chopper}}$ is calculated by

$$P_{\mathrm{loss\_cond\_chopper}} = r_{\mathrm{on\_chopper}} \left(I_{\mathrm{in}}^2 + \frac{\Delta i_{\mathrm{in}}^2}{3} \right). \tag{31}$$

Moreover, $P_{\mathrm{loss\_swi\_chopper}}$ is the total switching loss by the MOSFET Sp and Sn, the switching losses of which are obtained

TABLE I
COMPONENT SPECIFICATIONS

Circuit	Part	Marking	Maximum ration	Circuit	Part	Marking	Maximum ration
Boost type active buffer	C_{buf}	Murata Manufacturing EVS20329S2G306MS09	400 V 30 μF	Boost chopper	Sp Sn	ROHM SiC-MOSFET, SCT120AF	650 V 29 A
	SW1 SW2	ROHM SiC-MOSFET, SCH2080KE	1200 V 40 A	Flying capacitor converter	S1 S2 S3 S4	ROHM SiC-MOSFET, SCT120AF	650 V 29 A
		Fuji Electric IGBT, FGW30N120HD	1200 V 30 A			ROHM SiC-MOSFET, SCTMU001F	400 V 20 A
		Fuji Electric Si-MOSFET, FMH30N60S1	600 V(2 series connection) 30 A		C_{fc}	Murata Manufacturing EVS20329S2G306MS09	400 V 30 μF
Step down type active buffer	C_{buf}	Murata Manufacturing EVS20329S2G306MS09	400 V 30 μF		C_f	Murata Manufacturing KC355WD72E225MH01	450 V 1 μF
	SW1 SW2	ROHM SCT2120AF	650 V 29 A				

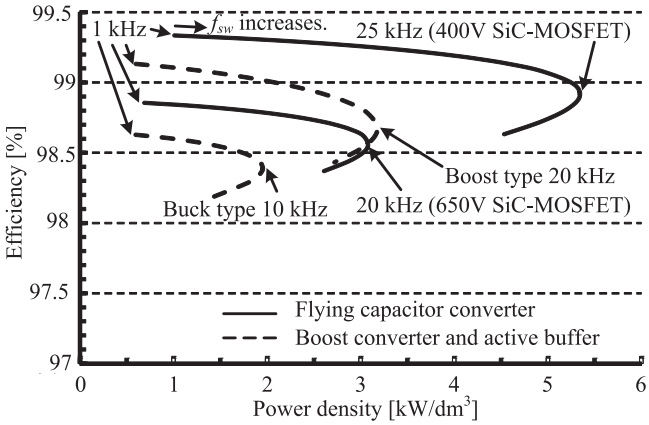

Fig. 13. Pareto front of FCC, and conventional active power decoupling circuit.

TABLE II
EXPERIMENTAL PARAMETERS

Symbol	Quantity	value
$V_{\rm in}$	Input voltage	200 V
$P_{\rm out}$	Output power	1.5 kW
$P_{\rm rated}$	Rated power	1.5 kW
$f_{\rm sw\_FCC}$	Switching frequency of FCC	20 kHz
$f_{\rm sw\_VSI}$	Switching frequency of VSI	20 kHz
$V_{\rm DC\_ave}$	DC-link average voltage	350 V
$C_{\rm fc}$	Flying capacitor	180 μF
$C_{\rm dc}$	DC-link capacitor	20 μF
$L_{\rm fc}$	Boost inductor	1 mH
$v_{\rm ac}$	Grid voltage	200 $V_{\rm rms}$
$f_{\rm ac}$	Grid frequency	50 Hz

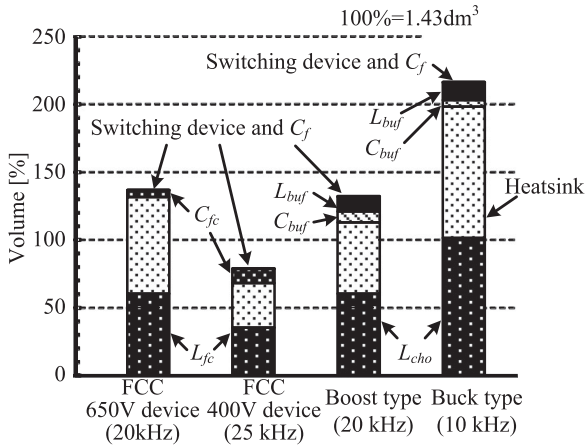

Fig. 14. Volume distribution at maximum power density point.

by

$$P_{\rm loss\_sw\_sp} = \frac{1}{E_{\rm dcd} I_{\rm md}} f_{\rm sw} V_{\rm dc} \left[e_{\rm on} \left(i_{\rm in} + \Delta i_{\rm in} \right) + e_{\rm off} \left(i_{\rm in} - \Delta i_{\rm in} \right) \right] \tag{32}$$

$$P_{\rm loss\_sw\_sn} = \frac{1}{E_{\rm dcd} I_{\rm md}} f_{\rm sw} V_{\rm dc} \left[e_{\rm on} \left(i_{\rm in} - \Delta i_{\rm in} \right) + e_{\rm off} \left(i_{\rm in} + \Delta i_{\rm in} \right) \right]. \tag{33}$$

D. Pareto Front Optimization With Proposed Converter

Fig. 13 shows the Pareto front of the proposed FCC and the conventional active power decoupling circuit implemented in the boost converter. Table I shows the selected component specifications. Switching devices with a rating voltage of 650 and 400 V are selected for the FCC, as shown in Table II, and the rating current chosen to be five times the rating input current. The maximum voltages of the flying capacitor are set to 340 and 250 V for each selected switching device. According to Fig. 13, the power density approaches the maximum value, when a SiC-MOSFET with a rated voltage of 400 V is used in the FCC at 25 kHz. In particular, a maximum power density of 5.3 kW/dm^3 with an efficiency of 98.9% is achieved.

Fig. 14 shows the volume ratio of the components at the maximum power density point. The component volumes are normalized with the total volume of the passive topology as 100%. In the FCC with a 400 V-SiC MOSFET, the volume of the flying capacitor is reduced by 54.6%, as compared to that

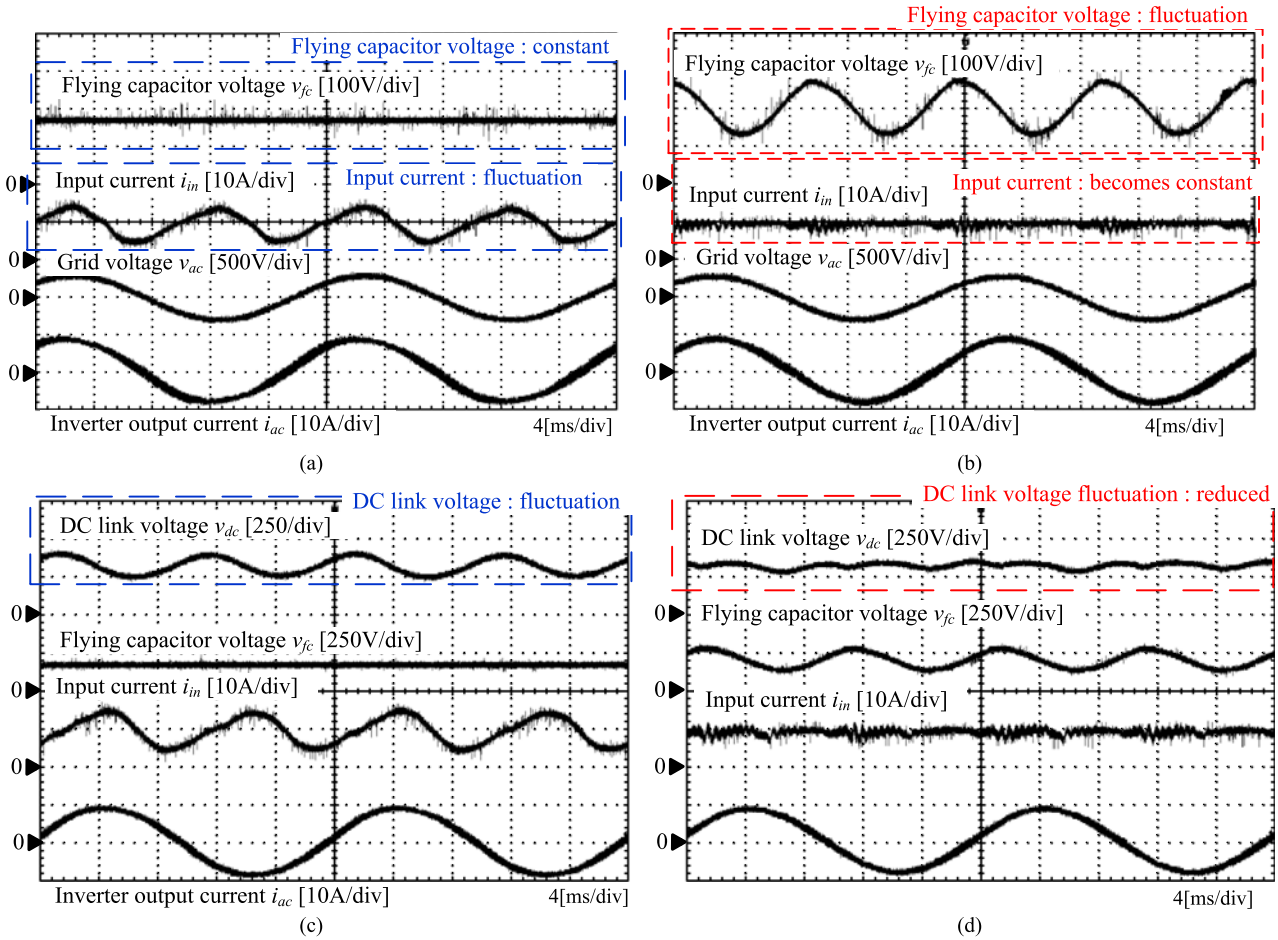

Fig. 15. Experimental result. (a) Flying capacitor voltage and input current without proposed control. (b) Flying capacitor voltage and input current with proposed control. (c) DC-link voltage and flying capacitor voltage without proposed control. (d) DC-link voltage and flying capacitor voltage with proposed control.

of the electrolytic capacitor. When a flying capacitor voltage of 400 V is applied to the FCC, the flying capacitor volume is twice that for the case of a rated voltage of 650 V. However, the volumes of the boost inductor and the cooling system are reduced by 58.3% and 46.2%, respectively. As a result, the total volume of the FCC with switching devices with a rated voltage of 400 V is 57.5% of that of the FCC with switching devices with a rated voltage of 650 V.

VI. Experimental Result

In order to confirm the validity of the proposed circuit, a 1.5-kW prototype circuit is tested. Table II shows the experimental parameters, and the experimental results are shown in Fig. 15. In this experiment, for simplicity, MPPT control is not introduced. In addition, a flying capacitor with $180\,\mu$F is used for voltage derating for each switching devices.

As show in Fig. 15(a) and (c), the flying capacitor voltage $v_{\rm fc}$ is constant. However, the inverter dc voltage $v_{\rm dc}$ fluctuates at twice the single-phase grid frequency, because the instantaneous difference between the input and output power is compensated by only the dc-link capacitor $C_{\rm dc}$. The fluctuation of the dc-link voltage also acts as a disturbance to the control of the inverter output current. Consequently, the total harmonic distortion (THD) of the inverter output current becomes 5.1%. More importantly, the input current $i_{\rm in}$ fluctuates greatly due to the power mismatch between the dc input side and the ac output side. As a result, the performance of MPPT control decays owing to this input current fluctuation.

On the other hand, in Fig. 15(b) and (d), the flying capacitor voltage $v_{\rm fc}$ is fluctuated by the proposed control, and $v_{\rm dc}$ and $i_{\rm in}$ become approximately constant. These results confirm that the single-phase power fluctuation is compensated by the flying capacitor $C_{\rm fc}$. In addition, the flying capacitor average voltage is balanced at half the dc-link voltage.

Fig. 16 shows the harmonic analysis of the dc-link voltage. The second-order harmonic component with the proposed control is reduced by 74.5% as compared to that without the power decoupling control. However, a small second-order harmonic component still appears in the dc-link voltage. This is because the power fluctuation compensation value has a small error as compared to the actual single-phase power fluctuation.

Fig. 17(a) shows the THD characteristic of the inverter output current with respect to the output power. Over the entire output power range, the inverter output current THD is improved with the proposed control because the second-order harmonics of the

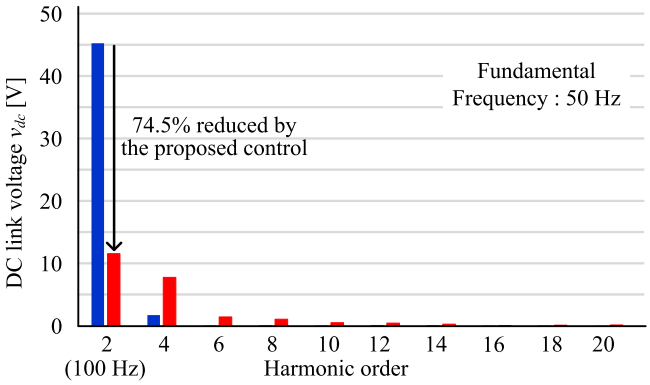

Fig. 16. Harmonic analysis of dc-link voltage.

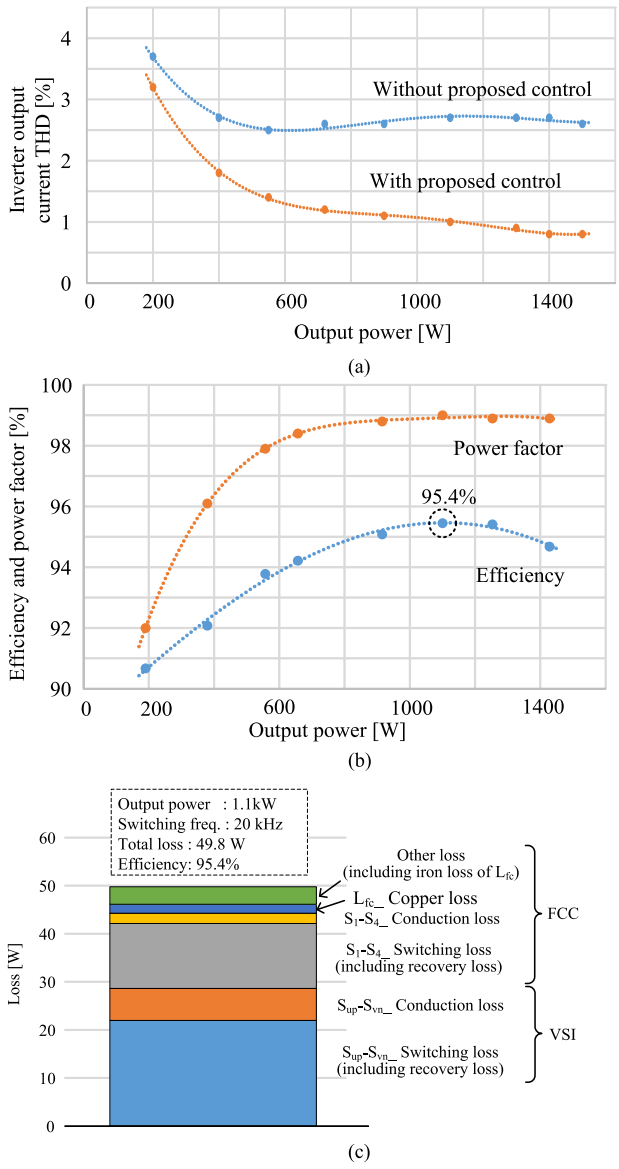

Fig. 17. Inverter output current THD, efficiency, power factor, and loss analysis. (a) Inverter output current THD characteristics. (b) Efficiency and power factor. (c) Loss analysis result obtained at an output power of 1.1 kW.

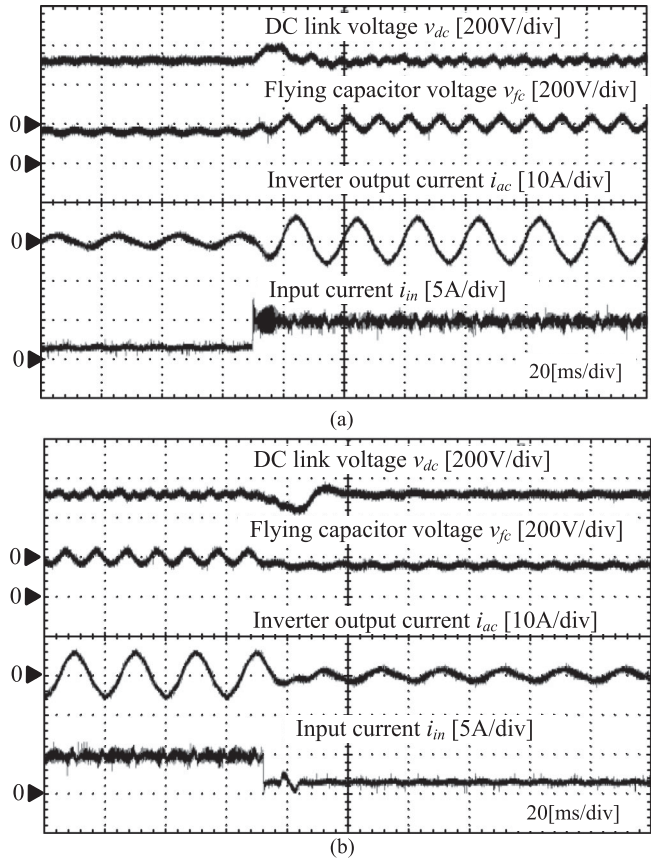

Fig. 18. Experimental result in the load transient response test. (a) 0.1 to 0.7 p.u. (b) 0.7 to 0.1 p.u.

dc-link voltage is eliminated by the power decoupling control. In addition, under a light load, the inverter output current THD decays, because the ratio between the fundamental frequency and the harmonics increases.

Fig. 17(b) shows the efficiency and the power factor characteristics when the proposed control is applied. The power factor is approximately unity due to the feedforward control for grid disturbance, whereas the maximum system efficiency reaches 95.4% at the output power of 1.1 kW.

Fig. 17(c) shows the loss analysis results for the proposed converter for an output power of 1.1 kW. According to Fig. 18, the switching loss is dominant in the FCC and VSI due to the high recovery loss. When a wideband gap device, such as a SiC-MOSFET is applied, it is possible to reduce the switching loss. On the other hand, the conduction loss of the FCC is small because a low on-resistor switching device can be used owing to the multilevel topology.

Fig. 18 shows the experimental waveforms obtained in the load transient response test. According to Fig. 18, the input current is regulated to be constant by the proposed control even when the output power is abruptly changed. In addition, the fluctuation of the flying capacitor voltage becomes large when the output power is changed from 0.1 to 0.7 p.u. This is because the power ripple increases under the heavy load

condition, and the charge and discharge values of the flying capacitor becomes larger. Moreover, the stable control of the inverter output current without any spike current is also confirmed.

The proposed FCC converter does not use the dc-link capacitor with high capacitance. Thus, in the load transient period, a large overshoot occurs on the dc-link voltage. In order to reduce the overshoot, the design of the PI control for AVR is important. In the load transient test result of Fig. 18, the PI control gain is adjusted in order to reduce the voltage overshoot. However, dc-link voltage still has several frequency components because the control design is not optimized in this paper. As a result, the inverter output current distorts in comparison with Fig. 15. Note that, the inverter output current THD is 1.9% at 1 kW.

VII. Conclusion

In this paper, a novel active power decoupling method with a FCC was proposed. The proposed converter does not require additional components for the active power decoupling, and the boost inductor value could be reduced, as compared to the typical boost converter. In addition, the active power decoupling control that uses a small flying capacitor, was proposed along with the clarification of the component design.

A high power density, high efficiency design was demonstrated by the Pareto optimization. In this paper, three topologies, a boost-type active power decoupling topology, a buck-type active power decoupling topology, and the proposed active power decoupling were compared in term of the power density. As a result, the proposed converter was shown to achieve the highest power density of 5.3 kW/dm^3

Finally, the experimental results confirmed that the dc-link voltage fluctuation was reduced by 74.5% by the proposed active power decoupling method. Moreover, in the boost-up inductor design, the inductor current ripple approximately agreed with the design value with an error of 4.7%. Thus, the experimental results confirmed the validity of the inductor design.

The maximum efficiency achieved in the experiment was 95.4%. In order to improve the efficiency, the converter loss was evaluated. As a result, it was confirmed that the switching loss should be reduced. Moreover, the inverter output current THD was less than 5%, and the output power factor was approximately unity at the rated output power. Based on these results, fundamental operation was confirmed.

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