Characterisation and Modeling of Gallium Nitride Power Semiconductor Devices Dynamic On-State Resistance

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***Abstract*—Gallium nitride high-electron-mobility transistors (GaN-HEMTs) suffer from trapping effects that increases device on-state resistance ($R_{\mathrm{DS(on)}}$) above its theoretical value. This increase is a function of the applied dc bias when the device is in its off state, and the time which the device is biased for. Thus, dynamic $R_{\mathrm{DS(on)}}$ of different commercial GaN-HEMTs are characterised at different bias voltages in the paper by a proposed new measurement circuit. The time-constants associated with trapping and detrapping effects in the device are extracted using the proposed circuit and it is shown that variations in $R_{\mathrm{DS(on)}}$ can be predicted using a series of RC circuit networks. A new methodology for integrating these $R_{\mathrm{DS(on)}}$ predictions into existing gallium nitride-high-electron-mobility transistors models in standard SPICE simulators to improve model accuracy is then presented. Finally, device dynamic $R_{\mathrm{DS(on)}}$ values of the model is compared and validated with the measurement when it switches in a power converter with different duty cycles and switching voltages.**

***Index Terms*—Dynamic on-state resistance, equivalent circuit, gallium nitride high-electron-mobility transistors (GaN-HEMT), power semiconductor device characterisation, power semiconductor device modeling.**

I. Introduction

BECAUSE of small device on-state resistance and inter-electrode capacitance, gallium nitride (GaN) power semiconductor devices produce low power loss in electrical energy conversion. Thus, it is interesting to apply GaN devices in high-frequency, high-efficiency, and high power density power converters [1]–[3]. Understanding GaN devices characteristics is very helpful to better use those devices in power electronics systems. High-electron-mobility transistors (HEMTs) are the most widely used GaN power electronic devices, but they suffer from electron trapping effects that decreases device performance [4], [5].

It is reported in [6] and [7] that GaN-HEMT trapping effects can be attributed to device surface trapping and buffer layer trapping. As shown in [6], when GaN-HEMT is biased, the electrical field between drain and gate terminal causes some electrons to be trapped at the surface close to the gate. Meanwhile, large vertical electrical field under the drain terminal causes some electrons to be trapped in device buffer layer. All the trapped electrons are not freed instantaneously when device changes from off-state to on-state, which reduces device on-state current carrying capability by two-dimensional electron gas (2-DEG). Trapped electrons positions and their influence on 2-DEG is illustrated in Fig. 1. Some techniques, such as employing appropriate passivation and filed plate structures, using p-GaN layer to device drain electrode [8] and optimizing device buffer layer design [9] in device fabrication, can help to alleviate trapping effect.

The reduced GaN device current conduction capability caused by the trapping effect increases device channel resistance, which is important for power converters design when considering efficiency and cooling system size. Illustrated in Fig. 2, this trapping

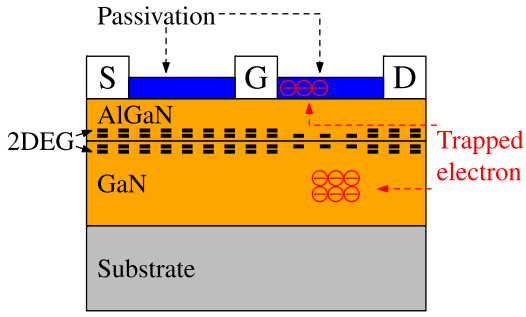

Fig. 1. Trapped electrons positions and their influence on 2-DEG in a GaN-HEMT.

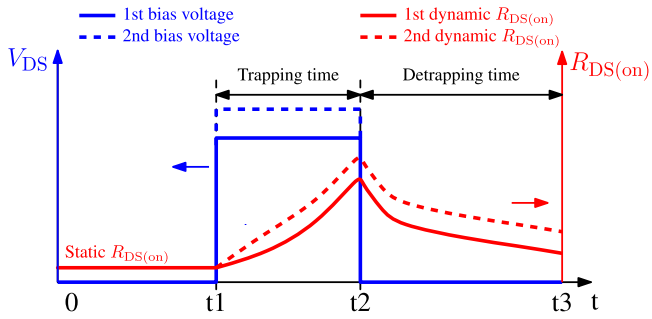

Fig. 2. GaN-HEMT dynamic $R_{\mathrm{DS(on)}}$ values due to trapping effects.

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effect is related mainly with two parameters when device in off-state, one is the bias $V_{\rm DS}$ voltage value and another is the bias time (trapping time), which would give rise to the increase of GaN device on-state resistance ($R_{\rm DS(on)}$) value. In the on-state, detrapping process occurs and the $R_{\rm DS(on)}$ values decrease to the static value at a rate characterized by detrapping time. In [10], Lu *et al.* present that GaN device $R_{\rm DS(on)}$ values would increase by a maximal factor of 4 after 1ms bias time depending on bias $V_{\rm DS}$ voltage value, while device dynamic $R_{\rm DS(on)}$ values would decrease 30% after 10 μs detrapping time. Badawi *et al.* [11] show that device dynamic $R_{\rm DS(on)}$ values would reach more than 10 times bigger than its static $R_{\rm DS(on)}$ values, and it decrease to about a half after a few microseconds detrapping time.

When employing GaN transistors in power electronics circuits, GaN devices normally switch with different periods and duty cycles leading to a combination of trapping and detrapping effects and consequently uncertainty in the actual value of $R_{\rm DS(on)}$. This will lead to uncertainty in device power loss, making predictions of converter efficiency and cooling system design challenging. As only device static $R_{\rm DS(on)}$ values are given in its technical datasheet, the ability to characterise and model GaN-HEMT dynamic $R_{\rm DS(on)}$ values is thus an important design consideration.

Two different methods are commonly used to measure GaN-HEMT dynamic $R_{\rm DS(on)}$ values: one method is by using directly a measurement equipment [12], and another one is by using an electrical circuit, where different circuit topologies are proposed in [10], [11], [13]–[15]. In this paper, a new characterisation circuit is presented to measure GaN-HEMT dynamic $R_{\rm DS(on)}$ values, which can be easily implemented. Compared to the above different circuits, this new measurement circuit needs fewer components and offers an alternative method to characterise the device and to compare the results.

Regarding device dynamic $R_{\rm DS(on)}$ values modeling, it is not addressed in the reported GaN-HEMT models using for power electronics simulation [16], [17] and it is not included in the models offered by device manufacturers. For this reason, based on device dynamic $R_{\rm DS(on)}$ measurement results, an equivalent circuit is thus proposed in the paper to present device trapping and detrapping effect, which can be used in a circuit simulator to study device $R_{\rm DS(on)}$ variation when it switches in a power converter.

Initial GaN-HEMT dynamic $R_{\rm DS(on)}$ characterisation and modeling results are reported in [18]. More device dynamic $R_{\rm DS(on)}$ measurement results together with more analysis on simulation and experimental results are presented in this paper.

The paper is structured with following sections. First the measurement circuit to characterise GaN-HEMT dynamic $R_{\rm DS(on)}$ values is presented. Afterward, measurement results of different trapping and detrapping time on $R_{\rm DS(on)}$ values are shown. Based on the measurement results, a model using equivalent circuit is proposed to represent device dynamic $R_{\rm DS(on)}$ values. The model is further validated by comparing with the measurement when device switches in a power converter. Finally, some conclusion are given.

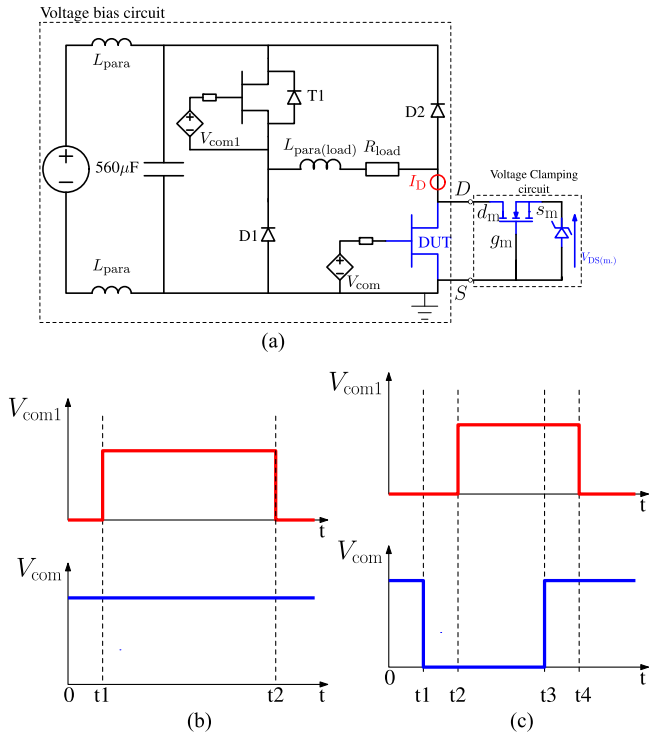

Fig. 3. GaN-HEMT dynamic on-state resistance measurement circuit and control signals. (a) Measurement configuration. (b) Control signal to measure static $R_{\rm DS(on)}$. (c) Control signal to measure dynamic $R_{\rm DS(on)}$.

II. GaN-HEMT Dynamic On-State Resistance Measurement

A. Measurement Circuit

GaN device $R_{\rm DS(on)}$ values can be obtained by measuring device on-state voltage $V_{\rm DS(on)}$ across it and current $I_{\rm D}$ through it in an electrical circuit. As the measured bias voltage when device is OFF ($V_{\rm DS(off)}$) can be more than several hundred times higher than device $V_{\rm DS(on)}$, a voltage clamping circuit is necessary to reduce the measured $V_{\rm DS(off)}$ in order to increase measurement accuracy, where a low voltage range probe can then be used, which is more accurate to measure small voltage than a high voltage range probe using in a direct $V_{\rm DS}$ voltage measurement. For this reason, the measurement circuit shown in Fig. 3 is constituted by two parts: one is a voltage bias circuit to control device trapping time when it is OFF and another is a voltage clamping circuit to measure device $V_{\rm DS(on)}$ value when it is ON.

In the voltage bias circuit, a transistor T1 is used to control device under test (DUT) trapping time. A resistive load $R_{\rm load}$ is used to set the current level when DUT is in on-state. Because of the parasitic inductance $L_{\rm para(load)}$ of the $R_{\rm load}$, two diodes D1, D2 offer a free wheeling path of the current when either T1 or DUT is switched from ON to OFF.

The voltage clamping circuit is constituted by a depletion mode (D-mode) Si-MOSFET and a Zener diode. DUT measurement voltage $V_{\rm DS(m.)}$ is measured across the Zener diode as shown in Fig. 3(a). The principle of the voltage clamping circuit is that when DUT is ON, D-mode Si-MOSFET is in

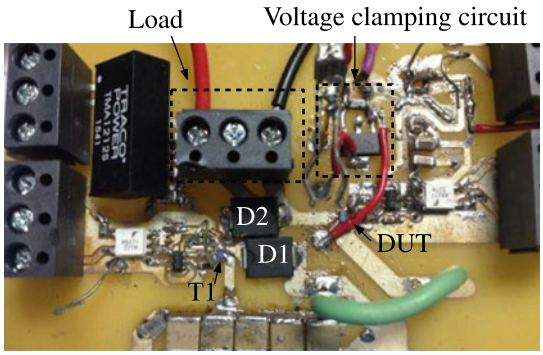

Fig. 4. Realization of the measurement circuit.

on-state ($V_{\mathrm{g_m\,s_m}}$ is superior to MOSFET threshold voltage V_{th}), so terminals s_{m} and d_{m} are almost in the same potential (Zener diode only reversely conducts a few microamperes, so its conduction loss do not affect the measurement) and DUT $V_{\mathrm{DS(on)}}$ can thus be measured directly ($V_{\mathrm{DS(m.)}} = V_{\mathrm{DS(on)}}$). When DUT is OFF, Zener diode junction capacitance is charged at first, so $V_{\mathrm{DS(m.)}}$ increases until $V_{\mathrm{g_m\,s_m}}$ is inferior to MOSFET V_{th} ($V_{\mathrm{g_m\,s_m}} = -V_{\mathrm{DS(m.)}}$). Afterward, D-mode MOSFET is pinched OFF and its interelectrode capacitance $C_{\mathrm{d_m\,s_m}}$ is charged to withstand almost the whole bias V_{DS} voltage ($V_{\mathrm{DS}} \gg V_{\mathrm{DS(m.)}}$). It is to be noted when DUT is OFF, there is a leakage current balance between D-mode MOSFET and Zener diode, so $V_{\mathrm{DS(m.)}}$ is inferior to Zener diode clamping voltage V_{clamp} in steady state. Instead of measuring voltage range between $V_{\mathrm{DS(on)}}$ and V_{DS}, a much smaller voltage range between $V_{\mathrm{DS(on)}}$ and V_{clamp} is measured, thus the measurement sensitivity is increased. Compared to the similar type voltage clamping circuits that are analyzed in [14], fewer components and no external power supply are used in this clamping circuit.

Device static $R_{\mathrm{DS(on)}}$ value can be measured by applying the control signal shown in Fig. 3(b), where DUT is kept always in on-state and T1 is controlled by a single pulse.

Device dynamic $R_{\mathrm{DS(on)}}$ values can be measured by applying the control signal shown in Fig. 3(c), where DUT is initially kept in on-state and T1 blocks all the bias voltage. Then at t1, DUT is switched OFF and at t2, T1 is switched ON, thus all the bias voltage is across DUT. Afterward, at t3, DUT is switched ON again, so current I_{D} flows through the DUT. Finally at t4, T1 is switched OFF. Thus, DUT trapping time is controlled by t2-t3 while detrapping time is controlled by t3-t4, so $R_{\mathrm{DS(on)}}$ values under different trapping and detrapping time can be measured.

The realization of the measurement circuit is shown in Fig. 4. In the measurement, $R_{\mathrm{load}} = 100\,\Omega$, T1 is a commercial GaN-HEMT (EPC2012C, 200 V/5A) while D1 and D2 are the same Schottky diode (MBRS4201T3G, 200 V/4A). Dynamic $R_{\mathrm{DS(on)}}$ values of a DUT, which is the same as T1, is measured by the above circuit, of which the results are presented in the next section.

B. Measurement Results

Several major parameters of the measurement equipments and clamping circuit devices are summarized in Table I. In the measurement, the maximal measured V_{DS} voltage is 3.3 V, which can achieve a measurement accuracy of at least $\frac{3.3}{2^8} = 0.013$ V by using an 8-bit resolution oscilloscope.

In order to validate the proposed measurement circuit and demonstrate the dynamic $R_{\mathrm{DS(on)}}$ effect in GaN-HEMTs, $R_{\mathrm{DS(on)}}$ of a SiC-MOSFET (C3M0065090D, 900 V/36 A) with similar static $R_{\mathrm{DS(on)}}$ value as GaN-HEMT is measured and set as a measurement benchmark, because SiC-MOSFET does not exhibit dynamic $R_{\mathrm{DS(on)}}$ behaviour. Both devices are biased at 120 V for 1 ms. SiC-MOSFET is switched from 0 V to 10 V while GaN-HEMT is switched from $-$ 3 V to 5 V. The obtained measurement waveforms are compared in Fig. 5.

Device conduction current I_{D} and measurement voltage $V_{\mathrm{DS(m.)}}$ waveforms shown in Fig. 5(a) corresponds to the time range t3-t4 when applying gate signal of Fig. 5(c). It is observed that because of the voltage clamping circuit, $V_{\mathrm{DS(m.)}}$ is about 1.5 V when DUT is OFF, which is much smaller than the bias voltage (120 V), thus, the measurement accuracy is improved in comparison to a direct measurement. It is also shown in the measurement results that measured $V_{\mathrm{DS(m.)}}$ is almost constant for SiC-MOSFET. However, it decreases for GaN-HEMT, indicating an obtained dynamic $R_{\mathrm{DS(on)}}$ value variation.

When each electrical parameter stabilizes after OFF–ON transition, which is 1 μs in the measurement, the device's dynamic $R_{\mathrm{DS(on)}}$ values are calculated and they are compared in Fig. 5(b).

As shown in the results, an almost constant $R_{\mathrm{DS(on)}}$ value is obtained for SiC-MOSFET[1], indicating no trapping effect for this device. The obtained $R_{\mathrm{DS(on)}}$ value is close to device datasheet value, which helps to validate the proposed measurement circuit. In contrary to that, the obtained $R_{\mathrm{DS(on)}}$ value of GaN-HEMT is higher than its static $R_{\mathrm{DS(on)}}$ value, which shows that device suffer from a trapping effect after 120 V and 1 ms bias. Device $R_{\mathrm{DS(on)}}$ value then decreases with detrapping time, showing a detrapping effect influence.

At 20 °C, dynamic $R_{\mathrm{DS(on)}}$ of the GaN-HEMT is thus characterized with applied bias voltages of 80 V and 120 V under different trapping time and detrapping time, where the measurement results are shown in Fig. 6.

As shown in the results, device dynamic $R_{\mathrm{DS(on)}}$ values increase with trapping time and it decreases with detrapping time, and it increases more under a higher bias voltage. For this device, it is observed that when device biased by a certain trapping time, it needs a longer detrapping time to reduce its dynamic $R_{\mathrm{DS(on)}}$ values to the static values, which shows that effective $R_{\mathrm{DS(on)}}$ values are likely to be higher than theoretical values due to this trapping effect, especially in higher voltage applications with low duty cycles.

It is also observed in Fig. 6 that the device suffers from fast trapping effect that only 1 μs trapping time can increase its $R_{\mathrm{DS(on)}}$ value. Between 1 μs to 100 μs, slow trapping effect occurs, so device $R_{\mathrm{DS(on)}}$ values vary a little by trapping time. After 100 μs, $R_{\mathrm{DS(on)}}$ values increase again with trapping time

[1]Obtained $R_{\mathrm{DS(on)}}$ value is slightly higher than its nominal value, because $R_{\mathrm{DS(on)}}$ value is measured when gate voltage is 10 V, which is lower than device recommended turn-ON gate voltage 15 V.

TABLE I
MAJOR PARAMETERS OF THE MEASUREMENT EQUIPMENTS AND CLAMPING CIRCUIT DEVICES

Oscilloscope	Current probe	Voltage probe	D-mode MOSFET	Zener diode
64xi (600 MHz, 8-bit)	CP030 (50 MHz, 30 A)	ZD1500 (1.5 GHz, 8 V)	BSP149 (200 V, $V_{\rm th} \approx -1.4$ V)	BZT52C3V3 (3.3 V)

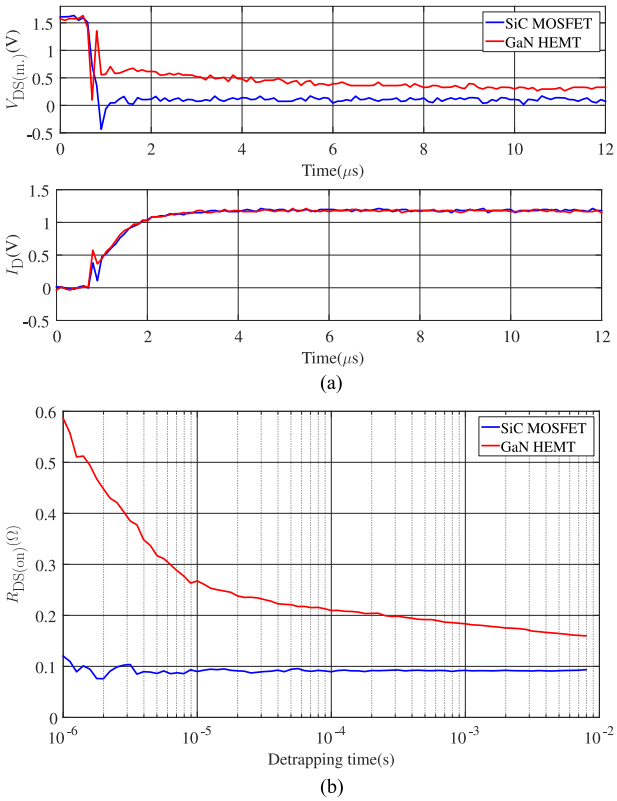

Fig. 5. Setting SiC-MOSFET as measurement benchmark to demonstrate GaN-HEMT dynamic $R_{\rm DS(on)}$ effect.

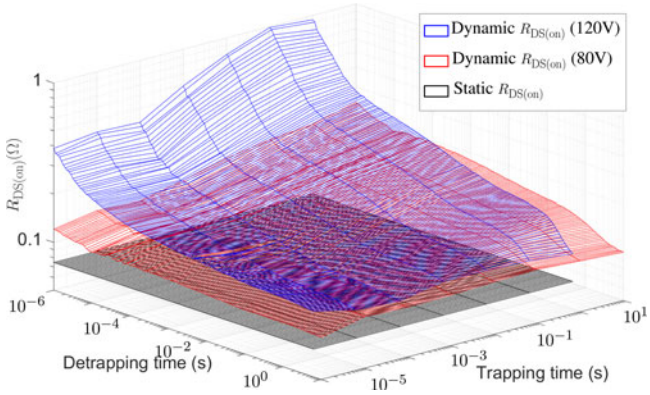

Fig. 6. Comparison of GaN-HEMT (EPC2012C) static and dynamic $R_{\rm DS(on)}$ values at 20 °C.

until 1 s. In terms of detrapping effect, it is observed in Fig. 6 that device has fast detrapping effect from 1 μs to 10 μs, where device $R_{\rm DS(on)}$ values decrease about a half. Then from 10 μs to 1 s, $R_{\rm DS(on)}$ decreases slowly with detrapping time. After 1 s, another fast detrapping effect is observed. Those characterization results correspond to the GaN device trapping and detrapping time constants presented in [19].

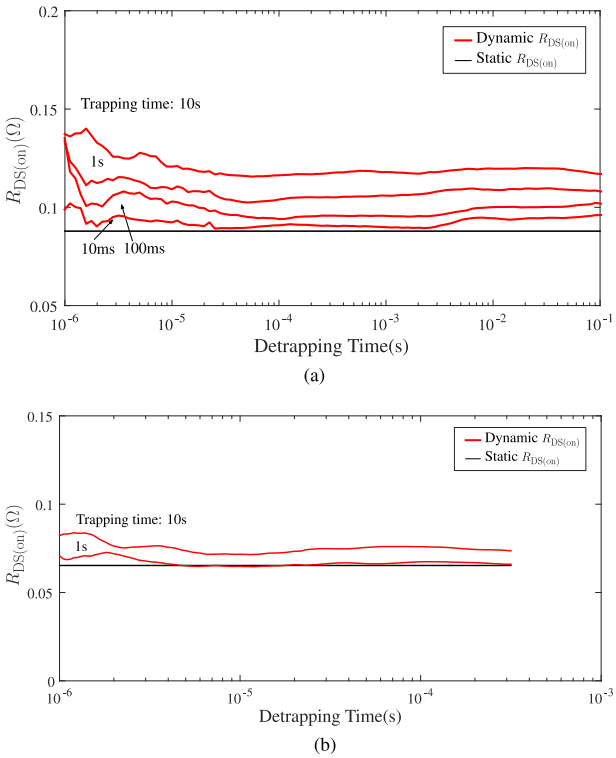

Fig. 7. Dynamic $R_{\rm DS(on)}$ measurement results of different GaN transistors. (a) 650 V/15 A GaN transistor (GS66504B) biased at 400 V. (b) 100 V/1 A GaN transistor (EPC2036) biased at 100 V.

It is to be noted that by choosing devices T1, D1, D2, and D-mode MOSFET to corresponding DUT power ratings, the presented measurement circuit can be used to characterise dynamic $R_{\rm DS(on)}$ of different commercial GaN transistors with different voltage and current ratings, where the measurement results are shown in Fig. 7 for a 650 V/15A GaN transistor (GS66504B) from GaNSystems and another 100 V/1A GaN transistor from EPC (EPC2036).

For transistor GS66504B, as shown in Fig. 7(a), when biased at 400 V for 10 s, device maximal $R_{\rm DS(on)}$ value increase to around 65% in comparison with its static $R_{\rm DS(on)}$ value. For transistor EPC2036, as shown in Fig. 7(b), when biased at 100 V for 10 s, device maximal $R_{\rm DS(on)}$ value increase to around 30% in comparison with its static $R_{\rm DS(on)}$ value, which shows less dynamic $R_{\rm DS(on)}$ variation.

In order to study GaN-HEMT $R_{\rm DS(on)}$ values variation when device applied in power converter, a device trapping and detrapping model is proposed based on the measurement results, which will be presented in the next section.

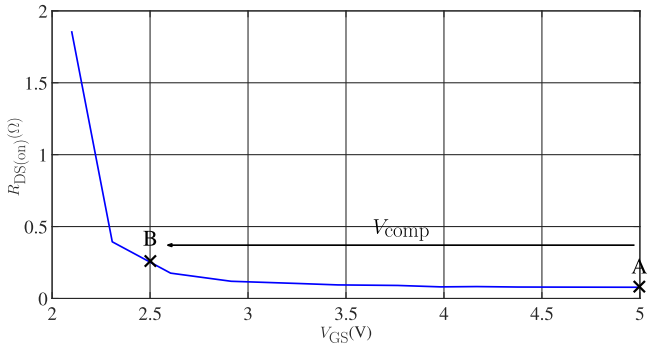

Fig. 8. Device static $R_{\mathrm{DS(on)}}$ values of different V_{GS} voltages at 20 °C.

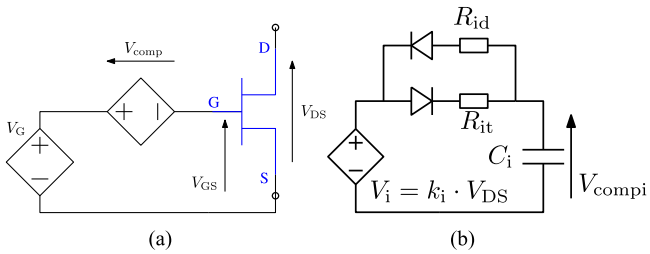

Fig. 9. Dynamic $R_{\mathrm{DS(on)}}$ values representation by equivalent circuit. (a) Using V_{comp} to represent device effective gate voltage. (b) Using RC unit to represent V_{comp}.

III. GaN-HEMT Dynamic On-State Resistance Modeling

A. Trapping and Detrapping Model

Device static $R_{\mathrm{DS(on)}}$ values can be modulated by the applied V_{GS} gate voltage. Characteristics for the EPC2012C device are shown in Fig. 8, but this applies to all GaN transistors.

According to this $R_{\mathrm{DS(on)}}$-V_{GS} relation, the obtained device dynamic $R_{\mathrm{DS(on)}}$ values can be represented by its static $R_{\mathrm{DS(on)}}$ values at an equivalent gate voltage shown in Fig. 8, where point A corresponds to the device static $R_{\mathrm{DS(on)}}$ value, and point B corresponds to the device $R_{\mathrm{DS(on)}}$ value after certain trapping time. The V_{GS} voltage difference between point A and point B, which is defined as V_{comp}, is applied to represent $R_{\mathrm{DS(on)}}$ variation during trapping and detrapping process. After adding V_{comp} in gate circuit, which is shown in Fig. 9(a), device effective V_{GS} voltage ($V_{\mathrm{GS}} = V_{\mathrm{G}} - V_{\mathrm{comp}}$) after trapping and detrapping time is adjusted, thus, a dynamic $R_{\mathrm{DS(on)}}$ value is obtained. According to the reported trapping mechanism of GaN device by different researchers in [6], [9], and [20], no matter the origin of the trapping is from either device gate electrode or device buffer layer, the consequence is that those trapped electrons would deplete 2-DEG channel, resulting a decreased current conduction capability and device dynamic $R_{\mathrm{DS(on)}}$ degradation. Using V_{comp} in the proposed model is able to model device current conduction capability, even though it is an equivalent circuit, it still represents device physical behaviour.

In order to modulate device effective gate voltage, V_{comp} value increases with the trapping time and it decreases with the detrapping time. V_{comp} can then be further modeled in the form of an RC circuit, which is presented in Fig. 9(b). In one RC unit, V_{compi} increases when capacitor C_{i} is charged by a controlled voltage source V_{i} through resistor R_{it} and it decreases when C_{i} is discharged through resistor R_{id}. As defined by the following equation (1), V_{i} values are expressed by multiplying a coefficient k_{i} to the device bias voltage V_{DS} when device is OFF and V_{i} values are zero when device is ON

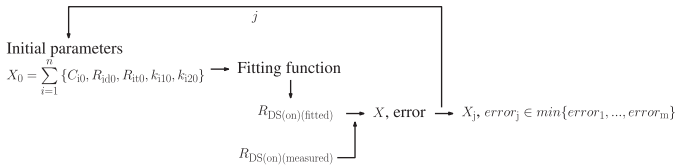

Fig. 10. Flowchart when using fitting method to obtain model parameters.

$$V_{\mathrm{i}} = k_{\mathrm{i}} \cdot V_{\mathrm{DS}} \quad \text{(Device is OFF)}$$
$$V_{\mathrm{i}} = 0 \quad \text{(Device is ON).} \tag{1}$$

After trapping time t_1 and detrapping time t_2, V_{compi} values can be easily obtained by the following equations

$$V_{\mathrm{compi}}(t_1) = V_{\mathrm{i}} \cdot \left(1 - \exp\left(-\frac{t_1}{R_{\mathrm{it}} \cdot C_{\mathrm{i}}}\right)\right) \tag{2}$$

$$V_{\mathrm{compi}}(t_2) = V_{\mathrm{compi}}(t_1) \cdot \left(\exp\left(-\frac{t_2}{R_{\mathrm{id}} \cdot C_{\mathrm{i}}}\right)\right). \tag{3}$$

In order to model different trapping and detrapping time constants observed in the characterisation results, a series of the RC units are used in the model, so V_{comp} value is the sum of the capacitor voltage in each unit

$$V_{\mathrm{comp}} = \sum_{i=1}^{n} V_{\mathrm{compi}}. \tag{4}$$

By obtaining V_{comp} value, device effective V_{GS} voltages can be obtained at different trapping and detrapping time, so device dynamic $R_{\mathrm{DS(on)}}$ values can be finally obtained based on the $R_{\mathrm{DS(on)}}$-V_{GS} relation shown in Fig. 8

$$R_{\mathrm{DS(on)}} = f(V_{\mathrm{GS}}) = f(V_{\mathrm{G}} - V_{\mathrm{comp}}). \tag{5}$$

It is shown in the measurement results that device dynamic $R_{\mathrm{DS(on)}}$ values increase in a higher bias voltage, indicating a bigger V_{comp} value in the model after same trapping time. In order to apply the proposed model in different bias voltages and easily implement it in the simulation software, only k_{i} is chosen as a function of bias voltage [$k_{\mathrm{i}} = f(V_{\mathrm{DS}})$], because its trend is easier to be found (variation within one order of magnitude) and to be implemented in the model than other parameters (variation may exceed more than one order of magnitude). Thus, in the model, following number of parameters need to be determined: $\sum_{i=1}^{n} \{C_{\mathrm{i}}, R_{\mathrm{id}}, R_{\mathrm{it}}, k_{\mathrm{i1}}, k_{\mathrm{i2}}\}$, where n is the number of RC units used, k_{i1} and k_{i2} are different coefficients at different bias voltages V_{DS1} and V_{DS2}.

All the above parameters in the model are needed to be extracted and the results are presented in the next subsection.

TABLE II
PARAMETERS USING TO REPRESENT GAN-HEMT TRAPPING AND DETRAPPING EFFECT IN THE MODEL

k_{11}	k_{21}	k_{31}	k_{41}	k_{51}	k_{61}	k_{71}
0.0015	0.0013	0.0039	0.0297	0.0013	0.0046	0.0256
C_1	C_2	C_3	C_4	C_5	C_6	C_7
8.8 F	3.92×10^{-9} F	0.314 F	351 F	6.678×10^{-5} F	952.038 F	3.051×10^{-8} F
R_{1t}	R_{2t}	R_{3t}	R_{4t}	R_{5t}	R_{6t}	R_{7t}
0.043 Ω	0.0019 Ω	0.0025 Ω	5.416×10^{6} Ω	0.011 Ω	2.567×10^{3} Ω	0.206 Ω
R_{1d}	R_{2d}	R_{3d}	R_{4d}	R_{5d}	R_{6d}	R_{7d}
1.673×10^{6} Ω	2.185×10^{3} Ω	1.609×10^{5} Ω	8.261×10^{4} Ω	47.188 Ω	6.756×10^{7} Ω	1.305×10^{8} Ω
k_{12}	k_{22}	k_{32}	k_{42}	k_{52}	k_{62}	k_{72}
0.0011	0.0019	0.0012	0.0027	0.0015	0.00088	0.02

B. Model Parameters Extraction

Illustrated in Fig. 10, a fitting method is used to minimize the error of the following equation.

$$\begin{aligned}\text{error} = &\left|R_{\text{DS(on)(fitted,V}_{\text{DS}}=80\text{ V)}}\right. \\ &\left.-R_{\text{DS(on)(measured,V}_{\text{DS}}=80\text{ V)}}\right|^2 \\ &+\left|R_{\text{DS(on)(fitted,V}_{\text{DS}}=120\text{ V)}}\right. \\ &\left.-R_{\text{DS(on)(measured,V}_{\text{DS}}=120\text{ V)}}\right|^2 \end{aligned} \tag{6}$$

where fitted $R_{\text{DS(on)}}$ values can be obtained from (2)–(5).

The fitting function starts with initial parameters X_0 and attempts to find adequate parameters X in order to minimize error. Based on the measurement results shown in Fig. 6, seven RC units are finally used to represent device dynamic $R_{\text{DS(on)}}$ values, because it is found that the increase of the number of RC units does not help decrease the error further. As there are 35 parameters to be determined in the model, one fitting process might result in a local error minimization, because fitting result is dependent on its initial parameters. For this reason, enough fitting iterations are tried with random initial parameters to guarantee that a global error minimization is achieved. Model parameters X_{j} are obtained when error_{j} is the minimal value of all the iterations.

All the obtained parameters k_{11}–k_{71}, C_1–C_7, R_{1t}–R_{7t}, R_{1d}–R_{7d}, and k_{12}–k_{72} are given in Table II. The comparison between the model and the measurement on dynamic $R_{\text{DS(on)}}$ values as a function of trapping and detrapping times at different bias V_{DS} voltages are shown in Figs. 11 and 12 separately. It is to be noted that $R_{\text{DS(on)}}$ values shown in Fig. 11 are the values obtained 1 μs after OFF–ON transition which explained in Section II-B.

As shown in Fig. 11, device $R_{\text{DS(on)}}$ values show almost no change when the trapping time is varied between 1 μs and 100 μs, which leads to almost overlapping detrapping curves at 1 μs, 10 μs, and 100 μs trapping time shown in Fig. 12.

In Fig. 12(a), when device is biased at 80 V, maximal error between model and measurement is about 0.018 Ω, which corresponds to a maximal 13% difference. The model yields an average 4% difference to the measurement. It is found that in the results shown in Fig. 12(b) when device is biased at 120 V, the maximal error between model and measurement is about 0.097 Ω, which corresponds to a maximal 23% difference. The average difference between model and measurement in this

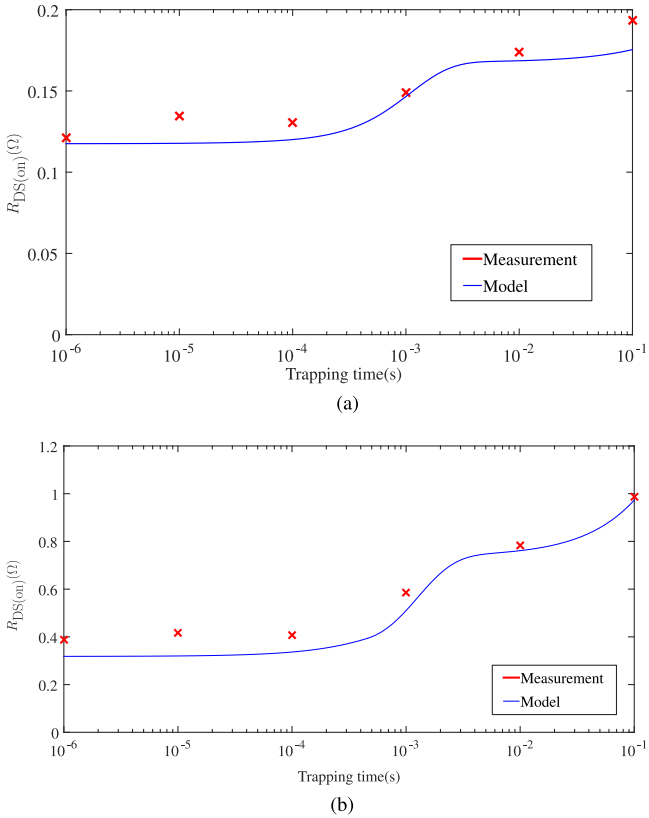

Fig. 11. Comparison between the measurement and model on dynamic $R_{\text{DS(on)}}$ values as a function of trapping time at different bias V_{DS} voltages. (a) $V_{\text{DS}} = 80$ V. (b) $V_{\text{DS}} = 120$ V.

condition is about 6%. Despite those difference, it is shown that the model generally follow measured $R_{\text{DS(on)}}$ values variation over six orders of magnitude of time, so it can be stated that the model represents the measurement in a reasonable way.

Once all the above parameters are obtained, for any bias voltage V_{DSx} between V_{DS1} and V_{DS2}, its corresponding V_{ix} value used in the model can be obtained by a numerical interpolation of V_{i1} and V_{i2}. Here, a linear interpolation method is chosen to reduce model computational complexity, so V_{ix} value can be obtained by

$$V_{\text{ix}} = \frac{V_{\text{i2}} - V_{\text{i1}}}{V_{\text{DS2}} - V_{\text{DS1}}} \times (V_{\text{DSx}} - V_{\text{DS1}}) + V_{\text{i1}}. \tag{7}$$

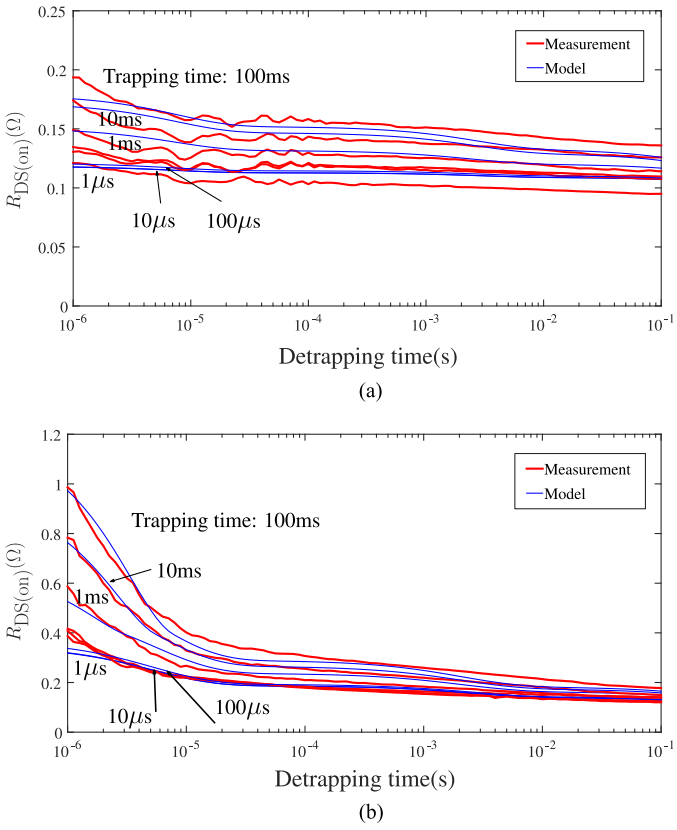

Fig. 12. Comparison between the measurement and model on dynamic $R_{\mathrm{DS(on)}}$ values as a function of detrapping time for different trapping times and at different bias V_{DS} voltages. (a) $V_{\mathrm{DS}} = 80$ V. (b) $V_{\mathrm{DS}} = 120$ V.

Finally, coefficients k_{ix} used in the model can be obtained by

$$k_{\mathrm{ix}} = \frac{V_{\mathrm{DS2}} \cdot k_{\mathrm{i2}} - V_{\mathrm{DS1}} \cdot k_{\mathrm{i1}}}{V_{\mathrm{DS2}} - V_{\mathrm{DS1}}} \times \frac{(V_{\mathrm{DSx}} - V_{\mathrm{DS1}})}{V_{\mathrm{DSx}}} + \frac{V_{\mathrm{DS1}}}{V_{\mathrm{DSx}}} \cdot k_{\mathrm{i1}}. \tag{8}$$

After obtaining the above parameters, the model illustrated in Fig. 9 can be easily implemented in a circuit simulator. In a SPICE-like circuit simulator, V_{comp} and $V_1 \cdots V_7$ can be represented by voltage controlled voltage source. It is also to be noted that the proposed model can be easily added in the behavioural model proposed by manufacturers to study device trapping effect, which is normally missing in those manufacturer behavioural models.

As GaN-HEMT suffered from trapping effect, its $R_{\mathrm{DS(on)}}$ values might increase when it switches continuously in a power converter. For this reason, $R_{\mathrm{DS(on)}}$ values estimated by the above model are compared with the measurement, and the results will be presented in the next section.

IV. Model Validation

A. Model Validation at Different Switching Voltages

The same electrical circuit shown in Fig. 3(a) with the control signal shown in Fig. 13 is used to measure device dynamic $R_{\mathrm{DS(on)}}$ values when it switches continuously. In order to avoid the influence of switching losses of both DUT and D-mode MOSFET of the voltage clamping circuit on device temperature,

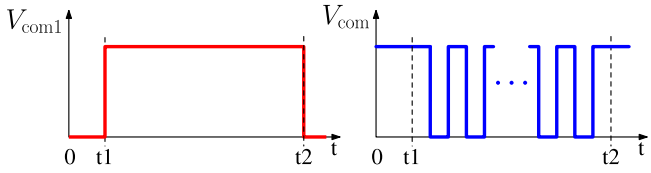

Fig. 13. Control signal when device switches continuously in a power converter.

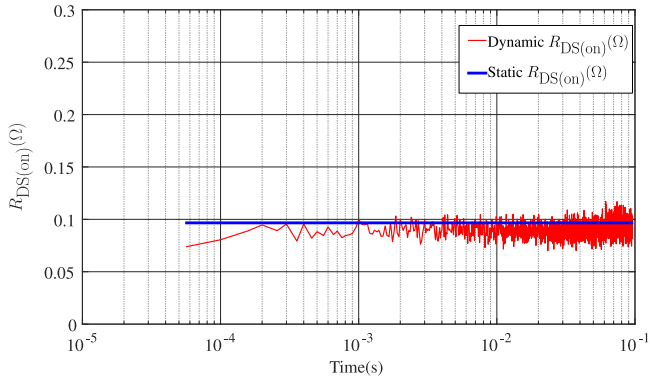

Fig. 14. SiC-MOSFET measured static and dynamic $R_{\mathrm{DS(on)}}$ values comparison.

it switches at 10 kHz with a duration of 0.1 s. In the measurement, sampling time is 400 ns. Device $R_{\mathrm{DS(on)}}$ mean value between 1 μs and 3 μs after OFF–ON transition is chosen as its trapping value of each switching cycle, while its detrapping value is calculated at the end of each on-state.

The same SiC-MOSFET is tested at first in order to compare its static and dynamic $R_{\mathrm{DS(on)}}$ values when device switches continuously (10 kHz, 50% duty cycle), of which the result is shown in Fig. 14.

As shown in the measurement results, obtained SiC-MOSFET dynamic $R_{\mathrm{DS(on)}}$ values when device switches remains the same as its static $R_{\mathrm{DS(on)}}$ value obtained previously, indicating a constant device $R_{\mathrm{DS(on)}}$ value.

Afterward, the same GaN-HEMT device is switched under different conditions. When switching voltages are 80 V and 120 V with 50% duty cycle (corresponding to 50 μs trapping and detrapping time), the comparison between the measurement and simulation of device $R_{\mathrm{DS(on)}}$ values is shown in Fig. 15(a) and (b) separately.

In Fig. 15(a), measured device $R_{\mathrm{DS(on)}}$ values increase to a factor of around two higher than its static value after 0.1 s, because device trapping time constants are faster than its detrapping time constants as shown in Fig. 6. Furthermore, trapping effects can increase device $R_{\mathrm{DS(on)}}$ values very quickly when trapping time inferior to 10 μs, which indicates that device effective $R_{\mathrm{DS(on)}}$ values are likely to be bigger than its static value if switching frequency increases to more than 100 kHz. When comparing the simulation with the measurement, the simulation results represent well the measurement, which confirms the $R_{\mathrm{DS(on)}}$ increase trend. Meanwhile, there are mainly two mismatches between the model and the measurement: one is that model estimates smaller $R_{\mathrm{DS(on)}}$ trapping values of each switching cycle, because model produces smaller $R_{\mathrm{DS(on)}}$ values than the measurement after different trapping time [see Fig. 11(a)];

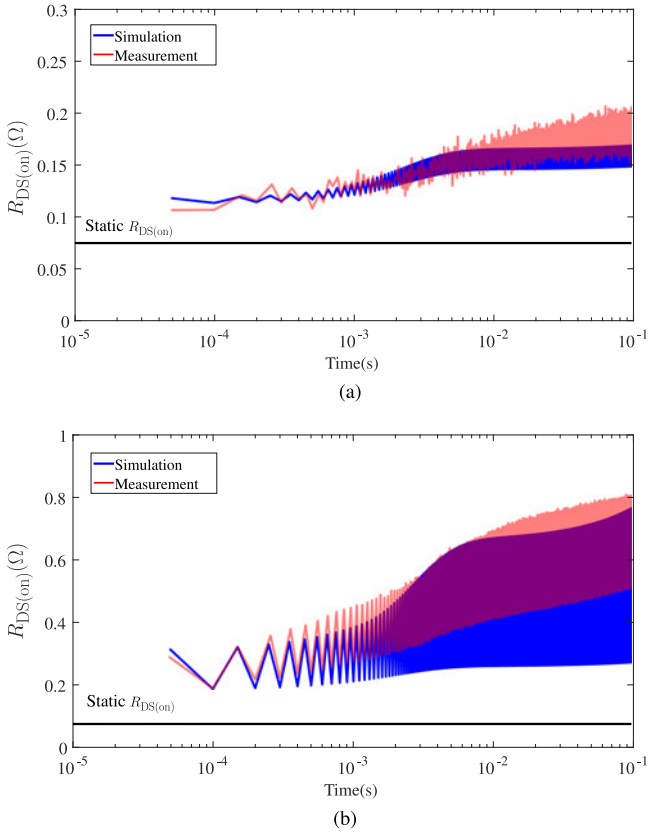

Fig. 15. Comparison between the measurement and simulation on $R_{\mathrm{DS(on)}}$ values when device switches at 80 V and 120 V (50% duty cycle). (a) Switching at 80 V. (b) Switching at 120 V.

another is that model estimates smaller $R_{\mathrm{DS(on)}}$ values ripple after each cycle, because model produces smaller $R_{\mathrm{DS(on)}}$ values variation after 50 μs detrapping time [see Fig. 12(a)].

As shown in Fig. 15(b) when biasing by a bigger voltage, device produces a bigger $R_{\mathrm{DS(on)}}$ value which reaches almost 10 times bigger than its static $R_{\mathrm{DS(on)}}$ value at the end of 0.1 s due to trapping effect. $R_{\mathrm{DS(on)}}$ ripple is bigger than that observed in the measurement results when device is biased at 80 V, which reveals a bigger influence of detrapping effect on device $R_{\mathrm{DS(on)}}$ value. Similar to the measurement results in Fig. 15(a), device $R_{\mathrm{DS(on)}}$ values keeps increasing because of the same reason.

When comparing the simulation with the measurement, the increase trend of device $R_{\mathrm{DS(on)}}$ values and $R_{\mathrm{DS(on)}}$ trapping values of each switching cycle are represented well by the model. However, the main mismatch is on device $R_{\mathrm{DS(on)}}$ detrapping values of each cycle, where notably that the model estimates a bigger $R_{\mathrm{DS(on)}}$ ripple than the measurement after 500 μs.

Despite the difference between the model and the measurement on device $R_{\mathrm{DS(on)}}$ detrapping values illustrated in Fig. 12(b), which may cause the above mismatch, it is found that characterised device $R_{\mathrm{DS(on)}}$ variation due to detrapping effect does not correspond to the values observed in each switching cycle. In Fig. 12(b), for 1 ms and 10 ms measurement curves, $R_{\mathrm{DS(on)}}$ variation after 50 μs detrapping time is about 0.4 Ω and 0.5 Ω. In contrary, at the same time range when device switches,

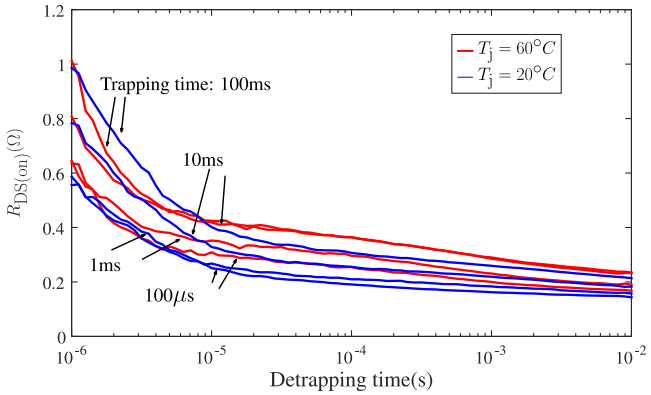

Fig. 16. Device $R_{\mathrm{DS(on)}}$ comparison of different T_{j}.

the $R_{\mathrm{DS(on)}}$ variation is only about 0.2 Ω and 0.25 Ω as shown in Fig. 15(b).

It is supposed that with the increase of the device effective $R_{\mathrm{DS(on)}}$ value, the conduction losses might increase the device junction temperature T_{j} due to the poor thermal impedance of the packaging (device mounted onto an FR4 PCB substrate, which yields a big device junction to ambient thermal resistance up to 85 °C/W found in device datasheet). The temperature difference might cause variation on charcterised device $R_{\mathrm{DS(on)}}$ values. In order to validate this hypothesis, device is characterised again at 60 °C with the same characterisation method.

B. Temperature Influence on Device $R_{\mathrm{DS(on)}}$ Values

Device $R_{\mathrm{DS(on)}}$ values at different temperatures are compared in Fig. 16. As shown in the results, device junction temperature T_{j} mainly influence on device detrapping effect, where it is illustrated that device $R_{\mathrm{DS(on)}}$ values are bigger in 60 °C than in 20 °C in the detrapping time range from 10 μs to 100 μs, which results a smaller $R_{\mathrm{DS(on)}}$ ripple. This characterisation result seems to be consistent with the obtained $R_{\mathrm{DS(on)}}$ values when device switches in Fig. 15(b).

In order to further investigate the influence of the new characterised $R_{\mathrm{DS(on)}}$ values on device switching, the parameters in the model is adjusted by using the characterised $R_{\mathrm{DS(on)}}$ values at 60 °C when device biased at 120 V. The curve fitting process is the same as described in Section III-B. The new parameters using in the model (see Table IV) and the comparison between the model and the measurement on device $R_{\mathrm{DS(on)}}$ values (see Figs. 20 and 21) are given in Appendix.

After obtaining the new parameters, the comparison between the model and the measurement on device $R_{\mathrm{DS(on)}}$ values when it switches at 120 V is shown in Fig. 17. The model estimates device $R_{\mathrm{DS(on)}}$ values more closer to the measurement than previous results in Fig. 15(b). Thus, the hypothesis that the measurement and model difference due to T_{j} difference can be validated.

Afterward, in order to validate the model in different operation conditions, the device is then switched at 80 V (90% duty cycle) and 100 V (50% duty cycle), of which the comparison between the measurement and simulation results is shown in Fig. 18. When duty cycle is 90%, device average conduction power loss increase to 1.8 times bigger than the duty

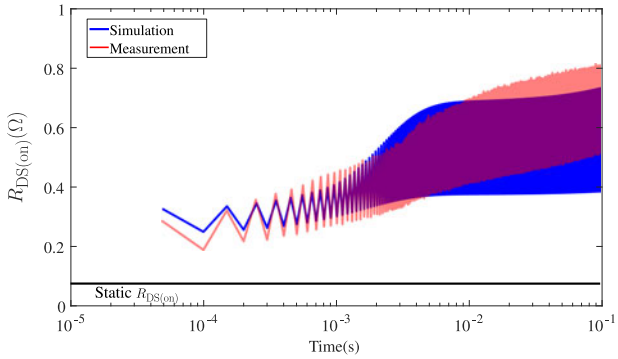

Fig. 17. Comparison between the measurement and simulation (with new parameters) on $R_{\mathrm{DS(on)}}$ values when device switches at 120 V.

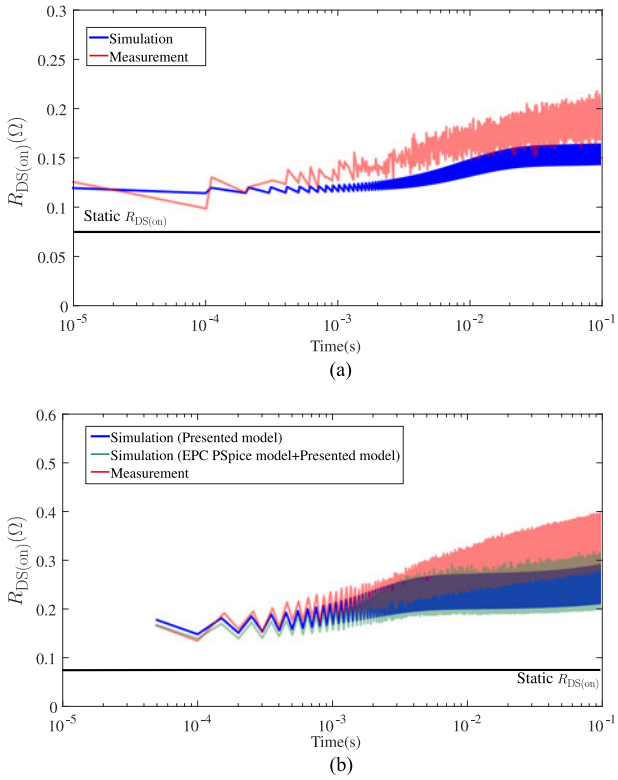

Fig. 18. Comparison between the measurement and simulation on $R_{\mathrm{DS(on)}}$ values when device switches at different voltages and duty cycles. (a) Device switches at 80 V (90% duty cycle). (b) Device switches at 100 V (50% duty cycle).

cycle is 50%, which might cause device T_{j} increase, resulting in $R_{\mathrm{DS(on)}}$ values mismatch observed in Fig. 18(a). The mismatch observed in Fig. 18(b) is supposed to be the linear interpolation method used in the model. More complexly numerical interpolation methods can be used in the model, however it might make model unsuitable for a circuit simulator. Despite some difference between the model and the measurement, $R_{\mathrm{DS(on)}}$ increase trend and values are represented in a reasonable way in the simulation.

In all the above switching operation conditions, mean value of the error between the model (with and without dynamic $R_{\mathrm{DS(on)}}$ modeling) and the measurement on $R_{\mathrm{DS(on)}}$ values is compared in Table III, where the error is defined by error $= \left|\frac{R_{\mathrm{DS(on)(measure)}} - R_{\mathrm{DS(on)(simulation)}}}{R_{\mathrm{DS(on)(measure)}}}\right|$. Without dynamic $R_{\mathrm{DS(on)}}$ modeling, device static $R_{\mathrm{DS(on)}}$ values are used in the model, which is the case of a device manufacturer SPICE model.

TABLE III
COMPARISON OF MEAN ERROR BETWEEN THE MODEL AND THE MEASUREMENT ON $R_{\mathrm{DS(on)}}$ VALUES OF DIFFERENT SWITCHING CONDITIONS

	Without dynamic $R_{\mathrm{DS(on)}}$ modeling	With dynamic $R_{\mathrm{DS(on)}}$ modeling
80 V, $D = 50\%$	56.4%	9.7%
80 V, $D = 90\%$	58.2%	17.1%
100 V, $D = 50\%$	75.4%	22.4%
120 V, $D = 50\%$	86.9%	13.4%

As shown in Table III, by adding device dynamic $R_{\mathrm{DS(on)}}$ modeling, mean error between the model and the measurement is decreased at least three times when comparing to a model with only device static $R_{\mathrm{DS(on)}}$ values, which improves the model accuracy in conduction loss calculation. Even with some difference, all the above results can validate the proposed model. The presented modeling method is then implemented in EPC2012 PSpice model offered by the manufacturer. As illustrated in Fig. 18(b), PSpice simulation shows similar results as presented model, which confirms that the presented modeling method can then be easily applied to existing GaN-HEMT models in standard SPICE simulators so as to estimate device conduction loss including trapping effect in power converters at different switching voltages and switching cycles.

In order to verify the presented method can be applied to estimate device $R_{\mathrm{DS(on)}}$ values of different GaN transistors, it is then applied to the characterised 650 V GaN transistor GS66504B, where four RC units are used to model different trapping and detrapping time constants observed in the measurement. The parameters used in the model is given in Table V, while the comparison between the model and the measurement is shown in Fig. 22 in Appendix, where it is shown in the results that the measurement is represented well by the model. The device is then switched in a power converter at 400 V/2 A (10 kHz, 50% duty cycle), of which its dynamic $R_{\mathrm{DS(on)}}$ values are measured and compared with the model in Fig. 19 after 0.1 s and 1 s. As shown in the results, device dynamic $R_{\mathrm{DS(on)}}$ increase 40% after 1 s switching operation. Device dynamic $R_{\mathrm{DS(on)}}$ increase trend and value are represented well by the model, where the difference between the simulation and the measurement is less than 5%.

Even though this device shows less dynamic $R_{\mathrm{DS(on)}}$ variation than the presented 200 V/5 A EPC GaN device in the paper, the presented modeling method is still able to represent device dynamic $R_{\mathrm{DS(on)}}$ variation trend when device switches in a power converter. This is because the model represents device dynamic $R_{\mathrm{DS(on)}}$ variation by its effective gate source voltage V_{GS} modulation, which represents dynamic $R_{\mathrm{DS(on)}}$ physical behaviour.

Some commercial GaN gate injection transistors (GIT) add additional p-GaN layer to drain electrode to suppress trapped electrons, which makes the device free from current collapse

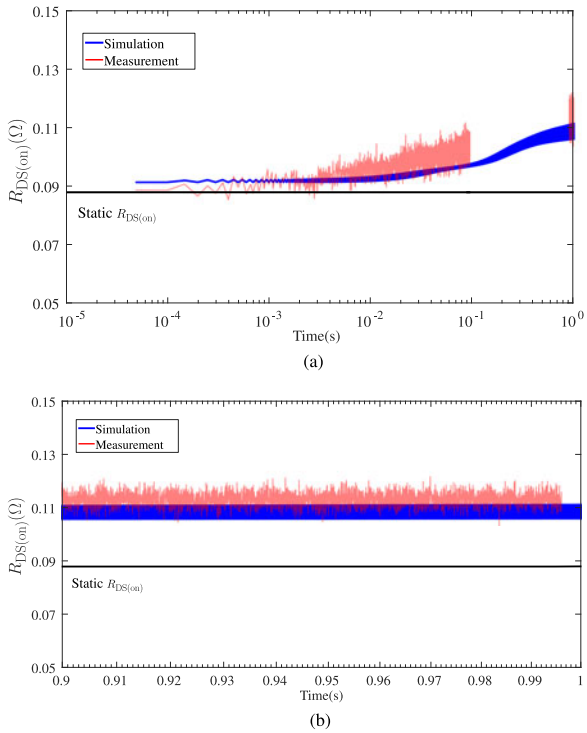

Fig. 19. Comparison between the measurement and simulation on $R_{\mathrm{DS(on)}}$ values when device GS66504B switches at 400 V/2 A (50% duty cycle). (a) Dynamic $R_{\mathrm{DS(on)}}$ values at 0.1 s. (b) Dynamic $R_{\mathrm{DS(on)}}$ values at 1 s.

[8]. However, GIT needs a constant gate current to maintain device on-state, which brings additional power losses. This additional on-state power losses of GIT might be bigger than the power losses caused by device dynamic $R_{\mathrm{DS(on)}}$ of some HEMTs in low-current application. Thus, different commercial GaN transistors of different packaging types and power ratings have different applications. The presented work in the paper to characterise and model GaN device dynamic $R_{\mathrm{DS(on)}}$ can help designers to evaluate device and choose the one suitable in their design by considering device dynamic $R_{\mathrm{DS(on)}}$ variation when device is in switching operation.

V. Conclusion

In this paper, dynamic on-state resistance ($R_{\mathrm{DS(on)}}$) values of a commercial GaN-HEMT is measured at different bias voltages by a proposed electrical circuit, which is constituted by a voltage bias circuit to control DUT trapping time and a voltage clamping circuit to measure DUT on-state voltage. Compared to other electrical characterisation circuits, this circuit has less electrical components and can be easily implemented.

It is shown in the characterisation results that both trapping and detrapping time influence device dynamic $R_{\mathrm{DS(on)}}$ values and a higher bias voltage would give rise to a higher dynamic $R_{\mathrm{DS(on)}}$ value. Based on the characterisation results, device dynamic $R_{\mathrm{DS(on)}}$ values are modeled by its static $R_{\mathrm{DS(on)}}$ values modulation by gate voltage. Thus, an equivalent circuit, which is constituted by a series of RC network, represents different trapping and detrapping time constants observed in the measurement. The model is proposed to represent device dynamic $R_{\mathrm{DS(on)}}$ values of different bias voltages and can be easily implemented in any circuit simulation software.

By comparing the model with the measurement on obtained $R_{\mathrm{DS(on)}}$ values when device switches in a power converter with different duty cycles and switching voltages, it is shown that despite some difference, the model is able to represent the measurement in a reasonable way and it estimates the trend that device $R_{\mathrm{DS(on)}}$ values keep increasing. Furthermore, the model is applicable to different power rated commercial GaN transistors. By adding device dynamic $R_{\mathrm{DS(on)}}$ modeling, mean error between the model and the measurement is decreased at least three times when comparing a model with only device static $R_{\mathrm{DS(on)}}$ values, which improves the model accuracy in conduction loss calculation. The proposed model can be easily added into manufacturer behavioural models to study GaN device trapping effect, which is normally missing.

It is also illustrated thermal influence on device dynamic $R_{\mathrm{DS(on)}}$ values, so following communications will be focused on linking device trapping model presented in the paper with device electrical-thermal model in order to estimate device dynamic $R_{\mathrm{DS(on)}}$ values in a wide temperature and switching range.

Appendix

A. Device EPC2012C Dynamic $R_{\mathrm{DS(on)}}$ Model: New parameters using in the model when using $R_{\mathrm{DS(on)}}$ measurement results when device biased at 120 V and at 60 °C are given in Table IV. The comparison between the model and the measurement on $R_{\mathrm{DS(on)}}$ values of different trapping times are shown in Fig. 20, while those of different detrapping times are shown in Fig. 21.

TABLE IV
New Parameters Using to Represent GaN-HEMT Trapping and Detrapping Effect in the Model

k_{11}	k_{21}	k_{31}	k_{41}	k_{51}	k_{61}	k_{71}
0.0158	0.0069	0.0013	0.0021	0.0023	0.0103	0.0033
C_1	C_2	C_3	C_4	C_5	C_6	C_7
1.632×10^{-7} F	5.443 F	1.04×10^{-9} F	2.33×10^{-9} F	2.76×10^{-7} F	4×10^{-5} F	0.662F
$R_{1\mathrm{t}}$	$R_{2\mathrm{t}}$	$R_{3\mathrm{t}}$	$R_{4\mathrm{t}}$	$R_{5\mathrm{t}}$	$R_{6\mathrm{t}}$	$R_{7\mathrm{t}}$
0.0124 Ω	0.111 Ω	0.001 Ω	0.001 Ω	0.0416 Ω	0.001 Ω	0.001 Ω
$R_{1\mathrm{d}}$	$R_{2\mathrm{d}}$	$R_{3\mathrm{d}}$	$R_{4\mathrm{d}}$	$R_{5\mathrm{d}}$	$R_{6\mathrm{d}}$	$R_{7\mathrm{d}}$
8.5×10^8 Ω	4.25×10^4 Ω	5.15×10^5 Ω	784.91 Ω	0.0014 Ω	2.56×10^4 Ω	4.48×10^6 Ω
k_{12}	k_{22}	k_{32}	k_{42}	k_{52}	k_{62}	k_{72}
0.0098	0.00083	0.0015	0.0013	0.0152	0.0115	0.0011

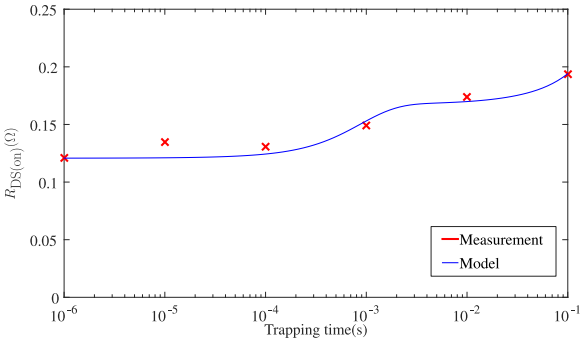

Fig. 20. Comparison between the measurement and model on dynamic $R_{\mathrm{DS(on)}}$ values as a function of trapping time at different bias V_{DS} voltages and different T_{j}. (a) $V_{\mathrm{DS}} = 80$ V. (b) $V_{\mathrm{DS}} = 120$ V ($T_{\mathrm{j}} = 60\,^{\circ}$C).

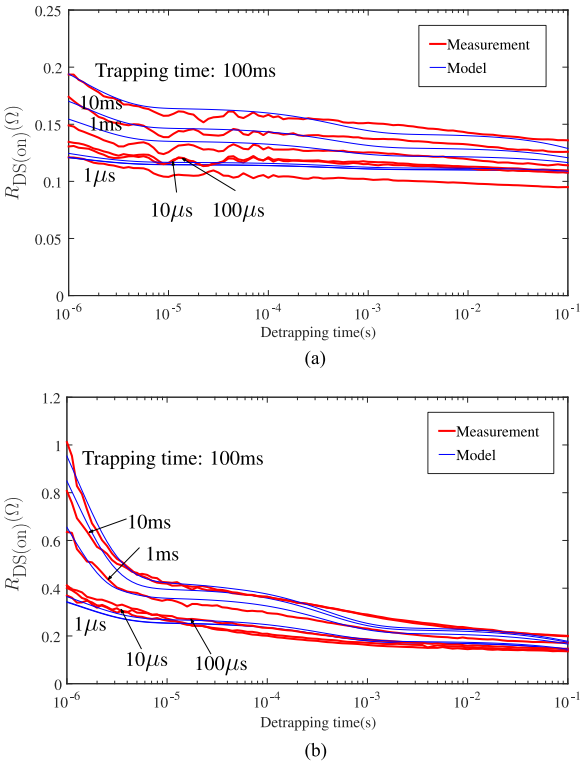

Fig. 21. Comparison between the measurement and model on dynamic $R_{\mathrm{DS(on)}}$ values as a function of detrapping time for different trapping times and at different bias V_{DS} voltages and different T_{j}. (a) $V_{\mathrm{DS}} = 80$ V. (b) $V_{\mathrm{DS}} = 120$ V ($T_{\mathrm{j}} = 60\,^{\circ}$C).

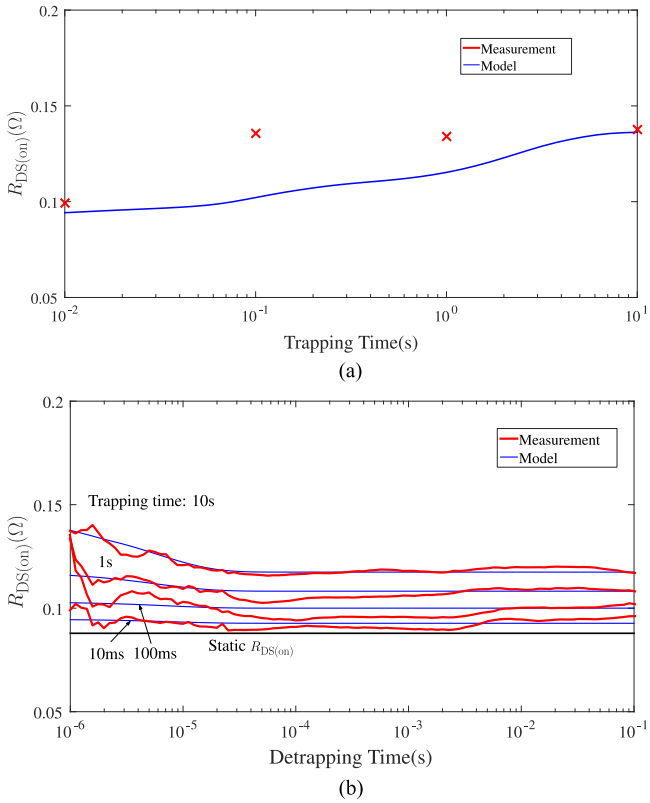

Fig. 22. Dynamic $R_{\mathrm{DS(on)}}$ comparison between the measurement and model of a 650 V/15 A device when it is biased at 400 V. (a) Dynamic $R_{\mathrm{DS(on)}}$ values of different trapping time. (b) Dynamic $R_{\mathrm{DS(on)}}$ values of different trapping and detrapping time.

TABLE V
PARAMETERS USING TO REPRESENT 600 V/15 A GAN DEVICE (GS66504B) TRAPPING AND DETRAPPING EFFECT IN THE MODEL

k_{11}	k_{21}	k_{31}	k_{41}
0.0038	0.001	0.0005	0.0039
C_1	C_2	C_3	C_4
0.097 F	0.1 F	2.3×10^{-8} F	0.014 F
$R_{1\mathrm{t}}$	$R_{2\mathrm{t}}$	$R_{3\mathrm{t}}$	$R_{4\mathrm{t}}$
0.648 Ω	14.23 Ω	2.2 Ω	0.0017 Ω
$R_{1\mathrm{d}}$	$R_{2\mathrm{d}}$	$R_{3\mathrm{d}}$	$R_{4\mathrm{d}}$
$3.35 \times 10^{4}\,\Omega$	$2.84 \times 10^{3}\,\Omega$	357.5 Ω	$1.96 \times 10^{5}\,\Omega$

B. Device GS66504B Dynamic $R_{\mathrm{DS(on)}}$ Model: It is shown in Fig. 22 the comparison between the model and the measurement on 650 V device GS66504B dynamic $R_{\mathrm{DS(on)}}$ values of different trapping and detrapping time. The parameters using in the model is given in Table V.

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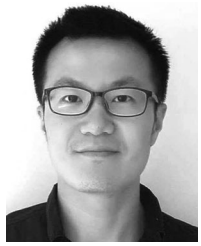

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