CCM Noninverting Buck–Boost Converter With Fast Duty-Cycle Calculation Control for Line Transient Improvement

Pang-Jung Liu, *Member, IEEE*, and Che-Wei Chang

***Abstract*—A continuous-conduction mode (CCM) noninverting buck–boost (NBB) converter with a fast duty-cycle calculation (FDCC) control and duty-cycle locking strategy is proposed in this paper. Utilizing auxiliary and adjustable slopes of the modulation signal, the FDCC control not only rapidly determines an accurate duty cycle but also keeps the compensator output constant when the input voltage changes. The theoretical dc value of the numerator of the closed-loop line-to-output voltage transfer function is equal to zero whether the CCM NBB converter operates in boost or buck mode. It indicates that adopting the FDCC control can achieve ideal feedforward compensation for CCM buck and boost operations. Consequently, the output transient ripple of the CCM NBB converter with FDCC control can be eliminated significantly regardless of the unit-gain bandwidth of the NBB converter. To alleviate pulse skipping and to avoid changing buck and boost modes frequently, a duty-cycle locking method is adopted in the transition region of the buck and the boost. Hence, the duty-cycle locking method enhances power conversion and maintains the output voltage. The experimental results demonstrate that the proposed control schemes not only effectively reduce the line transient ripple but also obtain high efficiency in a wide range of input voltage.**

***Index Terms*—Boost converter, buck converter, buck–boost converter, efficiency, line transient response.**

I. Introduction

DUE to a wide range of operating input voltage, the buck–boost topology is an appropriate choice for battery-powered power supplies, telecommunication systems, power factor correction (PFC) applications, and fuel-cell power systems [1]–[3]. Several basic converters are capable of performing both buck and boost operations, depending on the output and input voltage relationship, such as inverting buck–boost, single-ended primary-inductance (SEPIC), Cuk, and noninverting buck–boost (NBB) converters [4]–[6]. The NBB converter shown in Fig. 1 is widely used because of the positive output voltage, lower voltage stress of the components, and single inductor and output capacitor [7]–[10].

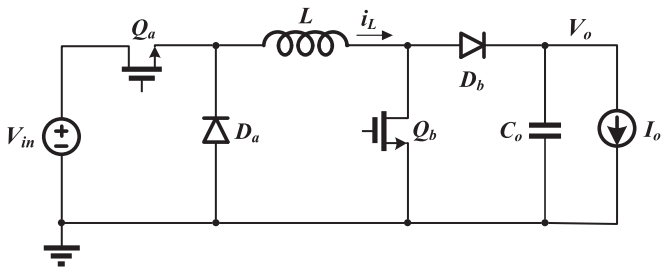

Fig. 1. NBB converter.

Two active switches Q_a and Q_b are employed in the NBB converter, which provide flexible control methods. For instance, when Q_a and Q_b are turned on and off concurrently, the NBB converter works in the buck–boost mode. If Q_b remains off and Q_a is sequentially turned on and off, the NBB converter operates in buck mode. The NBB converter performs in boost mode when Q_a remains on and Q_b is sequentially switched on and off.

If the continuous-conduction mode (CCM) NBB converter operates in buck–boost mode when the input voltage $V_{\rm in}$ approaches the output voltage V_o, based on the inductor volt-second balance method, the average inductor current $i_{L,\rm avg}$ can be expressed as $I_o/(1-d)$, where the duty cycle d is about 0.5. Hence, the value of $i_{L,\rm avg}$ is around twice as large as that of the output current. For the same conditions of the input and output voltage, if the NBB converter works in boost mode, $i_{L,\rm avg}$ is equal to $I_o/(1-d)$, but the duty cycle in this case is close to zero. Therefore, the values of $i_{L,\rm avg}$ and I_o are the same when $d=0$. When the NBB converter operates in buck mode, $i_{L,\rm avg}$ is always equal to I_o. The relationships of the average inductor current and the output current in three operation modes are given in Fig. 2. When the NBB converter works in buck–boost mode, the value of average inductor current is larger than that when operating in buck and boost modes, resulting in larger power losses and output voltage ripples. Thus, it is essential to prevent the NBB converter from operating in buck–boost mode to achieve high efficiency in a wide range of input voltage.

In the battery-powered system or PFC applications, the input voltage varies with battery status or sinusoidal input voltage. Moreover, to increase reliability, flexibility, and

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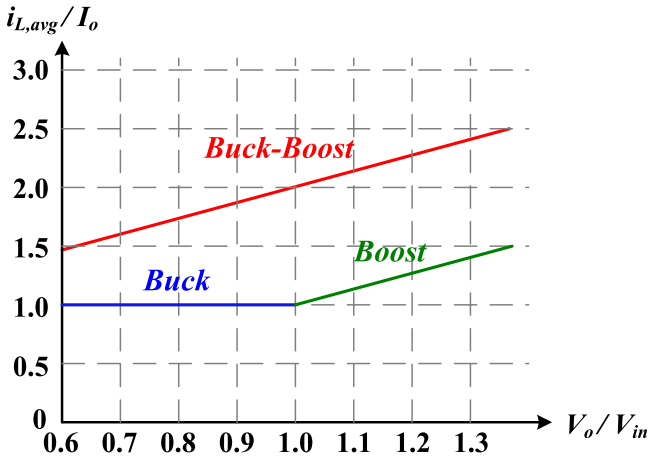

Fig. 2. Relationships of the average inductor current and output current in three operation modes.

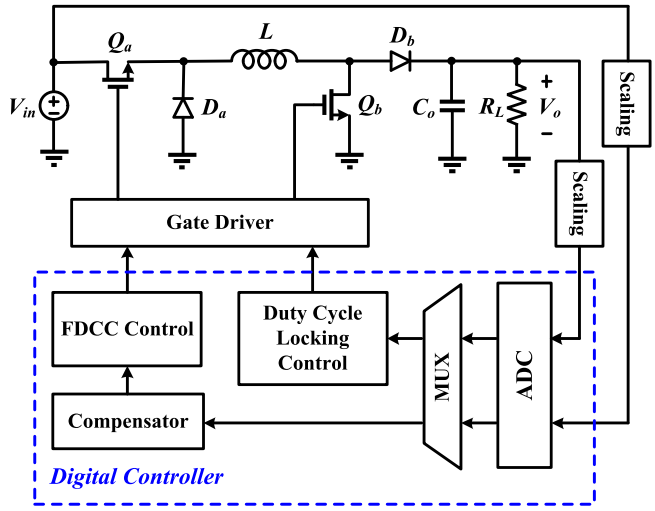

Fig. 3. Block diagram of the proposed NBB converter.

utilization, multiple input sources are allowed in application systems such as laptop computers, smartphones, and telecommunication power systems [11], [12]. The different sources such as batteries, power grids, photovoltaic cells, and fuel cells have different voltage and current characteristics. Thus, when users switch to different input sources, the power converters would suffer from sudden input voltage change. Hence, the NBB converter also requires adequate line transient response to prevent large output transient ripples when the input voltage varies. Many studies had presented different approaches to enhance the line transient response of a converter [13]–[25]. Peak current mode control and average current mode control are adopted to enhance the bandwidth of the NBB converter [13]–[18]. The output transient ripple caused by input voltage change can be diminished, but current sensing mechanism is required, which causes additional power losses. Combination of buck and boost modes of the NBB converter is employed to distribute the output voltage transients [19], but the output transient ripples cannot be fully eliminated with this control scheme. To improve the line transient response of a dc–dc converter, a sampling signal of the input voltage connected to the inverting pin of an error amplifier is proposed in [21], [22]. However, this simple control method doesn't include a path of output voltage feedback, so the output voltage is only determined by the amplitude of the modulation signal. The valley and peak values of the sawtooth signal vary with the input voltage in boost and buck modes, respectively. Then, smooth transition of the NBB converter can be implemented [24], [25]. However, the sawtooth generator needs careful design; additional control blocks and a mode detector increase the complexity of the control design.

In this paper, a CCM NBB converter with a fast duty-cycle calculation (FDCC) control algorithm is presented. The FDCC control includes auxiliary slopes that are related to the input and output voltages. When the input voltage changes, utilizing the modulation signal and auxiliary slopes can rapidly determine an expected duty cycle. Therefore, fast-line transient response of the NBB converter is achieved. The NBB converter avoids operating in buck–boost modes to keep high conversion efficiency in a wide range of input voltage. In Section II, the proposed NBB converter with the FDCC control is addressed. Section III introduces the frequency response of the proposed NBB converter. Finally, experimental results and conclusions are drawn in Sections IV and V, respectively.

II. CCM NBB Converter with Proposed Control Schemes

A CCM NBB converter with the proposed control schemes is shown in Fig. 3. To enhance power conversion efficiency, the NBB converter operates in buck or boost mode only. In buck mode, the switch Q_a is controlled to adjust the output voltage V_o and the switch Q_b is always turned off when the input voltage $V_{\rm in}$ is equal to or larger than the output voltage. In boost mode, Q_a is always turned on and Q_b is controlled to adjust V_o when $V_{\rm in}$ is smaller than V_o. Hence, the output voltage of NBB converter in two operating modes is formulated as

$$V_o = \begin{cases} d_a V_{\rm in}, & d_b = 0 \text{ for buck mode} \\ \frac{V_{\rm in}}{1-d_b}, & d_a = 1 \text{ for boost mode} \end{cases} \quad (1)$$

where d_a and d_b are the duty cycles of switches Q_a and Q_b, respectively. To achieve fast-line transient, FDCC control adopts auxiliary slopes, which include the input voltage, output voltage and output of the compensator. Utilizing the modulation signal and auxiliary slopes can quickly determine an accurate duty cycle when the input voltage changes. Therefore, an adjustment amount of the compensator output can be eliminated effectively, and thus fast-line transient response of the CCM NBB converter is accomplished. The FDCC control and duty-locking strategy are described in the following sections.

A. Compensator Response With PWM Control

Before the FDCC control is introduced, the compensator response with PWM control is reviewed for the case where the input voltage varies, as shown in Fig. 4. V_H and V_L represent the maximum and the minimum values of the sawthooth signal, respectively. When the input voltage drops, the output voltage

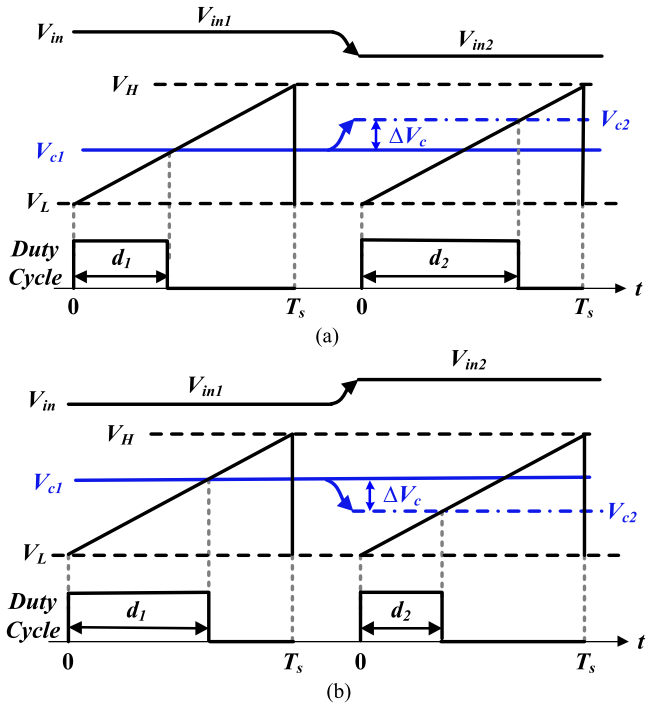

Fig. 4. Compensator response with PWM control when the input voltage (a) drops and (b) rises.

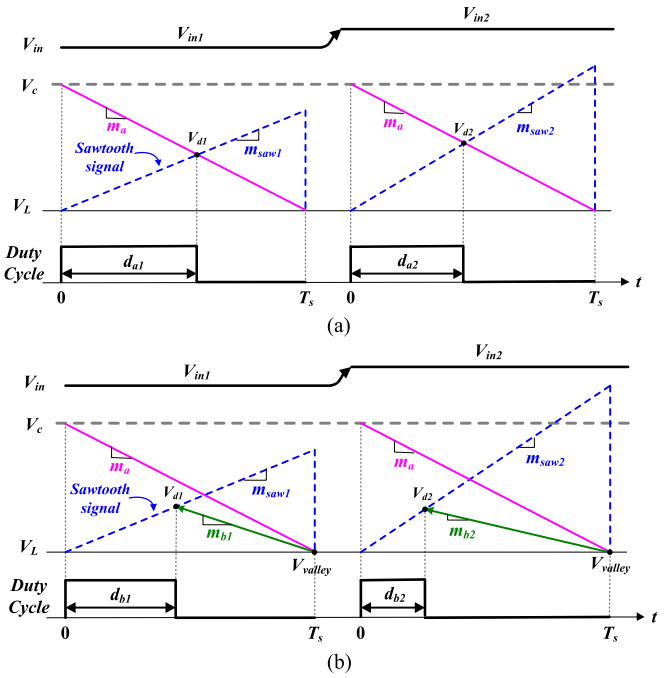

Fig. 5. Compensator response with FDCC control in (a) buck and (b) boost modes when the input voltage rises.

also decreases. Through the voltage-mode PWM feedback path, the compensator output slowly rises from V_{c1} to V_{c2} to approach the expected duty cycle. However, owing to large compensation capacitance at the output node of the compensator and a large adjustment amount ΔV_c, it takes a long time for a converter to adjust the output voltage back to the nominal value. Similarly, when the input voltage rises, it takes a long time to regulate the compensator output to be V_{c2}, as shown in Fig. 4(b). Hence, the FDCC control is required to immediately adjust the duty cycle to minimize the adjustment amount of the compensator output. Based on Fig. 4, the relationship between the modulation signal and the compensator output V_c can be calculated in buck and boost modes as

$$\begin{cases} V_{c,\text{buck}} = \frac{V_o}{V_{\text{in}}} V_M + V_L \\ V_{c,\text{boost}} = \left(1 - \frac{V_o}{V_{\text{in}}}\right) V_M + V_L \end{cases} \quad \text{where } V_M = V_H - V_L. \tag{2}$$

When the input voltage changes from $V_{\text{in}1}$ to $V_{\text{in}2}$, ΔV_c in both modes can be expressed as

$$\begin{cases} \Delta V_{c,\text{buck}} = V_M V_o \left(\frac{1}{V_{\text{in}2}} - \frac{1}{V_{\text{in}1}}\right) \\ \Delta V_{c,\text{boost}} = \frac{V_M}{V_o} \left(V_{\text{in}1} - V_{\text{in}2}\right) \end{cases}. \tag{3}$$

After the changes of the input voltage are known, the corresponding adjustment amount of the compensator output will be determined.

B. Compensator Response With FDCC Control

To perform FDCC control in buck mode, the sawtooth signal V_{saw} with variable slope m_{saw} and an auxiliary slope m_a is added, as shown in Fig. 5(a). The slope m_{saw} is proportional to the difference between the input and output voltages, while the slope m_a is proportional to the output voltage. Since the slope m_{saw} varies with the input voltage, subscripts 1 and 2 represent the different values of m_{saw} when the input voltage is equal to $V_{\text{in}1}$ and $V_{\text{in}2}$, respectively. d_{a1} represents the duty cycle of switch Q_a when the input voltage is $V_{\text{in}1}$. The steady-state duty cycle can be calculated with the sawtooth signal and auxiliary slope. Since the sawtooth signal and auxiliary slope m_a intersects at V_{d1}, the corresponding duty cycle is d_{a1}. When the input voltage rises, the slope of the sawtooth signal instantly becomes $m_{\text{saw}2}$, and then the new intersection voltage V_{d2} can be quickly calculated with the auxiliary slope. Hence, the new duty cycle d_{a2} is determined immediately and accurately to keep a regulated output voltage. Since the compensator output V_c is kept constant, the fast-line transient response of the NBB converter operating in buck mode can be realized. The more detailed analysis and equations are described in the next section.

For operating in boost mode with FDCC control, the sawtooth signal V_{saw} with variable slope m_{saw} and two auxiliary slopes m_a and m_b are added, as shown in Fig. 5(b). Since the output voltage of the NBB converter in boost mode is a nonlinear function of the duty cycle, two auxiliary slopes are required to obtain an accurate duty cycle and minimize the variation of the compensator output. The slopes m_{saw}, m_a, and m_b are proportional to the input voltage, the output voltage, and the difference between the output and input voltages, respectively.

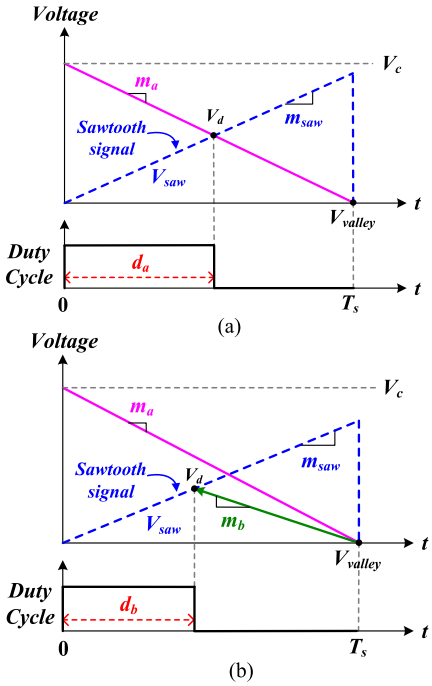

Fig. 6. CCM NBB converter with FDCC control in (a) buck mode and (b) boost mode at steady state.

Since the slopes $m_{\rm saw}$ and m_b vary with the input voltage, subscripts 1 and 2 represent the different values of $m_{\rm saw}$ and m_b when the input voltage is equal to $V_{\rm in1}$ and $V_{\rm in2}$, respectively. d_{b1} represents the duty cycle of switch Q_b when the input voltage is $V_{\rm in1}$. First, the value of the voltage $V_{\rm valley}$ can be obtained from the compensator output V_c, the slope m_a, and the switching period T_s. Then, the intersection voltage V_{d1} and steady-state duty cycle d_{b1} can be calculated from the slopes of $m_{\rm saw1}$ and m_{b1}. When the input voltage rises from $V_{\rm in1}$ to $V_{\rm in2}$, V_c is not changed, and the slopes $m_{\rm saw}$, m_a, and m_b are increased, fixed, and decreased, respectively. Thus, the duty cycle d_{b2} can be calculated rapidly and accurately with $m_{\rm saw2}$ and m_{b2}. Since V_c is maintained at the same value, the fast-line transient response of the NBB converter in boost mode can be realized.

C. Analysis of FDCC Control

For the CCM NBB converter with FDCC control in buck mode, as shown in Fig. 6(a), the auxiliary slope m_a and the slope $m_{\rm saw}$ of sawtooth signal are set as

$$m_a = -\alpha V_o \tag{4}$$

$$m_{\rm saw} = \beta\left(V_{\rm in} - V_o\right) \tag{5}$$

where α and β are constant values per unit time. The compensator output V_c and intersection voltage V_d can be expressed as

$$V_c = V_{\rm valley} + \alpha V_o T_s \tag{6}$$

$$V_d = V_c + m_a d_a T_s = 0 + m_{\rm saw} d_a T_s. \tag{7}$$

By substituting (4) to (6) into (7), the duty cycle can be derived as

$$d_a = \left[V_{\rm valley} + \alpha V_o T_s\right] \times \frac{1}{\left[\beta\left(V_{\rm in} - V_o\right) + \alpha V_o\right] T_s}. \tag{8}$$

At steady state, the duty cycle with FDCC control should be equal to that of the conventional voltage conversion with PWM control, and $V_{\rm valley}$ is set to zero for the inductor voltage-second balance. Hence, a conditional equation can be obtained as

$$\left(\alpha - \beta\right) V_{\rm in} V_o = \left(\alpha - \beta\right) {V_o}^2. \tag{9}$$

In order for (9) to hold, α and β should be identical. If $V_{\rm valley}$ is not zero, $V_{\rm valley}$ can be substituted using (6) and then (8) can be rewritten as

$$d_a = \frac{V_o}{V_{\rm in}} + \frac{V_c - \alpha V_o T_s}{\beta V_{\rm in} T_s}. \tag{10}$$

For the buck mode at steady state, d_a is equal to $V_o/V_{\rm in}$, so the second term on the right-hand side of (10) should be zero because of inductor voltage–second balance. It is noted that V_c will change to compensate the voltage drops in the components of the power stage under different load currents. To minimize the V_c variation, α can be set as

$$\alpha = \frac{V_{c,\rm buck}}{V_o T_s} \tag{11}$$

where $V_{c,\rm buck}$ is the middle value of the compensator output region when the NBB converter operates in buck mode. Similarly, for the CCM NBB converter with FDCC control in the boost mode, as shown in Fig. 6(b), the slope $m_{\rm saw}$ of sawtooth signal and two auxiliary slopes m_a and m_b are set as

$$m_{\rm saw} = \beta V_{\rm in} \tag{12}$$

$$m_a = -\alpha V_o \tag{13}$$

$$m_b = \gamma\left(V_{in} - V_o\right) \tag{14}$$

where α, β, and γ are per unit time values. The valley and intersection voltages $V_{\rm valley}$ and V_d can be expressed, respectively, as

$$V_{\rm valley} = V_c - \alpha V_o T_s \tag{15}$$

$$V_d = V_{\rm valley} - m_b\left(1 - d_b\right) T_s = 0 + m_{\rm saw} d_b T_s. \tag{16}$$

By substituting (12) to (15) into (16), the duty cycle can be derived as

$$d_b = \left[V_{\rm valley} - \gamma\left(V_{\rm in} - V_o\right) T_s\right] \times \frac{1}{\left(\beta V_{\rm in} - \gamma V_{\rm in} + \gamma V_o\right) T_s}. \tag{17}$$

The duty cycle with FDCC control in steady state should be equal to that of the conventional voltage conversion with PWM control, and $V_{\rm valley}$ is zero when the inductor voltage-second balance is satisfied. Hence, a conditional equation can be obtained as

$$V_o V_{\rm in}\left(\beta - \gamma\right) = {V_{\rm in}}^2\left(\beta - \gamma\right). \tag{18}$$

Fig. 7. Relationship between mode operation and input voltage.

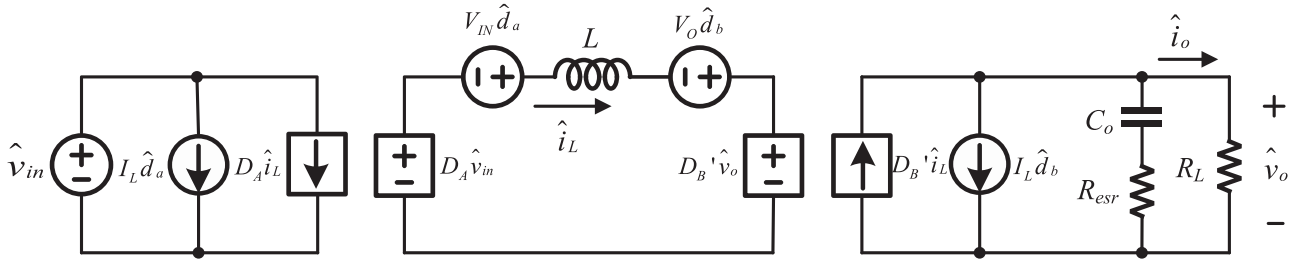

Fig. 8. Small-signal model of the CCM NBB converter.

In order for (18) to hold, β and γ should be identical. If $V_{\rm valley}$ is not zero, (17) can be rewritten as

$$d_b = \frac{V_o - V_{\rm in}}{V_o} + \frac{V_c - \alpha V_o T_s}{\beta V_o T_s}. \tag{19}$$

For the boost mode in steady state, d_b is equal to $(V_o - V_{\rm in})/V_o$, so the second term on the right-hand side of (19) should be zero because of inductor voltage-second balance. To minimize the V_c variation, α can be set as

$$\alpha = \frac{V_{c,\rm boost}}{V_o T_s} \tag{20}$$

where $V_{c,\rm boost}$ is the middle value of the compensator output region when the NBB converter operates in boost mode. The numerator $(V_c - \alpha V_o T_s)$ of the second term in (10) and (19) can be treated as an adjustment amount ΔV_c of the compensator output. Compared with (3), the ΔV_c with FDCC control is much smaller than that with PWM control. Hence, the FDCC control improves the line transient response of the NBB converter on the disturbance of the input voltage.

D. Duty-Cycle Locking Method

When the input voltage approaches the output voltage, the NBB converter will suffer pulse skipping phenomenon due to a time delay between the controller's output and the power transistor's gate [1], [7], [26]. For analog PWM scheme, the major time delay results from propagation delay of the PWM comparator and rising/falling time of the gate driver for switches [1], [26]. Due to the time delay, the duty cycles of switches Q_a and Q_b have jumps from maximum and minimum effective duty cycles $d_{\max}$ and $d_{\min}$ to 100% and 0%. Hence, a dead zone is formed around the transitions between the buck and the boost modes. The dead zone causes uncontrolled pulse skipping, leading to increased output voltage ripple and additional power losses.

Since digital PWM scheme is employed in this work, the major time delay is constrained by the rising/falling time of the gate driver only. Therefore, the range of dead zone can be diminished. To alleviate pulse skipping and to avoid changing the buck and the boost modes frequently, a duty-cycle locking method is adopted in the transition region of the buck and the boost, as shown in Fig. 7. When the input voltage $V_{\rm in}$ is between the voltages V_A and V_B, the NBB converter operates in the duty-cycle locking mode. On the other hand, the NBB converter operates in the buck or boost mode based on the $V_{\rm in}$ value. In the duty-cycle locking region, the switches Q_a and Q_b are kept on and off, respectively, which represents input power directly transfers to load. While considering the turn-on resistance of the switch Q_a, the equivalent series resistance of the inductor, and the forward voltage of the diode D_b, the voltage V_A and V_B are set as 20.6 and 19.9 V, respectively. Although the output voltage has a slight offset, which is less than $\pm 2\%$, the simple control method enhances the power conversion and maintains the output voltage.

III. FDCC Control Scheme for the CCM NBB Converter

A. Derivation of Small-Signal Model of the NBB Converter

According to the averaged switch modeling method, the small-signal model of the power stage is shown in Fig. 8 [27], [28], where $D_B' = (1 - D_B)$. In Fig. 8, the upper-case letters represent dc terms, and the lower-case letters with hat represents small-signal ac terms. As shown in (1), by setting $D_B = 0$ and $\hat{d}_b = 0$ in the small-signal model of the NBB converter, the small-signal model in buck mode is obtained. Then, the transfer functions of the line-to-output voltage $G_{vin,\rm buck}(s)$ and duty cycle-to-output voltage $G_{vd,\rm buck}(s)$ can be calculated as [29]

$$\begin{aligned} G_{vin,\rm buck}(s) &= \left.\frac{\hat{v}_o}{\hat{v}_{\rm in}}\right|_{\hat{d}_a = 0} \\ &= D_A \frac{1 + sC_oR_{\rm esr}}{s^2 LC_o\left(1 + R_{\rm esr}/R_L\right) + s\left(C_oR_{\rm esr} + L/R_L\right) + 1} \end{aligned} \tag{21}$$

$$G_{vd,\mathrm{buck}}(s) = \left.\frac{\hat{v}_o}{\hat{d}_a}\right|_{\hat{v}_{\mathrm{in}}=0} = \frac{V_O}{D_A}\frac{1+sC_oR_{\mathrm{esr}}}{s^2LC_o\left(1+R_{\mathrm{esr}}/R_L\right)+s\left(C_oR_{\mathrm{esr}}+L/R_L\right)+1}. \tag{22}$$

Similarly, as shown in (1), by setting $D_A = 1$ and $\hat{d}_a = 0$ in the small-signal model of the NBB converter, the small-signal model in boost mode is derived. The transfer functions of the line-to-output voltage $G_{v\mathrm{in},\mathrm{boost}}(s)$ and duty cycle-to-output voltage $G_{vd,\mathrm{boost}}(s)$ can be formulated as

$$G_{v\mathrm{in},\mathrm{boost}}(s) = \left.\frac{\hat{v}_o}{\hat{v}_{\mathrm{in}}}\right|_{\hat{d}_b=0} = \frac{1}{D_B{}'}\frac{(1+s/\omega_{\mathrm{esr}})}{1+2\xi s/\omega_0+s^2/{\omega_0}^2}$$

$$\text{where } D'_B = 1-D_B, \omega_0 = \frac{D'_B}{\sqrt{LC_o\left(1+R_{\mathrm{esr}}/R_L\right)}},$$

$$\xi = \frac{\mathrm{L}+C_oR_{\mathrm{esr}}R_LD'_B{}^2}{2D'_B\sqrt{LC_o\left({R_L}^2+R_{\mathrm{esr}}R_L\right)}}, \omega_{\mathrm{esr}} = \frac{1}{C_oR_{\mathrm{esr}}} \tag{23}$$

$$G_{vd,\mathrm{boost}}(s) = \left.\frac{\hat{v}_o}{\hat{d}_b}\right|_{\hat{v}_{\mathrm{in}}=0} = \frac{V_O}{D'_B}\frac{(1-s/\omega_{\mathrm{RHPZ}})(1+s/\omega_{\mathrm{esr}})}{1+2\xi s/\omega_0+s^2/{\omega_0}^2}$$

$$\text{where } \omega_{\mathrm{RHPZ}} = \frac{{D'_B}^2R_L}{L}. \tag{24}$$

B. Derivation of Small-Signal Model of the FDCC Control

According to the averaged switch modeling approach, the average values of duty cycle and voltage include dc and ac terms, so V_d shown in Fig. 6(a) can be written as

$$\begin{aligned} V_d &= V_D+\hat{v}_d \\ &= V_C+\hat{v}_c-\alpha\left(V_O+\hat{v}_o\right)\left(D_A+\hat{d}_a\right)T_s \\ &= \beta\left(V_{\mathrm{IN}}+\hat{v}_{\mathrm{in}}-V_O-\hat{v}_o\right)\left(D_A+\hat{d}_a\right)T_s. \end{aligned} \tag{25}$$

Since the ac variations are much smaller than the dc values, the nonlinear ac terms can be neglected. Thus, the small signal of the compensator output in (25) can be derived as

$$\begin{aligned} \hat{v}_c = {}& \hat{d}_a\left(\beta V_{\mathrm{IN}}T_s-\beta V_OT_s+\alpha V_OT_s\right) \\ & +\beta\hat{v}_{\mathrm{in}}D_AT_s-\hat{v}_o\left(\beta D_AT_s+\alpha D_AT_s\right). \end{aligned} \tag{26}$$

Based on Section II-C for operating in buck mode, α is equal to β, so the transfer functions of modulation gain $G_{\mathrm{mod},\mathrm{buck}}(s)$ and feedforward gain $G_{ff,\mathrm{buck}}(s)$ can be formulated as

$$G_{\mathrm{mod},\mathrm{buck}}(s) = \left.\frac{\hat{d}_a}{\hat{v}_c}\right|_{\hat{v}_{\mathrm{in}}=0,\hat{v}_o=0} = \frac{1}{\beta V_{\mathrm{IN}}T_s} \tag{27}$$

$$G_{ff,\mathrm{buck}}(s) = \left.\frac{\hat{d}_a}{\hat{v}_{\mathrm{in}}}\right|_{\hat{v}_c=0,\hat{v}_o=0} = -\frac{D_A}{V_{\mathrm{IN}}}. \tag{28}$$

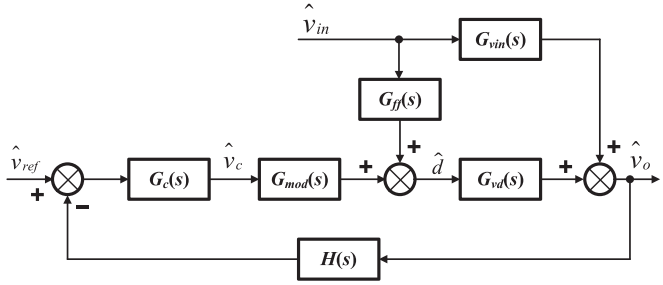

Fig. 9. General small-signal block diagram of the NBB converter with FDCC control.

Likewise, V_d shown in Fig. 6(b) can be expressed as

$$\begin{aligned} V_d &= V_D+\hat{v}_d \\ &= V_C+\hat{v}_c-\alpha\left(V_O+\hat{v}_o\right)T_s \\ &\quad +\gamma\left(V_O+\hat{v}_o-V_{\mathrm{IN}}-\hat{v}_{\mathrm{in}}\right)\left(1-D_B-\hat{d}_b\right)T_s \\ &= \beta\left(V_{\mathrm{IN}}+\hat{v}_{\mathrm{in}}\right)\left(D_B+\hat{d}_b\right)T_s. \end{aligned} \tag{29}$$

By neglecting the nonlinear ac terms, the small signal of the compensator output in (29) can be obtained as

$$\begin{aligned} \hat{v}_c = {}& \hat{d}_b\left(\gamma\left(V_O-V_{\mathrm{IN}}\right)T_s+\beta V_{\mathrm{IN}}T_s\right) \\ & +\hat{v}_{\mathrm{in}}\left(\gamma\left(1-D_B\right)T_s+\beta D_BT_s\right) \\ & -\hat{v}_o\left(-\alpha T_s+\gamma\left(1-D_B\right)T_s\right). \end{aligned} \tag{30}$$

Based on Section II-C for operating in boost mode, β is equal to γ, so the transfer functions of modulation gain $G_{\mathrm{mod},\mathrm{boost}}(s)$ and feedforward gain $G_{ff,\mathrm{boost}}(s)$ can be formulated as

$$G_{\mathrm{mod},\mathrm{boost}}(s) = \left.\frac{\hat{d}_b}{\hat{v}_c}\right|_{\hat{v}_{\mathrm{in}}=0,\hat{v}_o=0} = \frac{1}{\gamma V_OT_s} \tag{31}$$

$$G_{ff,\mathrm{boost}}(s) = \left.\frac{\hat{d}_b}{\hat{v}_{\mathrm{in}}}\right|_{\hat{v}_c=0,\hat{v}_o=0} = -\frac{1}{V_O}. \tag{32}$$

C. Line-to-Output Voltage Transfer Function of the CCM NBB Converter with FDCC Control

The general small-signal block diagram of the NBB converter with FDCC control is shown in Fig. 9. The block diagram includes the feedback network $H(s)$, the compensator $G_c(s)$, the modulation gain $G_{\mathrm{mod}}(s)$, the feedforward gain $G_{ff}(s)$, the line-to-output voltage $G_{v\mathrm{in}}(s)$, and the duty cycle-to-output voltage $G_{vd}(s)$. $G_{v\mathrm{in}}(s)$, $G_{vd}(s)$, $G_{\mathrm{mod}}(s)$, and $G_{ff}(s)$ are derived in (21)–(24), (27), (28), (31), and (32), respectively, when the NBB converter operates in buck mode and boost mode. Based on Fig. 9, the loop gain of the NBB converter can be written

$$T(s) = G_c(s)G_{\mathrm{mod}}(s)G_{vd}(s)H(s). \tag{33}$$

TABLE I
DESIGN PARAMETERS OF THE NBB CONVERTER

Input dc voltage, $V_{\rm in}$	12−30 V
Output voltage, V_o	19 V
Rated output current, I_o	5 A
Switching frequency, f_s	100 kHz
Switches, Q_a and Q_b	IRFZ34NL
Diodes, D_a and D_b	MBR1645
Output inductor, L	76 μH
Output capacitor, C_o	200 μF
Feedback network, H	0.1112
Modulation gain, $G_{\rm mod,buck}$	0.2932
Modulation gain, $G_{\rm mod,boost}$	0.3858

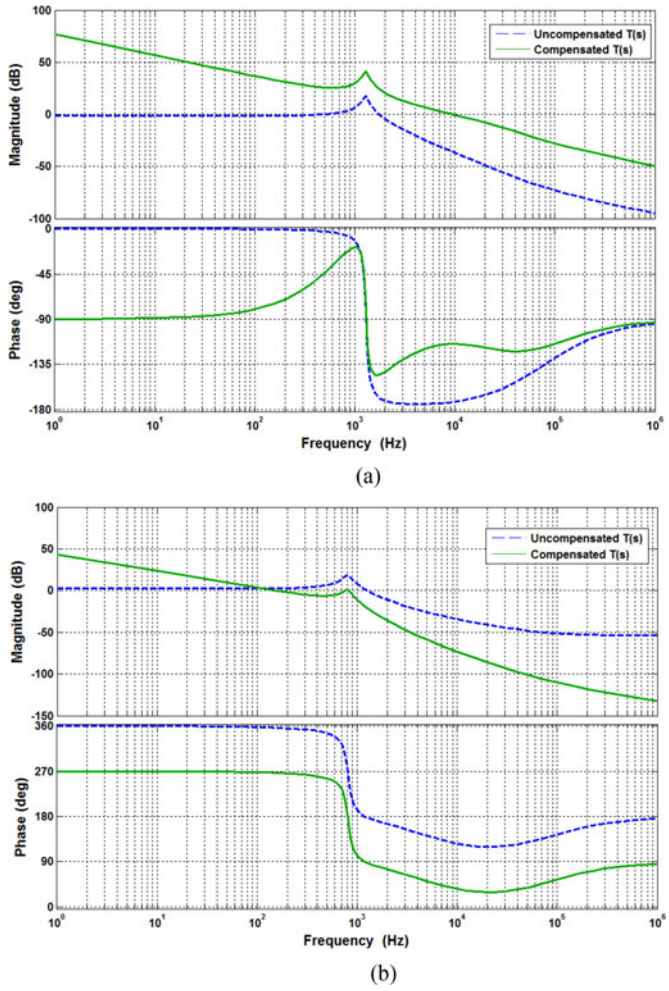

Fig. 10. Bode plots of the loop gain for (a) buck mode ($V_{\rm in}$ = 30 V) and (b) boost mode ($V_{\rm in}$ = 12 V).

By setting $G_c(s) = 1$ and substituting $G_{vd}(s)$ and $G_{\rm mod}(s)$ into (33), the uncompensated loop gains $T_{u,{\rm boost}}(s)$ and $T_{u,{\rm buck}}(s)$ in boost and buck modes can be obtained, respectively. Based on the parameters of the prototype listed in Table I, the bode plots of the uncompensated loop gain in buck and boost modes are given with dashed lines in Fig. 10. Compared with $T_{u,{\rm buck}}(s)$, $T_{u,{\rm boost}}(s)$ has an additional right-half-plan (RHP)

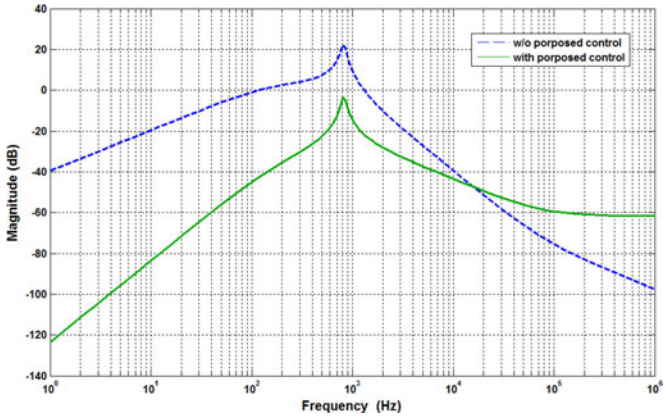

Fig. 11. Bode plots of the closed-loop line-to-output voltage transfer function for boost mode ($V_{\rm in}$ = 12 V).

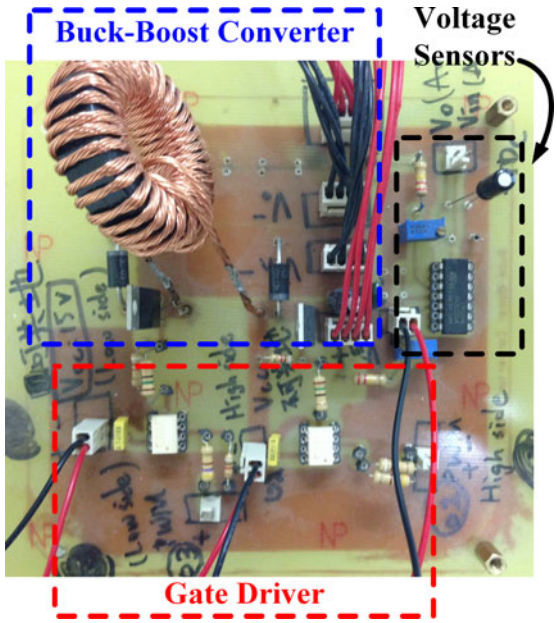

Fig. 12. Experimental prototype.

zero $\omega_{\rm RHPZ}$ described in (24). For $T_{u,{\rm boost}}(s)$ with the minimum input voltage and rated load current, the ratios of $\omega_{\rm RHPZ}$ to the complex poles ω_0 and ESR zero $\omega_{\rm esr}$ to $\omega_{\rm RHPZ}$ are 3.9 and 25.2, respectively. In other words, $\omega_{\rm RHPZ}$ is closer to ω_0 and $\omega_{\rm esr}$ is far away from $\omega_{\rm RHPZ}$. Hence, the PID and dominant pole compensations are used for buck and boost modes, respectively, and the bode plot of the compensated loop gain are shown with solid lines in Fig. 10.

Based on Fig. 9, the disturbance $\hat{v}_{\rm in}$ influences the output voltage through two paths. One is $G_{vin}(s)$ generated from the power stage, and the other is $G_{ff}(s)$ produced from the FDCC control, so the closed-loop line-to-output voltage transfer function can be expressed as

$$T_{vin}(s) = \frac{\hat{v}_o}{\hat{v}_{\rm in,\ closed-loop}} = \frac{(G_{vin}(s) + G_{ff}(s)G_{vd}(s))}{1 + T(s)}. \tag{34}$$

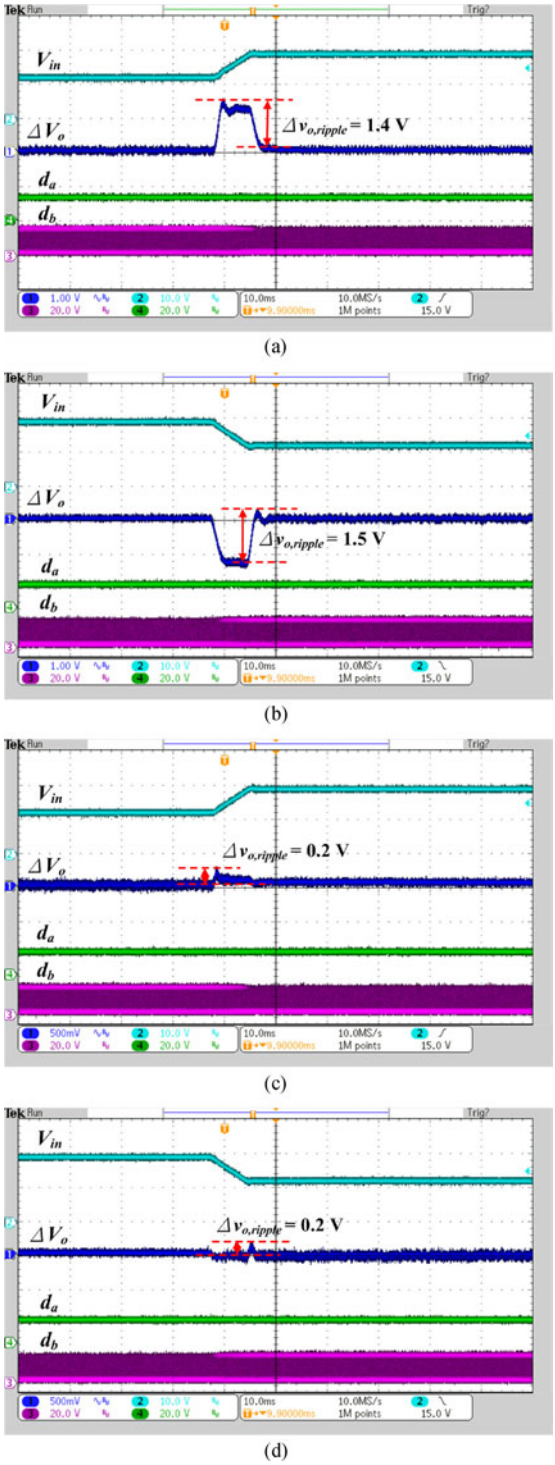

Fig. 13. Line transient responses in boost mode (a) and (b) without and (c) and (d) with the FDCC control.

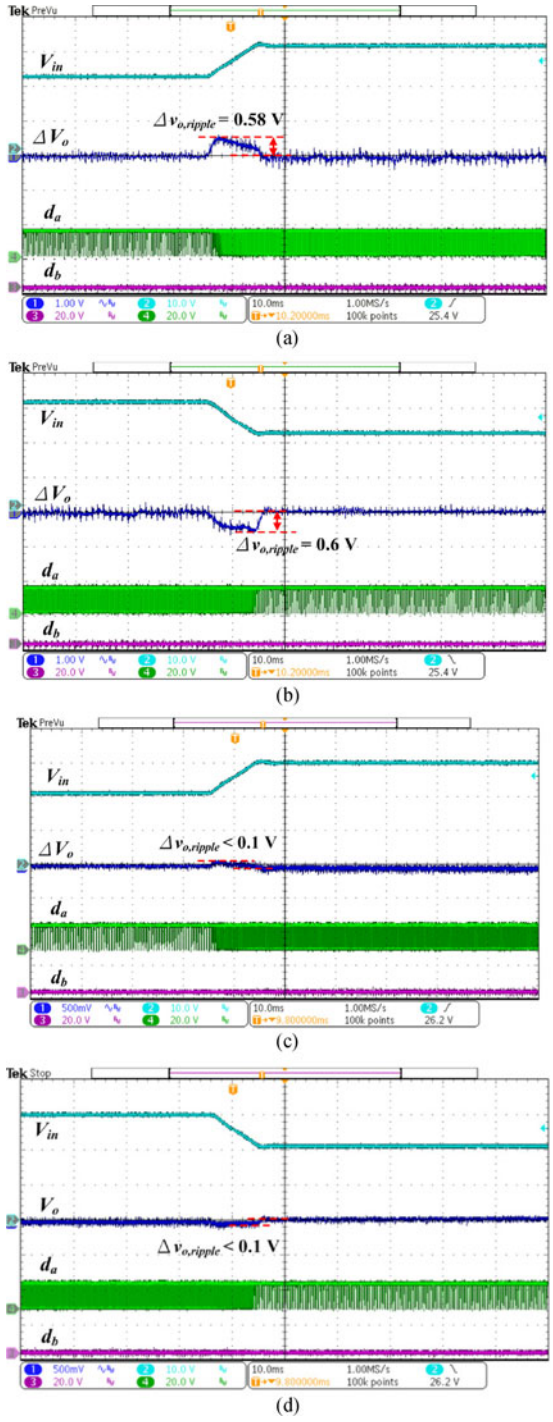

Fig. 14. Line transient responses in buck mode (a) and (b) without and (c) and (d) with the FDCC control.

$G_{ff}(s)$ is set to zero for an NBB converter without the FDCC control. When $G_{vin}(s)$, $G_{ff}(s)$, and $G_{vd}(s)$ are substituted into (34), the theoretical dc value of the numerator in (34) is equal to zero whether the NBB converter operates in boost or buck mode. It indicates that adopting the FDCC control can realize ideal feedforward compensation for buck and boost operations. Hence, the magnitudes of $T_{vin}(s)$ at low frequencies are very tiny for both modes. The FDCC control through $G_{ff}(s)$ can effectively eliminate the input-voltage-induced variations that propagate through $G_{vin}(s)$. However, in boost mode, the RHP zero alleviates the effect of the FDCC control. Therefore, the contribution of FDCC control in buck mode is more prominent than that in boost mode. The magnitudes of $T_{vin}(s)$ with and without the FDCC control in boost mode are shown in Fig. 11.

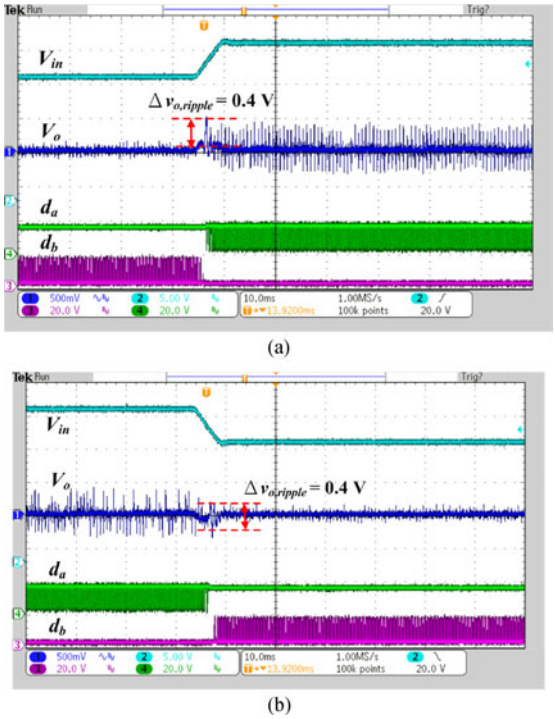

Fig. 15. Line transient responses of the NBB converter with the FDCC control (a) from boost mode to buck mode and (b) from buck mode to boost mode.

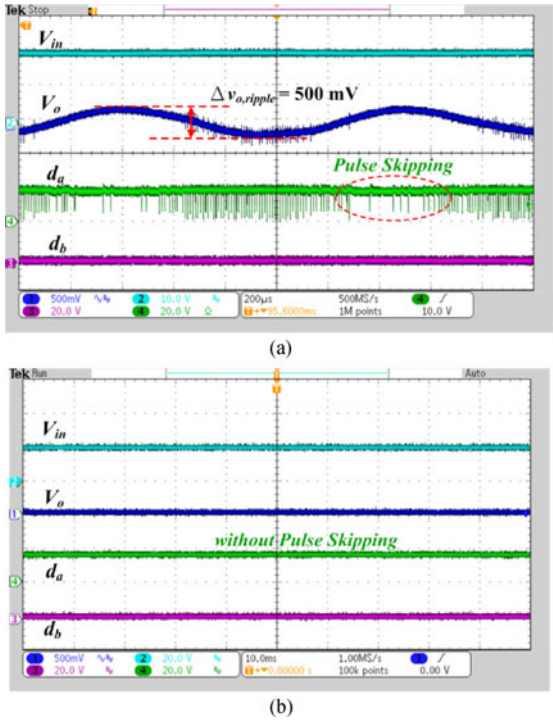

Fig. 16. Waveforms for (a) without and (b) with the duty cycle locking method when the input voltage approaches the output voltage.

IV. Experimental Results

To verify the feasibility of the FDCC control, a 100-W laboratory NBB converter was implemented with a DSP TMS320F28035. The design parameters of the NBB converter are listed in Table I. The photograph of the experimental prototype is shown in Fig. 12. Figs. 13 and 14 show the line transient response without and with the FDCC control, when the NBB converter operates in different modes with a load current of 3 A, and the input voltage steps between 12 and 19 V and between 21 and 30 V, respectively. The signals from top to bottom are the input voltage $V_{\rm in}$, output voltage ripple ΔV_o, and duty cycles d_a and d_b. The reaction of the NBB converter without FDCC control depends on the voltage feedback loop, so V_o induces a large transient ripple, which is larger than 0.58 V, during the line transient period. Because the unit-gain bandwidth of the NBB converter in boost mode is much smaller than that in buck mode as shown in Fig. 10, the output transient ripple without FDCC control in boost mode is much bigger than that in buck mode. On the other hand, the output voltage can be kept at its nominal value due to the feedforward path of the FDCC control. Thus, regardless of the unit-gain bandwidth of the NBB converter, the FDCC control can eliminate the output transient ripple during line transient period. In Fig. 15, when the input voltage changes between 18 and 23 V and load current is 3 A, the NBB converter switches between the buck and the boost modes. Owing to FDCC, the output transient ripple is less than 0.4 V.

Fig. 16 shows the waveforms of the NBB converter without and with the duty-cycle locking method when the input

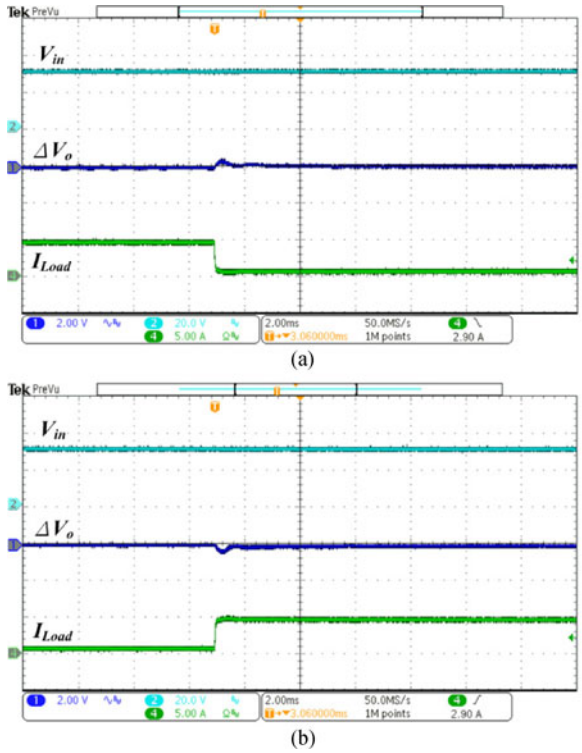

Fig. 17. Load transient responses in buck mode for (a) step-down and (b) step-up loads.

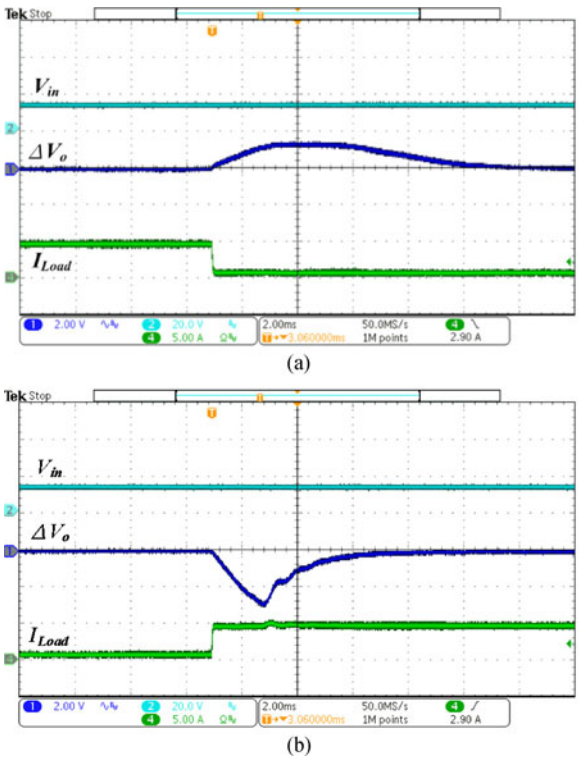

Fig. 18. Load transient responses in boost mode for (a) step-down and (b) step-up loads.

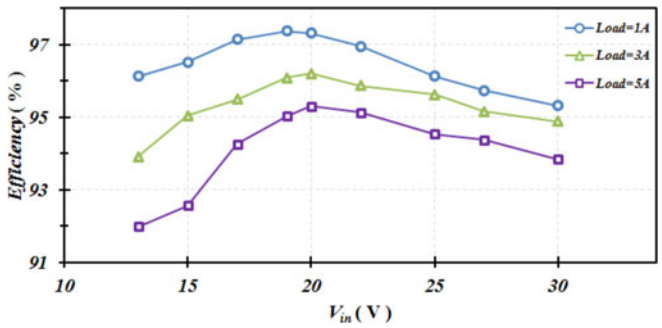

Fig. 19. Power conversion efficiency of the NBB converter with FDCC control.

voltage is 20 V. The pulse skipping issue increases output ripple when the input voltage is close to the output voltage. With the duty-cycle locking method, the output voltage is kept constant. Figs. 17 and 18 show the measured waveforms of the NBB converter in buck and boost modes, respectively, for the load current change between 1 and 5 A. Fig. 10 shows the unit-gain bandwidth of the NBB converter in buck mode is much larger than that in boost mode. It results in much better transient response of the NBB converter operating in buck mode than that in boost mode. Fig. 19 shows the power conversion efficiency of the NBB converter with different load currents and input voltages under the proposed control scheme. The maximum and average efficiencies with 3-A load current are 96.2% and 95.4%, respectively. The NBB converter accomplishes high efficiency in a wide range of input voltage.

V. Conclusion

A CCM NBB converter with the FDCC control and duty-locking strategy is proposed in this paper. When the input voltage changes, the FDCC control adopts auxiliary slopes and variable slope of the modulation signal to rapidly determine an accurate duty cycle and effectively keep the compensator output in the buck and the boost modes. It is shown that the theoretical dc value of the numerator of the closed-loop line-to-output voltage transfer function is zero when the CCM NBB converter operates in boost and buck mode. It represents that employing the FDCC control in the NBB converter can achieve ideal feedforward compensation. Hence, the output transient ripple of the NBB converter with FDCC control can be reduced dramatically regardless of the unit-gain bandwidth of the NBB converter. To reduce power losses of the switches and diodes and to alleviate pulse skipping, the duty-cycle locking method is used in the transition region of the buck and boost. Thus, power conversion is enhanced and the output voltage can be maintained. Experimental results demonstrate that the output transient ripple is eliminated significantly during line transient period. The maximum and average efficiencies with 3-A load current are 96.2% and 95.4%, respectively.

Acknowledgment

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