Letters

An Interleaved PWM Method With Better Voltage-Balancing Ability for Half-Bridge Three-Level DC/DC Converter

Wei Liu, Han Jin, Wenxi Yao, *Member, IEEE*, and Zhengyu Lu, *Senior Member, IEEE*

***Abstract*—Since the voltage stress on the power switches is only half of the input voltage, three-level (TL) converters have been widely used in high-voltage applications. To ensure normal operation of TL converters, the voltages on the input divided capacitors and the blocking capacitor must be essentially balanced. In practice, asymmetry of the main circuit and the drive circuit may result in unbalance of these voltages, leading to higher voltage stress on the power switches and other problems. This letter proposes a novel pulse-width modulation (PWM) method with better voltage-balancing ability, which is implemented by interleaving two traditional PWM methods. First, the mechanism of voltage unbalance is analyzed. The new PWM method decouples the blocking capacitor voltage from the voltages of the input divided capacitors, and ensures that the former voltage is always kept around its ideal value, which can greatly simplify the sampling circuit and the voltage-balancing control scheme. Then, a voltage-balancing strategy aiming to adjust the phase shift of the drive signals only is given. Finally, experimental results are presented to verify the effectiveness of the proposed method and voltage-balancing strategy.**

***Index Terms*—Pulse-width modulation (PWM), three-level (TL), voltage-balancing.**

I. Introduction

THREE-LEVEL (TL) converters have been widely used in high-voltage applications, mainly because the voltage stress on the power switches is only half of the input voltage. There are several commonly applied TL structures at present, and among them the structure proposed by Barbi *et al*. without any clamping diode or flying capacitor, uses the least amount of components [1]–[4], as illustrated in Fig. 1.

Voltage-sharing among the input divided capacitors and blocking capacitor must be achieved to ensure the normal operation of TL converters. Topology with voltage auto-balance ability, constructed by introducing a flying capacitor between A and B in Fig. 1, seems an attractive choice [5], [6]. The divided capacitors are alternately connected in parallel with the flying capacitor in different switching mode, so their voltages are balanced. However, these topologies can only use frequency modulation, and symmetrical pulse-width modulation (PWM) is forbidden, because switching combinations such as (S_1, S_4) and (S_2, S_3) are not allowed, where (S_x, S_y) means S_x and S_y are ON. Besides, large current spike may occur when there is voltage difference between the divided capacitors and the flying capacitor. The duty cycle and phase shift of the drive signals are typically used to balance these capacitor voltages while maintaining the diversity of the modulation method without any extra components. For the nonisolated TL converter without the blocking capacitor, the duty cycles are adjusted to balance the voltages on the divided capacitors while the phase

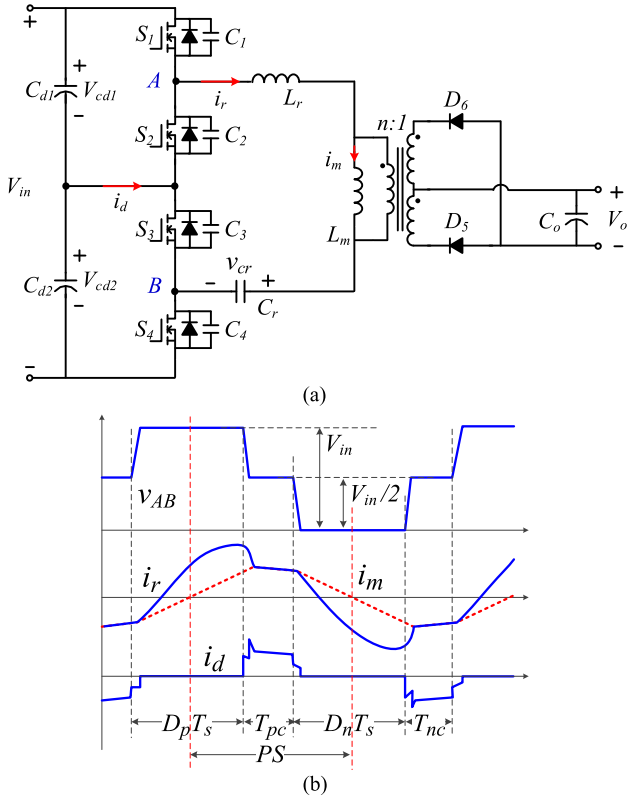

Fig. 1. (a) Half-bridge TL LLC converter. (b) Key waveforms of traditional PWM method.

Manuscript received July 12, 2017; revised August 16, 2017 and October 19, 2017; accepted November 6, 2017. Date of publication November 13, 2017; date of current version February 22, 2018. This work was supported by the National Key Research and Development Program (2016YFB0900205) and by the National Natural Science Foundation of China under Grant 51677168. *(Corresponding author: Wenxi Yao.)*

The authors are with the College of Electrical Engineering, Zhejiang University, Zhejiang 310027, China (e-mail: peliuw@zju.edu.cn; jinh26@zju.edu.cn; ywxi@zju.edu.cn; eeluzy@cee.zju.edu.cn).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2772900

shift is constant at 180° [7]. For the same TL structure shown in Fig. 1, the duty cycle is adjusted to balance the blocking capacitor voltage, while voltage-sharing of the divided capacitor voltages is obtained by adjusting the phase shift between the positive and negative half-cycles [8]. However, this strategy requires the sampling of three voltages, namely $V_{\rm in}$, V_{cd2}, and V_{cr} (see Fig. 1), and the parameter design of the control circuit is somewhat complicated owing to interaction between the control variables.

This letter presents a novel PWM method. Compared with the traditional ones, the proposed method can always keep the voltage of the blocking capacitor around half of the input voltage, and hence it greatly simplifies the complexity of the sampling circuit and the voltage-balancing control (VBC) scheme.

II. Problem of Traditional PWM Method

Fig. 1 shows the schematic of the half-bridge TL *LLC* converter and key waveforms of the traditional PWM method. C_{d1} and C_{d2} are the input divided capacitors. $\rm S_1 \sim S_4$ are the power switches, and $C_1 \sim C_4$ are the parasitic capacitors of $\rm S_1 \sim S_4$. C_r is the resonant capacitor, and it also acts as the blocking capacitor. D_p and D_n are the duty cycles of the positive and negative half-cycles, respectively. T_{pc} and T_{nc} are the charging or discharging time of C_{d1} and C_{d2}. PS is the phase shift between the positive and negative half-cycles. $v_{\rm AB}$ is the voltage between A and B, and $V_{\rm AB}$ is its mean value. $V_{\rm in}$ is the input voltage. The ripples in voltages of C_{d1} and C_{d2} are very small compared to their respective dc components V_{cd1} and V_{cd2}, thus, their dc components are used in the following analysis. V_{cdx} represents both V_{cd1} and V_{cd2}. V_{cr} is the mean voltage of C_r. i_r is the resonant current, and i_m is the magnetizing current. i_d is the charge current of C_{d1} and C_{d2}.

In ideal condition, the drive signals are symmetrical, $D_p = D_n$, $T_{pc} = T_{nc}$, hence $V_{cd1} = V_{cd2} = V_{cr} = V_{\rm in}/2$. However, in practice, there is time delay in the control and drive circuits, so $D_p \neq D_n$, $T_{pc} \neq T_{nc}$, causing the voltage of the divided capacitors and the blocking capacitor to deviate from $V_{\rm in}/2$.

It is stated in [8] that V_{cr} is only affected by the duty cycles, whereas V_{cd1} and V_{cd2} are related to both the duty cycles and the phase shift. V_{cr} is given by

$$V_{cr} = \frac{D_p}{D_p + D_n} V_{\rm in}. \tag{1}$$

However, (1) is just an approximate formula. V_{cr} is not only related to the duty cycle but also to V_{cdx}, whose exact expression is illustrated in (2). Since both V_{cr} and V_{cdx} are affected by the duty cycle and phase shift, parameters of the voltage-sharing circuit must be carefully selected, otherwise the interaction will lead to low frequency oscillation of the divided capacitor voltages.

III. Interleaved PWM Method

To maintain the charge balance of the input divided capacitors, there are two common PWM methods for the topology in Fig. 1, as shown in Fig. 2. During T_{pc} and T_{nc}, $v_{\rm AB}$ is equal to V_{cd1} in PWM1 and is equal to V_{cd2} in PWM2. Phase shift modulation is

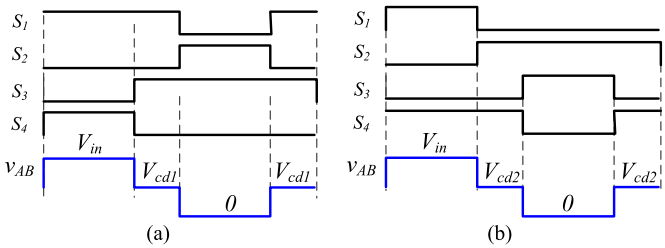

Fig. 2. Traditional PWM methods: (a) PWM1 and (b) PWM2.

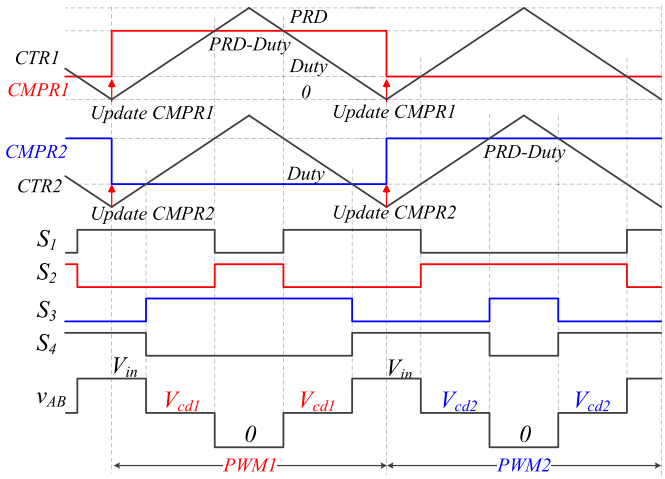

Fig. 3. Interleaved PWM method.

forbidden here, because it will charge or discharge the divided capacitor during both T_{pc} and T_{nc}.

In steady state, the mean voltage across the inductor is zero, so the mean voltages of v_{cr} and $v_{\rm AB}$ are equal

$$V_{cr} = V_{\rm AB} = \begin{cases} D_p \cdot V_{\rm in} + (1 - D_p - D_n) \cdot V_{cd1}, & \text{PWM1} \\ D_p \cdot V_{\rm in} + (1 - D_p - D_n) \cdot V_{cd2}, & \text{PWM2}. \end{cases} \tag{2}$$

Adding the two expressions in (2) together and dividing both sides by two, one obtains

$$\begin{aligned} V_{cr} &= \frac{1}{2}(V_{cr,\rm PWM1} + V_{cr,\rm PWM2}) \\ &= \frac{1}{2}\left(1 + (D_p - D_n)\right) \cdot V_{\rm in}. \end{aligned} \tag{3}$$

This can be realized by alternately using PWM1 and PWM2 method in two adjacent switching periods, as shown in Fig. 3, called the Interleaved PWM method. Equation (3) indicates that V_{cr} is proportional to the duty cycle difference only and is no longer affected by the voltages of the divided capacitors. Although the duty cycle difference is unavoidable in practice, its value is usually very small and would not cause a significant deviation of V_{cr} when the Interleaved PWM method is applied. For example, supposing $|D_p - D_n| = 1\%$, the deviation degree of V_{cr} is just 1%. This is even lower than the error of the isolated sampling circuit, so it is not necessary to sample V_{cr} any more.

The Interleaved PWM method can be easily realized by digital controllers, such as the C2000 series Microcontrollers of Texas Instrument. There are several PWM generators in one Microcontroller. Each PWM generator contains a counter

(CTR) and a compare register (CMPR), and can generate two PWM signals that can be used to drive two power switches. As shown in Fig. 3, CTR1 and CMPR1 are the carrier signal and modulation signal of the upper switch pair (S_1 and S_2), respectively, and CTR2 and CMPR2 are signals of the lower switch pair (S_3 and S_4). PRD is the parameter determined by the switching frequency, and Duty is the parameter used to adjust the duty cycle of the PWM methods. CMPR1 of PWM1 is equal to $(\mathrm{PRD}-\mathrm{Duty})$, and CMPR2 of PWM2 is equal to Duty. Thus, for the Interleaved PWM method, CMPR1 switches between $(\mathrm{PRD}-\mathrm{Duty})$ and Duty in two adjacent switching cycles, which can be realized by update CMPR1 when CTR1 equals zero. Generally, the value of Duty changes in every switching cycle owing to output voltage regulation, which means that CMPR1 and CMPR2 in the traditional methods also need to be updated in each switching cycle. Therefore, the Interleaved PWM method does not generate additional tasks.

A. Mechanism of Voltage Unbalance

In practice, problems in the drive circuits, such as different time delays and duty cycle losses, may result in asymmetrical drive signals, and consequently unbalanced capacitor voltages. Asymmetry of the drive signals in the interleaved PWM method can be summarized into two basic types: 1) the phase shift between the carrier signals is not zero; 2) the duty cycle of the positive half-cycle is not equal to that of the negative half-cycle.

1) Phase Shift Between Carrier Signals is Not Zero: Fig. 4(a) depicts the key waveforms when CTR2 lags behind CTR1, which is an equivalent result when the time delays in the drive circuits of S_3 and S_4 are longer than those of S_1 and S_2. Since the duty cycles of the positive and negative half-cycles are equal, $D_{p1}+D_{p2}=D_{n1}+D_{n2}$, it can be concluded that $V_{cr}=V_{\mathrm{in}}/2$ from (3).

In Fig. 4(a), $T_{pc1}=T_{nc2}<T_{nc1}=T_{pc2}$. The polarity of i_d indicates that C_{d1} discharges during T_{pc1} and T_{nc2} and charges during T_{pc2} and T_{nc1}. Compared with the operation condition of the symmetrical drive signals, the discharging time of C_{d1} is shorten and the charging time is prolonged, so V_{cd1} will be greater than V_{cd2}, $V_{cd1}>V_{cd2}$.

2) Duty Cycles of Positive and Negative Half-Cycle are Not Equal: If the sum of CMPR1 or CMPR2 in two adjacent switching periods is not equal to PRD, the duty cycles will not be equal. Specifically, if the sum is greater than PRD, then $D_p>D_n$, otherwise $D_p<D_n$.

The key waveforms of $D_p>D_n$ are shown in Fig. 4(b), where both the sum of CMPR1 and the sum of CMPR2 in two adjacent switching periods are equal to $\mathrm{PRD}+\mathrm{delta}$, greater than PRD. According to (3), $V_{cr}>V_{\mathrm{in}}/2$.

It should be noted that the time intervals of two adjacent periods are identical: $D_{p1}=D_{p2}$, $D_{n1}=D_{n2}$, $T_{pc1}=T_{pc2}$, and $T_{nc1}=T_{nc2}$. C_{d1} is discharged during T_{pc1} and is charged during T_{pc2}. Assuming $V_{cd1}>V_{cd2}$, v_{AB} in T_{pc1} will be greater than that of T_{pc2}. Then, the decline rate of i_r during T_{pc1} will decrease, so the discharge amount of C_{d1} will increase. Meanwhile, the decline rate of i_r in T_{pc2} will increase, which leads to less charge amount of C_{d1}. All of the above processes will cause V_{cd1} to decrease and V_{cd2} to increase, and eventually they will be balanced, i.e., $V_{cd1}=V_{cd2}$. Operation during T_{nc1} and T_{nc2} is similar to that of T_{pc1} and T_{pc2}, and will lead to the same result.

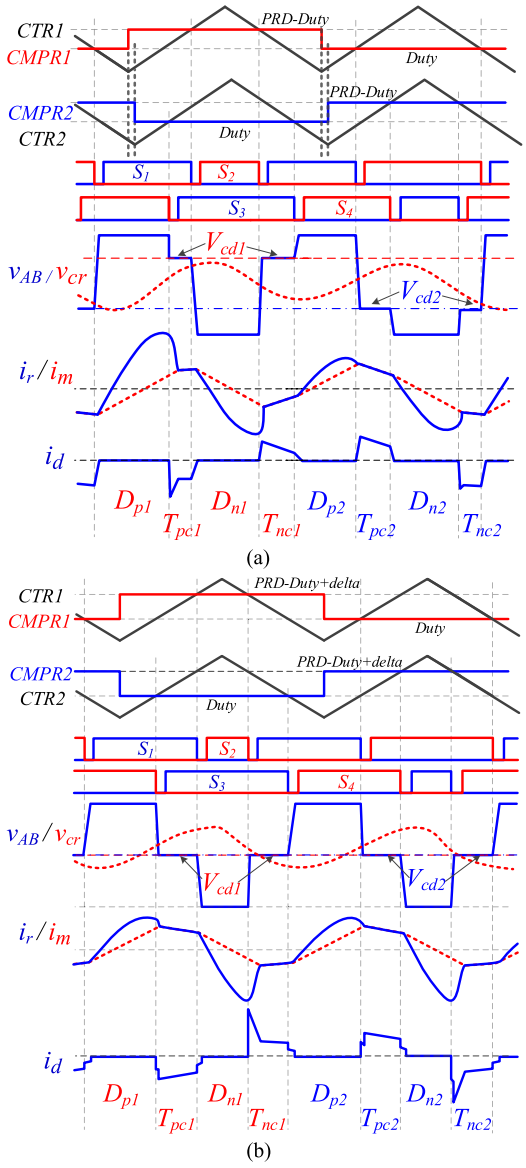

Fig. 4. Operation under asymmetrical drive signals. (a) CTR2 lags behind CTR1 and (b) $D_p>D_n$.

Therefore, conclusions can be drawn that when the phase shift between CTR1 and CTR2 is not zero, if CTR2 lags behind CTR1, V_{cd1} will be greater than V_{cd2}, and V_{cr} is not affected. When D_p is not equal to D_n, if $D_p>D_n$, V_{cr} will be greater than $V_{\mathrm{in}}/2$ and proportional to the difference between D_p and D_n, and V_{cd1} and V_{cd2} are not affected.

B. Voltage-Balancing Strategy

Diagram of the proposed voltage-balancing circuit is shown in Fig. 5, which includes two completely separate control loops: the output voltage regulator and the divided capacitor voltage regulator. The output voltage V_o is regulated by adjusting the parameter Duty, with $D_p=D_n=\mathrm{Duty}/\mathrm{PRD}$. Since the

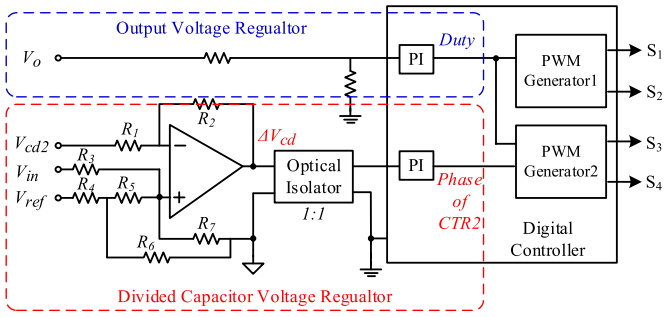

Fig. 5. Voltage control circuit diagram.

Interleaved PWM method can always keep V_{cr} around its ideal value, only the divided capacitor voltages need to be balanced, which can be achieved by adjusting the phase shift between CTR1 and CTR2.

Owing to the same ground of V_{cd2} and $V_{\rm in}$, one optical isolator is sufficient to detect the relationship between V_{cd2} and $V_{\rm in}/2$, whereas the number is three when using the traditional PWM methods [8]. Because the analog-to-digital pin of the digital controller cannot recognize negative voltages, a bias voltage is added to the sampling circuit. Therefore, the output voltage of the operational amplifier ΔV_{cd} is given by

$$\begin{aligned}\Delta V_{cd} &= \frac{R_{p1}}{R_{p1}+R_3}\cdot\frac{R_1+R_2}{R_1}V_{\rm in} - \frac{R_2}{R_1}V_{cd2} + \frac{R_{p2}}{R_{p2}+R_4} \\ &\quad\times\frac{R_1+R_2}{R_1}V_{\rm ref} \\ &= K\left(\frac{V_{\rm in}}{2}-V_{cd2}\right)+V_{\rm bias} \end{aligned} \tag{4}$$

where $R_{p1}=[(R_4\|R_6)+R_5]\|R_7$ and $R_{p2}=[(R_3\|R_7)+R_5]\|R_6$. K is determined by the amplitude of $V_{\rm in}$ and the input voltage range of the analog-to-digital pin. The reference voltage $V_{\rm ref}$ can be easily constructed by a shunt regulator such as TL431, and its value can be set to 2.5 V. $V_{\rm bias}$ is adjusted by the resistor divider and can be set to 1.6 V, because the input voltage of the analog-to-digital pin typically ranges from 0 to 3.3 V.

The phase of CTR2 is controlled by a digital proportional-integral (PI) compensator. If V_{cd2} is less than $V_{\rm in}/2$, then $\Delta V_{cd} > V_{\rm bias}$, the phase of CTR2 will be advanced, otherwise it will be delayed.

IV. Experimental Results

A prototype was built to verify the theoretical analysis. The parameters of the prototype are: $C_{d1}=C_{d2}=40$ μF, $L_r=63$ μH, $C_r=33$ nF, $L_m=370$ μH, turns ratio: 34 : 1, $S_1\sim S_4$: $IPP65R190CFD$, $D_5\sim D_6$: $BSC010NE2LS$, $C_o=2.64$ mF, $V_{\rm in}=400$ V, switching frequency: $f_s=100$ kHz, output resistance: $R_o=1\ \Omega$, and Digital controller: TMS320F28035. The clock frequency of the PWM generators is 60 MHz, hence PRD $=60\ \text{MHz}/(2*100\ \text{kHz})=300$.

Fig. 6 shows the experimental waveforms under asymmetrical drive signals. In order to match the experimental condition with the theoretical analysis condition, the time delays and duty cycle losses in the four drive circuits are adjusted to similar values, and asymmetrical drive signals are generated by the digital controller.

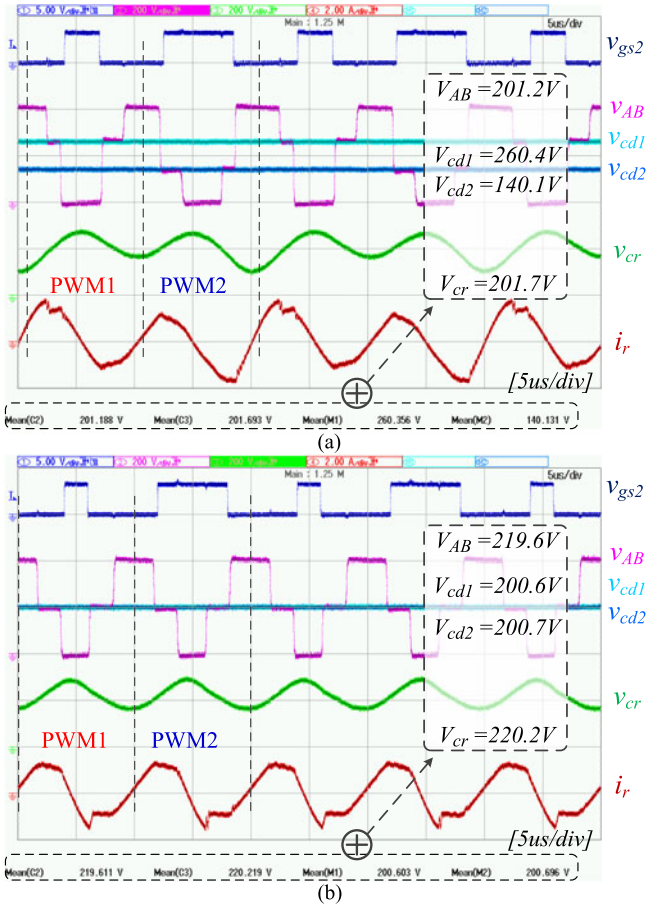

Fig. 6. Experimental results under asymmetrical drive signals. (a) CTR2 lags behind CTR1, (b) $D_p > D_n$.

The experimental waveforms under asymmetrical phase shift are reported in Fig. 6(a), where CTR2 lags 333 ns behind CTR1, 3.33% of the switching period. Meanwhile, CMPR1 and CMPR2 are switched between 105 and 195 so that $D_p=D_n=0.35$. The ripples of V_{cd1} and V_{cd2} are very small compared to their dc components. Also, the intermediate level between zero and $V_{\rm in}$ of $v_{\rm AB}$ in PWM1 has the same amplitude as V_{cd1}, and that in PWM2 has the same amplitude as V_{cd2}, which can be used to recognize them. It can be seen that $V_{cd1} > V_{cd2}$ and the mean voltage of v_{cr} is 201.7 V, very close to the calculated value, 200 V, according to (3).

The experimental waveforms under asymmetrical duty cycles are shown in Fig. 6(b), where $D_p=0.35$, $D_n=0.25$, and CTR2 is in phase with CTR1. CMPR1 and CMPR2 are switched between 105 and 225 in the manner shown in Fig. 4(b). $V_{cr}=220.2$ V, which is in good agreement with the theoretical value 220 V. Meanwhile, the divided capacitor voltages are not affected, $V_{cd1}=200.6$ V and $V_{cd2}=200.7$ V, and the waveform of $v_{\rm AB}$ also confirms this. It should be noted that the asymmetry of the drive signals is exaggerated to show the voltage unbalance more clearly, and the duty cycle difference

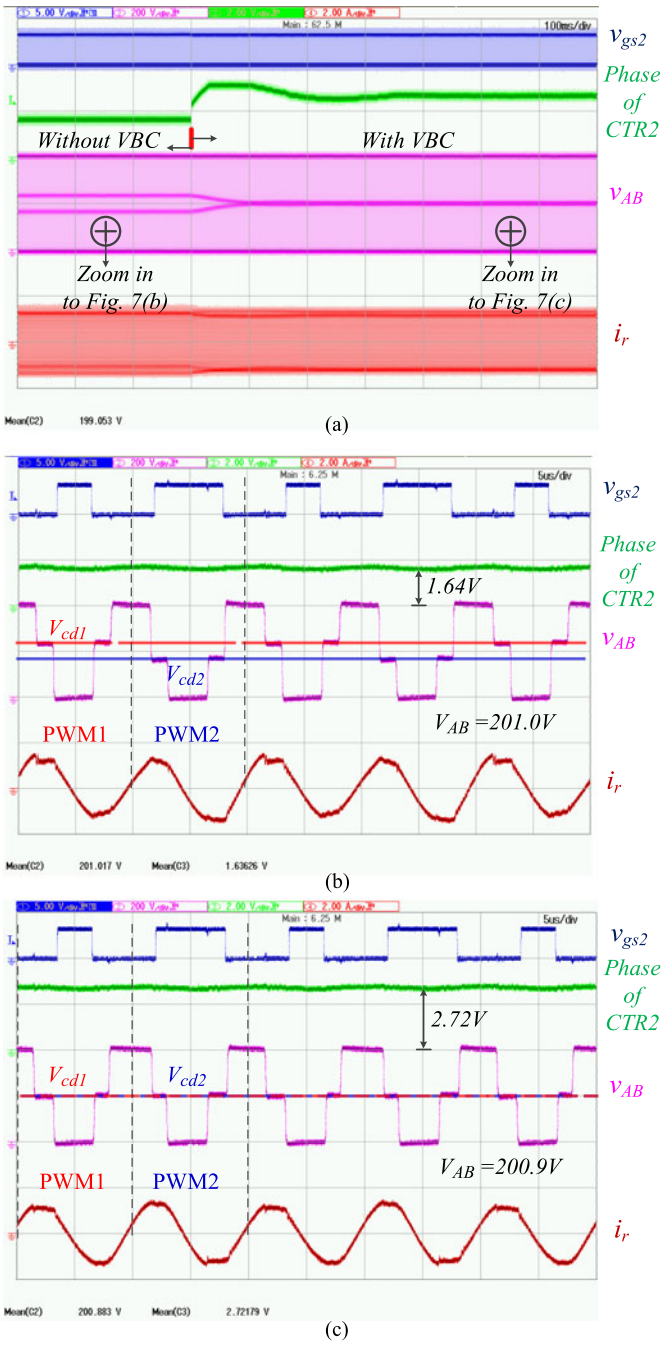

Fig. 7. Experimental results with and without the VBC. (a) Transition from Without to With, (b) zoomed-in waveform of Without, and (c) zoomed-in waveform of With.

in practice is usually much less than 0.1, so V_{cr} can be always kept around $V_{\rm in}/2$, as shown in Fig. 6(a).

Fig. 6 not only validates that the asymmetrical drive signals will cause the capacitor voltages to be unbalanced, but also indicates that the divided capacitor voltages can be corrected by adjusting the phase of CTR2, and the blocking capacitor voltage is only proportional to the difference between D_p and D_n.

Fig. 7 shows the key waveforms with and without the proposed VBC. In Fig. 7(b), where the VBC is disabled, although the drive signals generated by the digital controller are symmetrical, V_{cd1} is not equal to V_{cd2} owing to the different time delay and duty cycle loss in the drive circuits, the asymmetry of the main circuit, etc. However, $V_{\rm AB} = 201.0$ V, which means $V_{cr} = 201.0$ V and C_r is essentially balanced, because the Interleaved PWM method is used. Fig. 7(a) illustrates the transition process when the VBC is enabled, and the trajectory of the phase of CTR2 is also provided. Since the phase of CTR2 is a register in the digital controller, it is obtained by linear digital-to-analog conversion. If the amplitude of the converted signal is equal to 1.65 V, it indicates that CTR is in phase with CTR1. If the amplitude is greater than 1.65 V, it means that CTR2 is ahead of CTR1, otherwise CTR2 lags behind CTR1. Therefore, as shown in Fig. 7, when the VBC is disabled, CTR2 is in phase with CTR1, and then after the VBC is enabled, the phase of CTR2 is advanced to balance V_{cdx}. Eventually, all capacitor voltages are balanced in Fig. 7(c), $V_{cd1} = V_{cd2}$ and $V_{cr} = V_{\rm AB} = 200.9$ V.

V. Conclusion

This letter proposes an interleaved PWM method for half-bridge TL dc/dc converters. Operation under asymmetrical drive signals is analyzed, and a low-cost voltage-sharing strategy is presented. Compared with the traditional PWM method, the main advantages of the proposed method are as follows. 1) The complex relationship among V_{cr}, V_{cdx}, duty cycles, and phase shift is decoupled. The blocking capacitor voltage V_{cr} is affected only by the difference between the duty cycles, and the input divided capacitor voltage V_{cdx} is affected only by the phase shift. Thus, the parameter design of the voltage-sharing loop is simplified. 2) Only one isolated sample circuit is needed, so the cost is reduced.

The interleaved PWM method can also work well in flying capacitor TL structure.

References

[1] Y. Gu, Z. Lu, L. Hang, Z. Qian, and G. Huang, "Three-level LLC series resonant DC/DC converter," *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp. 781–789, Jul. 2005.

[2] W. Chen, X. Ruan, and R. Zhang, "Zero-voltage-switching PWM three-level converter with interleaved complementary modulation," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2007, pp. 949–954.

[3] F. Canales, P. M. Barbosa, J. M. Burdio, and F. C. Lee, "A zero-voltage switching three-level dc/dc converter," in *Proc. Int. Telecommun. Conf.*, Jun. 2000, pp. 512–517.

[4] I. Barbi, R. Gules, R. Redl, and N. O. Sokal, "DC-DC converter: Four switches Vpk=Vin /2, capacitive turn-off snubbing, ZV turn-on," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 918–927, Jul. 2004.

[5] W. Li, Q. Luo, Y. Mei, S. Zong, X. He, and C. Xia, "Flying-capacitor based hybrid LLC converters with input voltage auto-balance ability for high voltage applications," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1908–1920, Mar. 2016.

[6] B. R. Lin and S. Z. Zhang, "Analysis and implementation of a three-level hybrid DC–DC converter with the balanced capacitor voltages," *IET Power Electron.*, vol. 9, no. 3, pp. 457–465, 2016.

[7] X. Ruan, J. Wei, Y. Xue, and L. Zhou, "Voltage-sharing of the divided capacitors in non-isolated three-level converters," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2004, pp. 1725–1729.

[8] X. Yu, K. Jin, and Z. Liu, "Capacitor voltage control strategy for half-bridge three-level DC/DC converter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1557–1561, Apr. 2014.