An Integrated DC–DC Boost Converter Having Low-Output Ripple Suitable for Analog Applications

Samiran Dam and Pradip Mandal

***Abstract*—This paper presents an integrated boost converter having very low output voltage ripple making it suitable for analog applications, which are sensitive to supply noise. Architecturally, the converter consists of a conventional boost converter followed by an *L–C* filter, which drastically reduces the output ripple. The *L–C* filter has been realized using 30-nH bondwire inductance and 0.54-nF on-chip capacitance. The converter switches at 118 MHz and produces a regulated 3.2-V output from an input voltage ranging from 1.0 to 2.7 V. The converter is able to deliver up to 65-mA current for input voltage $\geq$ 2.4 V. The prototype has been implemented in 0.18-μm standard digital CMOS process and the entire design consumes only 0.52-mm^2 chip area resulting in a maximum power density of 0.387 W/mm^2. Peak efficiency of the converter is 77.4% at 32.2-mA current for 2.7-V input supply. The measured maximum output ripple noise is 21 mV that is less than 0.65% of the regulated output voltage.**

***Index Terms*—Bondwire, boost, dc–dc, ripple.**

I. Introduction

TODAY'S portable and low-power electronic devices are generally equipped with rechargeable battery, output voltage of which generally varies across wide range. For example, typical ranges of output voltage of Li-ion, Li-titanate, and Ni-MH batteries are 4.2→2.7 V, 2.7→1.5 V, and 1.5→1.0 V [1], respectively. However, the analog subsystems of a battery-powered device may require the supply voltage to be regulated at a level higher than the input voltage level coming from the battery. Moreover, precision analog circuits require low noise supply for achieving high performance. We have observed in an independent study that to obtain more than eight effective number of bit (ENOB) for a pipeline Analog-to-Digital Converter (ADC), the supply voltage ripple (at mere vicinity of the sampling frequency) must be within 0.8% of the nominal voltage. So, generating higher supply voltages having low output ripple from a widely varying input voltage is one of the important tasks for the power management unit of a portable device. This task can be performed efficiently by an inductor-based dc–dc boost converter.

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For a compact design solution, it is desirable to integrate the converter unit inside the chip along with its load. Integrating the converter also eliminates load-transient spikes caused by package parasitics. However, the need of passive components (L and C) of large values impedes a complete integration of the converter. So, in order to stretch the limit of integration, values of the passive components need to be reduced within a value suitable for on-chip realization.

Feasibility of complete integration has been demonstrated in [2]–[5], where the on-chip power inductance has been implemented using top metal layers and on-chip filter capacitance has been implemented using MOS/MIM capacitor. The quality factor (Q) of the on-chip inductor is, however, quite low resulting in high equivalent series resistance (ESR) loss, which drastically reduces the power efficiency. Moreover, it consumes a very large chip area. For example, 600 μm $\times$ 600 μm is required to implement a 2-nH inductor [3]. It may also be noted that a very small LC product requires higher switching frequency to maintain the output ripple within an acceptable range. Increasing the frequency has negative impact on the efficiency. So, it leads to a need for exploring possibilities of higher inductor and capacitor values but utilizing limited silicon area. There have been several approaches to integrate the converter at package level either using in-plane air-core copper spiral inductor [6] or air-core surface mount inductor along with flip-chip ball grid array (BGA) package [7] or parasitic inductance of package bondwires [8]–[10]. Use of the package to house the inductor, straightaway eliminates the tradeoff between the on-chip inductor area and the efficiency. In [6] and [7], special air-core surface-mount (SMD) inductors have been used. An alternate means to realize the package inductor as reported in [9] and [10] is by using bondwires along with the bondpads and lead frames, which are available in any standard IC package. Although, the ESR ($\approx$55.6 mΩ/nH [10]) of bondwire inductance is higher than that of the air-core surface-mount inductor, it is still significantly better than that of the on-chip metal inductor.

Likewise, there has been some attempts to fit the filter capacitor within a stringent on-chip area. Typically, the required value of the output filter capacitance is so high that the integrated capacitor consumes a major part of the chip area. In [9], both the on-chip capacitance and the bondwire inductance are stretched toward their respective limits to minimize the output ripple noise. Even then, with a 20 nH of bondwire inductor and 50 MHz of switching frequency, the output voltage ripple reduced only to 300 mV, which is 16.7% of the steady-state output voltage. The switching frequency may be increased

further to improve the ripple performance but only at the cost of efficiency. In [10], an alternative approach has been followed to reduce the voltage ripple. Multiple time-interleaved phases were used to reduce the output ripple. They have achieved 50-mV ripple (5.56%) at 100-MHz switching frequency using 3.73 nF of on-chip capacitance and 4 × 2 nH bondwire inductance.

In [11], Ridley had analyzed and discussed the influence of a secondary *L–C* filter section on the output ripple performance of a current-mode buck converter. It was proposed that the use of an additional *L–C* filter at the converter output suppresses the output switching noise. Although the paper had demonstrated the ripple reduction for a continuous conduction mode (CCM) buck converter, it was anticipated that the impact of the secondary *L–C* filter would be more effective for boost and buck–boost converters. This is because the output voltage ripple of a CCM boost converter is inversely proportional to only the capacitance (C) value, which results into a requirement of significantly large capacitor to satisfactorily filter out the voltage ripple. In spite of the said advantage, the secondary *L–C* filter section has hardly been utilized except in few works [12], possibly because of the following reason. In all discrete component based converters, the flexibility to use large values of capacitance does not bring on the requirement of using additional *L–C* filter section for ripple reduction. However, for integrated converter design, we realize that the use of an additional filter section has good potential to reduce the ripple significantly, without degrading the power density. In this paper, the aforesaid concept has been employed to design a prototype boost converter. Here, we propose to implement the output *L–C* filter using bondwire inductance and small on-chip capacitance, which is shown to be sufficient for maintaining the output voltage ripple within 0.65%. The proposed design is suitable to implement an integrated dc–dc converter for generating a regulated, low noise, and higher voltage supply required by precision analog circuits, from a rechargeable battery.

Rest of this paper is organized as follows. Tradeoffs among various performance parameters of an integrated converter is discussed in Section II. Thereafter, the proposed design is described thoroughly in Section III followed by a discussion on the design and implementation of the prototype in Section IV. Subsequently, the measured performance of the prototype and a comparison of its performance with that of the recent literature are provided in Sections V and VI, respectively. Finally, a conclusion is drawn in Section VII.

II. Performance Tradeoffs of Integrated Boost Converter

For an integrated converter, the most critical performance parameters are output ripple, power efficiency, and power density. The output ripple (Δv_O) for a boost converter is given by (1) [13]. Here, D is the duty ratio, I_O is the load current, F_{sw} is the switching frequency, and C is the output filter capacitance. This relationship indicates that output ripple can be decreased by increasing the capacitance value and/or increasing the switching frequency. However, increasing the capacitance value increases the chip area overhead and hence decreases the power density. On the other hand, increasing the switching frequency affects the power efficiency. The conduction power loss (P_{cond}) of an inductive converter is given by (2). Here, R_{on} is the "ON" resistance of the power switch and I_L and Δi_L are average inductor current and inductor current ripple, respectively. P_{cond} has an average power loss component and a loss component due to Δi_L. Both the loss components are proportional to R_{on} and the latter is inversely proportional to the square of F_{sw} as well to the square of the L value. For an integrated converter, where the L is small, the loss due to Δi_L is significant. P_{cond} can be reduced by increasing F_{sw} and L and/or decreasing R_{on}. However, both, increasing F_{sw} and decreasing R_{on}, reduce the power efficiency by increasing the loss in gate driver. Moreover, decreasing R_{on} requires bigger transistors that degrade the power density as well. The design becomes even more challenging when higher threshold devices are used to implement the power switches

$$\Delta v_O = \frac{DI_O}{F_{\text{sw}}C} \tag{1}$$

$$P_{\text{cond}} = \left(I_L^2 + \frac{\Delta i_L^2}{12}\right) R_{\text{on}} = \left(I_L^2 + \frac{V_I^2 D^2}{12 F_{\text{sw}}^2 L^2}\right) R_{\text{on}}. \tag{2}$$

The tradeoffs among the performance parameters are illustrated in Fig. 1. Here, the power efficiency has dependencies on two loss components, namely the conduction loss and the gate-drive or switching loss. In this paper, the tradeoff between the output ripple and the power density has been reduced by using the additional *L–C* filter section at the output.

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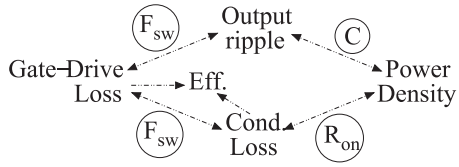

Fig. 1. Performance tradeoff polygon.

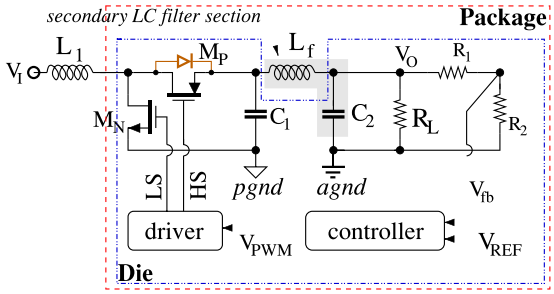

Fig. 2. Circuit diagram of the proposed boost converter.

III. Proposed Boost Converter

A block-level circuit diagram of the proposed boost converter is shown in Fig. 2. It is a conventional boost converter having a secondary *L–C* filter section comprising of inductor L_f and capacitor C_2.

In this design, inductance of both the inductors has been chosen in such a way that they can be implemented by standard package bondwires. Primary requirement for realizing sufficient inductance (few tens of nH) using standard bondwires is the availability of additional bondpads, which may not be a

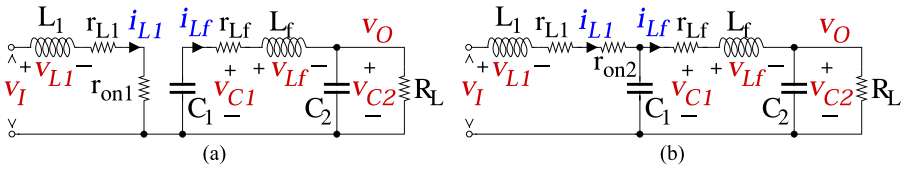

Fig. 3. Equivalent power stage in two phases. (a) ON state ($0 \le t \le dT_S$). (b) OFF state ($dT_S \le t \le T_S$).

bottleneck for core-limited designs. This prototype had to share total available test-chip area of 1.5 mm × 1.5 mm with two other designs due to some circumstantial issues. So, only less than half of the total bondpads of the test chip were available for use by this prototype out of which six bondpads have been used for implementing the filter inductance L_f. However, although the power inductor L_1 is implementable by bondwires, due to the restriction mentioned earlier, it could not be realized using bondwires that may have taken another four bondpads. So, we have decided to use small surface mount inductor for L_1 in this version of our prototype implementation. The capacitors C_1 and C_2 are on-chip and have been implemented using MOS capacitance. The controller employs a voltage-mode pulse width modulation (PWM) control to regulate the output voltage.

The additional *L–C* filter section helps to attenuate the output ripple noise significantly, using on-chip capacitance much smaller compared to that used by the existing integrated converters. More importantly, it isolates the analog ground (*agnd*) from the power ground (*pgnd*), which is badly affected by the switching noise. However, the additional *L–C* section makes the power stage a four-pole system, which influences the design of the controller. In the next section, derivation of the steady-state and small-signal models of the power stage is discussed.

A. Power Stage Model and Transfer Function

Traditional state-space averaging has been used to obtain the steady-state and small-signal models of the power stage. The effective power stage circuits, in two phases, are shown in Fig. 3. Here, we have considered switches with practical "ON" resistances (r_{on1} and r_{on2}) and inductors with parasitic series resistances (r_{L1} and r_{Lf}). It may be noted that as the ESR of the integrated capacitor is very small, we have ignored it in our analysis. T_S indicates the switching period. The averaged state-space equation is shown in (3). Here, $r_{\text{par}} = (Dr_{\text{on1}} + D'r_{\text{on2}} + r_{L1})$.

$$\frac{d}{dt}\begin{bmatrix} i_{L_1} \\ v_{C_1} \\ i_{L_f} \\ v_{C_2} \end{bmatrix} = \begin{bmatrix} \frac{-r_{\text{par}}}{L_1} & \frac{-D'}{L_1} & 0 & 0 \\ \frac{D'}{C_1} & 0 & \frac{-1}{C_1} & 0 \\ 0 & \frac{1}{L_f} & \frac{r_{Lf}}{L_f} & \frac{-1}{L_f} \\ 0 & 0 & \frac{1}{C_2} & \frac{-1}{R_L C_2} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ v_{C_1} \\ i_{L_f} \\ v_{C_2} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i \tag{3}$$

$$\frac{d}{dt}\begin{bmatrix} \hat{i}_{L_1} \\ \hat{v}_{C_1} \\ \hat{i}_{L_f} \\ \hat{v}_{C_2} \end{bmatrix} = \begin{bmatrix} -\frac{r_{\text{par}}}{L_1} & -\frac{D'}{L_1} & 0 & 0 \\ \frac{D'}{C_1} & 0 & -\frac{1}{C_1} & 0 \\ 0 & \frac{1}{L_f} & -\frac{r_{Lf}}{L_f} & -\frac{1}{L_f} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{R_L C_2} \end{bmatrix} \begin{bmatrix} \hat{i}_{L_1} \\ \hat{v}_{C_1} \\ \hat{i}_{L_f} \\ \hat{v}_{C_2} \end{bmatrix} + \begin{bmatrix} -\frac{(r_{\text{on2}} - r_{\text{on1}})}{L_1} & \frac{1}{L_1} & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{L1} \\ V_{C1} \\ I_{Lf} \\ V_{C2} \end{bmatrix} \hat{d}(t). \tag{4}$$

After perturbation and linearization steps, the state equation of the small-signal ac model of the control-to-output path is obtained, which is shown in (4). Here, the steady-state values of the state variables are given as: $I_{L1} = \frac{\lambda V_I}{R_L D'^2}$, $I_{Lf} = I_O = \frac{\lambda V_I}{R_L D'}$, $V_{C1} = \frac{\lambda V_I}{D'}(1 + \frac{r_{Lf}}{R_L})$, and $V_{C2} = V_O = \frac{\lambda V_I}{D'}$, where $\lambda = \frac{D'^2 R_L}{r_{\text{par}} + D'^2(r_{Lf} + R_L)}$. After solving the set of equations given by (4), the duty-to-output transfer function is obtained, which is shown in the following equation:

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{a_2 s + a_1}{b_4 s^4 + b_3 s^4 + b_2 s^2 + b_1 s + 1}. \tag{5}$$

The coefficients of the above transfer function are as follows:

$$a_2 = \frac{V_I L_1 \lambda^2}{D'^4 R_L},$$

$$a_1 = \frac{V_I \lambda}{D'^2}\left[1 + \frac{D'^2 r_{Lf} - r_{L1}}{D'^2 R_L} + \frac{D'(2r_{\text{on2}} - r_{\text{on1}}) + Dr_{\text{on1}}}{D'}\right]$$

$$b_4 = \frac{L_1 L_f C_1 C_2 \lambda}{D'^2},\ b_3 = b_4\left[\frac{1}{R_L C_2} + \frac{r_{\text{par}}}{L_1} + \frac{r_{Lf}}{L_f}\right]$$

$$b_2 = b_4 \times \left[\frac{1}{L_f C_1} + \frac{1}{L_f C_2} + \frac{D'^2}{L_1 C_1} + \frac{r_{\text{par}} r_{Lf}}{L_1 L_f} + \frac{r_{\text{par}}}{R_L L_1 C_2} + \frac{r_{Lf}}{R_L L_f C_2}\right]$$

$$b_1 = b_4 \times \left[\frac{(L_1 + D'^2 L_f)}{R_L L_1 L_f C_1 C_2} + \frac{r_{\text{par}}(C_1 + C_2)}{L_1 L_f C_1 C_2} + \frac{r_{\text{par}} r_{Lf}}{R_L L_f C_2} + \frac{D'^2 r_{Lf}}{L_1 L_f C_1}\right].$$

The transfer function shown in (5) captures the effect of the nonideal factors present in the circuit. This equation is helpful to

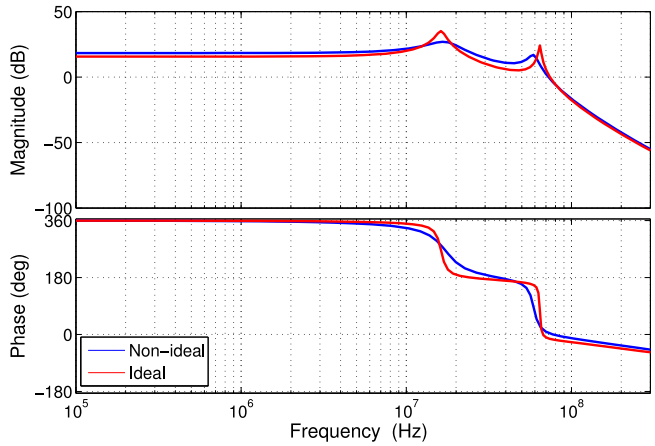

Fig. 4. Bode plot of $G_{vd}(s)|_{\text{ideal}}$ and $G_{vd}(s)|_{\text{nonideal}}$.

make precise assumption about the locations of poles and zeros after considering the effect of parasitic. However, this is also a little cumbersome to obtain first-cut design values of the main design parameters such as L_1, L_f, C_1, and C_2. Thus, (5) can be further simplified by equating the parasitic resistance values to zero, which gives

$$G_{vd}(s)=\frac{\frac{V_I}{D'^2}\left[1-\frac{s}{\frac{D'^2R_L}{L_1}}\right]}{\left(\begin{array}{l}\frac{L_1L_fC_1C_2}{D'^2}s^4+\frac{L_1L_fC_1}{D'^2R_L}s^3\\ \quad+\frac{L_1(C_1+C_2)+D'^2L_fC_2}{D'^2}s^2+\frac{L_1+D'^2L_f}{D'^2R_L}s+1\end{array}\right)}. \tag{6}$$

The obtained ideal (without considering parasitic) and nonideal (considering parasitic) expressions of the control-to-output transfer function have been evaluated for the given design point: $V_I = 1.8$ V, $V_O = 3.3$ V, $R_L = 82.5\ \Omega$, $L_1 = 20$ nH, $L_f = 30$ nH, $C_1 = 0.54$ nF, $C_2 = 0.54$ nF, $r_{L1} = 50\ \text{m}\Omega$, $r_{Lf} = r_{\text{on1}} = r_{\text{on2}} = 1\ \Omega$. Required duty ratio obtained by solving steady-state design equations is 0.454 for the ideal case and 0.498 for the nonideal case. So, the transfer functions at this design point are as follows:

$$G_{vd}(s)|_{\text{ideal}}=\frac{-4.93\times10^{-9}s+6.05}{\left(\begin{array}{l}5.88\times10^{-34}s^4+1.32\times10^{-26}s^3\\ \quad+1.02\times10^{-16}s^2+1.18\times10^{-9}s+1\end{array}\right)}$$

$$G_{vd}(s)|_{\text{nonideal}}=\frac{-5.33\times10^{-9}s+8.28}{\left(\begin{array}{l}6.12\times10^{-34}s^4+5.34\times10^{-26}s^3\\ \quad+9.26\times10^{-17}s^2+4.09\times10^{-9}s+1\end{array}\right)}.$$

Bode plot of the above two transfer functions is shown in Fig. 4. The deviation of $G_{vd}(s)|_{\text{ideal}}$ from $G_{vd}(s)|_{\text{nonideal}}$ is small. So, (6) can be used for the design purpose with a reasonable accuracy. It can further be used to approximate locations of poles and zeros. With the assumption: $D'^2L_f \le L_1$, frequencies of the first and second resonant poles (ω_1 and ω_2) and their Q-factors are given by the expressions shown in (7). The low-frequency gain of $G_{vd}(s)$ and the right-half plane (RHP) zero (Z_{RHP}) of the proposed boost converter are same as those of a conventional boost converter

$$\omega_1=\frac{D'}{2\pi\sqrt{L_1(C_1+C_2)}};\ Q_1=\frac{R_L}{\frac{1}{D'}\sqrt{\frac{L_1}{(C_1+C_2)}}-\frac{D'L_fC_1}{\sqrt{L_1(C_1+C_2)^3}}}$$

$$\omega_2=\frac{1}{2\pi\sqrt{L_f\frac{C_1C_2}{(C_1+C_2)}}};\ Q_2=R_L\sqrt{\frac{C_2}{L_f}\left(1+\frac{C_2}{C_1}\right)^3}$$

$$G_{d0}=\frac{V_I^2}{V_O};\quad Z_{\text{RHP}}=\frac{D'^2R_L}{2\pi L_1}. \tag{7}$$

State equation of the small-signal ac model of line-to-output path is obtained, which is shown in the following equation:

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_{L_1}\\ \hat{v}_{C_1}\\ \hat{i}_{L_f}\\ \hat{v}_{C_2}\end{bmatrix}=\begin{bmatrix}\frac{-r_{\text{par}}}{L_1} & \frac{-D'}{L_1} & 0 & 0\\ \frac{D'}{C_1} & 0 & \frac{-1}{C_1} & 0\\ 0 & \frac{1}{L_f} & \frac{-r_{Lf}}{L_f} & \frac{-1}{L_f}\\ 0 & 0 & \frac{1}{C_2} & \frac{-1}{R_LC_2}\end{bmatrix}\begin{bmatrix}\hat{i}_{L_1}\\ \hat{v}_{C_1}\\ \hat{i}_{L_f}\\ \hat{v}_{C_2}\end{bmatrix}+\begin{bmatrix}\frac{1}{L_1}\\ 0\\ 0\\ 0\end{bmatrix}\hat{v}_i(t). \tag{8}$$

After solving the set of equations given by (8), the line-to-output transfer function is obtained, which is shown in (9). As expected, $G_{vi}(s)$ contains no Z_{RHP}

$$G_{vi}(s)=\frac{\hat{v}_o(s)}{\hat{v}_i(s)}=\frac{\frac{\lambda}{D'}}{b_4s^4+b_3s^4+b_2s^2+b_1s+1}. \tag{9}$$

IV. Design and Implementation

In this section, we discuss some design criteria based on which the values of L_1, L_f, C_1, and C_2 are determined. Subsequently, implementation of L_f using bondwire is discussed. Then, final output ripple performance is analyzed based on the result obtained from transistor level simulation of the converter. Design of the power switches and the corresponding gate-driver is depicted followed by a discussion on the design of the controller.

A. Selection of the Component Values

There are three criteria that have been considered while designing the passive components.

1) First, L_1 is chosen so that it is feasible to be implemented by bondwires. Also, a smaller L_1 ensures a high-frequency Z_{RHP}, which is desirable to make the converter controllable in heavy load condition [14]. On the other hand, a small L_1 increases Δi_L, which increases P_{cond} (refer to [2]). So, aggressive reduction of L_1 may lead to a suboptimal design in terms of efficiency.
2) Second, the series combination (C_{eq}) of C_1 and C_2 along with L_f defines the second resonant frequency (ω_2). For a given value of ω_2, maximizing C_{eq} minimizes L_f to a value feasible for bondwire implementation. C_{eq} is maximum when C_1 and C_2 are equal.
3) Finally, for a given value F_{sw}, if ω_2 is pushed too close to F_{sw}, then attenuation of the switching ripple at the final output will not be significant.

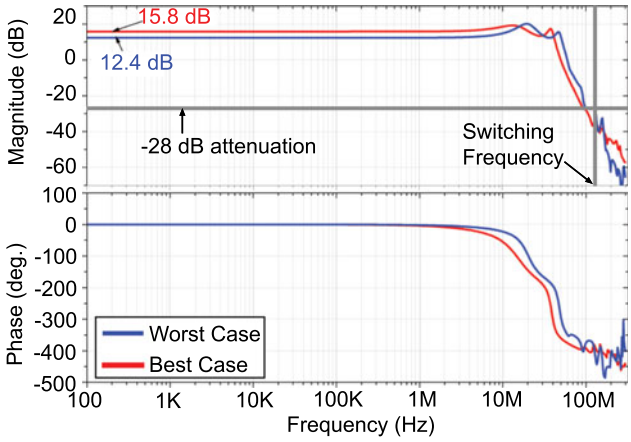

Fig. 5. Frequency response plot of $G_{vd}(s)$ of the actual circuit.

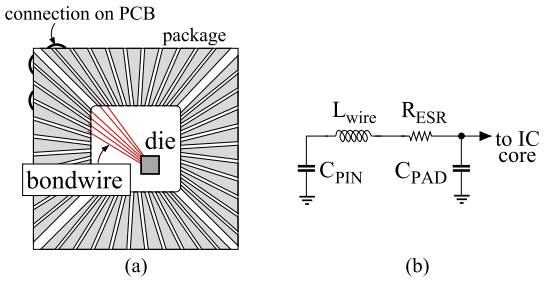

Fig. 6. (a) Bondwire connection. (b) Bondwire model.

Based on these design criteria, we chose $L_1 = 20$ nH, $L_f = 30$ nH, and $C_1 = C_2 = 0.54$ nF. Although ω_2 is independent of the load/line condition, different possible combinations of ω_1 and Z_{RHP} may arise depending upon the line/load conditions, which need to be considered carefully for controller design. The worst case occurs at minimum V_I and maximum I_O, when ω_1 and Z_{RHP} both become minimum. On the other hand, the best case occurs at maximum V_I and minimum I_O. $G_{vd}(s)$ (considering r_{on} and r_L) of the designed power stage is shown in Fig. 5 for the worst ($V_I = 1.8$ V and $I_O = 50$ mA) and the best ($V_I = 2.5$ V and $I_O = 10$ mA) conditions. In the worst case, ω_1 and ω_2 are 13.8 and 41.5 MHz, respectively, and the Z_{RHP} is 161 MHz, whereas, in the best case, ω_1 and ω_2 are 19.5 and 46.7 MHz, respectively, and Z_{RHP} is 1.39 GHz.

B. Realization of Filter Inductance Using Bondwires

The prototype has been packaged in a 44 pin Ceramic Leadless Chip Carrier (CLCC) package. As shown in Fig. 6(a), six bondwires are connected in series to realize L_f. The zigzag arrangement of the wires and alternate directions of current through adjacent bondwires give rise to a magnetic coupling effect. It effectively increases the overall inductance.

For each of the bondwires, the equivalent electrical model shown in Fig. 6(b) has been used for simulation. The values of L_{wire} and R_{ESR} have been calculated based on the data provided by the manufacturer, which are enlisted in Table I. Total nominal inductance of 30 nH has been used in the simulation. However, robustness of the design has been verified considering $\pm$ 20% deviation of the filter inductance with respect to its nominal value.

TABLE I
BONDWIRE PARAMETERS

Parameter	Value
Material	Gold (Au)
Diameter	1.2 mil (30.48 μm)
Self-inductance	0.95 nH/mm
K^*_{11}	0.56
Series resistance (ESR)	35 mΩ/mm

*Coupling coefficient between two adjacent bondwires.

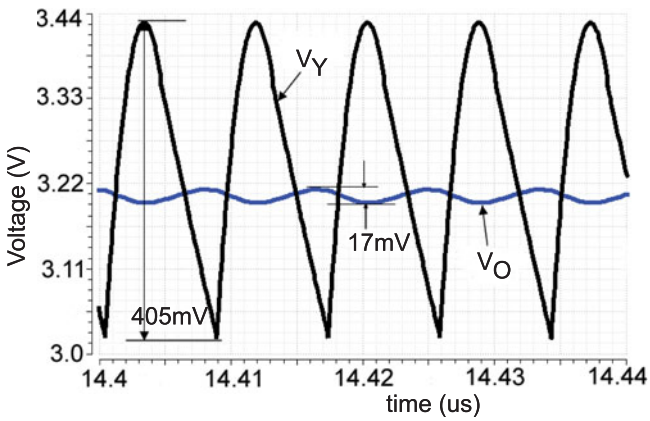

Fig. 7. Output ripple reduction.

C. Ripple Performance Analysis

High switching ripple present in the voltage at node V_Y is attenuated significantly by the subsequent L–C filter section, and the final output voltage ripple reduces to a very low value. The amount of attenuation can be predicted from the magnitude response of the $G_{vd}(s)$. The attenuation is $-$ 28 dB at the switching frequency of 120 MHz, as indicated in Fig. 5. The output voltage ripple obtained from simulation with $L_1 = 20$ nH, $L_f = 30$ nH, $C_1 = C_2 = 0.54$ nF, and $F_{\text{sw}} = 120$ MHz is shown in Fig. 7. The ripple present in the voltage at the node V_Y is 405 mV, whereas the final output voltage ripple is only 17 mV. To compare this output ripple, a baseline design of the conventional boost converter topology has been simulated with inductance of 50 nH and filter capacitance of 1.08 nF under the identical input–output condition and the switching frequency. It has been observed that the peak-to-peak ripple present in the output voltage of the conventional converter is 214 mV.

D. Power Circuit

In a high-frequency converter, the internal ground line of the power circuit becomes very noise because of the ground line inductance and very high frequency switching. That is why the supplies of the power circuit have been completely isolated from the supplies of the remaining circuits. It consists of power switches and driver.

1) Power Switches: In general, sizes of the M_n and M_p are optimized based on the tradeoff between the conduction loss

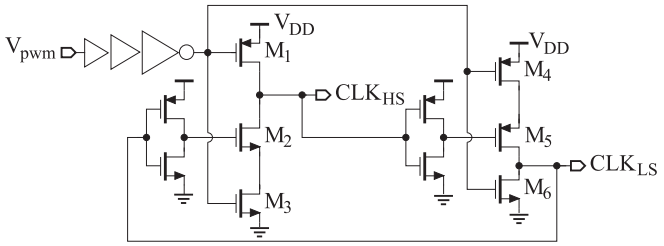

Fig. 8. Gate driver circuit.

(P_{cond}) and the gate-drive loss (P_{dyn}), which are given by

$$P_{\text{cond}} = \frac{I_O^2}{D'^2} \times \left[\frac{DL}{\mu_n C_{OX} W_n (V_{GS} - V_{tn})} + \frac{D'L}{\mu_p C_{OX} W_p (V_{GS} - V_{tp})}\right]. \tag{10}$$

$$P_{\text{dyn}} = [(W_n + W_p) L] C_{OX} V_{GS}^2 F_{\text{sw}} \tag{11}$$

The design has been optimized for the following nominal requirement: $V_I = 2.4$ V, $I_O = 50$ mA, and $F_{\text{sw}} = 110$ MHz by making the P_{cond} and P_{dyn} equal. The size of M_n is 1440 μm $\times$ 0.34 μm and the size of M_p is 2000 μm $\times$ 0.34 μm.

2) Gate Driver: The output of the controller (V_{pwm}) is level shifted to 0–3.3 V and fed to the switches through a gate driver, as shown in Fig. 8 [15]. It generates two nonoverlapped clocks, LS and HS for M_n and M_p, respectively. Here, the feedback signals at LS and HS are used to control the gate driving signals in such a way that the transistors do not turn ON simultaneously. It is necessary to minimize the nonoverlapped time (t_{dead}) between the transitions of two clock signals as much as possible to reduce the power loss in the body diode of M_p. In this design, sizes of the transistors of the driver are optimized to achieve $t_{\text{dead}} =$ 300 ps. The designed gate driver consumes about 14.2-mW power at 120-MHz switching frequency.

E. Control Circuit Design

Voltage-mode PWM is adopted to design the controller shown in Fig. 9 in detail. Here, we have used triangular ramp or double-edge PWM [16] to overcome the difficulty of precisely controlling the sharp-falling edge of a saw-tooth ramp in high frequency. The ramp waveform generator circuit is illustrated in Fig. 9. For stabilizing the control loop, dominant pole compensation has been used to push ω_1 and ω_2 beyond the crossover frequency (f_{gc}) to achieve stability margins. The compensator [$G_c(s)$] has been implemented by a simple differential-to-single ended operational trans-conductance amplifier (OTA) and a capacitance (C_C) of 30 pF has been used for creating the dominant pole. Loop gain of the feedback network is given by

$$T(s) = -\frac{1}{V_M} \times G_c(s) \times G_{vd}(s) \times \frac{R_2}{(R_1 + R_2)} \tag{12}$$

where V_M denotes height of the ramp waveform. The simulated frequency response of the loop gain is shown in Fig. 10. For the worst case ($V_I = 1.8$ V, $I_O = 50$ mA) scenario, f_{gc} is 1.76 MHz, and phase and gain margins are 79° and 17.5 dB, respectively. Locations of the poles and zeros of the closed-loop system on the *s* plane are shown in Fig. 11.

In the present design, f_{gc} has been limited in order to have sufficiently high phase margin apprehending the worst case variation of bondwire inductance. However, after characterizing the test chip and observing the similarity between the simulated and measured load regulation performances of the converter, we have realized that higher f_{gc} could have safely been achieved for nominal phase margin of 60° by using 10 pF of C_C. The simulated load transient responses with $C_C = 30$ pF and $C_C =$ 10 pF are shown in Fig. 12. The designed converter has also been simulated for a step change of 1.2–2.7 V and vice-versa (with 1μs ramp time) in the input supply line. The corresponding transient response of the converter to this given line step is shown in Fig. 13.

It may be noted that we have used a simpler compensation technique that limits (f_{gc}) and it is not the best for applications demanding faster transient response. So, there is a future scope of research on techniques to increase f_{gc}. This may be accomplished by pushing f_{gc} beyond ω_1 and ω_2. Traditionally, PID technique is used to compensate the effect of the single resonant frequency appearing before f_{gc} in a conventional boost converter topology. But, in case of the proposed converter, if f_{gc} is placed beyond ω_1 and ω_2, then compensating their combined effects will be difficult. The other option, which may be a feasible design choice, is to place f_{gc} in between ω_1 and ω_2. In this way, the effect of ω_1 (appearing before f_{gc}) can be compensated by the traditional PID technique. However, to achieve good stability margins, ω_2 should be at least 50$\times$ more than ω_1. Alternatively, one may explore feasibility of applying the current-mode control technique as used in [11] for a buck converter having output filter or the sliding-mode control technique as used in [12] for a boost converter with output filter.

V. Measurement Results

The designed prototype has been fabricated in 0.18 μm CMOS process. The prototype is a part of a test chip having 1.5 mm$\times$ 1.5 mm die area, as shown in Fig. 14. Total layout area of the design is 0.52 mm^2, which includes the area consumed by capacitors, power switches and drivers, controller, and on-chip dc load circuits. It may be noted that a bulk of the area (close to 60%) is consumed by the capacitors.

Measured performances of the prototype are discussed in the following sections.

A. Ripple

The measured voltage ripple at V_Y and V_O nodes of the converter for $V_I = 2.2$ V and $I_O = 40$ mA is shown in Fig. 15. As shown, 27.6-dB attenuation of switching ripple by the *L–C* filter stage has been achieved.

The ripple has been measured to be less than 0.62% for all line and load conditions indicated by the plot shown in Fig. 16. As anticipated in design and simulation, this measured ripple performance is 6$\times$ better compared to that of the existing integrated converters using in-package or on-chip passive components [2]–[4], [6]–[10].

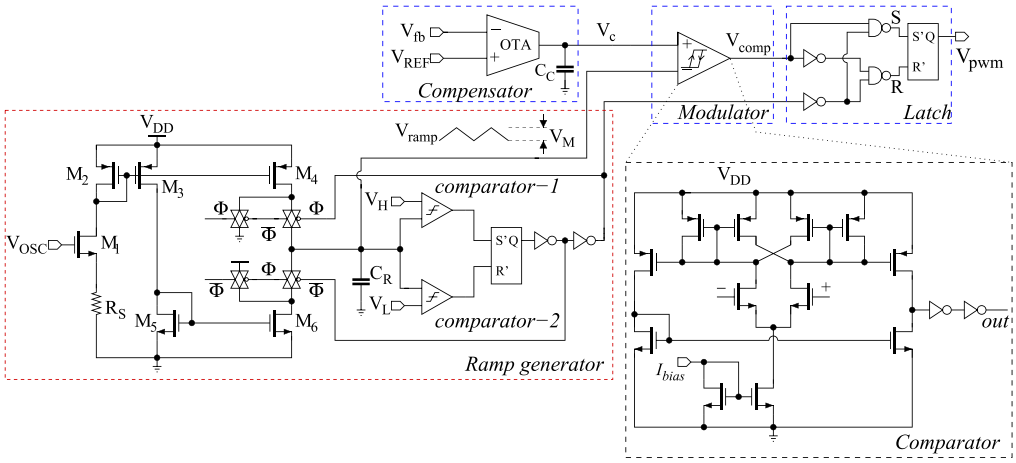

Fig. 9. Controller circuit.

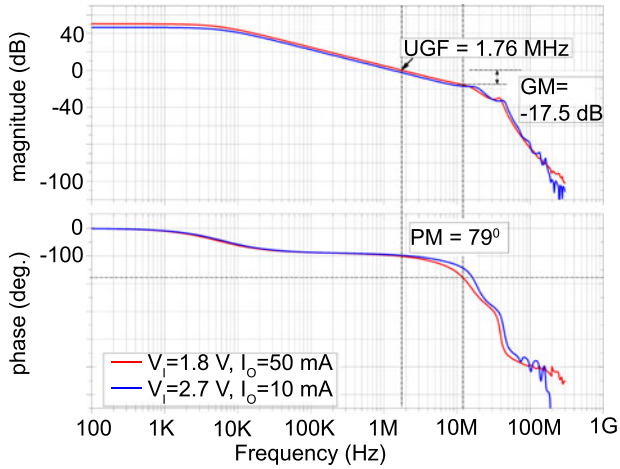

Fig. 10. Bode plot of the feedback loop gain $[T(s)]$.

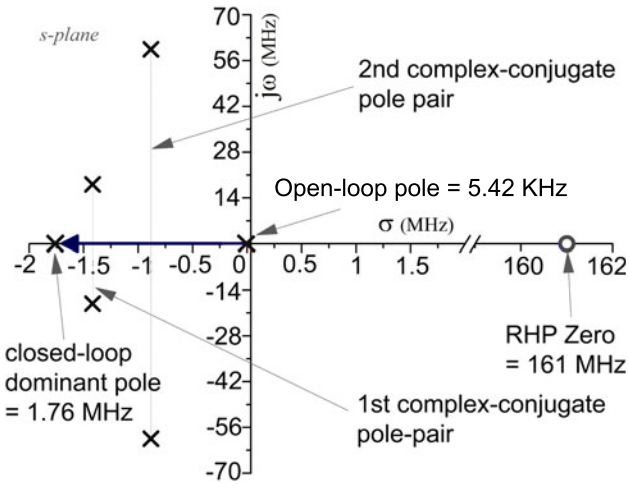

Fig. 11. Location of the system poles and zero on s plane.

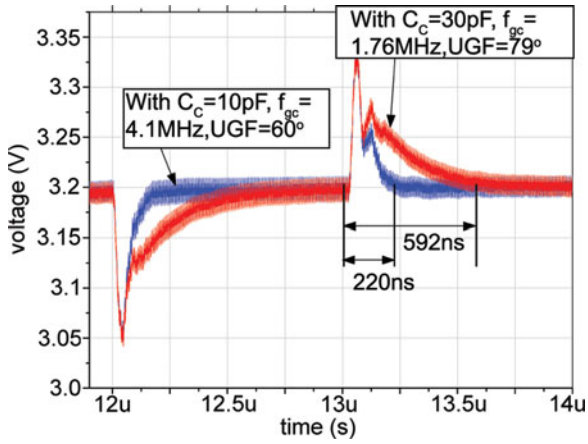

Fig. 12. Simulated load transient response.

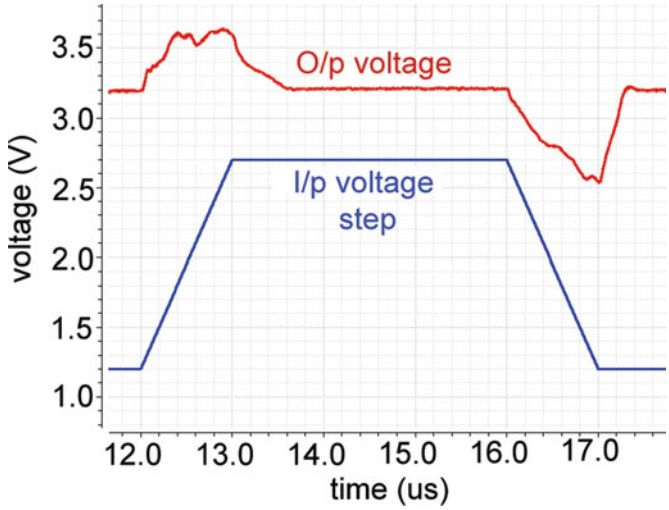

Fig. 13. Simulated line transient response.

B. Efficiency

The measured o/p voltage is 3.2 V. Although the converter has been designed for a nominal 3.3-V o/p, the measurement result shows that it has been drifted from the target because of a shift in the Band-Gap Reference (BGR) reference voltage. The converter produces the regulated output from different i/p voltages for a wide range of o/p current, as shown by the plot in Fig. 17.

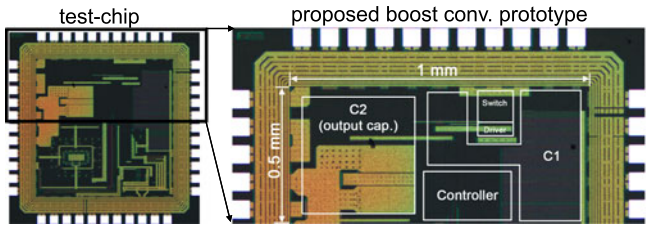

Fig. 14. Die micrograph and floor planning.

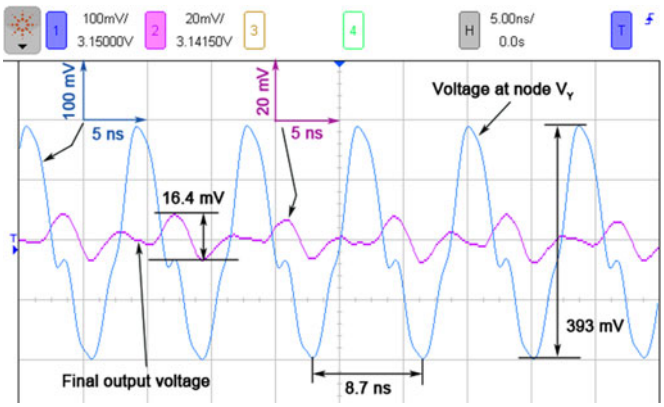

Fig. 15. Output voltage ripple waveform.

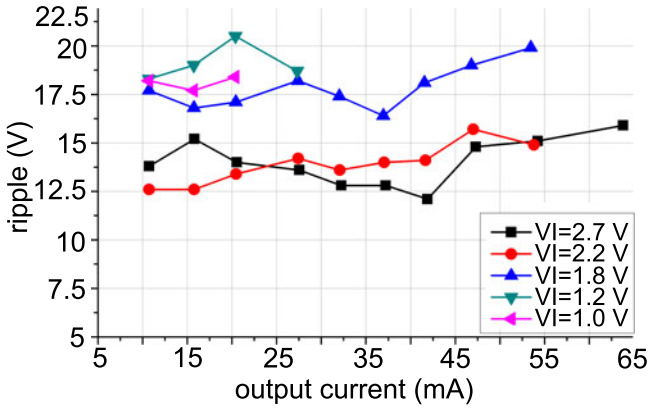

Fig. 16. Measured ripple for different o/p currents.

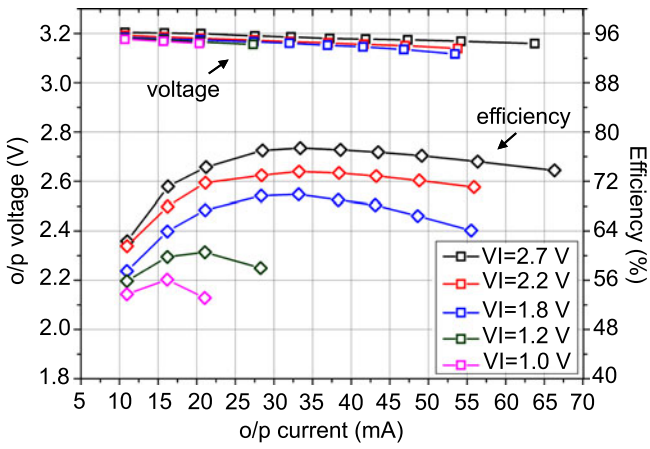

Fig. 17. Measured o/p voltage and efficiency.

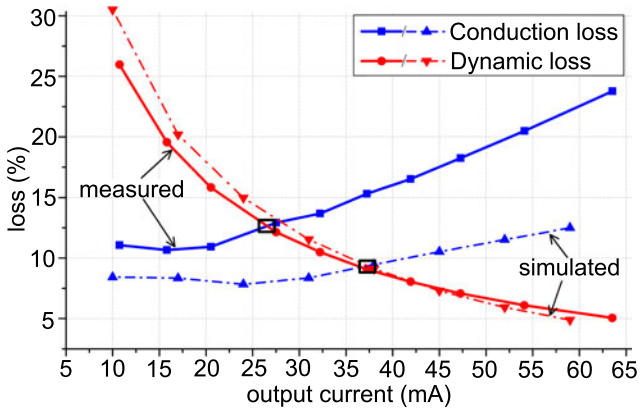

Fig. 18. Loss components of the converter for $V_I = 2.5$ V.

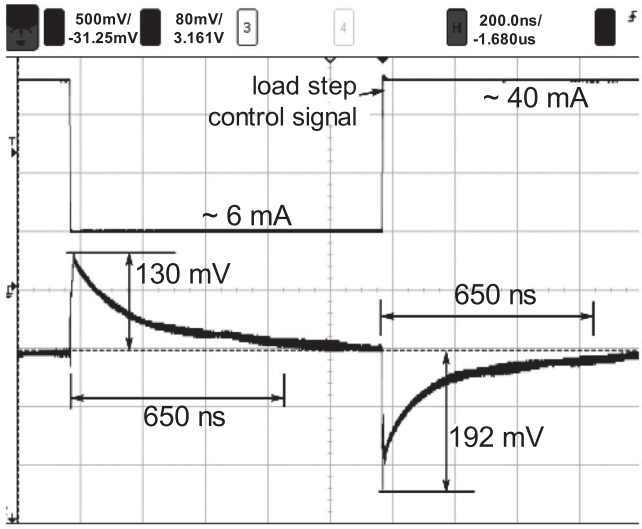

Fig. 19. Transient response of the regulated converter.

The converter has been characterized for i/p voltages lower than the target range of 1.5–2.7 V to verify its functionality. The efficiency for different o/p current and i/p voltage conditions is plotted in Fig. 17. Peak efficiency of 77.4% has been measured at $I_O = 32.2$ mA for $V_I = 2.7$ V. For a lower i/p voltage, efficiency decreases. However, it is still maintained above 70% for the i/p voltage more than 2 V. For $V_I = 1.8$ V, the peak efficiency is 69.9% at 37-mA load current. It may be noted that the quiescent current consumed by the converter is 258 μA, which includes all the bias currents taken by the PWM controller and the reference generator.

In our prototype, there is a provision to measure the conduction and the gate-drive losses. The measured percentage of these two losses is shown by solid lines in Fig. 18, for $V_I = 2.5$ V. The two components become equal at 26-mA current. Moreover, the total loss remains within 25–30% of the i/p power over a wide range of the o/p current. It may be noted that at the design phase, the target optimal point has been set at 50-mA output current by equating the loss components. However, apart from considering the switch "ON" resistance, we have assumed zero inductor and interconnect resistances during the analytical calculation.

TABLE II
PERFORMANCE COMPARISON WITH PRIOR WORKS

Ref.	[2]	[3]	[7]	[9]	[8]	[17]	This Work
Process	0.18 μm	0.13 μm	0.09 μm	0.13 μm	0.18 μm	0.18 μm	0.18μm
L (H)	22 n (on-chip)	4 n (on-chip)	27.2 n (in-package)	20 n (bondwire)	18 n (bondwire)	22 n (on-chip)	20 n (discrete)*, 30 n (bondwire)‡
C (F)	6 n (MOS)	5.2 n (MOS)	2.5 n	3.4 n (MIM)	1.3 n (MIM)	1.2 n (MOS)	1.08 n (MOS)
Freq. (Hz)	45 M	170 M	233 M	50 M	100 M	N/A	118 M
I/p (V)	2.8	1.2	1.2/1.4	2.5–3.3	1.6–2	0.3	1.0–2.7
O/p (V)	1.8	0.3–0.9	0.9/1.1	1.8	2.5–4	1.1	3.2
$I_{\max}$ (mA)	200	350	300	300	45	0.018	65
Area (mm^2)	6.75	1.5	1.15	10.08	1	0.63	0.52
Efficiency	64%@0.2 A, 2.8→ 1.8 V	77.9%@0.19 A, 1.2 → 0.9 V	83.2%@0.2 A, 1.2→ 0.9 V	76.8%@0.25 A, 2.5→ 1.8 V	63%@24 mA, 1.8→ 3.3 V	45%@18 μ, 0.3→ 1.1 V	75.9%@42 mA, 2.5→ 3.2 V; 69.9%@37 mA, 1.8→ 3.2 V
P. Density (W/mm^2)	0.053	0.21	0.234	0.054	0.149	0.032	0.387
O/p droop	N/A	15% @ 55% $I_{\max}$	10% @ 50% $I_{\max}$	9% @ 100% $I_{\max}$	N/A	N/A	6% @ 54% $I_{\max}$
$\frac{t_{settling}}{T_S}$	N/A	N/A	2.33 (5%)	10 (N/A)	N/A	N/A	29 (5%)
Ripple	6.95%	4.45%	N/A	16.67%	6.1%	N/A	0.62%

The dashed lines in Fig. 18 correspond to simulated data points, which indicates that optimal point (at simulation level, considering all nonideal factors) of the actual circuit has been shifted to 38 mA. The measured optimal point is further shifted to 26 mA probably because of the increase in resistance value of bondwires for which the curve corresponding to conduction loss has been shifted upward.

C. Transient Response

The transient response has been measured by applying a load current step from 6 to 40 mA (and vice-versa) with a 1 ns ramp time. The measured response is shown in Fig. 19. The maximum overshoot/undershoot is less than 6% of the steady-state voltage, whereas steady-state error of the converter is 0.32%.

VI. PERFORMANCE COMPARISON

Table II shows a comparison of the proposed converter with previously reported integrated converters. It may be observed that all of the converters listed in the table have on-chip capacitors, whereas means of implementation of the inductors are different. For example, [2], [3], and [17] have used on-chip metal inductor, [7] has used in-package air-core inductor, and [8] and [9] have used bondwire to implement the inductor. The second observation is that the type of the converters in [2], [3], [7], and [9] is buck, whereas the converter in [8] and [17] and our proposed converter is boost. The two types of converters have different levels of output driving capability except the one reported in [17], which was designed for energy harvesting application. The buck converters deliver higher output current and use higher value of capacitors than those of the boost converters. Table II also provides the information of power densities. However, taking only the on-chip power densities into consideration may not reveal the true form factors of all the designs listed in Table II. This is mainly because some of the designs use on-chip inductor [2], [3], [17], whereas the other designs use in-package inductor [7]–[9]. Naturally, power densities of the on-chip inductor based designs are much lower than those of the in-package inductor based designs. As the proposed design is based on in-package inductor, we emphasize on the comparison of power density of our design with the in-package inductor based designs and it may be noted that our work shows the best power density.

The most significant improvement in performance produced by the proposed converter is the reduction of the output ripple noise. A straightforward design in [2] yielded 6.95% ripple even with 6 nF on-chip capacitance. In [7], a stacked inductor based ripple reduction technique is proposed to reduce the ripple; however, the measured output ripple of this converter still remained quite high ($\geq$ 4.4%) even with a very high switching frequency of 170 MHz. Likewise, for the buck converter in [9] and the boost converter in [8] where bondwires are used to implement the inductors, the ripple performance remains poor (6%–16%). In contrast to these existing works, the ripple performance of the proposed work converter is 0.62%, which is sufficiently good to power an ADC producing 8 bit ENOB.

VII. CONCLUSION

On-chip or in-package integration of power management unit is the recent trend for low-power applications. However, limited value of the passive components (due to their size constraints) compels the converter to introduce considerable amount of output ripple noise, which restricts its application only for digital circuits. A precision analog circuit requires supply voltage ripple as minimum as possible in order to provide high performance. The lowest reported ripple noise of in-package/on-chip dc–dc converter in literature is 4.45% of its regulated output voltage. This noise performance is not good enough even to power a 6-b ADC. This paper proposes a boost converter that uses an integrated filter stage cascaded with a conventional boost converter, which reduces the output voltage ripple drastically. A prototype design has been implemented for a 3.2-V regulated output from an input ranging over 1.0–2.7 V. The filter has been implemented

using bondwire inductance and on-chip capacitance making it suitable to be integrated with the application inside the package. The measured output voltage ripple is less than 0.65% of its regulated output voltage. In this implemented prototype, the power inductor is an off-chip surface mount inductor. However, as its value is very small (20 nH), similar to the filter inductor, it could have been realized using bondwire to make the entire prototype encapsulated within the package without any external component. In fact, our original plan was to implement an encapsulated prototype converter. But, due to unavailability of sufficient number of bond pads in the small shared die could not do so. However, we believe that, for the designed converter, the noise performance will remain the same even if the power inductor is realized using bondwire.

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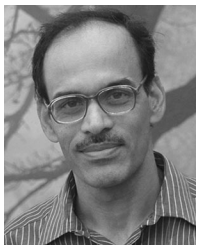

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