A Single-Phase PFC Rectifier With Wide Output Voltage and Low-Frequency Ripple Power Decoupling

Yonglu Liu, *Student Member, IEEE*, Yao Sun, *Member, IEEE*, Mei Su, Min Zhou, Qi Zhu, and Xing Li

***Abstract*—This paper proposes a single-phase power factor correction (PFC) rectifier to achieve high power factor, wide output voltage range, and ripple power decoupling without using electrolytic capacitors. It consists of two parts: PFC circuit and output voltage regulation circuit. The load side is involved in both parts, which is different from the regular two-stage conversion structure. The proposed rectifier can be directly applied to low voltage cases due to the wide output voltage range. And the decoupling capacitor voltage can be smaller than the peak grid voltage, which reduces the voltage stress. Besides, the low-frequency ripple power buffer is implemented without a dedicated power-buffering controller. This paper first introduces the circuit structure, operation principles, and control method. Then, the system design consideration is given. Finally, the effectiveness of the proposed topology is verified by the simulations and experimental results.**

***Index Terms*—Active power decoupling, closed-loop control, low-frequency ripple power, power factor correction (PFC), wide output voltage.**

I. Introduction

THE grid-connected current in single-phase power supplies is mandatory to be sinusoidal waveform and high power factor (PF) to achieve high conversion efficiency and meet harmonic standards such as IEC 61000-3-2 [1]. The simplest PF correction (PFC) converters are composed of a diode rectifier and a dc/dc circuit [2], [3], and used in various applications such as light-emitting diode (LED) drivers [4], electric vehicle chargers [5], and the electronic ballast [6].

However, the inherent ripple power at twice the line frequency is injected into the load side when doing ac–dc power conversion, which causes a low-frequency output voltage ripple. That degrades the system performances, for example, generating low-frequency flicker of LED [4], [7], [8] and causing overheating of the battery [9], [10]. Usually large electrolytic capacitors are used to restrict the ripple within allowable limit, which is simple and easy to implement. However, that is adverse to reliability and power density [11], [12]. For example, the relative low lifetime of electrolytic capacitors (<20 000 h [13]) cannot match with the long lifetime (80 000–100 000 h [14]) of LED devices.

Alternatively, active power decoupling method is an effective approach to cope with the low-frequency ripple power [15]–[17]. Its basic idea is to divert the low-frequency ripple power into a small capacitor, which allows a large voltage fluctuation, with employing the decoupling circuit. Therefore, the bulky electrolytic capacitor can be replaced with a small film or ceramic capacitor. Originally, the simple dc/dc circuit plays the role of the decoupling circuit. They are merged into the original converter in series [18], [19] or parallel [20]–[22]. This kind of decoupling concept is easy to implement because the decoupling circuit and original circuit work independently. However, usually a lot of active and passive components are involved. To reduce cost and volume, the integrated decoupling circuit topologies, in which active switches and/or passive components are shared between the decoupling circuit and original circuit, seem more popular [23]–[29].

Those two decoupling concepts are also applied for PFC rectifiers [30]–[36]. In [30]–[32], a buck–boost dc/dc converter is paralleled with the load to buffer the low-frequency ripple power. Then, the flicker-free electrolytic capacitor-less LED driver is achieved. And in [32] the decoupling capacitor voltage also serves as a high-voltage dc bus of a rear inverter. By combining the three-terminal cell with a diode rectifier in different ways, two kinds of PFC rectifier with power decoupling capability are obtained [33], [34]. The three-terminal cell consists of one capacitor, one diode, two switches, and an inductor. According to the location of the inductor, they can be respectively viewed as a buck rectifier [33] and a buck–boost rectifier [34]. In both of them, the PFC circuit and the decoupling circuit are merged, which improves the component usage and makes the converter compact and cost-effective. However, the decoupling capacitor voltage is high (greater than the peak grid voltage in [33] and greater than the sum of the peak grid voltage and output voltage in [34]). Moreover, a relative large input filter may be required due to discontinuous current before the diode rectifier. In [30]–[34], only one decoupling capacitor is used to buffer

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Y. Liu, Y. Sun, M. Su, M. Zhou, and Q. Zhu are with the School of Information Science and Engineering, Central South University, Changsha 410083, China (e-mail: liuyonglu@csu.edu.cn; yaosuncsu@gmail.com; sumeicsu@mail.csu.edu.cn; minzhou@csu.edu.cn; csu_zhuqi@163.com).

X. Li is with the College of Electrical and Information Engineering, Hunan University, Changsha 410082, China (e-mail: lxhnu@hnu.edu.cn).

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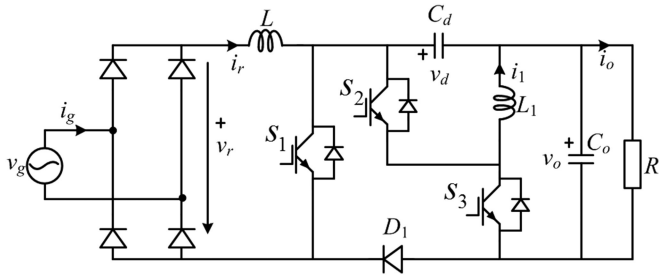

Fig. 1. Proposed circuit topology with wide output voltage and power decoupling capability.

the low-frequency ripple power. While in [35] and [36], two decoupling capacitors are used and they also play the role of the output filter. In [35], only the lower capacitor is involved to achieve PFC and the power can only be transferred from the lower capacitor to the upper one. So the ripple power cannot be decoupled completely and a 21.5% current ripple still exists. The proposed circuit in [36] is obtained by replacing the dc-link capacitor in the boost PFC rectifier with a symmetrical half-bridge circuit. As the power can flow between the two capacitors bidirectionally, the complete power decoupling is fulfilled. However, the proposed circuit is not suitable for low-voltage applications. One reason is the boost PFC rectifier can only output a high dc voltage. Another reason is the required decoupling capacitance is relatively large to guarantee the decoupling capacitor voltage is not beyond the dc voltage.

To achieve wide output voltage and low decoupling capacitor voltage stress, a new type of PFC rectifier is proposed in this paper. It consists of a classic boost PFC circuit and an output voltage regulation circuit. As the decoupling capacitor is in series with the dc bus, the proposed circuit shows a series power buffer structure, like the topologies proposed in [33] and [34]. But the constraint on the decoupling capacitor voltage is weaker and the minimum decoupling capacitor voltage can be less than the peak grid voltage. In the adopted closed-control strategy, the output voltage is regulated by controlling the output voltage regulation circuit, and the PFC and the averaged decoupling capacitor voltage are in the charge of the PFC circuit. Besides, the PFC control and the output voltage regulation are independent. That control idea achieves a fast output voltage regulation as well as a high PF [37]. In addition, the low-frequency ripple power buffer is implemented without a dedicated power-buffering controller.

The rest of the paper is arranged as follows: Section II introduces the topology of the proposed converter. Section III presents the operation principles and the controller design. Section IV presents the design consideration. Simulations and experimental results are provided in Section V. Finally, Section VI presents the conclusion.

II. Proposed Circuit and Operation States

Fig. 1 outlines the proposed circuit topology composed of a boost PFC circuit (consisting of the diode rectifier, inductor L, switch S_1, and diode D_1) and an output voltage regulation circuit. The output voltage regulation circuit includes switches S_2 and S_3, film capacitors C_d and C_o, and inductor L_1. C_d is in series with the dc bus to buffer the low-frequency ripple power and C_o is to filter high-frequency switching harmonics. S_1 and S_2 work without interference, and S_2 and S_3 work complementarily.

There are four switching states, as shown in Fig. 2. And v_r represents the rectified output voltage. When the switch S_1 is turned OFF (states 1 and 2), the current i_r flows through the decoupling capacitor C_d as well as the load. That means part of the energy in the grid is directly transferred to the load and the rest into C_d. When the switch S_1 is turned ON (states 3 and 4), the current i_r is bypassed, and the diode D_1 is reverse-biased to avoid the short circuit. As to the output voltage regulation circuit, when the switch S_2 is turned ON (states 1 and 3), the current i_1 flows through the decoupling capacitor C_d. When switch S_2 is turned OFF (states 2 and 4), the current i_1 flows through the load. The whole circuit is something like a Sepic PFC circuit. The output voltage can be wide and its polarity is positive.

III. Circuit Analysis and Controller Design

This section introduces the circuit analysis and the controller design. Assumes that the converter operates in a continuous current mode in both input and output inductors, the grid voltage is pure sinusoidal, all the components are ideal and lossless, and the switching voltage ripples are negligible during the switching period T_s.

A. Modeling and Analysis

According to Fig. 2, the state-space average model is formulated as follows:

$$L\frac{di_r}{dt} = v_r - v_d - v_o + d_1\left(v_d + v_o\right) \tag{1}$$

$$C_d\frac{dv_d}{dt} = d_1' i_r - d_2 i_1 \tag{2}$$

$$L_1\frac{di_1}{dt} = d_2\left(v_d + v_o\right) - v_o \tag{3}$$

$$C_o\frac{dv_o}{dt} = d_1' i_r + d_2' i_1 - i_o \tag{4}$$

where d_1 and d_2 represent the duty cycles of switches S_1 and S_2 and

$$d_1 + d_1' = 1$$
$$d_2 + d_2' = 1$$

Assume that the steady-state rectified output voltage v_r and the inductor current i_r are

$$v_r = V\left|\cos(\omega t)\right| \tag{5}$$

$$i_r = I\left|\cos(\omega t)\right| \tag{6}$$

where V and I are the peak values of v_r and i_r; and ω is the angular frequency of the grid voltage. According to (1) and (6),

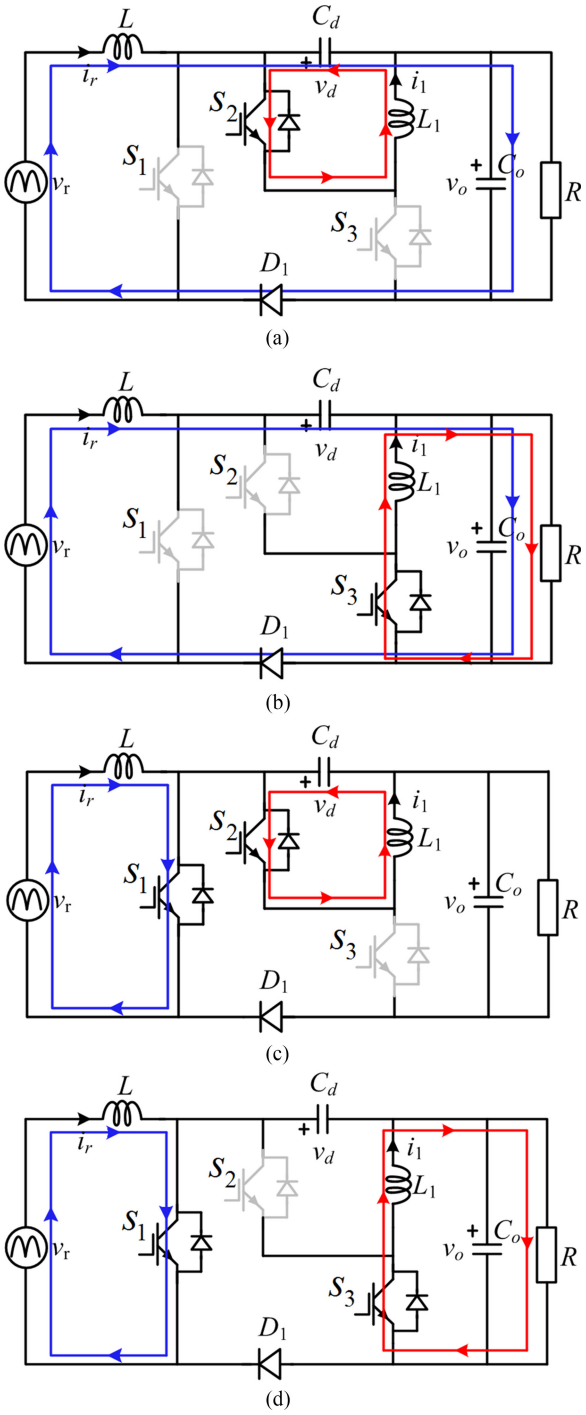

Fig. 2. Operating states of the proposed PFC rectifier. (a) State 1 (S_1 = OFF, S_2 = ON, S_3 = OFF). (b) State 2 (S_1 = OFF, S_2 = OFF, S_3 = ON). (c) State 3 (S_1 = ON, S_2 = ON, S_3 = OFF). (d) State 4 (S_1 = ON, S_2 = OFF, S_3 = ON).

the steady-state expression for d_1

$$d_1 = \frac{1}{v_d + v_o}[v_d + v_o - v_r - \text{sgn}(\cos(\omega t)) \cdot \omega L \sin(\omega t)] \tag{7}$$

where sgn() is the sign function. Generally, the last term on the right side of (7) is so small that it can be ignored [32], [38]. Then (7) is simplified to

$$d_1 = 1 - \frac{v_r}{v_d + v_o} \tag{8}$$

Similarly, according to (3) the steady-state expression for d_2 is obtained as follows:

$$d_2 = \frac{v_o}{v_o + v_d}. \tag{9}$$

According to (8) and (9), the relation between v_o and v_r is expressed as

$$v_o = \frac{d_2}{d_1' v_r}. \tag{10}$$

In theory d_2/d_1' could be any positive value. Then, the converter has a wide output voltage range.

The power at the grid side P_{ac} is given as

$$P_{\text{ac}} = v_r i_r = \underbrace{VI/2}_{P_o} + \underbrace{VI/2\cos(2\omega t)}_{\tilde{P}} \tag{11}$$

where $\tilde{p}$ is the ripple power and P_o is the load power.

Suppose that the ripple power is buffered by the capacitor C_d, and then

$$C_d \frac{dv_d}{dt} v_d = \tilde{p}. \tag{12}$$

By integrating both sides of (12) with respect to time, the decoupling capacitor voltage v_d can be expressed as

$$v_d = \sqrt{\bar{v}_d^2 + \frac{P_o \sin(2\omega t)}{\omega C_d}} \tag{13}$$

where $\bar{v}_d$ is the dc component. Then, the average current flowing through the capacitor C_d is

$$i_d = \frac{\tilde{p}}{v_d} = \frac{P_o \cos(2\omega t)}{\sqrt{\bar{v}_d^2 + \frac{P_o \sin(2\omega t)}{\omega C_d}}}. \tag{14}$$

Subtracting (2) from (4) leads to

$$i_1 = i_o - i_d. \tag{15}$$

i_1 can be positive or negative. If v_d is high enough, i_d can be always less than i_o. Then, i_1 will be always positive and the switch S_3 can be replaced with a diode.

The time domain waveforms of the grid voltage/current, power distribution, voltage v_d, and average current i_d are shown in Fig. 3 using the parameters in this paper. It can be seen that the low ripple power is buffered by the capacitor C_d. Then, C_d is charging when $\tilde{p} > 0$ and discharging when $\tilde{p} \leq 0$.

B. Controller Design

Two independent control loops are designed to achieve PFC, ripple power decoupling, decoupling capacitor voltage regulation, and output voltage regulation. The adopted control idea is well stated in [25], [31], [32], [34], [38], and [39]. So this paper only gives a brief introduction of it.

The first control loop is to control the current i_r (grid current i_g) and the control scheme is shown in Fig. 4. It is completed by controlling the switch S_1. The phase information of the current

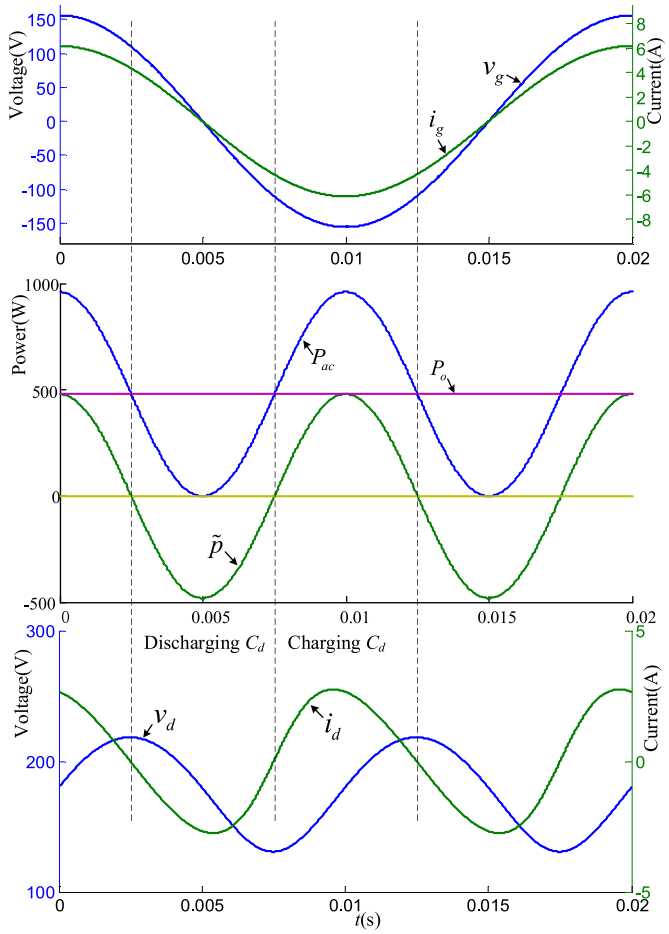

Fig. 3. Time domain waveforms of the grid voltage v_g, grid current i_g, power distribution, voltage v_d, and current i_d.

reference is obtained by using a digital phase locked loop. In this way, the reference signal is always proportional to the grid voltage, which is to achieve the PFC. The amplitude of current reference is obtained according to the error of the averaged decoupling capacitor voltage [38], [39]

$$I^* = \left(k_{p1} + \frac{k_{i1}}{s}\right)(\bar{v}_d^* - \bar{v}_d) \tag{16}$$

where k_{p1} and k_{i1} are the proportional term and the integral gain. $\bar{v}_d$ is obtained by a moving average filter in implementation. Finally, the current reference i_r^* is obtained as

$$i_r^* = I^*|\cos(\omega t)|. \tag{17}$$

To track i_r^*, according to (8), the control output d_1^* is designed as

$$d_1^* = \frac{\left(k_{p2} + \frac{k_{i2}}{s}\right)(i_i^* - i_i)}{v_d + v_o} + \frac{v_d + v_o - v_r}{v_d + v_o} \tag{18}$$

where k_{p2} and k_{i2} are the proportional and integral gains. The second term in (18) is a feed-forward to improve the dynamic response.

The second control loop is for output voltage regulation. The control block is shown inFig. 5. It is achieved by controlling switches S_2 and S_3. The classical dual-loop control strategy is used. The output voltage error is sent into PI-3 compensator and its output is taken as the inner loop current reference i_1^*. To track i_1^*, according to (9), the control output d_2^* is designed as

$$d_2^* = \frac{\left(k_{p4} + \frac{k_{i4}}{s}\right)(i_1^* - i_1)}{v_d + v_o} + \frac{v_o}{v_d + v_o} \tag{19}$$

where k_{p4} and k_{i4} are the proportional and integral gains. The second term in (19) is a feed-forward.

Note that once the output voltage v_o and the rectified current i_r are well regulated, the ripple power will be fully absorbed by the decoupling capacitor C_d. That control idea is called automatic-power-decoupling control in [39]. Its highlight is no extra dedicated power-buffering controller is required. In addition, other controllers, such as the adaptive voltage control [31] and the dual-loop control structure with parallel-connected multiresonant-bank-enhanced voltage loop [38], can be used to achieve a better control performance with increasing the control complexity.

IV. Selection of Components

A. Selection of C_d

Considering the limitations $0 \le d_1, d_2 \le 1$, the following constraint is obtained:

$$v_r \le v_d + v_o. \tag{20}$$

Solving (20) leads to

$$\sqrt{(v_r - v_o)^2 - \frac{P_o \sin(2\omega t)}{\omega C_d}} \le \bar{v}_d. \tag{21}$$

Then, the lower limit of $\bar{v}_d$ could be chosen as follows:

$$\bar{v}_d \ge \begin{cases} \sqrt{(V - v_o)^2 + \frac{P_o}{\omega C_d}}, & v_o \le V \\ \sqrt{\frac{P_o}{\omega C_d}}, & v_o > V \end{cases}. \tag{22}$$

Suppose that the permissible maximum voltage on semiconductors and passive components is $V_{\max}$, the upper limit of $\bar{v}_d$ is similarly obtained

$$\bar{v}_d \le \sqrt{V_{\max}^2 - \frac{P_o}{\omega C_d}}. \tag{23}$$

To guarantee $\bar{v}_d$ has a solution, according to (22) and (23), the following constraint should be met:

$$V_{\max} \ge \begin{cases} \sqrt{(V - v_o)^2 + \frac{2P_o}{\omega C_d}}, & v_o \le V \\ \sqrt{\frac{2P_o}{\omega C_d}}, & v_o > V \end{cases}. \tag{24}$$

Then, the voltage stress of capacitor C_d is

$$v_{d\max} = \sqrt{\bar{v}_d^2 + \frac{P_o}{\omega C_d}}. \tag{25}$$

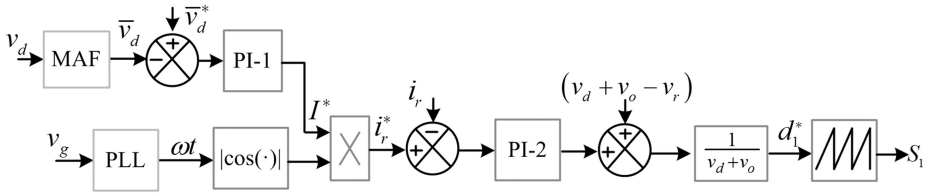

Fig. 4. Control scheme for the grid current.

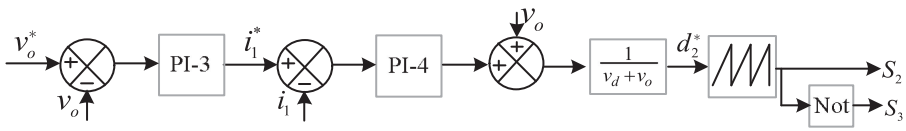

Fig. 5. Control scheme for the output voltage.

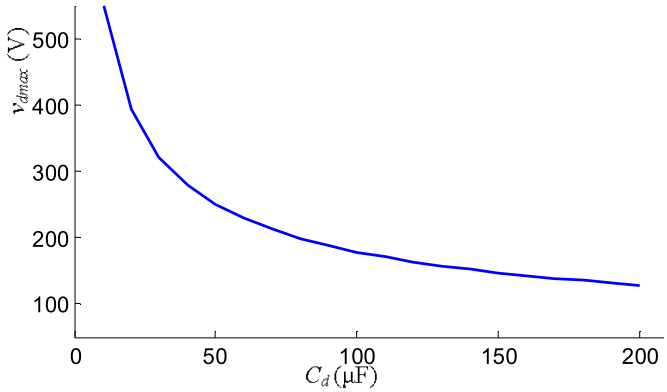

Fig. 6. Voltage stress versus the value of C_d.

Considering $\bar{v}_d$ being equal to its lower limit, the minimum C_d is

$$C_{d\min} = \begin{cases} \frac{2P_o}{\omega\left(v_{d\max}^2 - (V - v_o)^2\right)}, & v_o \le V \\ \frac{2P_o}{\omega v_{d\max}^2}, & v_o > V \end{cases}. \tag{26}$$

In practice $\bar{v}_d$ should be selected with a proper margin to ensure (22) is always satisfied. By adopting the parameters in this paper, the curve of the voltage stress against the capacitor C_d is shown in Fig. 6. As seen, the voltage stress decreases with the increase of the capacitance. Considering the tradeoff between the voltage stress and the capacitance, C_d is selected to be 90 μF.

B. Selection of L

Inductor L is selected according to the limit of the switching ripple. Since the switching frequency is much higher than the fundamental frequency, the average current of i_r over each switching period is assumed to be constant. Then, the peak–peak switching ripple of the inductor current i_r is given as

$$\Delta i_r = \frac{d_1 v_r}{f_s L} = \frac{v_r\left(v_d + v_o\right) - v_r^2}{f_s L\left(v_d + v_o\right)} \tag{27}$$

where f_s is the switching frequency. Then, L can be selected by

$$L \ge \frac{v_r\left(v_d + v_o\right) - v_r^2}{\Delta i_r f_s\left(v_d + v_o\right)} = \frac{v_r\left(1 - \frac{v_r}{\left(v_d + v_o\right)}\right)}{\Delta i_r f_s}. \tag{28}$$

In addition, L should be much smaller than $V/(I\omega)$ to avoid a large phase shift and then degrading the PF.

C. Selection of L_1

Similarly, the peak–peak switching current ripple of the inductor current i_1 can be determined as

$$\Delta i_1 = \frac{v_d d_2}{f_s L_1} = \frac{v_d v_o}{f_s L_1\left(v_d + v_o\right)}. \tag{29}$$

The maximum value of the ripple current appears at $v_{d\max}$. Then, L_1 can be selected according to

$$L_1 \ge \frac{v_o}{\Delta i_1 f_s\left(1 + \frac{v_o}{v_{d\max}}\right)}. \tag{30}$$

From (28) and (30), the voltage v_d is expected to be small from the view of reducing the ripple currents and, hence, the size of the inductor.

Another interesting phenomenon is that according to (15), the current rating of L_1 is not only related to the load power, but also the load current i_o and the decoupling capacitor C_d. For example, the peak value of i_1 increases with the increase of C_d, as shown in Fig. 7, which is plotted using the parameters in this paper. However, the slope decreases with the increase of C_d. That should be paid attention when determining the current rating.

D. Selection of C_o

C_o is only used to filter high switching harmonics. To reduce its voltage ripple, S_1 is turned ON during the subinterval $(1 - d_1,\ 1)T_s$ and S_2 is turned ON during the subinterval $(0,\ d_2)T_s$ in each switching period. Then, the peak–peak switching ripple of v_o is determined as (31) shown at the bottom of the next page.

Clearly, the analytic solution of the maximum voltage ripple $\Delta v_{\max}$ is hard to obtain. Then, the numerical analysis is adopted.

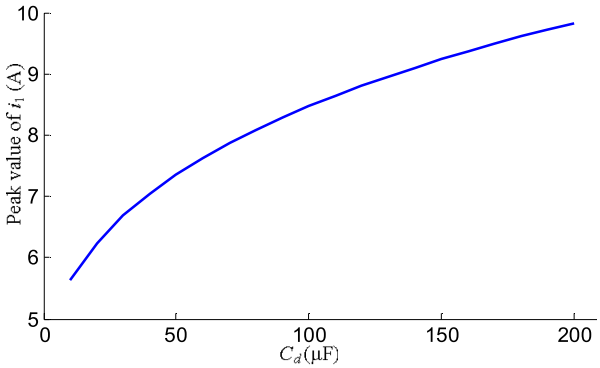

Fig. 7. Peak value of i_1 versus the value of C_d.

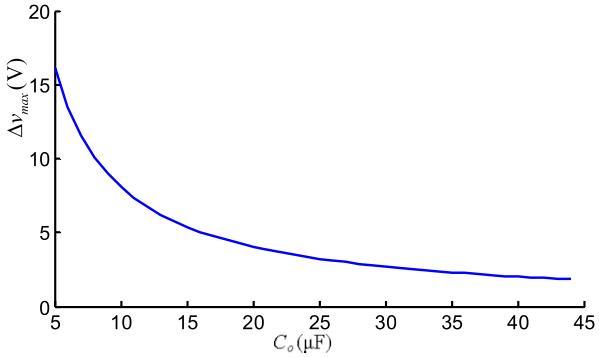

Fig. 8. Maximum value of the voltage ripple $\Delta v_{\max}$ versus the value of C_o.

By using specific parameters in this study, the curve of $\Delta v_{\max}$ against the capacitor C_o is shown in Fig. 8. It can be used to determine the value of C_o according to the voltage ripple limit.

E. Semiconductor Device

The threshold voltages across active switches and diodes are evaluated by the related maximum voltage. The averaged current and the square of the rms current over the mains period are evaluated by [40]

$$I_{\text{avg}} = \frac{1}{2\pi}\int_0^{2\pi} i_{T\_\text{avg}} d\varphi \tag{32}$$

$$I_{\text{rms}}^2 = \frac{1}{2\pi}\int_0^{2\pi} i_{T\_\text{rms}}^2 d\varphi \tag{33}$$

where

$$i_{T\_\text{avg}} = \frac{1}{T_s}\int_0^{T_s} i(\varphi, t_\mu) dt_\mu = d(\varphi) i(\varphi),$$

$$i_{T\_\text{rms}}^2 = \frac{1}{T_s}\int_0^{T_s} i^2(\varphi, t_\mu) dt_\mu = d(\varphi) i^2(\varphi),$$

$\varphi = \omega t$, $d(\varphi)$ is the duty ratio, and $i(\varphi)$ is the current flowing through the switch or the diode.

For the diode rectifier, the voltage stress is the amplitude of the grid voltage (V). Diodes switch at the grid frequency to conduct current i_r and the current stresses of each diode are calculated as

$$I_{D_r\_\text{avg}} = \frac{1}{4\pi}\int_0^{2\pi} i_r \, d\varphi = \frac{I}{\pi} \tag{34}$$

$$I_{D_r\_\text{rms}}^2 = \frac{1}{4\pi}\int_0^{2\pi} i_r^2 \, d\varphi = \frac{I^2}{4}. \tag{35}$$

For the switch S_1 and the diode D_1, they work complementarily. The voltage stress is both $(v_{d\max} + v_o)$. Both of them conduct current i_r and the current stresses are derived as

$$\begin{aligned} I_{D_1\_\text{avg}} &= \frac{1}{2\pi}\int_0^{2\pi} d_1' i_r d\varphi \\ &= \frac{P_o}{2\pi}\int_0^{2\pi} \frac{1+\cos(2\varphi)}{v_o + \sqrt{\bar{v}_d^2 + \frac{P_o \sin(2\varphi)}{\omega C_d}}} d\varphi \end{aligned} \tag{36}$$

$$\begin{aligned} I_{D_1\_\text{rms}}^2 &= \frac{1}{2\pi}\int_0^{2\pi} d_1' i_r^2 d\varphi \\ &= \frac{\frac{P_o}{2\pi}}{} \int_0^{2\pi} \frac{I\,|\cos(\varphi)|\,(1+\cos(2\varphi))}{v_o + \sqrt{\bar{v}_d^2 + \frac{P_o \sin(2\varphi)}{\omega C_d}}} d\varphi \end{aligned} \tag{37}$$

$$\begin{aligned} I_{S_1\_\text{avg}} &= \frac{1}{2\pi}\int_0^{2\pi} d_1 i_r d\varphi \\ &= \frac{1}{2\pi}\int_0^{2\pi} I\,|\cos(\varphi)| - \frac{P_o\,(1+\cos(2\varphi))}{v_o + \sqrt{\bar{v}_d^2 + \frac{P_o \sin(2\varphi)}{\omega C_d}}} d\varphi \end{aligned} \tag{38}$$

$$\begin{aligned} I_{S_1\_\text{rms}}^2 &= \frac{1}{2\pi}\int_0^{2\pi} d_1 i_r^2 d\varphi \\ &= \frac{1}{2\pi}\int_0^{2\pi} (I\cos(\varphi))^2 - \frac{2P_o I|\cos(\varphi)|^3}{v_o + \sqrt{\bar{v}_d^2 + \frac{P_o \sin(2\varphi)}{\omega C_d}}} d\varphi. \end{aligned} \tag{39}$$

$$\begin{cases} \Delta v = \begin{cases} \max(0, \Delta v_1, \Delta v_2) - \min(0, \Delta v_1, \Delta v_2), & d_1 + d_2 < 1 \\ \max(0, \Delta v_3, \Delta v_4) - \min(0, \Delta v_3, \Delta v_4), & d_1 + d_2 \geq 1 \end{cases} \\ \Delta v_1 = \frac{T_s d_2}{C_o}\left(i_r - i_o\right), \Delta v_2 = \Delta v_1 + \frac{T_s(1-d_1-d_2)}{C_o}\left(i_r + i_1 - i_o\right) \\ \Delta v_3 = \frac{T_s(1-d_1)}{C_o}\left(i_r - i_o\right), \Delta v_4 = \Delta v_3 + \frac{T_s(d_1+d_2-1)}{C_o}\left(-i_o\right) \end{cases} \tag{31}$$

TABLE I
VOLTAGE AND CURRENT STRESSES

Device	Voltage stress (V)		Current stress (average/A)		Current stress (rms/A)	
	Theoretical value	Simulation value	Theoretical value	Simulation value	Theoretical value	Simulation value
D_r	155.56	156.5	1.96	1.99	3.08	3.19
D_1	338.35	342	1.63	1.64	2.92	3.02
S_1	338.35	342	2.29	2.36	3.24	3.39
S_2	338.35	342	1.63	1.64	2.84	2.86
S_3	338.35	342	2.37	2.41	3.42	3.47

For switches S_2 and S_3, they work complementarily. The voltage stress is both $(v_{d\max} + v_o)$. Both of them conduct current i_1 and the current stresses are calculated as

$$I_{S_2\_\text{avg}} = \frac{1}{2\pi}\int_0^{2\pi} d_2\,|i_1|\,d\varphi$$

$$= \frac{1}{2\pi}\int_0^{2\pi} \frac{v_o}{v_o + \sqrt{\bar{v}_d^2 + \frac{P_o\sin(2\varphi)}{\omega C_d}}}\left| i_o - \frac{P_o\cos(2\varphi)}{\sqrt{\bar{v}_d^2 + \frac{P_o\sin(2\varphi)}{\omega C_d}}}\right| d\varphi \tag{40}$$

$$I_{S_2\_\text{rms}}^2 = \frac{1}{2\pi}\int_0^{2\pi} d_2 i_r^2 d\varphi$$

$$= \frac{1}{2\pi}\int_0^{2\pi} \frac{v_o}{v_o + \sqrt{\bar{v}_d^2 + \frac{P_o\sin(2\varphi)}{\omega C_d}}}\left(i_o - \frac{P_o\cos(2\varphi)}{\sqrt{\bar{v}_d^2 + \frac{P_o\sin(2\varphi)}{\omega C_d}}}\right)^2 d\varphi \tag{41}$$

$$I_{S_3\_\text{avg}} = \frac{1}{2\pi}\int_0^{2\pi} d_2' i_1 d\varphi$$

$$= \frac{1}{2\pi}\int_0^{2\pi} \frac{\sqrt{\bar{v}_d^2 + \frac{P_o\sin(2\varphi)}{\omega C_d}}}{v_o + \sqrt{\bar{v}_d^2 + \frac{P_o\sin(2\varphi)}{\omega C_d}}}\left| i_o - \frac{P_o\cos(2\varphi)}{\sqrt{\bar{v}_d^2 + \frac{P_o\sin(2\varphi)}{\omega C_d}}}\right| d\varphi \tag{42}$$

$$I_{S_3\_\text{rms}}^2 = \frac{1}{2\pi}\int_0^{2\pi} d_2' i_1^2 d\varphi$$

$$= \frac{1}{2\pi}\int_0^{2\pi} \frac{\sqrt{\bar{v}_d^2 + \frac{P_o\sin(2\varphi)}{\omega C_d}}}{v_o + \sqrt{\bar{v}_d^2 + \frac{P_o\sin(2\varphi)}{\omega C_d}}}\left(i_o - \frac{P_o\cos(2\varphi)}{\sqrt{\bar{v}_d^2 + \frac{P_o\sin(2\varphi)}{\omega C_d}}}\right)^2 d\varphi. \tag{43}$$

Using the parameters in this paper, the voltage and current stresses by calculation and simulation are summarized in Table I. As seen, the theoretical and simulation results are consistent with each other. Table I presents a basis for the selection of the semiconductor devices.

V. SIMULATIONS AND EXPERIMENTAL RESULTS

A. Simulations

In order to verify the correctness of the theoretical analysis before, simulations under ideal conditions are carried out in MATLAB/Simulink environment. The circuit was designed for 110 V_{rms} ac-input, 120 V dc-output, 30-Ω load resistance, and runs at $f_s = 20$ kHz. L and L_1 are 3 mH and 1.5 mH. The values of C_d and C_o are 90 μF and 20 μF, respectively. The dc component of v_d is set to be 180 V with considering proper margin.

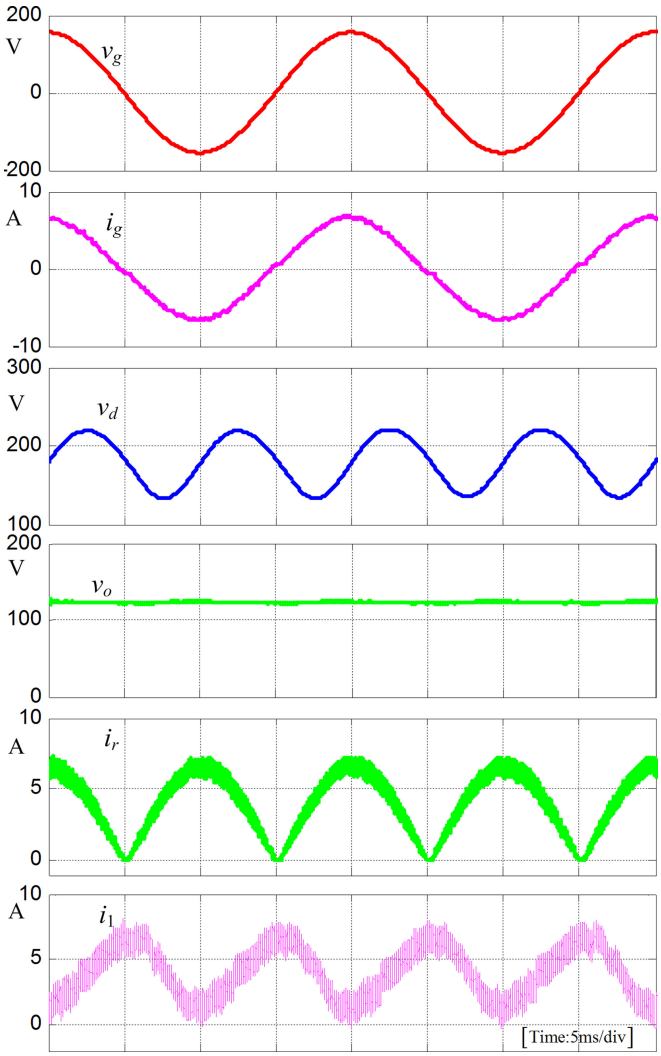

Fig. 9. Steady-state simulation waveforms of the grid voltage v_g, grid current i_g, capacitor voltage v_d, load voltage v_o, inductor current i_r, and inductor current i_1.

Fig. 9 shows the steady-state simulation results. As can be observed, the input current i_g is sinusoidal and in phase with

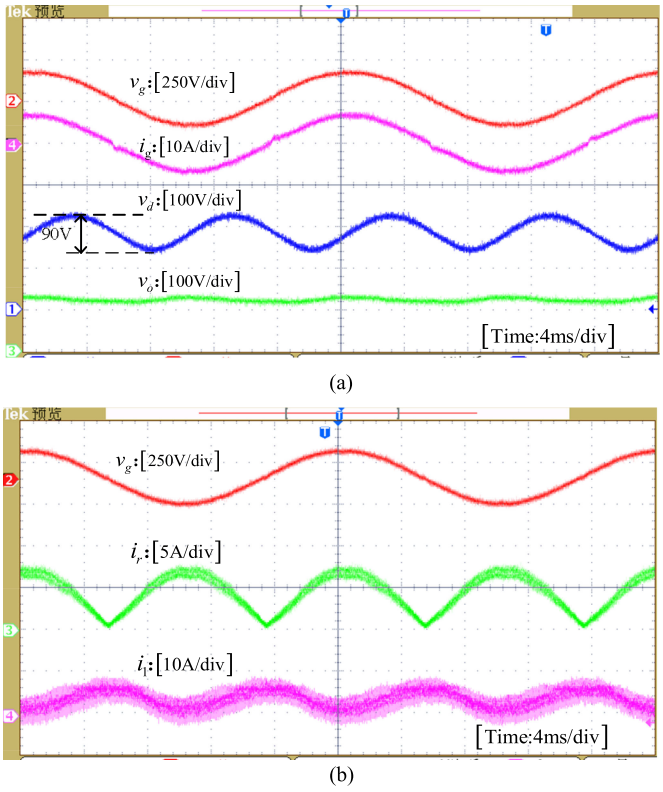

Fig. 10. Steady-state experimental waveforms when $V_o = 120$ V. (a) Grid voltage v_g, grid current i_g, capacitor voltage v_d, and load voltage v_o. (b) Inductor currents i_r and i_1.

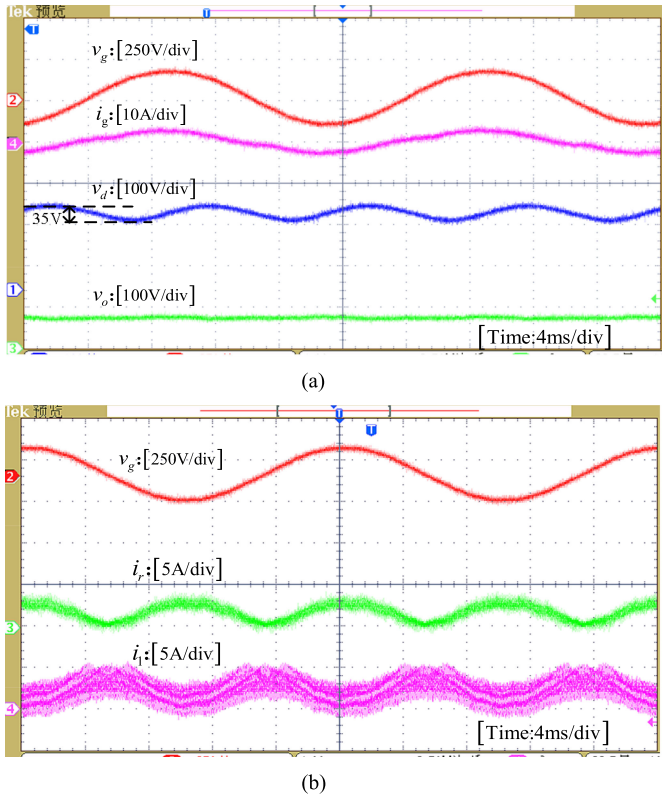

Fig. 11. Steady-state experimental waveforms when $V_o = 70$ V. (a) Grid voltage v_g, grid current i_g, capacitor voltage v_d, and load voltage v_o. (b) Inductor currents i_r and i_1.

the input voltage v_g. The PF is 0.998 and the total harmonic distortion (THD) is 3.36%. The output voltage v_o is flat because the ripple power is diverted to the capacitor C_d. Therefore, the voltage v_d swings at twice the grid frequency. Its minimum value is about 137 V, which is less than the peak value of the gird voltage (156 V).

B. Experiments

A prototype was built to verify the feasibility of the proposed circuit topology and control scheme. The control algorithm of the converter is realized by a universal control board which consists of a digital signal processor TMS320F28335 and a field programmable gate array FPGA EP2C8T144C8N. The circuit parameters are the same as those using in the simulation. Considering a proper margin for the overvoltage due to the turn-OFF, the selected insulated-gate bipolar transistors and diodes are IKW50N65H5 (650 V, 50 A) from INFINEON and IXYS DSEP 30-06BR (600 V, 30 A) from IXYS, respectively.

Fig. 10 shows the steady-state experimental waveforms with 120 V output voltage. As seen, the experimental results are in good agreement with the simulation results. Fig. 11 shows the experimental waveforms with 70 V output voltage. Good input and output performances are still obtained. The peak–peak value of the decoupling capacitor voltage is reduced to 35 V due to the reduction of ripple power. The percentage of the harmonics versus its dc component is shown in Fig. 12. It is clear that in

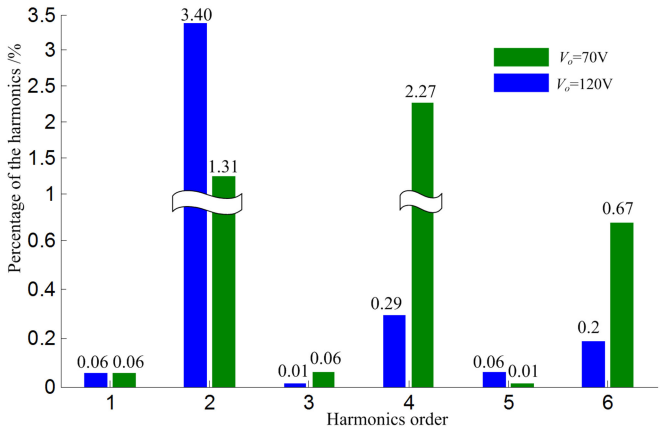

Fig. 12. Percentage of the output voltage harmonics versus its dc component.

both cases the rms of the second harmonic voltage (100 Hz) is small [ratio to the dc component is 3.4% (1.31%) with 120 V (70 V) output voltage]. To realize the same voltage ripple level with large electrolytic capacitors, the required capacitance is 1.1 mF (2.9 mF). Therefore, the reliability and the power density are improved with the proposed circuit.

Fig. 13 shows the gate-emitter voltages of switches S_1 and S_2, inductor current i_r, and inductor current i_1. At the zero crossing of the grid voltage, the duty ratio of switch S_1 is close to one and at the peak value point it is about 0.5. The drive signal of S_1

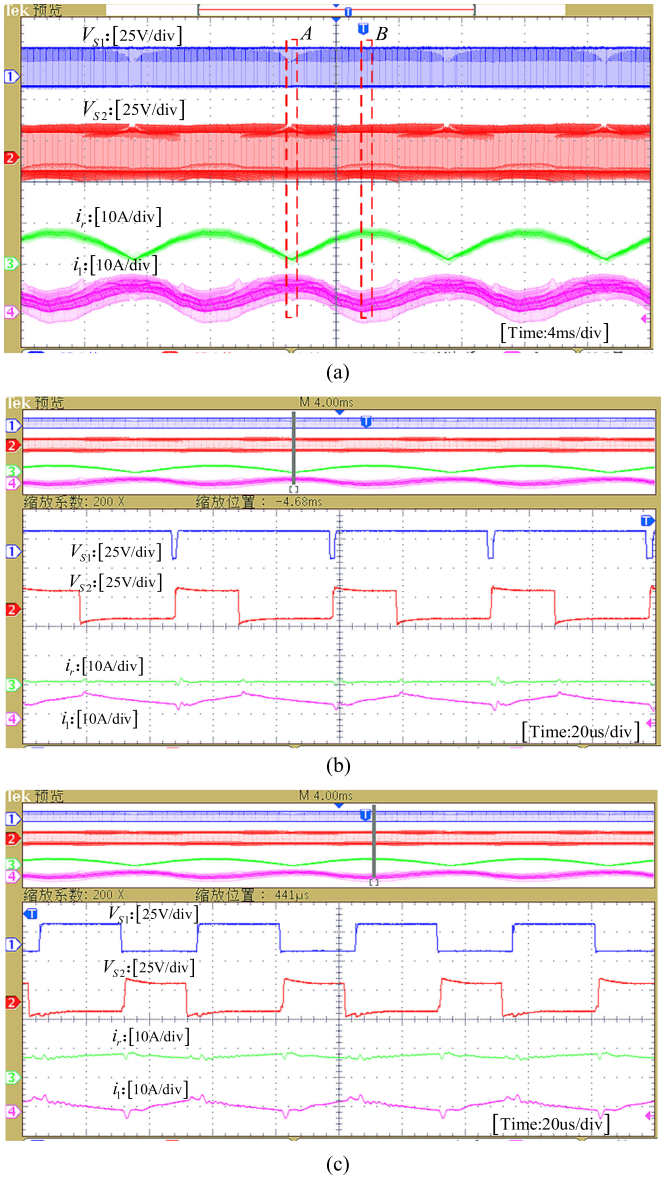

Fig. 13. Experimental waveforms of gate-emitter voltages, inductor currents i_r and i_1 when the output voltage is 120 V (the load power is 480 W). (a) Waveforms of V_{s1}, V_{s2}, i_r, and i_1. (b) Zoom-in waveforms of point A. (c) Zoom-in waveforms of point B.

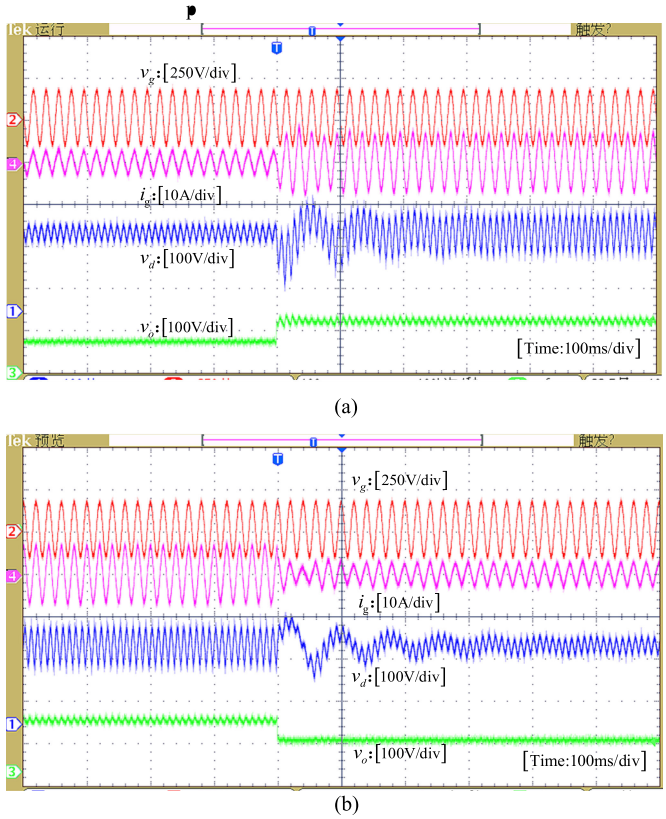

Fig. 14. Dynamic experimental waveforms. (a) Step-up load change from 70 to 120 V. (b) Step-down load change from 120 to 70 V.

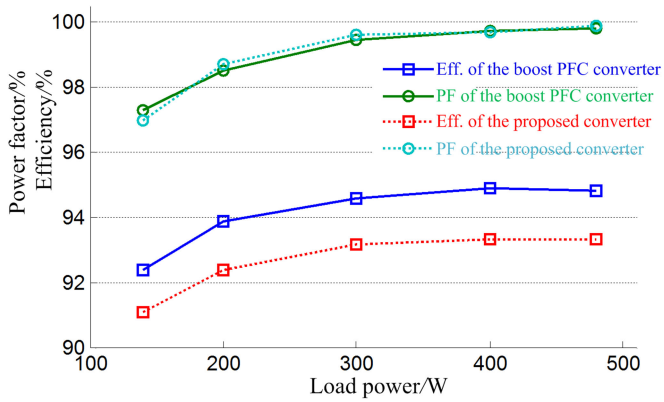

Fig. 15. System efficiency and PF of the proposed circuit.

varies in a wide range to track the grid current reference. The duty ratio of S_2 is always about 0.4, which is helpful to avoid narrow pulse.

Fig. 14 shows the dynamic response of the system. In Fig. 14(a), the load voltage reference is changed from 70 to 120 V suddenly. As seen, the output voltage tracks its reference quickly. And the fluctuation range of v_d increases accordingly due to the increased ripple power. Fig. 14(b) shows the opposite transient process.

Fig. 15 shows the efficiency and the grid current PF as a function of the load power. The tests have been done with a fixed load resistance and the output voltage varies from 65 to 120 V. For the proposed converter, the peak efficiency can be 93.32% and the PF is above 0.97 within the overall power range. However, the efficiency is lower than that of the classical boost PFC rectifier and the extra power losses are mainly introduced by the output voltage regulation circuit.

C. Comparison

Table II presents a comparison between different PFC converters with power decoupling function. The term of "added semiconductor devices" is a result compared with the classic boost PFC rectifier. It can be found that all the existing methods add extra semiconductor devices and an extra capacitor to buffer the low-frequency ripple power. But the proposed circuit does

TABLE II
COMPARISON BETWEEN DIFFERENT PFC COVERTERS WITH POWER DECOUPLING FUNCITON

Decoupling circuit	Power rating	Decoupling component (Value)	Added semiconductor devices	Efficiency	Constraint of the decoupling capacitor voltage	Output voltage range
Ref. [30]	35 W	1 Capacitor (20 μF)	2 MOSFETs	87%	$v_o < v_d < V_{\max}$	$0 < v_o$
Ref. [32]	2 kW	1 Capacitor (20 μF)	3 IGBTs+ 1 Diode	93%	$\lvert v_g \rvert < v_d < V_{\max}$	$0 < v_o$
Ref. [33]	750 W	1 Capacitor (100 μF)	1 MOSFET	96.4%	$\lvert v_g \rvert < v_d < V_{\max}$	$0 < v_o < V/2$
Ref. [34]	100 W	1 Capacitor (15 μF)	1 MOSFET	93.5%	$(\lvert v_g \rvert + v_o) < v_d < V_{\max}$	$0 < v_o$
Ref. [35]	75 W	2 Capacitors (68 μF, 6.8 μF)	1 MOSFET + 1 Diode	91%	$0 < v_d < v_o$	$0 < v_o$
Ref. [36]	1 kW	2 Capacitors (90 μF)	2 IGBTs	92.1%	$0 < v_d < v_o/2$	$V < v_o$
In this paper	480 W	1 Capacitor (90 μF)	2 IGBTs	93.3%	$(\lvert v_g \rvert - v_o) < v_d < V_{\max}$	$0 < v_o$

not cost more compared to most other decoupling circuits. Note that the components used in the proposed circuit are identical to those in [36]. But the proposed method has a wider output voltage. On the other hand, the decoupling capacitor voltage in the proposed circuit is flexible and can be smaller than the peak grid voltage. However, in [32]–[34], the decoupling capacitor voltage has to be larger than the peak grid voltage. Overall, the proposed decoupling circuit can be competitive by a comprehensive consideration of cost, voltage stress, and the scope of the output voltage.

VI. CONCLUSION

This paper proposed a single-phase PFC rectifier consisting of a PFC circuit and a buck–boost output voltage regulation circuit. Some highlights of the proposed rectifier include: high PF (0.99 at rated load power), wide output voltage range, flexible control due to utilizing two independent control loops, and having no electrolytic capacitors in the power stage (E-cap-less structure). In addition, the ripple power is buffered without a dedicated power-buffering controller. A laboratory prototype was built to verify the effectiveness of the proposed circuit topology. The results indicate that the proposed circuit can be a good candidate for volume-critical and lifetime-critical applications.

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Yonglu Liu (S'16) was born in Chongqing, China, in 1989. He received the B.S. and M.S. degrees in electrical engineering, in 2012 and 2015, respectively, from Central South University, Changsha, China, where he is currently working toward the Ph.D. degree in electrical engineering.

His research interests include matrix converter and ac/dc converter.

Yao Sun (M'13) was born in Hunan, China, in 1981. He received the B.S. degree in automation, and the M.S. and Ph.D. degrees in electric engineering from the School of Information Science and Engineering, Central South University, Changsha, China, in 2004, 2007, and 2010, respectively.

He has been an Associate Professor in the School of Information Science and Engineering, Central South University. His research interests include matrix converter, microgrid, and wind energy conversion system.

Mei Su was born in Hunan, China, in 1967. She received the B.S. degree in automation, and the M.S. and Ph.D. degrees in electric engineering from the School of Information Science and Engineering, Central South University, Changsha, China, in 1989, 1992, and 2005, respectively.

Since 2006, she has been a Professor in the School of Information Science and Engineering, Central South University. Her research interests include matrix converter, adjustable speed drives, and wind energy conversion system.

Min Zhou was born in Hunan, China, in 1993. He received the B.S. degree in automation in 2016 from Xiangtan University, Xiangtan, China. He is currently working toward the M.S. degree in electrical engineering at Central South University, Changsha, China.

His research interests include matrix converter and ac/dc converters.

Qi Zhu was born in Anhui Province, China, in 1993. He received the B.S. degree in electrical engineering and automation from Central South University, Changsha, China, in 2014. He is currently working toward the Ph.D. degree in electrical engineering.

His research interests include matrix converters and wireless power transmission.

Xing Li was born in Hunan, China, in 1988. She received the B.S. degree in automation, and the M.S. and Ph.D. degrees in electric engineering from the School of Information Science and Engineering, Central South University, Changsha, China, in 1989, 2009, and 2014, respectively.

She is currently an Assistant Professor in the College of Electrical and Information Engineering, Hunan University, Changsha, China. Her research interests include power electronic converter and wind energy conversion system.