A Deep Insight Into the Degradation of 1.2-kV 4H-SiC MOSFETs Under Repetitive Unclamped Inductive Switching Stresses

Xintian Zhou, Hongyuan Su, Ruifeng Yue, Gang Dai, Juntao Li, Yan Wang, and Zhiping Yu, *Fellow, IEEE*

***Abstract*—In this paper, the long-term reliability of commercial 1.2-kV 4H-SiC MOFSETs under repetitive unclamped inductive switching stresses is evaluated experimentally. The degradation of device characteristics, including the threshold voltage $V_{\rm th}$, drain leakage current $I_{\rm dss}$, and on-state resistance $R_{\rm on}$, is observed after 80k avalanche cycles. The regular charge pumping (CP) measurements reveal that the failure mechanism characterized by the hot holes injection and trapping into the gate oxide above the channel and JFET region may occur during the aging experiments, which is further ascertained by the succeeding electrothermal simulations and should be responsible for the degradation of $V_{\rm th}$ and $I_{\rm dss}$. After decapping the failed devices, the bond wires lift off due to thermal fatigue is discovered and regarded as the main reason for the degradation of $R_{\rm on}$. The poststress high-temperature treatment is also carried out as an approach to indirectly corroborate the aforementioned failure mechanisms. Moreover, the impact of different test conditions on the degradation rate of electrical characteristics is discussed to thereby find ways to relieve these degeneration phenomena.**

***Index Terms*—4H-SiC MOSFETs, bond wires lift-off, electrical parameters degradation, hot holes, repetitive unclamped inductive switching (UIS).**

NOMENCLATURE

$V_{\rm ds}$	MOSFET drain–source voltage (V).
$I_{\rm ds}$	MOSFET drain–source current (A).
$V_{\rm gs}$	MOSFET gate–source voltage (V).
$V_{g,\rm on}$	High level of the gate pulse to switch on the MOSFET (V).
$V_{g,\rm off}$	Low level of the gate pulse to switch OFF the MOSFET (V).
R_g	MOSFET external gate resistance (Ω).
I_g	MOSFET gate current (A).
$T_{\rm case}$	The device case temperature (K).
$V_{\rm th}$	MOSFET threshold voltage (V), measured at $V_{\rm gs} = V_{\rm ds}$, $I_{\rm ds} = 5$ mA, $T_{\rm case} = 300$ K.
$I_{\rm dss}$	MOSFET drain leakage current (mA), measured at $V_{\rm gs} = 0$ V, $V_{\rm ds} = 1200$ V, $T_{\rm case} = 300$ K.
$R_{\rm on}$	MOSFET drain–source on-state resistance (mΩ), measured at $V_{\rm gs} = 20$ V, $I_{\rm ds} = 20$ A, $T_{\rm case} = 300$ K.
$I_{\rm gss}$	MOSFET gate–source leakage current (nA), measured at $V_{\rm ds} = 0$ V, $V_{\rm gs} = 20$ V, $T_{\rm case} = 300$ K.
$I_{\rm cp}$	Charge pumping current (A).
V_b	Pulse base level in the charge pumping test (V).
V_p	Pulse amplitude in the charge pumping test (V).
$V_{\rm (br)DSS}$	MOSFET avalanche breakdown voltage (V).
$I_{\rm av}$	MOSFET avalanche current (A).
$t_{\rm on}$	Gate pulse duration (μs).
$t_{\rm av}$	MOSFET avalanche time (μs).
$E_{\rm av}$	Avalanche energy sustained by the MOSFET (J).
L	Load inductance in the UIS test circuit (mH).
$V_{\rm DD}$	Bus voltage in the UIS test circuit (V).

Manuscript received June 6, 2017; accepted July 17, 2017. Date of publication July 21, 2017; date of current version February 22, 2018. Recommended for publication by Associate Editor J. Rabkowski. *(Corresponding author: Yan Wang.)*

X. Zhou, R. Yue, Y. Wang, and Z. Yu are with the Institute of Microelectronics, Tsinghua University, Beijing 100084, China (e-mail: 18810371895@139.com; yuerf@mail.tsinghua.edu.cn; wangy46@tsinghua.edu.cn; yuzhip@tsinghua.edu.cn).

H. Su is with the Key Laboratory of Silicon Device Technology, Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China (e-mail: suhongyuan@ime.ac.cn).

G. Dai and J. Li are with the Microsystem and Terahertz Research Center, China Academy of Engineering Physics, Chengdu 610200, China (e-mail: free.dai@qq.com; hijetlee@126.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2017.2730259

I. INTRODUCTION

SILICON carbide (SiC) has been proven to be a promising candidate for the next generation semiconductor material. Because of their superior properties, SiC devices can be used for higher temperature, higher switching frequency, and higher power density applications [1], [2]. Especially, with the development of material fabrication process technology in recent years, SiC MOSFETs have been commercially available in large quantities from different manufacturers. Nevertheless, before they could completely replace silicon (Si) counterparts, robustness and reliability remain a main issue [3], [4] for the devices under a number of extreme operational conditions, such as overcurrent [5]–[7], overtemperature [8]–[12], short circuit [13]–[15], and unclamped inductive switching (UIS) [16]–[21].

In UIS test, the MOSFET is usually connected to an inductance without antiparallel free-wheeling diode to commutate the loop current when switching OFF the device. As a consequence of this, the device has to absorb all the energy previously stored in the inductance during the operation stage. The MOSFET, therefore, will be driven into the avalanche mode as long as the stored energy is sufficiently high, resulting in a gradual increase

in the junction temperature of the device [22]. Generally, a rugged device can withstand a certain amount of avalanche energy for a limited time prior to catastrophic device destruction caused by the activation of parasitic transistor or the thermally driven failure. Although the UIS measurement is regularly used for assessing the avalanche capability of the device in industrial field, avalanche mode operation is encountered frequently in automotive applications as well, like the fuel injector coil circuit, antilock braking module, etc. For this reason, detailed investigations of the avalanche ruggedness of the devices are particularly important in order to improve the system stability and reliability.

Many recent papers have investigated the avalanche capability and failure mechanism of commercial discrete SiC MOSFETs [16]–[19] and MOSFET power modules [20] under harsh single pulse UIS stress. As for the repetitive UIS tests, the electrical parameters degradation of the device was first reported by Yang *et al.* [17], yet lack of theoretical research. Liu *et al.* attributed the degradation to the hot holes injection and trapping into the gate oxide above the JFET region [21], while the number of avalanche cycles employed in the tests was insufficient (only 30k cycles were considered), which may cover up some degradation phenomena and lead to an incomprehensive conclusion. In this paper, the aging experiments have been conducted by imposing the repetitive UIS stress up to 80k cycles to the commercially available SiC MOSFETs manufactured by CREE (C2M0080120D [23]) to evaluate their long-term reliability. The sample size of 3 is chosen to generalize the experimental results. The degradation of device electrical parameters, including the threshold voltage ($V_{\rm th}$), drain leakage current ($I_{\rm dss}$), and on-state resistance ($R_{\rm on}$), has been explored in detail. A better understanding of the aging mechanism is gained by the subsequent three-terminal charge pumping (CP) tests, technology computer-aided design (TCAD) simulations, devices decapsulation, and poststress high-temperature treatment. Additionally, contrast experiments have also been performed to reveal the impact of different test conditions on the degradation rate of electrical characteristics in the aging experiments.

II. Experiments Setup

The UIS experiments are performed on ITC55X00B testers, as the test bed shown in Fig. 1. The touch screen allows for easier parameter selections and inputs, whereas the outputs will be displayed on the computer. The operating voltage of the heating plate tied to the device under test (DUT) is provided by the transformer, whose working is commanded by the temperature controller according to detecting if the case of the DUT reaches the required temperature. The simplified decoupled circuit schematic and ideal output waveforms for the device are shown in Fig. 2 [24]. At first, a continuity check of all three leads of the DUT and a device leakage test at zero gate bias are conducted before the avalanche energy is applied to the unclamped inductive load. Once the check is passed, the high-speed switch S will be closed, leading the bus voltage $V_{\rm DD}$ to be applied to the inductance. The pulse generator is activated to turn ON the DUT through the gate resistance R_g simultaneously.

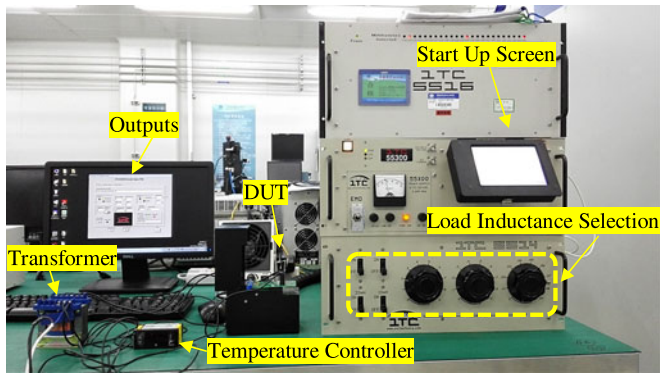


Fig. 1. Photograph of test platform.

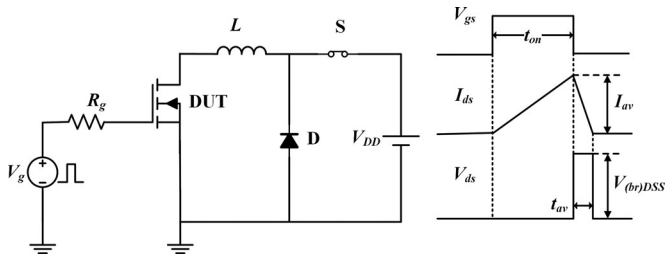


Fig. 2. Simplified UIS test circuit (left), and ideal output waveforms for the studied MOSFET (right).

Thereafter, the drain–source current of the device $I_{\rm ds}$ starts to increase as a function of L and $V_{\rm DD}$, which is given by

$$dI_{\rm ds}/dt = V_{\rm DD}/L. \tag{1}$$

Then, the gate pulse duration for charging the inductance can be derived as follows for a user specified avalanche current:

$$t_{\rm on} = \frac{L}{V_{\rm DD}} \times I_{\rm av}. \tag{2}$$

As the peak current level is reached, the gate drive to the DUT is removed together with the applied power source by opening the high-speed switch. All the energy stored in the inductance will be dumped directly into the DUT by the current path sustained by a free-wheeling diode and drives it into avalanche mode. The drain–source current will hence decrease at a rate given by

$$dI_{\rm ds}/dt = V_{\rm (br)DSS}/L. \tag{3}$$

Accordingly, the avalanche time and energy dissipated by the DUT can be derived by (4) and (5), respectively

$$t_{\rm av} = \frac{L}{V_{\rm (br)DSS}} \times I_{\rm av} \tag{4}$$

$$E_{\rm av} = \frac{1}{2} \times L \times I_{\rm av}^2. \tag{5}$$

Compared with the conventional UIS test circuit [21], the same avalanche energy can be obtained regardless of the value of $V_{\rm DD}$ using decoupled circuit, which can be seen from the

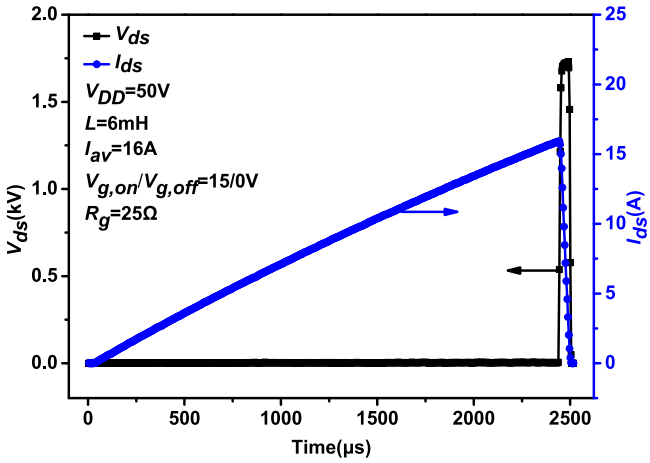


Fig. 3. Output waveforms for the studied SiC MOSFET under single pulse UIS test.

preceding analysis. It means that higher $V_{\rm DD}$ can save much more test time without influencing the actual device experimental conditions in any way. In addition, the error introduced by the power source can be eliminated, especially in the case of testing low-voltage devices.

III. Measurements and Discussions

A. Single Pulse UIS Tests

Fig. 3 shows the typical measured waveforms as functions of time for the SiC MOSFET from CREE under single pulse UIS test. To achieve an avalanche current of 16 A (80% of the device rated maximum current), the gate pulse duration is set to 2445 μs by ITC55X00B testers with a 6-mH load inductance and 50-V bus voltage, which corresponds to avalanche energy of 0.768 J (76.8% of the device rated capability). The measured avalanche breakdown voltage is 1738.5 V, and the avalanche time is 51 μs. The safe turn OFF of the DUT can be observed from the figure due to the relatively low UIS stress applied to the device. It should be noted that the inductance charge time and discharge time obtained from the testers are not in accordance with the calculation results using the aforementioned equations strictly. This is due to the losses caused by the loop resistance, solid-state switching, and the forward conduction losses of the device. As a result, the energy the DUT dissipates is actually less than the energy that is stored in the inductance.

B. Repetitive UIS Tests

The repetitive UIS tests are carried out on a sample set of SiC MOSFETs with the same stress as the single pulse test illustrated above. According to our previous experiments, the interval of 500 ms between pulses is long enough to prevent the device from catastrophic destruction after continuous 80k cycles. Hence, the heat accumulation inside the device during the tests is thought to be limited and will not influence the research results. The electrical parameters, including $V_{\rm th}$, $I_{\rm dss}$, $R_{\rm on}$, and $I_{\rm gss}$, are measured (test methods are included in the nomenclature section) when the device is cooled down after every 10k avalanche

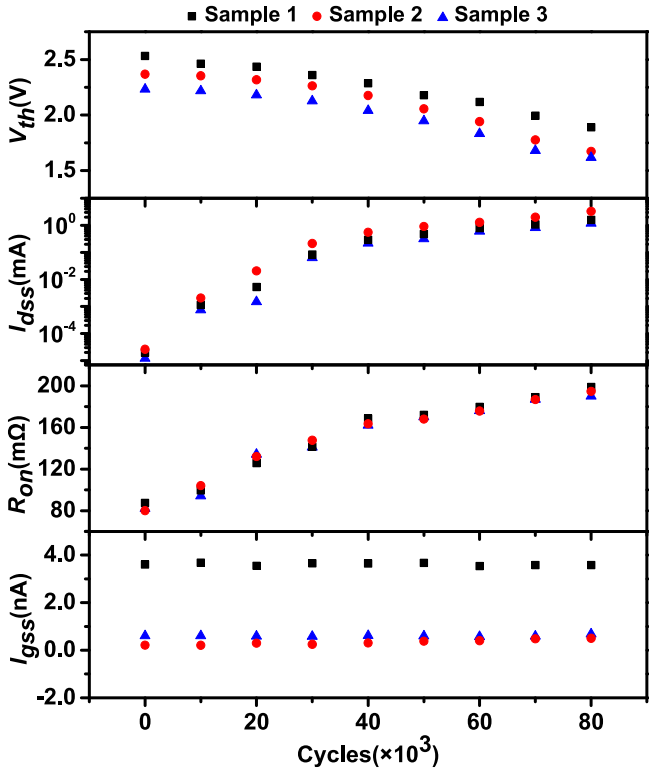


Fig. 4. Variations of $V_{\rm th}$, $I_{\rm dss}$, $R_{\rm on}$, and $I_{\rm gss}$ of the sample set of devices with the increase of avalanche cycles.

cycles. Consequently, the sample set of devices shows the uniform degradation tendencies in terms of $V_{\rm th}$, $I_{\rm dss}$, and $R_{\rm on}$, as shown in Fig. 4. A big deviation from their initial values for the three parameters can be observed, which demonstrates that the cumulative deterioration is taking place inside the device. As illustrated in the figure, $V_{\rm th}$ shows a reduction of 27% on average after 80k cycles. Whereas, $I_{\rm dss}$ increases by almost five orders of magnitude as well as $R_{\rm on}$ with an average increase of 111 mΩ. With respect to $I_{\rm gss}$, no significant degradation occurs over the testing period yet. It should be noted that the degradation phenomena observed are quite different from those discovered in [21] except the increase of $I_{\rm dss}$ due to the more avalanche cycles employed in this paper to evaluate the long-term reliability of the device. Further discussion is needed to reveal this degradation mechanism, since the static characteristics of the device do make great influence on the stability of the systems in power electronic applications.

C. Damage Region Determination

A MOSFET device is usually divided into two regions. The active region sitting in the middle of the die conducts the current in the forward operating mode, whereas the surrounding junction termination region is designed to enhance the device blocking ability during reverse mode. In fact, it is difficult to determine the degradation regions or the main region resulting in the degradation due to the similar degeneration phenomena induced by them, such as the increase of $I_{\rm dss}$ [15], [25]. That drive the device into catastrophic destruction with a harsh stress

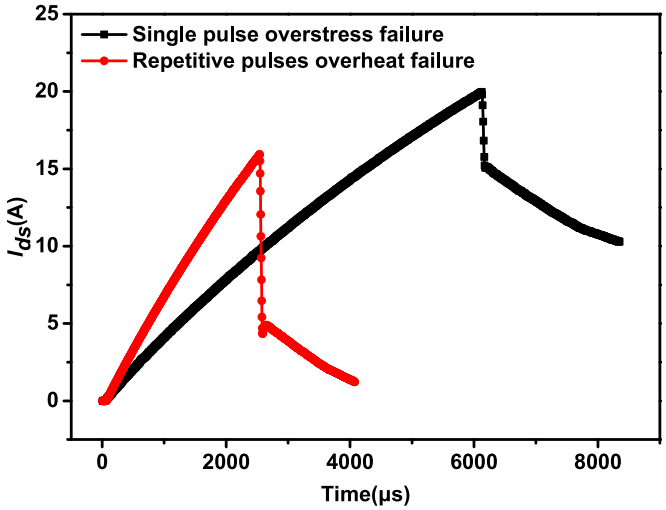


Fig. 5. Drain current characteristics resulting from different failure mechanisms during the UIS tests.

and, then, check the location of the failure site, however, seems a plausible way to realize the discrimination [26]. Accordingly, failure experiments caused by two different mechanisms are carried out. As the drain current waveforms shown in Fig. 5, the single pulse overstress failure takes place when the device suffers from the avalanche energy beyond its rated capability and the repetitive pulses overheat failure is due to the shortened time interval between pulses (5 ms is used here). The decapsulated devices under these two failure mechanisms are displayed in Fig. 6. It can be discerned that both cases show the failures that are localized at the source terminal in close proximity to the bond wires, implying that the active region mainly contributes to the degradation of the device rather than the termination region during the aging experiments. Moreover, the bubbles can also be observed on the insulating polyamide in Fig. 6(b), which is put down to the heat accumulation [27].

D. CP Measurements

CP measurements have already become one of the most effective and reliable technique to detect the distributions of interface traps and hot-carrier injection (HCI) inside the device [28], which are the critical concerns for the device after high-stress tests. In terms of the power MOSFETs with three ports (there are no contacts connected to the substrate), the conventional CP test method, however, is no longer applicable. In the modified three-terminal CP biasing scheme [29], the source is grounded and the CP current is measured at the drain while pulsing the gate with an increasing base level (V_b) and constant pulse amplitude (V_p) signal. The channel region is switched between inversion and accumulation under the successive function of gate pulse. When the surface is pulsed into inversion, the interface traps will be populated with the electrons coming from the source and drain. When the surface is in the state of accumulation, the populating electrons will recombine with channel holes, leading to the CP current collected by the drain. As a result, the threshold and flatland ($V_{\rm fb}$) voltages are the main parameters to define the range of CP current in conjunction with the value of V_p, namely $V_{\rm th} - V_p < V_b < V_{\rm fb}$. In fact, the charges in the channel region (p-type) are pumped along with the JFET region (n-type) during the CP experiments on account of the fact that both of them are covered by the gate oxide in a power MOSFET structure. Whereas, because of their different threshold and flatband voltages, there must be two CP signals detected (one is $V_{{\rm fb}j} - V_p < V_b < V_{{\rm th}j}$, and the other is $V_{{\rm th}c} - V_p < V_b < V_{{\rm fb}c}$) as long as the sweeping range of base level is set appropriate, as shown in the left part of Fig. 7. Moreover, it appears that the CP method is only suitable for detecting the degradation regions under the metal electrodes, that is, the active region here. As for the case of termination region, it is no longer applicable.

Fig. 8 shows the typical CP results of the investigated device at regular intervals. The measurements are carried out with a gate pulse frequency of 5 MHz and pulse amplitude of 5 V. The rising time and falling time are both set to 10 ns. And the base level varies from −10 to 4 V. The black curve shown in Fig. 8 is the CP current of fresh device, which reveals two different CP signals obviously. From the foregoing, such a conclusion can be drawn that the CP signal at low base level stems from the JFET region, whereas the CP signal at high base level arises from the channel region. It should be noted that unlike the CP current of the channel region, the populating electrons in the JFET region have to be supplied by the drain all the time due to the non-inverted channel, thus, resulting in a much lower CP current, as shown by the black curve. From the red curve, which is the CP result measured after 20k avalanche cycles, it can be seen that the CP signal of the JFET region shows a shift toward the negative direction, whereas a new CP signal emerges that can be regarded as the movement of the signal from partial channel region. Subsequently, the continuous left shift of the emerging signal can be observed until the end of the aging experiments. As for the signal of JFET region, it has already disappeared due to the motion when after 40k cycles of repetitive UIS tests, as exhibited by the blue curve. The negative shift of the CP curve indicates the threshold and flatband voltages of the JFET region and a part of the channel region start to decrease as demonstrated in the right part of Fig. 7. It follows that the holes injection and trapping into the gate oxide above the corresponding regions are taking place during the aging experiments [15], based on the fact that the trapped holes can induce negative charges inside the semiconductor to move toward the surface, which are the main factors responsible for these changes. Furthermore, it is worthwhile pointing out that there is no interface traps generation during the tests due to the almost unchanged peak CP current of the two regions [30]. For a better understanding of this failure mechanism, the following TCAD electrothermal simulations will be carried out using Sentaurus.

E. TCAD Simulations

A planar SiC MOSFET structure is reproduced with TCAD Synopsys Suite to analyze what happens inside the device during the UIS stress tests, as shown in Fig. 9. It should be noted that the calibrated structure does not represent the actual device in the experiments while taken as a more general case study here.

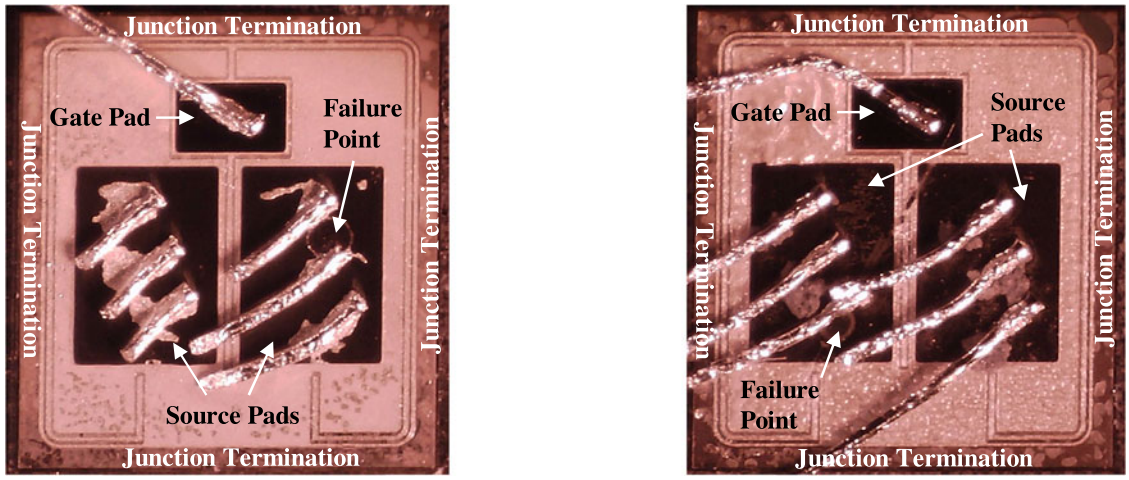


Fig. 6. Decapsulated devices under different failure mechanisms. (a) Single pulse overstress failure and (b) repetitive pulses overheat failure.

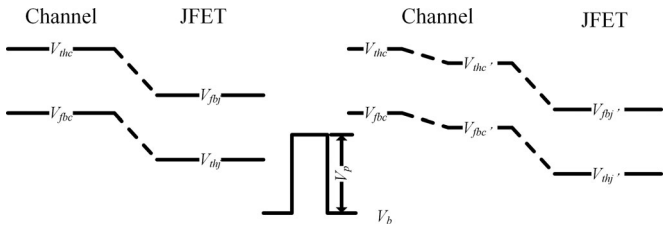


Fig. 7. Threshold and flatband voltages of the channel ($V_{\mathrm{th}c}$, $V_{\mathrm{fb}c}$) and JFET ($V_{\mathrm{th}j}$, $V_{\mathrm{fb}j}$) regions for the studied MOSFET before the repetitive UIS tests (left), and after the repetitive UIS tests (right).

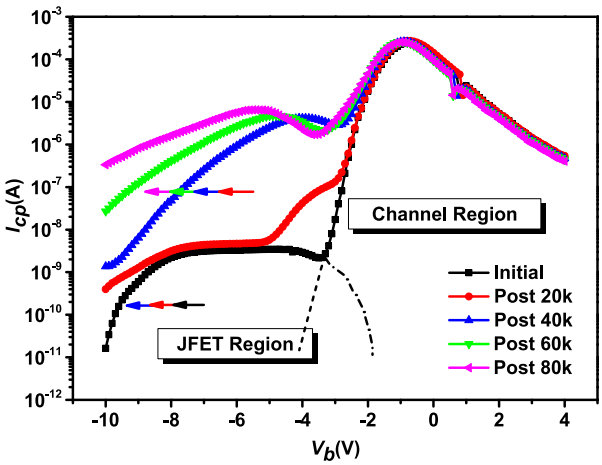


Fig. 8. Three-terminal CP measurements after every 20k avalanche cycles.

Referring to the literature data and design criteria to define the doping and dimension parameters is to make the static characteristics of this simulated device more reasonable. Meanwhile, mixed mode simulation is conducted to generate the circuit description, as shown in Fig. 2, whose function is to reproduce the same UIS stress applied to the device. In view of the temperature rise of the device during the tests, the thermodynamic model is included together with a small thermal resistance connected to the drain contact, representing that of the soldering pad and

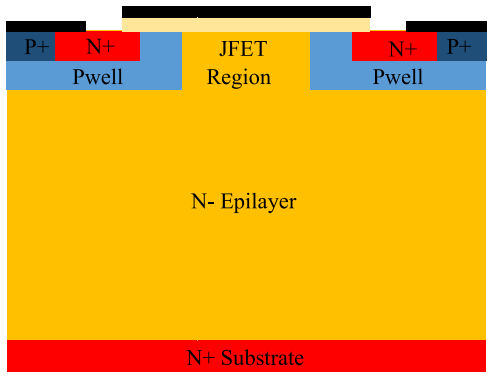


Fig. 9. Schematic cross section of the simulated MOSFET.

the plastic package. With appropriate boundary conditions and models selected in the simulation, the simulated behaviors of the device can be found in Fig. 10 after solving a series of physical and circuit equations by Sentaurus. And the local enlarged drawing of the output curves is shown in the upper part.

In order to gain more insight into the entire procedure of the single pulse UIS test, we divide it into three phases to discuss in detail, respectively.

1) Phase 1 (Conduction Mode): The turn ON of the MOSFET is initiated by closing the high-speed switch S while pulsing the gate. The drain–source current starts to rise at a specific rate determined by the peripheral circuit. Although the current density flowing through the channel is becoming increasingly high, the carriers cannot get enough energy required for being hot carriers due to the low-voltage drop across the device in on-state, which results in a nearly unexpanded depletion layer and low impact ionization (I.I.) generation rate inside the device. Hence, it can be concluded that the HCI will not happen in this conduction operation mode, which is defined as the current increase part of the output curves, as shown in Fig. 10.

2) Phase 2 (Miller Plateau): The gate–source voltage V_{gs} does not completely drop to zero in order to discharge the reverse transfer capacitance C_{gd} of the MOSFET during this phase, even

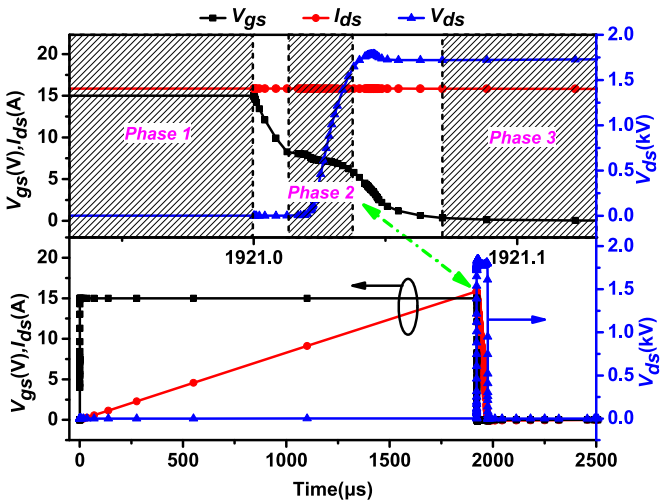


Fig. 10. Simulation results of the device under the same UIS stress test as the experiments, and the local enlarged drawing is shown in the upper part.

if the gate pulse V_g has already been switched OFF, as shown in the local enlarged drawing in Fig. 10. It means that the channel has not been turned OFF thoroughly and it is still the main conductive path to transport the high density current. Since the gate current I_g cannot discharge the gate–source capacitance $C_{\rm gs}$ anymore because of the unchanged $V_{\rm gs}$, it flows entirely through $C_{\rm gd}$. Therefore, the drain–source voltage $V_{\rm ds}$ increases at a given rate by [31]

$$\frac{dV_{\rm ds}}{dt} = \frac{I_g}{C_{\rm gd}} = \frac{V_{\rm gs} - V_{g,\rm off}}{R_g \times C_{\rm gd}}. \tag{6}$$

At this moment, $V_{\rm gs}$ is low, and both of $V_{\rm ds}$ and $I_{\rm ds}$ are high, all of which seem likely to contribute to the occurrence of HCI events. In addition, the junction temperature of the device starts to rise from now on due to the gradually increased power dissipation. Fig. 11 shows the distributions of the I.I. generation rate and perpendicular electric field along the SiC/SiO_2 interface during this miller plateau stage, respectively. As described in Fig. 11(a), two comparable peak I.I. generation rates can be observed close to the surface of semiconductor. One is located on both sides of the middle of JFET region, and the other appears in the channel region near the Pwell/JFET junction. As a result, a noticeable number of electron–hole pairs will be generated by the drastic impact and ionization of carriers in these areas. Concerning the distribution of perpendicular electric field, as shown in Fig. 11(b), basically identical situation can be found except that the peak electric field occurs in the middle of JFET region as well as the whole channel region under the combined action of gate and drain voltages. On account of the poor quality of SiC/SiO_2 interface and small valence band offset between SiC and SiO_2, the hot holes among the electron–hole pairs aforementioned are easily surmounting the SiC/SiO_2 barrier to enter the gate oxide by the high positive electric field (direction is from the drain pointing to the gate), yet the hot electrons will be swept into the drain side. Generally, one part of the injected holes can break the Si–O bonds to constitute the interface traps; the other part of injected holes, however, are captured by the

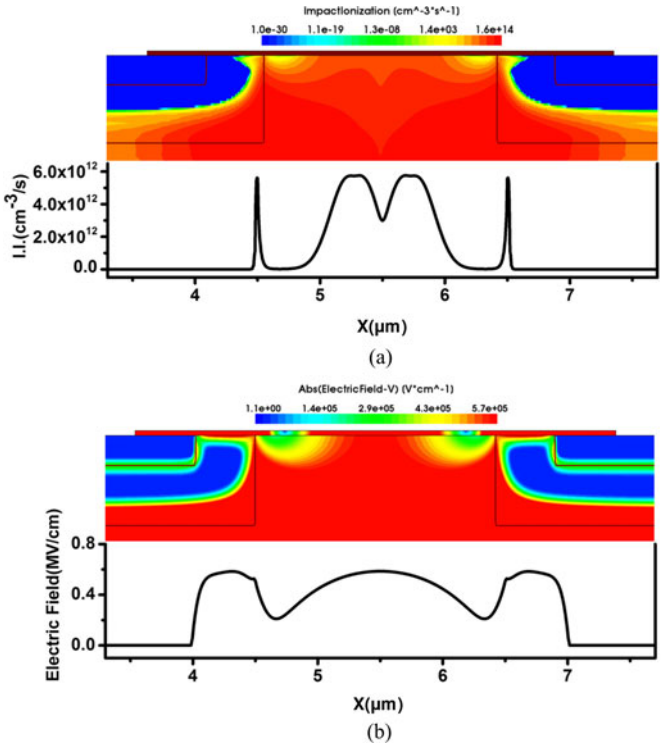


Fig. 11. Distributions of (a) I.I. generation rate and (b) perpendicular electric field along the SiC/SiO_2 interface during the miller plateau phase.

traps in the SiO_2 and form the trapped charges. The increased interface states will primarily lead to the increased $R_{\rm on}$ as a result of reduced carrier mobility, whereas the trapped holes are apt to induce the shift in the electrical parameters by changing the electric field distribution inside the device. Because no interface states generation is observed according to the CP measurements, conclusions can be drawn that the hot holes injection and trapping into the gate oxide above the area near Pwell/JFET junction and on both sides of the middle of JFET region may be the main failure mechanism at the stage of miller plateau.

3) Phase 3 (Avalanche Mode): The third phase is defined as the avalanche mode, which is encountered when $V_{\rm gs}$ completely reduces to zero, and $V_{\rm ds}$ stays at the level of avalanche breakdown voltage, as depicted in the local enlarged drawing in Fig. 10. The channel has been shut down right now, and the high $I_{\rm ds}$ is sustained by the avalanche current of body diode. The catastrophic device destruction could take place easily if the avalanche current is strong enough to activate the latchup of parasitic transistor during this phase. Likewise, the distributions of the I.I. generation rate and perpendicular electric field along the SiC/SiO_2 interface are extracted, as shown in Fig. 12. It can be discerned that the peak I.I. generation rate only appears on both sides of the middle of JFET region, whereas the peak perpendicular electric field merely concentrates in the middle of JFET region. Compared with the previous case, the I.I. generation rate and electric field in the channel region are nowhere near as large as those of the JFET region after losing the role of gate voltage on the device. Therefore, the hot holes trapping into the gate oxide above both sides of the middle of JFET region, as discussed before, is very likely to happen at this stage. In ad-

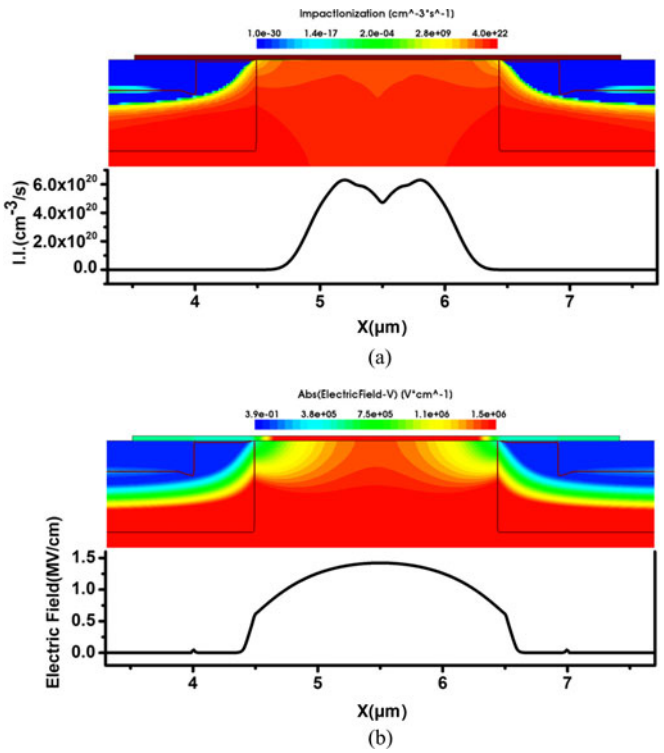


Fig. 12. Distributions of (a) I.I. generation rate and (b) perpendicular electric field along the SiC/SiO_2 interface during the avalanche mode phase.

dition, it is worthwhile pointing out that the peak I.I. generation rate during avalanche mode is nearly eight orders of magnitude larger than that during miller plateau, indicating a more severe oxide charges trapping problem. By comparison, the number of charges injected into the gate oxide above the JFET region is negligible in the second stage. However, the holes injection taking place in the channel region, which is deemed to be the most probable cause of the threshold voltage shift, cannot be neglected in spite of the same low I.I. generation rate in there. As a result, the degradation of $V_{\rm th}$ is imperceptible and can be easily ignored if the aging experiments are carried out with insufficient number of avalanche cycles [21].

To sum up, throughout the entire UIS test process, the degradation due to the holes trapping into the gate oxide above a part of channel region (near Pwell/JFET junction) is only discovered during the miller plateau phase, while the degradation related to the gate oxide above the JFET region mainly occurs in the avalanche mode phase. These simulation results show high coherence and correspondence with the CP measurements as a result of cumulative degeneration during the repetitive UIS stress tests.

The trapped holes in the gate oxide above a part of channel region will attract negative charges to move toward the surface of the semiconductor, leading to a reduced background doping concentration in here. This implies that the effective channel length will become shorter than that of the fresh device. In addition, things will get worse as the repetitive UIS experiments continue. It seems to achieve the same result as the short-channel effect, which may give rise to the reduction of $V_{\rm th}$, the increase of $I_{\rm dss}$, and the decrease of $R_{\rm on}$ [32]. With respect to the trapped holes in the gate oxide above both sides of the middle of JFET region, the failure mechanism has been discussed in [21] at length. On the one hand, the presence of trapped holes will change the potential distribution near the Pwell/JFET junction and enhance the local electric field strength when the device is in the off-state, resulting in the increase of $I_{\rm dss}$, on the other hand, contrary to the situation in the channel region, the negative charges induced by the trapped holes will increase the background doping concentration of the JFET region and reduce the specific resistance of the conduction path, leading to the decrease of $R_{\rm on}$. Due to that this part of injected holes are away from the channel region, they do not make any contribution to the threshold voltage degradation. Besides, the oxide trapped holes would lead to the increase of $I_{\rm gss}$ as well. But as the experimental results shown in Fig. 4, no obvious change of $I_{\rm gss}$ can be observed. This is because although $V_{\rm th}$ shows a 27% decrease on average, the decrement is actually limited (around 0.6 V). Hence, the additional electric field pointing to the channel area induced by the oxide holes is negligible when compared with the high gate bias ($V_{\rm gs} = 20$ V) used in $I_{\rm gss}$ measurement, resulting in a seemingly stable $I_{\rm gss}$. It is noted that all the degradation phenomena occurring in the repetitive UIS stress tests can be well explained by the injected hot holes aside from the increase of $R_{\rm on}$, which seems contradictory to the results accounted for by this failure mechanism. Further probe trials, thus, will be carried out to investigate the on-state resistance degradation in the next part.

F. Decapsulation

Decapsulation of fresh devices and failure devices after repetitive UIS stress tests has been performed to understand what happens at die level. The bond wires and bond joints are shown to be intact along with the contact metallization from the internal view of fresh devices, as exhibited in Fig. 13(a) and (b). Nevertheless, an apparent aging phenomenon on the bond wire contacts can be observed with regard to the failed ones. The thermomechanical stress induced by the repetitive UIS tests easily enhances the thermal fatigue of metallic material, resulting in the bond wires lift-off. As shown in Fig. 13(c), the gate and source bond wires are lifted off, leaving behind the melted holes on their footprints as a consequence of the local melting of the bond ends. While Fig. 13(d) shows the lift-off patterns after the wire bonds lift off from the source contact, which are the residues of bond wire material. The bond contact resistance as a component of $R_{\rm on}$, hence, is increasing due to the degradation at the interface between bond wires and chip metallization [33], [34]. Combining with the previous discussions, it is tempting to conclude that the effect of injected hot holes on the on-state resistance of the studied devices is far more than offset by that of the bond wires degradation, leading to the increase in $R_{\rm on}$ finally.

G. High-Temperature Treatment

The poststress high-temperature treatment has also been done to indirectly validate the existence of hot holes injection in the gate oxide on account of that the high-temperature measurements could provide adequate activation energy to help the

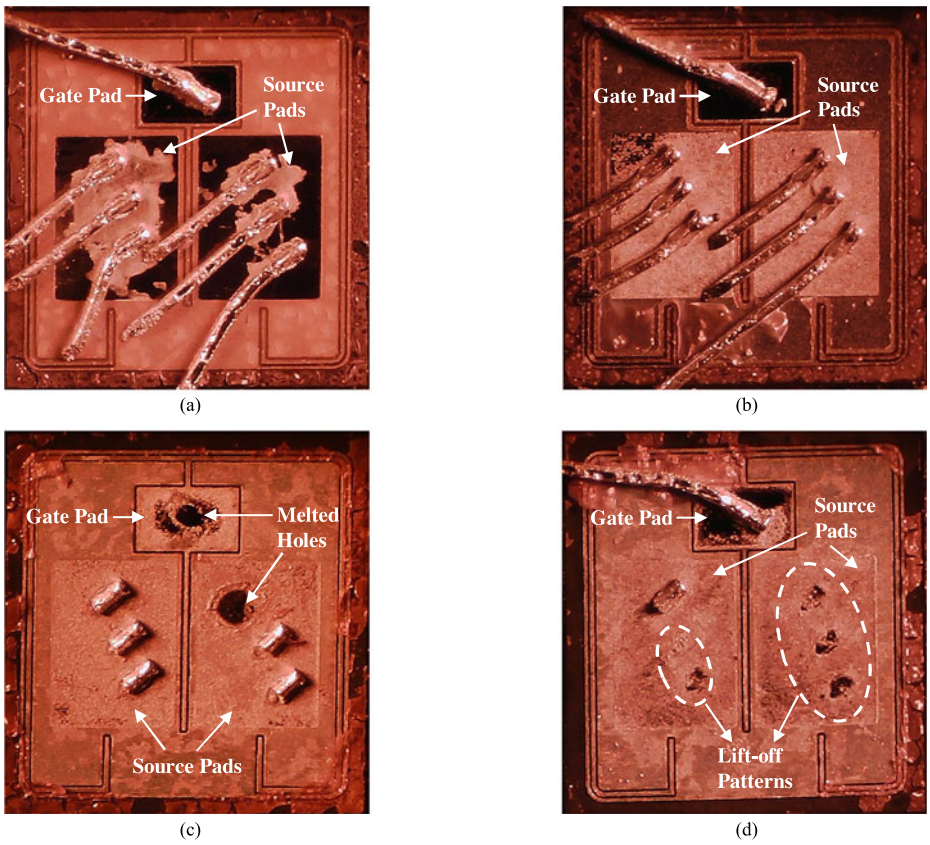


Fig. 13. (a) and (b) Decapsulated fresh devices and (c) and (d) failure devices after repetitive UIS stress tests.

trapped holes release. The degradation of device performance arising from HCI, therefore, will be gradually recovered with prolonged heat treatment time [15], [21], [26]. The normalized $V_{\rm th}$ and $I_{\rm dss}$ represent the ratio of test data to their respective values of fresh devices, which can basically reach one after 200 °C high-temperature treatment on the failure devices for 30 min, as shown in Fig. 14. Whereas, a slight increase in $R_{\rm on}$ can be observed in the bottom plot. This is mainly because the hot holes inducing the decrease of $R_{\rm on}$ can be released by the high temperature while this treatment almost has no influence on the recovery of bond wires degradation. As a result, the effect of hot holes injection once overshadowed by that of the failure at die level is gradually reflected and verified by the slight increase of $R_{\rm on}$.

IV. Contrast Tests

Contrast tests have also been carried out to investigate the effect of different UIS test conditions on the degradation rate of electrical parameters in the aging experiments. Adjusting R_g and $V_{g,\rm off}$ to show the dependence on the duration of miller plateau (referring to (6)) is not included in this paper because of the embedded gate driver in the test equipment. The test conditions for different cases are summarized in Table I with the single pulse avalanche test result under each condition being displayed. The condition employed in Section III is named Case 1 and treated as a reference here. The test parameters adjustment in Case 2 is to reduce $t_{\rm av}$ by half on the basis of the circuit analysis in Section II. Moreover, in order to clearly study the impact of $T_{\rm case}$, the case temperature of the devices in Case 3 and Case 4 is increased to 350 and 400 K, respectively.

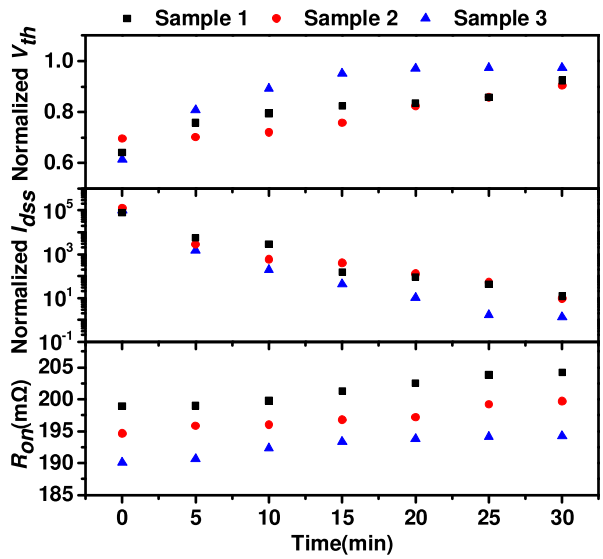


Fig. 14. Variations of normalized $V_{\rm th}$, $I_{\rm dss}$, and $R_{\rm on}$ as functions of high-temperature treatment time.

Another three sample sets, total nine devices, are used to conduct the repetitive UIS experiments under the other three test

TABLE I
DIFFERENT UIS TEST CONDITIONS FOR CONTRAST

	Case 1	Case 2	Case 3	Case 4
$V_{\rm DD}$	50 V	26 V	50 V	50 V
L	6 mH	3 mH	6 mH	6 mH
$I_{\rm av}$	16 A	16 A	16 A	16 A
$V_{\rm (br)DSS}$	1738.5 V	1730 V	1778 V	1807.3 V
$t_{\rm on}$	2445 μs	2441 μs	2459 μs	2465 μs
$t_{\rm av}$	51 μs	26 μs	50 μs	50 μs
$T_{\rm case}$	300 K	300 K	350 K	400 K

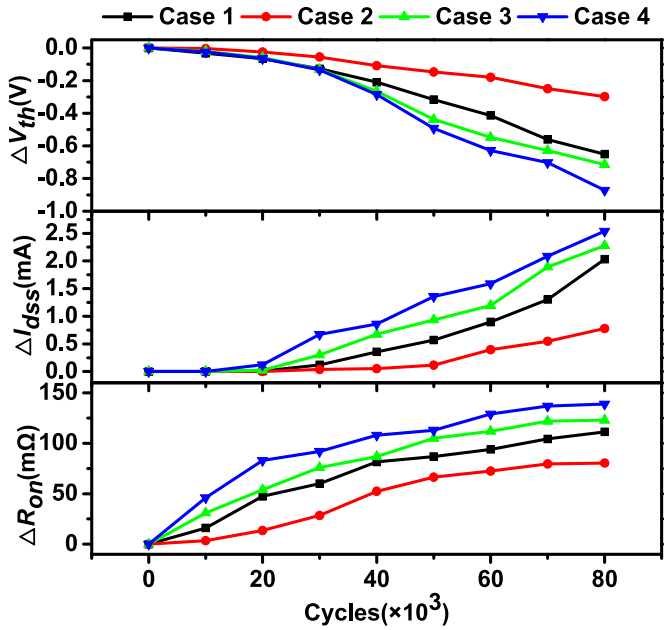


Fig. 15. Variations of $\triangle V_{\rm th}$, $\triangle I_{\rm dss}$, and $\triangle R_{\rm on}$ with the increase of avalanche cycles for the sample set of devices under repetitive UIS tests with different stresses.

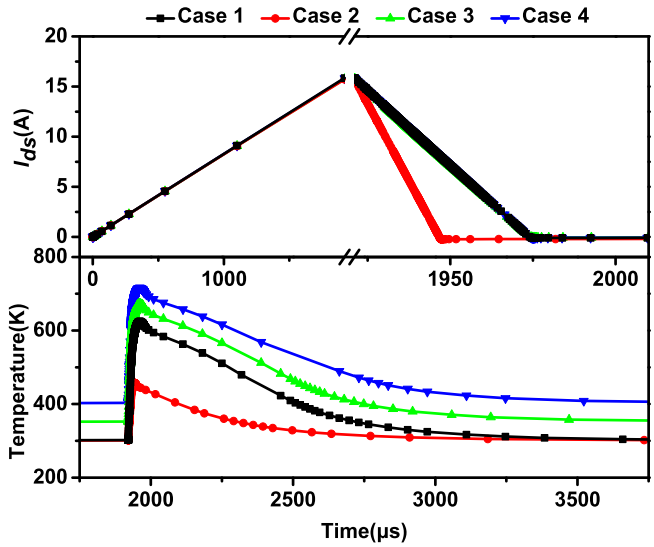


Fig. 16. Simulation results of drain current and junction temperature for the device under different test conditions.

TABLE II
TEMPERATURE STRESS FACTORS

	Case 1	Case 2	Case 3	Case 4
$T_{\rm low}$	300 K	300 K	350 K	400 K
$T_{\rm high}$	624 K	457 K	672 K	715 K
ΔT_j	324 K	157 K	322 K	315 K
$T_{\rm jm}$	462 K	378.5 K	511 K	557.5 K

$T_{\rm low}$: minimum junction temperature, $T_{\rm high}$: maximal junction temperature, ΔT_j: junction temperature swing, $T_{\rm jm}$: mean junction temperature.

conditions. Fig. 15 shows the variations of average $V_{\rm th}$ shift ($\triangle V_{\rm th}$), $I_{\rm dss}$ shift ($\triangle I_{\rm dss}$), and $R_{\rm on}$ shift ($\triangle R_{\rm on}$) as functions of the number of avalanche cycles for different cases. It can be observed that the degradation of the electrical parameters in Case 1 is more serious than that in Case 2 and the wear out will be worsened with the increase of $T_{\rm case}$. For better understanding, Fig. 16 gives the simulation results of drain current and junction temperature under different test conditions. As can be seen from the figure, the average drain current of the device in Case 2 is lower due to the smaller $t_{\rm av}$. On the one hand, the lower average drain current will result in fewer carriers generated by I.I., and hence fewer injected hot holes; on the other hand, the smaller $t_{\rm av}$ means that the time for the hot holes injection and trapping into the gate oxide is shorter. As a consequence, the electrical parameters degradation mainly due to the HCI becomes slight, e.g., $V_{\rm th}$ and $I_{\rm dss}$. In terms of the temperature dependence of degradation, it is well known that the HCI effect will be generally weakened as the temperature rises due to the enhanced phonon scattering [35]. However, as shown by Case 3 and Case 4 in Fig. 15, the degradation degree is accelerated at a high $T_{\rm case}$. Note that the avalanche voltage $V_{\rm (br)DSS}$ at which the device is always clamped during UIS test increases with temperature due to the declining ionization rates, as can be seen in Table I. In other words, the avalanche event must happen and the carrier energy lost by phonon scattering will be compensated by the higher $V_{\rm (br)DSS}$ eventually. Therefore, the HCI effect will not be suppressed but instead exacerbated by the enhancement in the vertical electric field at the interface. With regard to the degradation of $R_{\rm on}$, it is primarily ascribed to the thermal fatigue of metallic material and, thus, can be treated as the issue of power cycling tests [36], [37]. The temperature stress factors of the simulated temperature profiles in the bottom plot of Fig. 16 are summarized in Table II. As the lifetime model tells, the number of cycles to failure decreases with the increase of $\triangle T_j$ and $T_{\rm jm}$, that is to say, the faster growth of the on-resistance.

Conclusions can be drawn from our study that the static characteristics degeneration is inevitable for this type of commercial 1.2-kV 4H-SiC MOSFETs under repetitive UIS stresses. In order to alleviate the degradation of device performance, efforts should be made in the aspects of device design and fabrication. For one thing, some novel structures have been proposed to relieve the electric field strength and I.I. generation rate inside the device during the avalanche tests [21], for another, the manufacture process needs to be further improved to enhance

the quality of the interface between SiC and SiO_2. In addition, from the perspective of application, minimizing the duration of miller plateau by means of either reducing R_g or decreasing the low level of the gate pulse $V_{g,\mathrm{off}}$ or reducing the load inductance in the circuit to shorten the avalanche time and lessen the average avalanche current are another ways to maintain the device reliability effectively. Meanwhile, the efficient cooling system would help the device to work more ruggedly as well.

V. Conclusion

The avalanche ruggedness of commercial 1.2-kV 4H-SiC MOSFETs subjected to the repetitive pulses is investigated in this paper. ITC55X00B testers are utilized to generate the UIS stress below the rated avalanche capability to impose on the devices. After 80k avalanche cycles, the sample set of devices show an almost consistent degradation tendency characterized by the decrease of V_{th} and increase of I_{dss} and R_{on}. While no significant change of I_{gss} can be found. The three-terminal CP measurements are carried out to help detecting the distribution change of interface traps and HCI inside the device. Results show that the hot holes injection and trapping into the gate oxide above the channel and JFET region may be directly responsible for the failure phenomena. The subsequent electrothermal simulation results demonstrate that the holes trapping into the gate oxide above a part of channel region only happens during the miller plateau phase, while the holes injection related to the gate oxide above the JFET region mainly occurs in the avalanche mode phase, based on the distributions of electric field and I.I. generation rate along the SiC/SiO_2 interface. This failure mechanism can well account for the degradation of V_{th} and I_{dss} except R_{on}. After decapping the failed devices, the bond wires lift off due to thermal fatigue can be clearly seen, which should be the main reason for the increased R_{on}. In addition, the poststress high-temperature treatment has been performed to indirectly confirm the aforementioned failure mechanism as well. At last, we address the impact of different test conditions on the degradation rate of electrical characteristics in the aging experiments and put forward some feasible schemes to alleviate these degeneration phenomena.

References

[1] Q. Zhang, R. Callanan, M. K. Das, S. Ryu, A. K. Agarwal, and J. W. Palmour, "SiC power devices for microgrids," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2889–2896, Dec. 2010.

[2] S. Hazra *et al.*, "High switching performance of 1700-V, 50-A SiC power MOSFET over Si IGBT/BiMOSFET for advanced power conversion applications," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4742–4754, Jul. 2016.

[3] J. Lutz and R. Baburske, "Some aspects on ruggedness of SiC power devices," *Microelectron. Rel.*, vol. 54, no. 1, pp. 49–56, 2014.

[4] A. Castellazzi, A. Fayyaz, G. Romano, L. Yang, M. Riccio, and A. Irace, "SiC power MOSFETs performance, robustness and technology maturity," *Microelectron. Rel.*, vol. 58, pp. 164–176, Mar. 2016.

[5] Z. Wang, X. Shi, Y. Xue, L. Tolbert, F. Wang, and B. Blalock, "Design and performance evaluation of overcurrent protection schemes for silicon carbide power MOSFETs," *IEEE Trans. Ind. Electron.*, vol. 61, no. 10, pp. 5570–5581, Oct. 2014.

[6] J. A. Schrock *et al.*, "High-mobility stable 1200-V, 150-A 4H-SiC DMOSFET long-term reliability analysis under high current density transient conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2891–2895, Jun. 2015.

[7] J. A. Schrock *et al.*, "Failure analysis of 1200-V/150-A SiC MOSFET under repetitive pulsed overcurrent conditions," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1816–1821, Mar. 2016.

[8] P. Ning, F. Wang, and K. D. T. Ngo, "High-temperature SiC power module electrical evaluation procedure," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3079–3083, Nov. 2011.

[9] W. Zhou, X. Zhong, and K. Sheng, "High temperature stability and the performance degradation of SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2329–2337, May 2014.

[10] P. Alexakis, O. Alatise, J. Hu, S. Jahdi, L. Ran, and P. A. Mawby, "Improved electrothermal ruggedness in SiC MOSFETs compared with silicon IGBTs," *IEEE Trans. Electron Devices*, vol. 61, no. 7, pp. 2278–2286, Jul. 2014.

[11] D. P. Hamilton *et al.*, "High temperature electrical and thermal aging performance and application considerations for SiC power DMOSFETs," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7967–7979, Oct. 2017, doi: 10.1109/TPEL.2016.2636743.

[12] J. O. Gonzalez, O. Alatise, J. Hu, L. Ran, and P. Mawby, "An investigation of temperature sensitive electrical parameters for SiC power MOSFETs," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7954–7966, Oct. 2017, doi: 10.1109/TPEL.2016.2631447.

[13] T. Nguyen, A. Ahmed, T. V. Thang, and J. Park, "Gate oxide reliability issues of SiC MOSFETs under short-circuit operation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2445–2455, May 2015.

[14] Z. Wang *et al.*, "Temperature-dependent short-circuit capability of silicon carbide power MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1555–1566, Feb. 2016.

[15] X. Zhou, H. Su, Y. Wang, R. Yue, G. Dai, and J. Li, "Investigations on the degradation of 1.2-kV 4H-SiC MOSFETs under repetitive short-circuit tests," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4346–4351, Nov. 2016.

[16] A. Fayyaz, L. Yang, and A. Castellazzi, "Transient robustness testing of silicon carbide (SiC) power MOSFETs," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–10.

[17] L. Yang, A. Fayyaz, and A. Castellazzi, "Characterization of high-voltage SiC MOSFETs under UIS avalanche stress," in *Proc. IET Int. Conf. Power Electron., Mach. Drives*, 2014, pp. 1–5.

[18] J. Hu, O. Alatise, J. A. O. González, R. Bonyadi, L. Ran, and P. A. Mawby, "The effect of electrothermal nonuniformities on parallel connected SiC power devices under unclamped and clamped inductive switching," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4526–4535, Jun. 2016.

[19] M. D. Kelley, B. N. Pushpakaran, and S. B. Bayne, "Single pulse avalanche mode robustness of commercial 1200 V/80 mΩ SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6405–6415, Jun. 2017, doi: 10.1109/TPEL.2016.2621099.

[20] M. Nawaz, "Evaluation of SiC MOSFET power modules under unclamped inductive switching test environment," *Microelectron. Rel.*, vol. 63, pp. 97–103, Aug. 2016.

[21] S. Liu, C. Gu, J. Wei, Q. Qian, W. Sun, and A. Q. Huang, "Repetitive unclamped-inductive-switching-induced electrical parameters degradations and simulation optimizations for 4H-SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 63, no. 11, pp. 4331–4338, Nov. 2016.

[22] K. Fischer and K. Shenai, "Dynamics of power MOSFET switching under unclamped inductive loading conditions," *IEEE Trans. Electron Devices*, vol. 43, no. 6, pp. 1007–1015, Jun. 1996.

[23] *Cree-C2M0080120D-Silicon Carbide MOSFET Datasheet*. Oct. 2015. [Online]. Available: http://www.wolfspeed.com/downloads/dl/file/id/167/product/10/c2m0080120d.pdf/. Accessed on: Oct. 20, 2016.

[24] Integrated Technology Co., Tempe, AZ, USA. *ITC55X00B User's Manual*, 2005.

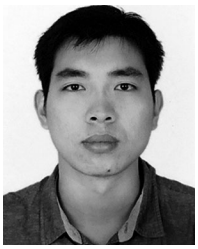
[25] M. Bakowski, U. Gustafsson, and Z. Ovuka, "Walk-out phenomena in 6H-SiC diodes with SiO_2/Si_3N_4 passivation and charge trapping in dry and wet oxides on N-type 6H-SiC," *Microelectron. Rel.*, vol. 38, no. 3, pp. 381–392, 1998.

[26] S. Liu *et al.*, "Repetitive-Avalanche-Induced electrical parameters shift for 4H-SiC junction barrier schottky diode," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 601–605, Feb. 2015.

[27] E.-P. Eni *et al.*, "Short-Circuit degradation of 10 kV 10 A SiC MOSFET," *IEEE Trans. Power Electron.*, to be published, 2017, doi: 10.1109/TPEL.2017.2657754.

[28] P. Heremans, J. Witters, G. Groeseneken, and H. E. Maes, "Analysis of the charge pumping technique and its application for the evaluation of MOSFET degradation," *IEEE Trans. Electron Devices*, vol. 36, no. 7, pp. 1318–1335, Jul. 1989.

[29] L. J. Passmore *et al.*, "Fowler–Nordheim and hot carrier reliabilities of U-shaped trench-gated transistors studied by three terminal charge pumping," *Thin Solid Films*, vol. 504, no. 1/2, pp. 302–306, May 2006.
[30] B. S. Doyle *et al.*, "The generation and characterization of electron and hole traps created by hole injection during low gate voltage hot-carrier stressing of n-MOS transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 8, pp. 1869–1876, Aug. 1990.
[31] S. Linder, *Power Semiconductors*, 1st ed. Lausanne, Switzerland: EPFL Press, 2006.
[32] T. L. Chiang, "A compact model for threshold voltage of surrounding-gate MOSFETs with localized interface trapped charges," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 567–571, Feb. 2011.
[33] M. Berkani, S. Lefebvre, and Z. Khatir, "Saturation current and on-resistance correlation during during repetitive short-circuit conditions on SiC JFET transistors," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 621–624, Feb. 2013.
[34] D. Martineau, T. Mazeaud, M. Legros, P. Dupuy, and C. Levade, "Characterization of alterations on power MOSFET devices under extreme electro-thermal fatigue," *Microelectron. Rel.*, vol. 50, no. 9–11, pp. 1768–1772, 2010.
[35] J. I. Kim *et al.*, "Effect of temperature and electric field on degradation in amorphous InGaZnO TFTs under positive gate and drain bias stress," *IEEE Electron Device Lett.*, vol. 35, no. 4, pp. 458–460, Apr. 2014.
[36] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Proc. 2nd Int. Conf. Power Electron. Drive Syst.*, May 1997, pp. 425–430.
[37] U.-M. Choi, F. Blaabjerg, and S. Jorgensen, "Study on effect of junction temperature swing duration on lifetime of transfer molded power IGBT modules," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6434–6443, Jan. 2017.



Xintian Zhou received the M.S. degree in microelectronics from the College of Electronic Information and Control Engineering, Beijing University of Technology, Beijing, China, in 2014. He is currently working toward the Ph.D. degree in microelectronics and nanoelectronics from the Institute of Microelectronics, Tsinghua University, Beijing, China.

His research interests include the modeling, fabrication, and reliability of silicon carbide power devices.

Hongyuan Su received the M.S. degree in microelectronics from the College of Electronic Information and Control Engineering, Beijing University of Technology, Beijing, China, in 2015.

He is currently in the Institute of Microelectronics of Chinese Academy of Sciences, Chinese Academy of Sciences, Beijing, China. His research interests include testing, analyzing, and reliability of power devices.

Ruifeng Yue received his B.S., M.S., and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1986, 1991, and 1997, respectively.

From 1997 to 1999, he was a Postdoctoral Fellow, he worked with Institute of Microelectronics, Tsinghua University, where he was promoted to full professor in 2006. His current research interests include SiC power devices, MEMS, smart sensors, and microneedle arrays for transdermal drug delivery.

Gang Dai received the B.S. and Ph.D. degrees in physics from Tsinghua University, Beijing, China, in 2006 and 2011, respectively.

He is the Director of Microsystem Technology Laboratory, Microsystem & Terahertz Research Center, China Academy of Engineering Physics, Mianyang, China, where he focuses on R&D of integrated microsystems, power electronics, and advanced MEMS sensors. His work is published in more than 20 peer-reviewed journal and refereed conference papers.

Juntao Li received the B.S. degree in materials science and engineering from Huazhong University of Science and Technology, Wuhan, China, and the Ph.D. Degree in microelectronics from Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai, China, in 2009 and 2014, respectively.

He is currently a Research Assistant in the Microsystem and Terahertz Research Center, Chengdu, China, where he works on compound semiconductor power device and microsystem. His previous industrial experience includes four years as an Intern in the Semiconductor Manufacturing International Corporation. Most recently, he has been focused on the development of SiC power device and high-voltage microsystem design.

Yan Wang received the B.S. and M.S. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, and the Ph.D. degree in semiconductor device and physics from the Institute of Semiconductors, Chinese Academy of Science, Beijing, China, in 1988, 1991, and 1995, respectively.

Since 1999, she has been a Professor in the Institute of Microelectronics, Tsinghua University, Beijing, China. Her research interests include device modeling and circuit design in MMW/THz range.

Zhiping Yu (F'08) received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1967, 1980, and 1985, respectively.

He is currently a Professor in the Institute of Microelectronics, Tsinghua University, and since 2008, he has been a Visiting Professor in the Department of Electrical Engineering, Stanford University.