Trapezoidal Approximation of *LCC* Resonant Converter and Design of a Multistage Capacitor Charger for a Solid-State Marx Modulator

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***Abstract*—This paper describes the circuit of a capacitor charger for a solid-state Marx modulator. A high-efficiency *LCC* resonant inverter is proposed for the simultaneous charging of many capacitors in parallel using a multistage transformer and rectifier. Using a high-voltage insulation cable, the charging loop, which represents the primary winding of transformer, is implemented to transfer the power from the resonant inverter to each stage. In addition to the simultaneous charging of separate capacitors, the advantages of the proposed circuit and structure include compact design and reliable insulation performance against high-voltage pulses. Based on the relevant approximation, the simplified analysis of an *LCC* resonant converter with a trapezoidal shape of resonant current is provided and a 50-kW high-voltage capacitor charger is designed for a 40-kV solid-state Marx modulator. The power stage, which consists of a transformer with four voltage-doubled rectifiers, is designed, and six power stages are configured for generating a pulse output of 40 kV. The detailed implementation of the multistage transformer and rectifier is presented in accordance with the design requirements of a high voltage modulator. Finally, the developed charger achieves 96% of the maximum efficiency and 0.96 of the maximum power factor. The experimental results verify that the proposed circuit and structure can be effectively used for a solid-state Marx modulator.**

***Index Terms*—DC–DC power converters, pulsed power supplies, resonant inverters.**

I. Introduction

RECENTLY, a considerable number of studies related to the solid-state Marx modulator (SSMM) have been reported owing to the diversification of the applications of pulsed power [1]–[15]. Compared to the conventional high-voltage modulator using a gas discharging switch, the SSMM can be effectively used for highly repetitive applications owing to its advantages such as a long lifetime and ease of controlling the output pulse with low jitter. In addition, recent advances in power electronics and semiconductor device technology have led to the improvement of the performance of the SSMM and solved the limitations of SSMM such as limited handling voltage and current capability. Further, many types of SSMM topologies that use the capacitive energy storage with a closing switch have been presented to overcome the voltage and current ratings of the semiconductor switches [3]–[13]. A simple scheme of the SSMM is the high-voltage direct switching method, which uses the semiconductor switch stack between the high-voltage capacitor bank and the load [3], [4]. Although it shows a reliable operation with simple configuration, additional passive components are required for balancing the voltage in the series stacked switch. Furthermore, the output pulse voltage is limited to the maximum charging voltage of the capacitor bank. In contrast, a Marx modulator with a number of storage capacitors has an advantage in terms of increased output voltage capability, since all the capacitors are configured as a parallel connection for charging and a series connection for discharging. This operating principle of the Marx modulator facilitates the increase of output pulse voltage independent of the voltage ratings of the capacitor charging power supply. Therefore, many types of the solid-state Marx modulator schemes have been introduced [5]–[13]. One similarity among the existing solid-state Marx modulators is that the configuration of each Marx cell consists of a switch for generating a pulse, capacitor for storing the energy, and diode for clamping the voltage across the switch. By employing a diode per cell, a reliable operation of the semiconductor switch can be achieved against overvoltage. In contrast to the similar structure of the Marx cell, different approaches have been introduced for charging all the capacitors. The conventional method, which uses a high-voltage capacitor charger with a charging resistor, is generally applicable to relatively low power applications owing to the problem of efficiency. Instead of using the current limiting resistor, the current source type of the capacitor charger can be effectively used with the charging diode for reducing the losses [5]–[7]. Similarly, capacitor charging schemes that use the controllable semiconductor switch have been introduced [8]–[10]. For example, the power electronics building block (PEBB) uses

Manuscript received January 4, 2017; revised March 12, 2017 and April 28, 2017; accepted June 8, 2017. Date of publication June 19, 2017; date of current version February 1, 2018. This work was jointly supported by the Korea Electrotechnology Research Institute (KERI) Primary research program through the National Research Council of Science and Technology (NST) funded by the Ministry of Science, ICT, and Future Planning (MSIP) under Grant 17-12-N0101-23 and the National Research Foundation of Korea (NRF) funded by the Korea government (MSIP) under Grant NRF-2017R1A2B3004855. Recommended for publication by Associate Editor Z. Li. *(Corresponding author: Hong-Je Ryoo.)*

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Digital Object Identifier 10.1109/TPEL.2017.2716975

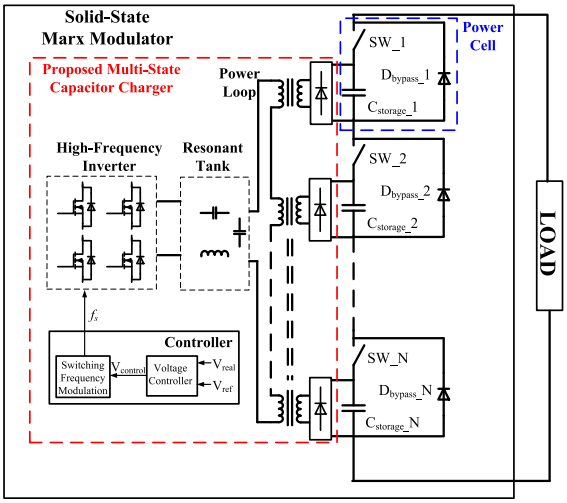


Fig. 1. Conceptual block diagram of the proposed multistage capacitor charger and SSMM.

additional Insulated Gate Bipolar Transistor (IGBT) for charging and achieves a modular design [8], [9]. The PEBB facilitates an increase of the maximum output pulse voltage via an additional module; however, it requires an additional switch and control. On the other hand, an SSMM, which includes not only high-voltage switching stack, but also a capacitor charger, was proposed for improving the performance in terms of simplicity, low cost, and high power density [11]–[13]. Using a transformer with multiple secondary windings, the charging scheme can be simplified without additional charging components. On the basis of the aforementioned charging scheme, this paper proposes a multistage capacitor charger mainly consisting of the *LCC* resonant inverter for supplying high-frequency ac power, power loop for delivering the charging power, and multiple transformers with rectifiers. An *LCC* resonant converter with a trapezoidal resonant current waveform is designed for low conduction loss. Based on the trapezoidal approximation of *LCC* resonant converter, a simplified design guideline is presented with analysis and PSpice simulation. In order to develop the solid-state Marx modulator for radar applications, the detailed design and implementation of a 50 kW multistage capacitor charger is described. Finally, it is experimentally verified that the proposed circuit and structure can be effectively used for a SSMM.

II. Design Concept and Considerations of the Proposed Multistage Capacitor Charger for SSMM

The conceptual block diagram of the SSMM that includes the switches (SW_1–SW_N) as well as the proposed multistage capacitor charger is shown in Fig. 1.

The power loop, which represents the primary winding of the transformer, transfers the charging power from the resonant inverter and each secondary winding charges the storage capacitor through the rectifier. In addition to the parallel charging of all the storage capacitors ($C_{\mathrm{storage}}\_1 - C_{\mathrm{storage}}\_\mathrm{N}$), this configuration provides electrical isolation between all any two storage capacitors.

Accordingly, effective insulation is achieved even if all the capacitors are connected in series by means of the switches (SW_1–SW_N). With this configuration, the proposed capacitor charging scheme provides the advantages of simplicity, low cost, and high power density. First, it is not necessary to use additional components for parallel charging of many capacitors. Compared to the conventional scheme where an external capacitor charger is used, the proposed scheme allows the implementation of the SSMM without any external component and simplifies the interface between the charger and the high-voltage switching part. In addition, the compact design is possible because the high-voltage insulation for both the charger and the switching part can be considered together. To provide closed-loop operation, the controller shown in Fig. 1 regulates the output voltage by controlling the switching frequency. Similar to the Marx modulator, the high-voltage pulse is generated by series stacking the power cell, which consists of SW, C_{storage}, and D_{bypass}. The main advantage of the power cell structure is that the bypass diode (D_{bypass}) limits the voltage across the switch even if the synchronized driving of all the switches fails. Therefore, it is not necessary to consider the dynamic and static voltage balancing between the output switches (SW_1–SW_N). Based on the aforementioned design concept of the SSMM, design considerations and criteria of the proposed capacitor charger are as follows.

A. High Efficiency, High Power Density, and High Power Factor

In order to achieve high efficiency and high power density, a converter topology that provides soft-switching should be considered. The high-frequency switching with a zero-voltage (ZV) and/or zero-current (ZC) condition reduces the switching loss and achieves compact design of the magnetic component. It is evident from the proposed multistate charger shown in Fig. 1 that the transformer of the proposed capacitor charger requires many secondary windings and insulation between the primary and secondary windings. Accordingly, relatively large values of the parasitic capacitance and leakage inductance are inevitable. These two parasitic components can be effectively used in the parallel resonant capacitor and the series resonant inductor when the proposed capacitor charger uses *LCC* resonant converter topology.

Minimizing the input capacitive filter is considered in this design for achieving a high power factor without an active correction circuit. Although the minimized input filter capacitor cannot compensate for the low-frequency ripple of the rectified input voltage, the charging voltage can be effectively regulated, since the storage capacitor can play the role of the output filter capacitor. Therefore, the aforementioned design criteria result in a high performance of the proposed capacitor charger in terms of efficiency, power density, and power factor.

B. Minimizing the RMS Value of the Resonant Current

The proposed multistage capacitor charger transfers all the charging power to each cell through the power loop that represents the primary winding of the transformer. As illustrated

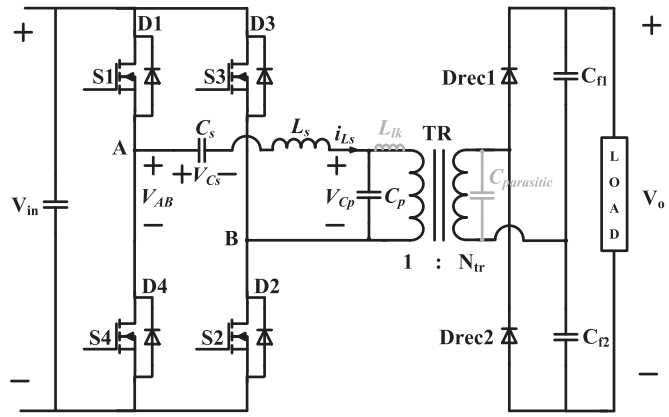


Fig. 2. Circuit of *LCC* resonant converter with voltage-doubled rectifier.

in Fig. 1, the comparatively long length of the power loop is expected to couple the primary winding to all the secondary windings, simultaneously. In addition, the insulation strength that is required between the primary and secondary windings should be greater than the maximum output voltage. Therefore, the high-voltage insulated cable is used for the primary winding. In order to reduce the conduction loss in the transformer primary winding, minimizing the root-mean-square (RMS) value of a high-frequency resonant current is the most important factor for designing the proposed multistage capacitor charger. Therefore, an *LCC* resonant converter, which operates above the resonance frequency and has a trapezoidal resonant current waveform, is used in designing the proposed capacitor charger.

C. Reliable Insulation Between Storage Capacitors

Depending on the voltage rating of the switch (SW) in Fig. 1, the charging voltage and the required number of the storage capacitors (*N*) is determined for generating the maximum pulse output voltage. In order to implement a high performance SSMM, it is preferable to decrease the charging voltage of each capacitor, since switches with relatively low voltage ratings generally provide a high performance in terms of losses and switching characteristics. However, decreasing the charging voltage results in an increase in the number of power cells, which is proportional to the number of secondary windings. Therefore, it is necessary to consider the insulation not only between the primary and secondary windings but also among the secondary windings. Notably, the maximum potential difference among the secondary windings is equal to the maximum pulse voltage. Owing to the restricted winding area of the core, a multistage transformer, which represents multiple cores coupled with the same primary winding, is proposed for securing a reliable insulation.

III. Analysis of the *LCC* Resonant Converter With Trapezoidal Resonant Current Approximation

As shown in Fig. 2, the circuit of the *LCC* resonant converter analyzed in this study consists of full-bridge inverter (S1–S4), an *LCC* resonant tank (a series resonant capacitor: C_s; a series resonant inductor: L_s; a parallel resonant capacitor: C_p),

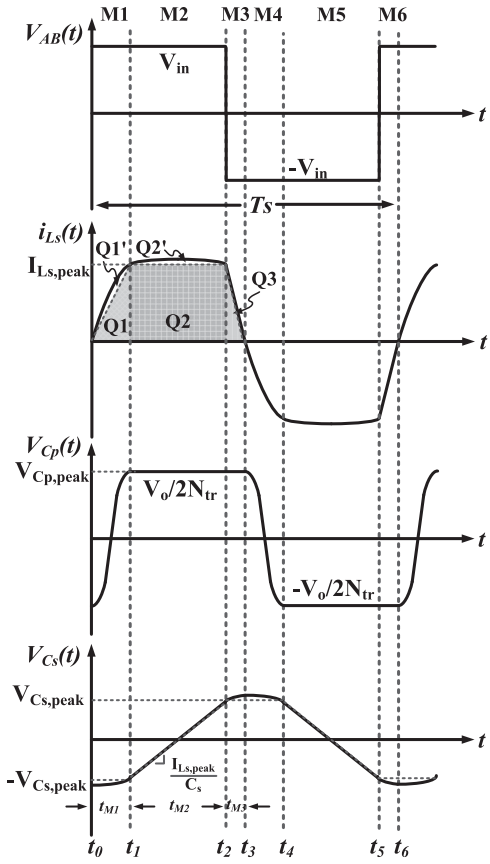


Fig. 3. Steady-state operating waveforms of *LCC* resonant converter with trapezoidal resonant current waveform.

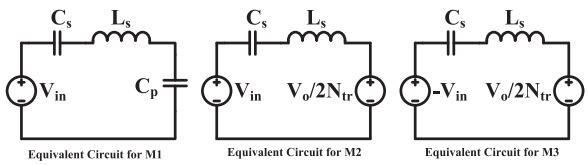


Fig. 4. Equivalent circuits for M1–M3.

a transformer (TR), and a voltage-doubled rectifier (Drec1, 2 and $C_{f1,2}$). From the perspective of designing the charger for SSMM, the configuration of the voltage-doubled rectifier has the advantage of effectively reducing the turns and/or the number of secondary windings. The effect of magnetizing inductance is ignored for simplified analysis of the *LCC* resonant converter because the higher value of the magnetizing inductance is generally considered and designed for neglecting the effect magnetizing current. The analysis and design procedure of the *LCC* resonant converter has already been introduced and is well known [14]–[18]. In this study, however, the objective of designing the *LCC* resonant converter is to minimize the crest factor of the resonant current, as described in Section II. It is evident that the trapezoidal shape of the resonant current provides a smaller crest factor compared to the sinusoidal waveform. Therefore, the analysis of the *LCC* resonant converter is provided based on the assumption that the resonant tank parameters are designed to shape the resonant current as shown in Fig. 3. Using the operational mode with an equivalent circuit illustrated in Fig. 4, the

analysis of *LCC* resonant converter with a trapezoidal shape of the resonant current is simplified as follows.

A. Definition of Resonant Tank Parameters

C_e: Equivalent resonant capacitor at *M*1 and *M*4

$\omega_{os,op,oe}$, $f_{os,op,oe}$, $T_{os,op,oe}$, and $Z_{os,op,oe}$: Resonant frequency, period, and characteristic impedance by means of C_s, C_p, C_e

$$C_e = \frac{C_s \cdot C_p}{C_s + C_p} \tag{1}$$

$$\omega_{os,op,oe} = \frac{1}{\sqrt{L_s \cdot C_{s,p,e}}} = 2\pi f_{os,op,oe}, T_{os,op,oe} = \frac{1}{f_{os,op,oe}} \tag{2}$$

$$Z_{os,op,oe} = \sqrt{\frac{L_s}{C_{s,p,e}}}. \tag{3}$$

B. Assumptions and Approximations (A1–A4) for Simplified Analysis of the LCC Resonant Converter with Trapezoidal Resonant Current Waveform

In order to shape the resonant current as trapezoidal, it is evident that the resonant frequency at M1 (f_{oe}) should be much greater than the resonant frequency at M2 (f_{os}). In contrast to the general design approach, which uses the same or similar value of the two capacitors C_p and C_s, this paper describes the analysis of *LCC* resonant converter based on the following assumptions and approximations.

A1. The value of C_s is considerably larger than the value of C_p.

A2. During M1 and M3, the voltage variation of $V_{Cs}(t)$ owing to the resonance is negligible and it can be considered as a dc voltage source, $V_{Cs,\mathrm{peak}}$. (During M1, the voltage variation of C_s is quite small owing to *A1*. During M3, t_{M3} is quite short owing to the steep slope of the resonant current.)

A3. During M2, the equation of the series resonant capacitor voltage $V_{Cs}(t)$ can be considered as a linear function against time owing to the trapezoidal approximation of the resonant current.

A4. Compared to the amp-second area (charge, *Q*) of Q1 and Q2 in Fig. 3, Q1' and Q2' are negligible in calculating the input and output power.

According to the aforementioned approximations, the operating waveforms of the resonant inductor current and the resonant capacitor voltage are shown in Fig. 3 and analyzed as follows.

C. Analysis of the LCC Resonant Converter Based on Trapezoidal Approximation

1) Mode1 (M1: t_0–t_1): Before starting M1, the switches S1 and S2 are turned on when the respective antiparallel diodes (D1 and D2) are conducting. Therefore, a ZV turn on is achieved for S1 and S2. When the polarity of the resonant current changes from negative to positive, M1 begins via the charging of C_p. As shown in Fig. 4, the value of the resonant current is determined by the input voltage and three resonant tank parameters (C_s, L_s, and C_p). According to the general expression of the resonant current (4), the equation of $i_{Ls}(t)$ during M1 can be simplified as (5). From (4), the cosine term is zero because the value of the resonant current at t_0 is zero. Based on the assumption *A1*, the equivalent characteristic impedance (Z_{oe}) and resonant frequency (ω_{oe}) are approximated to Z_{op} and ω_{op} (characteristic impedance and resonant frequency by means of L_s and C_p), respectively. The value of C_e calculated by (1) can be approximated to C_p when the value of C_s is considerably larger than the value of C_p (from *A1*). And, it can be seen from Fig. 3 that the value of $V_{Cp}(t_o)$ is equal to $-V_o/2N_{tr}$ (owing to transformer turns ratio and voltage-doubled rectifier) and the value of $V_{Cs}(t_o)$ is approximated to $-V_{Cs,\mathrm{peak}}$ (from *A2*). According to (5), it is evident that the value $I_{Ls,\mathrm{peak}}$ is determined by the voltage across the resonant inductor and Z_{op}

$$i_{Ls,\mathrm{M1}}(t) = i_{Ls}(t_0)\cos\omega_{oe}(t-t_0) + \frac{V_{in} - V_{Cp}(t_0) - V_{Cs}(t_0)}{Z_{oe}}\sin\omega_{oe}(t-t_0) \tag{4}$$

$$i_{Ls,\mathrm{M1}}(t) \cong \frac{V_{in} + V_o/2 \cdot N_r + V_{Cs,\mathrm{peak}}}{Z_{op}}\sin\omega_{op}(t-t_0). \tag{5}$$

2) Mode2 (M2: t_1–t_2): When the parallel resonant capacitor C_p is charged up to $V_o/2N_{tr}$, M2 starts with the conduction of the rectifier diode Drec1. In accordance with the clamping voltage of C_p, the series resonant tank determines the resonant current, as shown in Fig. 4. Based on (4), the expression for the resonant current during M2 can be written as (6). According to *A1*, the cosine term dominates the resonant current and it can be considered as a constant $I_{Ls,\mathrm{peak}}$. For the sine term, a smaller value of the numerator is desirable for shaping the resonant current as a trapezoid. Therefore, the transformer ratio N_{tr} is calculated on the premise that the primary winding voltage ($V_{Cp,\mathrm{peak}}$) is equal to the input voltage (V_{in}). On the basis of the earlier assumption, the equation for the resonant current during M2 is simplified as (7). This design provides a trapezoidal shape of the resonant current and reduces the RMS value. In addition, this resonant current waveform allows an increment in the snubber capacitor value when it is required to reduce the turn-off switching loss. Compared to the sinusoidal waveform, the stored energy in the resonant inductor does not strongly depend on the time interval t_{M2}. Therefore, the advantages of the trapezoidal resonant current include the reduction of the conduction loss and the turn-off switching loss by providing a low crest factor and increasing the value of snubber capacitor, respectively. As shown in Fig. 3, the peak value of the series resonant capacitor voltage $V_{Cs,\mathrm{peak}}$ is easily calculated as (8) based on *A3*

$$i_{Ls,\mathrm{M2}}(t) = I_{Ls,\mathrm{peak}}\cos\omega_{os}(t-t_1) + \frac{V_{in} - V_o/2 \cdot N_{tr} - V_{Cs}(t_1)}{Z_{os}}\sin\omega_{os}(t-t_1) \tag{6}$$

$$i_{Ls,\mathrm{M2}}(t) \cong I_{Ls,\mathrm{peak}} \cos\omega_{os}(t-t_1) + \frac{V_{Cs,\mathrm{peak}}}{Z_{os}} \sin\omega_{os}(t-t_1) \quad (7)$$

$$V_{Cs,\mathrm{peak}} = \frac{I_{Ls,\mathrm{peak}} \times t_{\mathrm{M2}}}{2 \cdot C_s}. \quad (8)$$

3) Mode3 (M3: t_2–t_3): By turning off S1 and S2, M3 starts with the conduction of the antiparallel diodes of S3 and S4. After turning on S3 and S4 with ZV, negative V_{in} is applied to the resonant tank and the resonant current reduces to zero. According to the equivalent circuit depicted in Fig. 4, the expression for the resonant current during M3 is written as (9), and it can also simplified based on *A1* and *A2*. The period, T_{os}, calculated from the series resonant frequency (ω_{os}), is much greater than the time interval t_{M3}. Therefore, the cosine term can be considered as the constant $I_{Ls,\mathrm{peak}}$. Based on *A2*, the effect of resonance can be ignored during M3, and $V_{Cs}(t_0)$ can be considered as a dc voltage source ($V_{Cs,\mathrm{peak}}$). According to this approximation, the sine term can be simplified as a linear function versus time. Therefore, the expression of the resonant current during M3 is simplified from (9) to (10)

$$i_{Ls,\mathrm{M3}}(t) = I_{Ls,\mathrm{peak}} \cos\omega_{os}(t-t_2) - \frac{V_{in} + V_o/2 \cdot N_{tr} + V_{Cs}(t_2)}{Z_{os}} \sin\omega_{os}(t-t_2) \quad (9)$$

$$i_{Ls,\mathrm{M3}}(t) = I_{Ls,\mathrm{peak}} - \frac{2 \cdot V_{in} + V_{Cs,\mathrm{peak}}}{L_s}(t-t_2). \quad (10)$$

D. Estimation of the Input and Output Power

As described in the mode analysis, it is reasonable to ignore Q1' and Q2' by applying the approximation *A4*. According to the ampere–second area of each mode (Q1–Q3) shown in Fig. 3, the following three power terms (input: P_{in}, transformer: P_{TR}, output: P_{out}) can be written as (11) to (13), respectively

$$P_{in} = V_{in} \cdot (\mathrm{Q1} + \mathrm{Q2} - \mathrm{Q3}) \cdot 2f_s \quad (11)$$

$$P_{TR} = V_{Cp,\mathrm{peak}} \cdot (\mathrm{Q2} + \mathrm{Q3}) \cdot 2f_s \quad (12)$$

$$P_o = V_o \cdot I_o = \frac{V_o}{2} \cdot 2I_o = \frac{V_o}{2N_{TR}} \cdot 2N_{TR} I_o \quad (13)$$

where

$$\mathrm{Q1} = \frac{1}{2} \cdot I_{Ls,\mathrm{peak}} \cdot t_{\mathrm{M1}} \cong \int_{t_0}^{t_1} i_{Ls,\mathrm{M1}}(t)dt = \mathrm{Q1} + \mathrm{Q1}' \quad (14)$$

$$\mathrm{Q2} = I_{Ls,\mathrm{peak}} \cdot t_{\mathrm{M2}} \cong \int_{t_1}^{t_2} i_{Ls,\mathrm{M2}}(t)dt = \mathrm{Q2} + \mathrm{Q2}' \quad (15)$$

$$\mathrm{Q3} = \frac{1}{2} \cdot I_{Ls,\mathrm{peak}} \cdot t_{\mathrm{M3}} \cong \int_{t_2}^{t_3} i_{Ls,\mathrm{M3}}(t)\ dt. \quad (16)$$

Further, (14) to (16) show the simplified expression for the charge of each mode, the approximation *A4* allows the simple calculation of power using (11) to (13). It also should be noted that the three voltage terms (V_{in}, $V_{Cp,\mathrm{peak}}$, $V_o/2N_{TR}$) are intentionally designed to have the same value in order to shape the resonant current as a trapezoid, as explained in M2 operation. Therefore, the following relationships are defined under the assumption of 100% efficiency.

TABLE I
NUMERICAL REQUIREMENTS OF A MULTISTAGE CAPACITOR CHARGER

Three-phase ac input voltage	380 $\mathrm{V_{ac,rms}}$ ± 10%
Rectified dc input voltage, V_{in}	513 V ± 10%
Maximum charging power, P_{max}	50 kW
Number of cell, N_{Cell}	48
Charging voltage of each cell, V_{Cell}	40 kV/48
Maximum efficiency, η_{max}	96%
Maximum power factor, $\mathrm{PF_{max}}$	0.96

By substituting (14)–(16) into (11) and (12) and equating (11) and (12), the relationship between t_{M1} and t_{M3} is given as

$$t_{\mathrm{M1}} = T_{op}/4 = \pi\sqrt{L_s \cdot C_p}/2 \cong 2t_{\mathrm{M3}}. \quad (17)$$

From (5), (10), and (17), t_{M1} can be calculated as a quarter of T_{op} and the value of $I_{Ls,\mathrm{peak}}$ can be calculated by

$$I_{Ls,\mathrm{peak}} = \frac{2 \cdot V_{in} + V_{Cs,\mathrm{peak}}}{Z_{op}}. \quad (18)$$

Accordingly, the time interval t_{M2} is given as (19), based on (17) and Fig. 3.

$$t_{M2} = \frac{T_s}{2} - t_{M1} - t_{M3} = \frac{(T_s - 3t_{M1})}{2} = \frac{(T_s - \frac{3}{4}T_{op})}{2} \quad (19)$$

By substituting (15)–(18) into (12), the power transferred through the transformer can be expressed again and (20) is derived by equating (12) and (13)

$$P_{TR} = V_{in} \cdot I_{Ls,\mathrm{peak}} \cdot \left(1 - \frac{5}{8}\frac{f_s}{f_{op}}\right) = \frac{V_o}{2N_{TR}} \cdot 2N_{TR} I_o = P_o. \quad (20)$$

IV. DESIGN AND IMPLEMENTATION OF A 50-KW MULTISTAGE CAPACITOR CHARGER FOR SSMM

According to the specifications summarized in Table I, the detailed design and implementation of a 50 kW multistage capacitor charger are presented in this section. The proposed capacitor charger consists of 48 power cells for generating a maximum output pulse of 40 kV when all the cells are connected in series. The following design is based on the maximum output voltage and current of 40 kV and 1.25 A, respectively. Depending on the connection between each cell, however, the maximum output current is adjustable for 50 kW rated power. For example, a dc power source with output voltage of 834 V and output current of 60 A can be implemented by connecting all the cells in parallel. Compared to the general capacitor charger that charges the capacitor from zero to maximum voltage with specific repetition rate, the designed capacitor charger is required to operate as a dc source for maintaining the charging voltage of the storage capacitors.

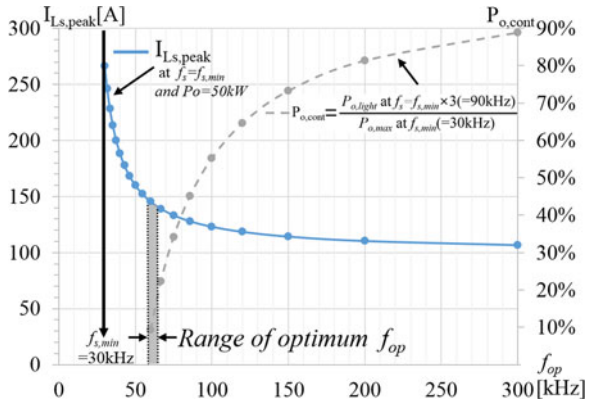


Fig. 5. Graph for finding the optimum value of f_{op}.

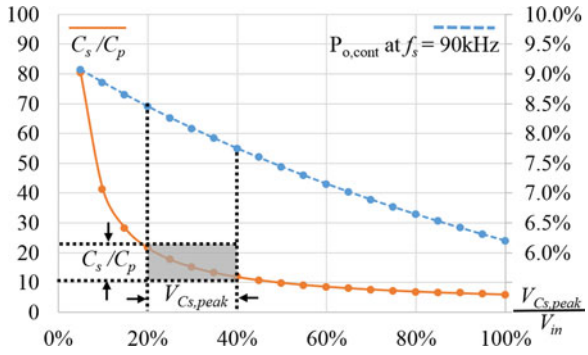


Fig. 6. Graph of C_s/C_p and $P_{o,\mathrm{cont}}$ versus $V_{Cs,\mathrm{peak}}$.

A. Design of a 50-kW Multistage Capacitor Charger Based on Trapezoidal Approximation of the LCC Resonant Converter

Based on the analysis of the proposed *LCC* resonant converter with trapezoidal approximation, the detailed design of a 50-kW capacitor charger is as follows.

1) Determining the Parallel Resonant Frequency (f_{op}) based on the Controllable Switching Frequency: To determine the controllable switching frequency, it is necessary to consider the losses of S1–S4 depending on the device characteristics. Practically, two silicon carbide MOSFET half-bridge modules (CAS300M12BM2, CREE) are used for implementing S1–S4 in Fig. 2. Based on the conduction and turn-off switching losses of MOSFET, a minimum switching frequency of 30 kHz is chosen. According to (20), the required peak value of the resonant current ($I_{Ls,\mathrm{peak}}$) for generating the desired output power depends on the parallel resonant frequency (f_{op}) when the switching frequency ($f_{s,\mathrm{min}}$) is determined. As shown in Fig. 5, it is evident that a higher f_{op} with fixed switching frequency provides a lower value of $I_{Ls,\mathrm{peak}}$ for generating 50 kW of maximum output power. This is because t_{M2} increases, and the value of $I_{Ls,\mathrm{peak}}$ can be reduced for maintaining Q2 as the value of t_{M1} calculated using (17) decreases. Therefore, it is preferable to increase f_{op} for reducing the peak value of the resonant current. On the other hand, f_{op} is also closely related to the controllable load range.

As derived in (20), the output power can be reduced by increasing the ratio of the two frequencies i.e., the maximum switching frequency should be increased with increasing f_{op} to achieve the desired light load operation. In order to find the optimum value of f_{op}, the graph showing all the relationships described above is presented in Fig. 5. Depending on the value of f_{op} from 1 to 10 times of the minimum switching frequency ($f_{s,\mathrm{min}}$), the required value of $I_{Ls,\mathrm{peak}}$ is calculated for the 50 kW operation. As shown in Fig. 5, the value of $I_{Ls,\mathrm{peak}}$ dramatically increases as f_{op} approaches $f_{s,\mathrm{min}}$. Therefore, f_{op} should be increased to reduce the conduction loss. On the other hand, the controllable load range should also be considered when choosing the optimum f_{op}. As defined dashed line in Fig. 5, $\mathrm{P}_{o,\mathrm{cont}}$ is the percentage load power ratio between $\mathrm{P}_{o,\mathrm{light}}$ (output power at 90 kHz of switching frequency) and $\mathrm{P}_{o,\mathrm{max}}$ (rated output power at 30 kHz of minimum switching frequency). Consequently, there is a restriction on the increase of f_{op} for achieving the light load operation within a controllable maximum switching frequency range, which can be determined by the switching characteristic of S1–S4 and the gate drive circuit. Fig. 5 clearly shows the trade-off relationship between the required $I_{Ls,\mathrm{peak}}$ for rated operation at $f_{s,\mathrm{min}}$ (solid line) and the controllable output at three times of $f_{s,\mathrm{min}}$ (dashed line). Finally, the value of f_{op} is selected in the range of optimum f_{op} illustrated in Fig. 5 that can provide $I_{Ls,\mathrm{peak}}$ less than 150 A, and achieves 10% of rated power at three times of $f_{s,\mathrm{min}}$.

2) Determining the Ratio Between Series Resonant Capacitor (C_S) and Parallel Resonant Capacitor (C_p): For choosing a suitable ratio between C_s and C_p, the peak value of the series resonant capacitor voltage ($V_{Cs,\mathrm{peak}}$) should be determined based on $I_{Ls,\mathrm{peak}}$. As expressed in (18), $I_{Ls,\mathrm{peak}}$ depends on the characteristic impedance of the parallel resonant tank (Z_{op}) and $V_{Cs,\mathrm{peak}}$. From the waveform of $V_{Cs}(t)$ in Fig. 3, it is evident that the value of $V_{Cs,\mathrm{peak}}$ reduces according to the decreasing t_{M2}. As a result, the value of $I_{Ls,\mathrm{peak}}$ calculated by (18) decreases with increasing switching frequency and it helps to improve the performance of the light load operation. Therefore, the value of $V_{Cs,\mathrm{peak}}$ that determines the ratio of C_s to C_p affects to the controllable load range.

In order to understand the aforementioned relationship, the ratio between the two capacitors (C_s/C_p) and $\mathrm{P}_{o,\mathrm{cont}}$ (at 90 kHz) versus the percentage of $V_{Cs,\mathrm{peak}}$ ($V_{Cs,\mathrm{peak}}/V_{in}$) are drawn in Fig. 6. The minimum boundary of the allowable value of $V_{Cs,\mathrm{peak}}$ can be determined based on the desired output power at a switching frequency of 90 kHz. On the other hand, it is suitable to choose a value of C_s greater than 10 times of C_s for satisfying *A1* and validating the trapezoidal approximation. Therefore, the reasonable range of $V_{Cs,\mathrm{peak}}$ and the ratio between the two capacitors are illustrated as gray color in Fig. 6 and 25% of $V_{Cs,\mathrm{peak}}/V_{in}$ is finally determined for designing capacitor charger.

3) Calculation and Verification of the Design Parameters: After determining the value of f_{op} and $V_{Cs,\mathrm{peak}}$, all the design parameters can be listed as shown in Table II. Owing to the trapezoidal approximation, the value of the resonant tank components is simply calculated from the equations listed in the second row of Table II.

TABLE II
DESIGN PARAMETERS OF *LCC* RESONANT TYPE 40 KV, 50 KW CAPACITOR CHARGER FOR SSMM

	$V_{\rm in}$ [$V_{\rm dc}$]	$N_{\rm TR}$	$f_{s,\rm min}$ (kHz)	f_{op} (kHz)	$f_{s,\rm light}$ (kHz)	$V_{\rm Cs,peak}$ (V)	C_s (μF)	Z_{op} (Ω)	L_s (μH)	C_p (μF)
From	Table I	$V_o/2/V_{in}$	Section II-C	Fig. 5	Eq. (20)	Fig. 6	Eqs. (8) and (19)	Eq. (18)	Eqs. (2) and (3)	
Value	513 ± 10%	40	30	60	90	128	5.91	7.94	21.06	0.334

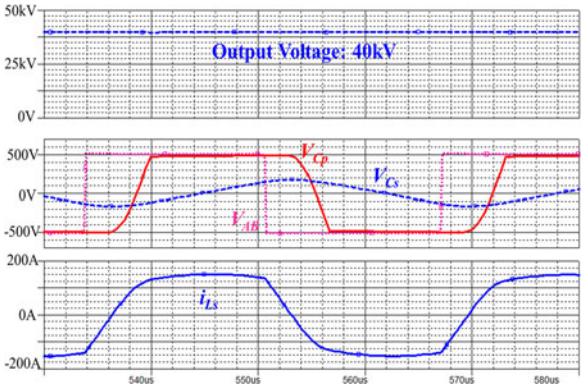


Fig. 7. PSpice simulation results at $f_s = 30$ kHz and $P_o = 50$ kW.

For verifying the designed parameters, a PSpice simulation is performed and the results are shown in Fig. 7. The simulated waveforms show the trapezoidal shape of the resonant current (i_{Ls}) and the triangular shape of C_s voltage (V_{Cs}) as illustrated in Fig. 3 and approximated in the analysis. As explained in M2, the transformer turns ratio is designed such that C_p voltage (V_{Cp}) equals the input voltage (V_{in}). According to (6), the value of $I_{Ls,\rm peak}$ at t_2 somewhat decreases when 0.9 times V_{in} is applied owing to the input voltage variation. In contrast, 1.1 times V_{in} provides a higher $I_{Ls,\rm peak}$ at t_2 and the switching frequency should be slightly increased for output voltage regulation.

This is because the sine term is approximated from (6) to (7) based on the assumption that $V_o/2N_{tr}$ is equal to V_{in}. When the input voltage is decreasing with fixed output voltage, the value of the numerator in (6) decreases correspondingly. Accordingly, the value of the resonant current at t_2 will be decreased. On the contrary, the higher value of the input voltage increases the numerator term and provides the higher value of the resonant current at $\rm t_2$. With V_{in} of 513 V, output voltage of 40 kV and output power of 50 kW are observed, and the value of $I_{Ls,\rm peak}$ also matched the estimated value.

B. Implementation of a 50-kW MultiStage Capacitor Charger for SSMM

Using the designed converter based on the circuit shown in Fig. 2, the detailed implementation of the proposed multistage capacitor charger for SSMM is described in this section.

Based on the number of cells, the detailed design of the multistage transformer and rectifier is given in Table I. Accordingly, the transformer and rectifier in Fig. 2 are required to be reconfigured as the conceptual circuit in Fig. 1. For charging 48 pieces of capacitor and maintaining the sum of charging voltage at 40 kV,

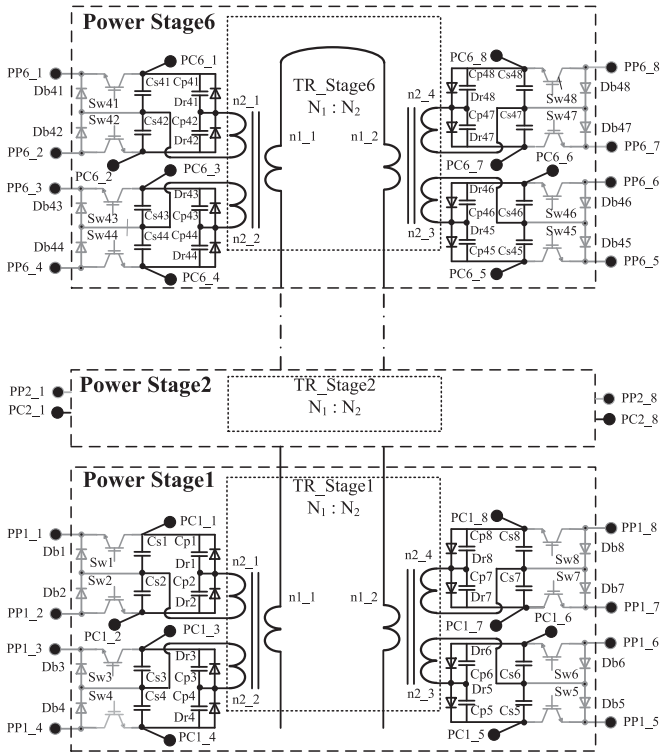


Fig. 8. Detailed circuit of a multistage transformer and rectifier.

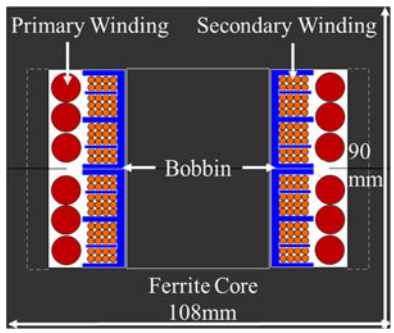


Fig. 9. Structure of transformer for each power stage.

24 secondary windings are required when the voltage-doubled scheme is connected to each secondary winding. The detailed circuit of the multistage transformer and rectifier is shown in Fig. 8. In order to secure reliable insulation, the structure of the power stage consisting of a transformer and four voltage-doubled rectifiers is designed, and 48 power cells are implemented in six power stages. As shown in Fig. 9, the primary winding of the resonant inverter is designed to penetrate the

TABLE III
CALCULATION OF PARAMETERS FOR IMPLEMENTATION

Design Parameter	Calculation	Value
N1: N2 (n1_1+n1_2):(n2_1+ ••• + n2_4)	$N1 : N1 \bullet N_{\mathrm{TR}}$	2: 80
Cp1–Cp48	$\frac{C_p \cdot N_{stage} \cdot N_{sec}}{2 \cdot N_{\mathrm{TR}}^2}$	2.5 nF

winding area of all the power stage transformers (TR_Stage1–TR_Stage6) to supply the charging power simultaneously. A high-voltage insulation cable is used for implementing the primary winding to guarantee the insulation and three cables are connected in parallel to increase the cross-section of the conductor. Four secondary windings are wound on a bobbin with eight partitions for the winding area. Two sections are arranged for one secondary winding to provide reliable insulation between the secondary wires [19].

Therefore, 2 turns of a primary winding and 20 turns of four secondary windings are effectively implemented for each stage as calculated in Table III. For choosing suitable core, area product (AP) can be calculated based on 30 kHz of minimum switching frequency and 50 kW of maximum output power. Accordingly, the number of turns of the primary winding (N1) is determined from the minimum switching frequency and maximum voltage of the primary winding (same as dc input voltage, V_{dc}). For the calculation of N1, 0.5 T of flux density swing is used for reducing the ferrite core loss. Owing to the structure of the transformer, a substantial value of leakage inductance is inevitable and it can be effectively used as the resonant inductor when the parallel resonant capacitor is implemented at the secondary side of the transformer. With the proposed structure of the transformer, the measured leakage inductance is 9.6 and 11.4 μH of additional inductor is added to satisfy the designed series resonant inductance of 21 μH. In practice, the parallel resonant capacitor (Cp1–Cp48) is implemented in parallel with the diode rectifier as shown in Fig. 8. In this case, the role of Cp1–Cp48 is not only to provide parallel resonance according to the designed value, but also to achieve voltage balance in the series stacked diodes. Practically, each diode (Dr1–Dr48) is implemented by connecting two diodes in series. In order to provide the same value of the parallel resonant capacitance, the value of Cp1–Cp48 is calculated as shown Table III where N_{stage} (number of stages) $= 6$ and N_{sec} (number of secondary windings per stage) $= 4$.

It should be noted that the effect of the parasitic capacitance ($C_{\mathrm{parasitic}}$) shown in Fig. 2 is negligible in this design. This is because the proposed structure of transformer has multiple secondary windings with the partitions. Therefore, the value of $C_{\mathrm{parasitic}}$ is relatively small compared to 2.5 nF of Cp1–Cp48. In addition, the junction capacitance of rectifier diode is also ignored because practically implemented diode (FFPF10F150S, Fairchild) has comparatively small junction capacitance. According to the aforementioned procedure, the designed *LCC* resonant converter based on the circuit in Fig. 2 is implemented as the proposed multistage capacitor charger for SSMM in Fig. 1. A picture of the developed capacitor charger depicted in Fig. 10 shows the practical configuration of all the parts including the resonant inverter and six power stages. The resonant inverter that is located at the bottom of the charger includes the switches and the series resonant tank components (S1–S4, *Cs*, *Ls* in Fig. 2). The upper side of Fig. 10 shows the structure of the power stages consisting of the storage capacitors (Cs1–Cs48), the rectifier diodes (Dr1–Dr48), and Tr_Stages (Tr_Stage1–Tr_Stage6), as depicted in Fig. 8.

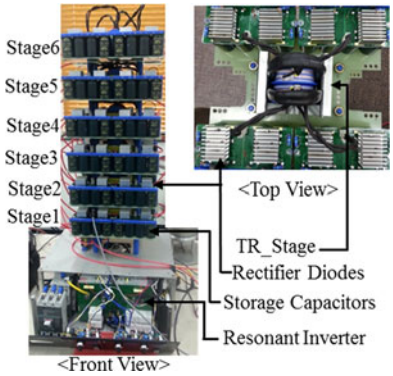


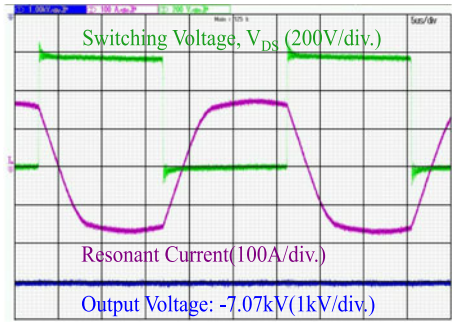
Fig. 10. Developed capacitor charger.

V. EXPERIMENTAL RESULTS OF THE DEVELOPED MULTISTAGE CAPACITOR CHARGER

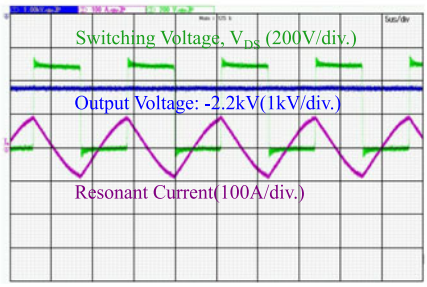
The developed capacitor charger based on the proposed circuit is tested with a resistor load without connecting switches for the generation of pulses. As shown in Fig. 8, the components in gray color, including the switches (SW1–SW48) and the diodes (Db1–Db48), can be connected for applying a pulse to the load. Depending on the connection between the power cells (PP1_1–PP6_8), the polarity of the output pulse can be chosen for different applications.

In order to verify the designed capacitor charger, eight power cells inside a power stage are connected in series (example of power stage 1 connection for negative output: Ground-PC1_1, PC1_2-PC1_3, . . . , PC1_6-PC1_7, PC1_8-Negative high voltage output) and each of the stages is connected in parallel (Ground-PC1_1-PC2_1- . . . -PC6_1, Negative high voltage output-PC1_8-PC2_8 . . . -PC6_8). This experimental configuration provides a rated output voltage and power of 7 kV and 50 kW, respectively, with a resistor load of 1 kΩ. The experimental waveforms in Fig. 11(a) show the resonant current, the drain–source switching voltage, and the output voltage at 50 kW operation.

The experimental results at the rated operation verify the analysis and design conducted with the trapezoidal approximation. It should be noted that the designed capacitor charger has a relatively large input voltage ripple owing to the small input filter capacitance for achieving a high power factor. As described in Section IV, the shape of the resonant current and the switching frequency will change slightly to regulate the output voltage regardless of the variation of input voltage. The waveforms in Fig. 11(a) are measured at 1.1 times V_{in} and a switching frequency of 36 kHz. The experimental result in Fig. 11(b) shows



(a)



(b)

Fig. 11. Experimental waveforms with a resistor load (1 kΩ). (a) Experimental waveforms at rated-load operation (at $f_s = 36$ kHz). (b) Experimental waveforms at light-load operation (at $f_s = 90$ kHz).

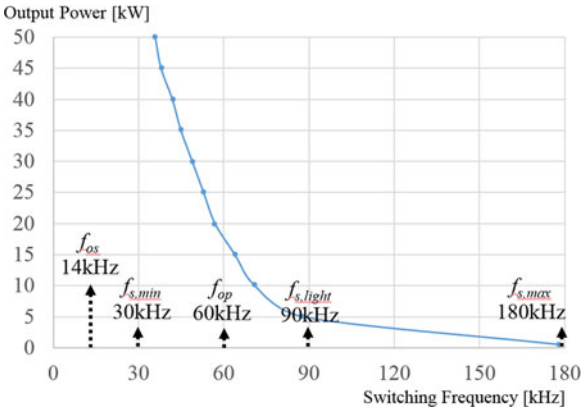


Fig. 12. Control characteristic of the developed capacitor charger.

the operating waveforms at a switching frequency of 90 kHz. Although the output voltage is reduced owing to the fixed load resistance, the triangular shape of the resonant current is measured, as discussed in Section IV. Owing to the decrease of the output voltage, the peak value of the triangular resonant current slightly decreases and it provides less output power compared to the estimated value illustrated in Fig. 6. With a fixed load resistance (1 kΩ), the output power measured against the control of switching frequency is shown in Fig. 12. Further, $f_{s,\mathrm{light}}$ represents the maximum switching frequency that can estimate the output power of the *LCC* resonant converter using (20). In Fig. 12, it can be observed that the designed capacitor charger operates under a load condition of 100% to 1% and a switching frequency range of 30–180 kHz. Depending on the output power,

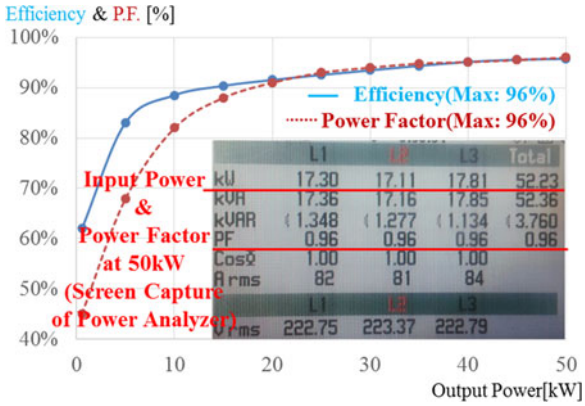


Fig. 13. Measured efficiency and power factor depending on the output power.

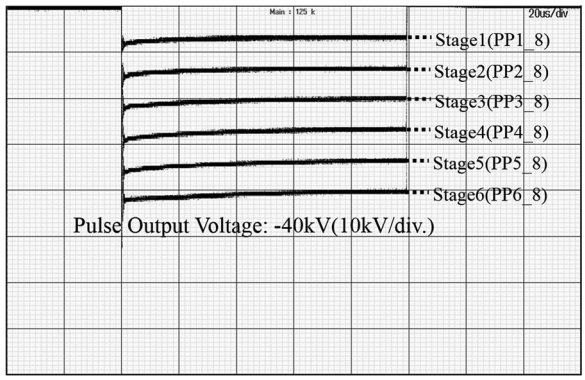


Fig. 14. Pulse operation of the developed multistage capacitor charger.

the efficiency and power factor are measured from ac line input to dc high voltage output as shown in Fig. 13 and the maximum value of both the efficiency and the power factor is 96%. In order to verify the experimental data in Fig. 13, the screen capture of a power analyzer (435 Power Quality Analyzer, FLUKE) at 50 kW operation is included, and it shows 0.96 of the power factor with displacement power factor ($\cos\phi = 1$). That is, the phase difference between the input voltage and the fundamental component of input current is almost zero. By means of minimizing input filter, 0.96 of high-power factor can be achieved as explained in Section II-A. It should be noted that the graphs Figs. 12 and 13 were drawn based on the experimental data when the developed charger operates with eleven different switching frequencies. In order to confirm the feasibility of the developed charger for SSMM, a preliminary pulse operation test with 5 kΩ resistor load is performed using the switches (SW1–SW48) and the diodes (Db1–Db48), as shown in Fig. 8. To generate high-voltage output pulse, the transformer that transfer bipolar short pulse is used for simultaneous driving all the switches as well as providing proper isolation [21]. By connecting 48 cells in series using the switches, an output pulse of −40 kV is measured, as shown in Fig. 14, and the insulation performance of the proposed charger is verified. In addition, the output of each power stage is measured to check the voltage balance between stages. Finally, the experimental results verify the analysis and

design of the proposed multistage capacitor charger based on the *LCC* resonant converter.

VI. Conclusion

This paper describes the design of a capacitor charger for SSMM. Based on the simplified analysis of an *LCC* resonant converter with a trapezoidal shape of the resonant current, a 50-kW high-voltage capacitor charger is designed for a 40-kV solid-state Marx modulator. The detailed design and implementation procedure are described. The experimental results verify the design and prove the superiority of the proposed circuit in terms of efficiency and power factor. Finally, it was confirmed that the proposed multistage capacitor charger can be effectively applied for developing the SSMM. A further direction of this study will be the development of 40 kV, 20 A, 300 μs, and 200 Hz SSMM for radar applications.

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