Temperature-Dependent Characterization, Modeling, and Switching Speed-Limitation Analysis of Third-Generation 10-kV SiC MOSFET

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***Abstract*—The temperature-dependent characteristics of the third-generation 10-kV/20-A SiC MOSFET including the static characteristics and switching performance are carried out in this paper. The steady-state characteristics, including saturation current, output characteristics, antiparallel diode, and parasitic capacitance, are tested. A double pulse test platform is constructed including a circuit breaker and gate drive with >10-kV insulation and also a hotplate under the device under test for temperature-dependent characterization during switching transients. The switching performance is tested under various load currents and gate resistances at a 7-kV dc-link voltage from 25 to 125 °C and compared with previous 10-kV MOSFETs. A simple behavioral model with its parameter extraction method is proposed to predict the temperature-dependent characteristics of the 10-kV SiC MOSFET. The switching speed limitations, including the reverse recovery of SiC MOSFET's body diode, overvoltage caused by stray inductance, crosstalk, heat sink, and electromagnetic interference to the control are discussed based on simulations and experimental results.**

***Index Terms*—10-kV silicon carbide (SiC) metal–oxide–semiconductor field-effect transistor (MOSFET), junction temperature, switching performance.**

I. Introduction

CONSIDERING that the breakdown field strength of silicon carbide (SiC) is ten times higher than silicon (Si), SiC power semiconductors show superior performance in medium- and high-voltage (HV) levels (>3.3 kV). Furthermore, due to a much lower switching loss of HV SiC devices, the switching frequency can be ten times more than their Si counterparts. Therefore, medium-voltage SiC-based converters can bring great benefits in weight, size, and control bandwidth over Si-based converters. In recent years, HV SiC devices (>3.3 kV) have been rapidly developed including junction barrier schottky (JBS) and p-i-n diodes [1]–[3], junction gate field-effect transistors (JFETs) [4], metal–oxide–semiconductor field-effect transistors (MOSFETs) [5]–[17], bipolar junction transistors [1], and insulated-gate bipolar transistors (IGBTs) [18], [19].

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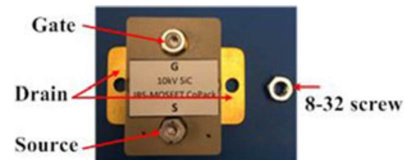

Fig. 1. 10-kV/20-A MOSFET.

These devices have potential applications in medium and HV power converters, e.g., medium-voltage motor drives [17] and power grid applications [5]–[8]. It is important to understand characteristics of these emerging devices.

Among these switches, SiC MOSFETs have many desirable features from users' perspective, including normally off operation, low turn-off loss due to the lack of bipolar tail current, low conduction loss, and low gate charge [9]. Recently, Wolfspeed has released its third-generation 10-kV/20-A MOSFET, which has significant improvement in specific on-resistance than the previous generation. With optimized doping in the drift and JFET regions, the specific on-resistance decreased from $160\ \mathrm{m\Omega \cdot cm^2}$ in the second-generation device to $100\ \mathrm{m\Omega \cdot cm^2}$ [14]. The enhanced short-circuit capability with >10-μs short-circuit withstand time is also achieved [10]. This paper focuses on Wolfspeed's third-generation 10-kV/20-A MOSFET/JBS copack module, as shown in Fig. 1. Some characteristics have been published in [14], but many key device temperature-dependent characteristics have not been extensively measured and will be essential to the application of the device in converters. This paper introduces the temperature-dependent characterization of the 10-kV SiC device both in steady-state and during switching transients, and carries out the device characterization from 25 to 125 °C.

Some researchers have modeled the 1.2- and 1.7-kV low-voltage (LV) SiC MOSFETs, which are helpful to theoretically explained device's characteristics [20]–[23]. These studies focus on MOSFET channel [24], base region [25], [26], parasitic capacitance [27], interaction with external circuits [28], [29], and parameter extraction [30], [31]. Several researchers modeled HV SiC devices [12], [32]. However, the temperature-dependent characteristics during the switching transient are not studied in these models. The validity of the LV SiC device model

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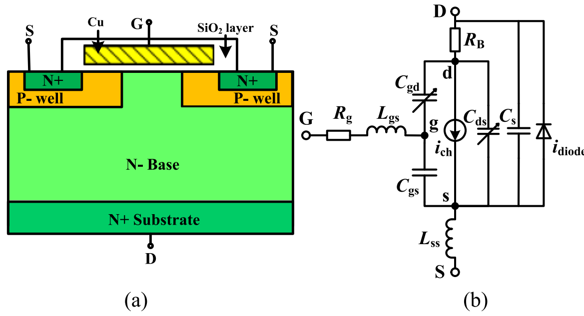

Fig. 2. Cell structure and equivalent circuit of 10-kV MOSFET. (a) Cell structure. (b) Equivalent circuit.

in the 10-kV SiC MOSFET is studied based on experimental results in this paper. Furthermore, a simple behavioral model with its parameter extraction method is proposed to predict the temperature-dependent characteristics both in steady-state and during switching transients.

The switching performance is the key characteristics of SiC MOSFETs. The *dv/dt* and switching loss are two critical parameters for the switching speed. Some works about impact factors on the switching performance have been conducted for LV SiC devices including signal isolator [33], parasitic [34], crosstalk issue [35], electromagnetic interference (EMI) [36], and impact of load [37], but these works have not been extended into HV SiC devices. The factors impacting the switching performance of the 10-kV SiC MOSFET will be discussed based on the model simulations and test results.

In this paper, the 10-kV/20-A MOSFET is characterized in steady state in Section II. The model is presented and the parameters are extracted based on test results. The temperature-dependent factors are discussed in each section. The double pulse test (DPT) platform construction including the overcurrent protection is presented in Section III. The switching performance at various temperatures is obtained under various load currents and gate resistances at 7-kV dc-link voltage from 25 to 125 °C, and the accuracy of the model during switching transient is verified. Furthermore, based on the model, the switching speed-limitation factors are discussed in Section IV.

II. Steady-State Characterization and Modeling

The 10-kV MOSFET studied in this paper is a third-generation DMOSFET. It is a MOSFET/JBS copack module which has a JBS diode die as its antiparallel diode. The simplified cell structure and equivalent circuit are shown in Fig. 2.

C_{gd}, C_{gs}, and C_{ds} are parasitic capacitances of the MOSFET. The parasitic capacitance of the antiparallel diode is included in C_{ds}. C_{gd} and C_{ds} vary with their withstanding voltages. C_s is the parasitic capacitance between the drain and the heat sink and only exists after the device is mounted. In a DPT platform, the heat sink is replaced by a hotplate. In a real converter, the analysis on C_s network can be very complicated due to the complex heat sink and grounding system design. i_{ch} is the current which flows through the channel of the MOSFET and is determined by voltage drop on the channel and gate-to-source voltage v_{gs}. R_B is the base resistance and mainly influenced by the parameters of N−base. i_{diode} is the current that flows through antiparallel diodes, including the JBS diode and body diode. R_g is lumped gate resistance consisting of the internal gate resistance of the device, the output resistance of gate drive buffers, and external gate resistance designed by users. L_{gs} and L_{ss} are the parasitic inductances in the gate drive loop and are impacted by the loop area in the gate drive board and parasitic inductance in the MOSFET module. Considering the four-terminal package is not applied in this module, L_{ss} is not negligible. L_{gs} and L_{ss} are, respectively, 5 and 1 nH based on model parameter extraction.

A. Saturation Current

The saturation current plays an important role during the switching transient, especially during the turn-on transient. During the switching transient, due to a high v_{DS}, i_{ch} reaches the saturation current which is mainly decided by v_{gs} and the gate threshold voltage v_T.

Datasheets of HV SiC MOSFETs commonly only show the devices' output characteristics in the ohmic region. Some studies have been done on the characteristics in the active region through a static characteristics test with an extended drain-to-source voltage [30]–[32]. Different from Si IGBTs, the saturation current of SiC MOSFETs cannot be directly obtained from $v_{DS} - i_d$ curves in the active region. v_{DS} is the drain-to-source voltage and i_d is the device current. For SiC MOSFETs, it has been concluded that i_{ch} increases with increasing voltage drop on the channel even in the active region due to its short-channel effects [38]. However, MOSFETs will not operate in this condition even during the switching transient. During the switching transient, because the drain-to-source voltage drops on the N− base rather than on the channel, i_{ch} reaches the saturation current, which is a function of v_{gs}, and does not change with the drain-to-source voltage.

The saturation current should be extracted from $v_{DS} - i_d$ curves in the active region. The MOSFET current when the channel voltage equals $v_{gs} - v_T$ is a good approximation to the saturation current. During a switching turn-on transient, i_d changes from 0 to 40 A corresponding to a variation of v_{gs} from v_T to around 10 V. $i_{ch}(v_{gs})$ in this range is extracted through the measurement of the curve tracer Keysight B1505A. A quadratic formula is applied to describe the relationship between v_{gs} and i_{ch}

$$i_{ch} = \frac{k_p}{2}(v_{gs} - v_T)^2 \tag{1}$$

where k_p is the saturation current transconductance factor (A/V^2). It should be noted that (1) is a model for the saturation current, but not for the active region. Considering the switching performance is mainly determined by the saturation current, (1) will be used to describe the channel, which is different from existing models. The gate threshold voltage v_T varies with the junction temperature T_j

$$v_T(T_j) = v_{T,25} + T_{kp}(T_j - 25) \tag{2}$$

where $v_{T,25}$ is the threshold voltage at 25 °C and T_{kp} is the temperature coefficient of the threshold voltage. The extracted v_T reduces from 3.85 V at 25 °C to 2.75 V at 125 °C, indicating a temperature coefficient of 11 mV/°C. The extracted k_p is

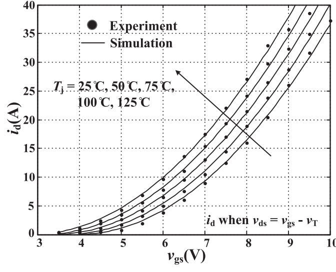

Fig. 3. Simulated saturation current comparison with experimental results.

nearly constant at various T_j from 25 to 125 °C and equals 2.02 A/V^2. The simulation results with (1) correlate well with experimental results, as shown in Fig. 3.

It should be noted that in most of models, the channel is modeled based on the output characteristics. This is not suitable for HV SiC MOSFETs. Generally, the output characteristics present $v_{DS} - i_d$ curves at high v_{gs}. In this case, the voltage drop on the MOSFET channel can be neglected compared with the base resistance for HV SiC MOSFETs. Therefore, the channel parameters cannot be obtained through the output characteristics. The saturation current also greatly affects the switching performance during the turn-on transient. Therefore, the saturation current model can also be verified by the DPT. The accuracy of the model to describe the turn-on performance cannot be guaranteed if the channel is modeled based on the output characteristics.

B. Output Characteristics

The output characteristics (on-state) are mainly determined by the base resistance R_B. Different from Si IGBTs and LV SiC MOSFETs, the voltage drop on R_B is much higher than that on the channel in the ohmic region. Especially with increasing v_{gs} which brings a lower voltage drop on the channel and increasing T_j which leads to a larger R_B, the base resistance becomes dominant in the output characteristics. R_B is determined by the doped concentration (6×10^{14} cm^{-3}), the thickness (100 μm), and the active area (27.5 mm^2) of N− base. R_B arises with elevated T_j due to the decrease of the electron mobility. R_B can be described by

$$R_B(T_j) = R_{B,25}\left(\frac{T_j + 273}{298}\right)^{\alpha_{T,\mathrm{MOS}}} \quad (3)$$

where $R_{B,25}$ is the base resistance at 25 °C and $\alpha_{T,\mathrm{MOS}}$ is the temperature coefficient of R_B. In the output characteristics test, the MOSFET operates in the ohmic region and the MOSFET channel can be described by

$$i_{ch} = k_p(v_{gs} - v_T - v_{ds}/2)v_{ds}. \quad (4)$$

The comparison of the output characteristics between the simulation results and the experimental results is shown in Fig. 4. The experimental results of R_B are calculated in terms of the $v_{DS} - i_d$ curves at $v_{gs} = 20$ V. R_B increases from 355 mΩ at 25 °C to 870 mΩ at 150 °C and the extracted temperature coefficient $\alpha_{T,\mathrm{MOS}}$ is 2.5.

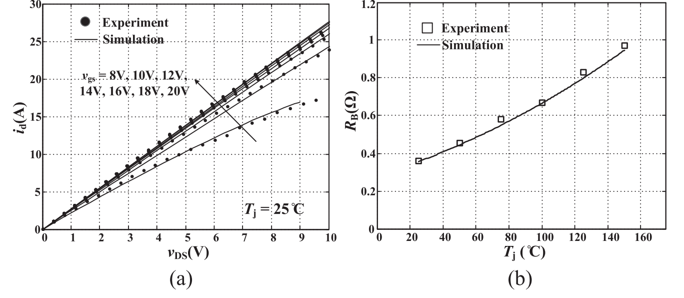

Fig. 4. Simulated output characteristics comparison with experimental results. (a) Output characteristics at 25 °C. (b) Base resistance at various junction temperature.

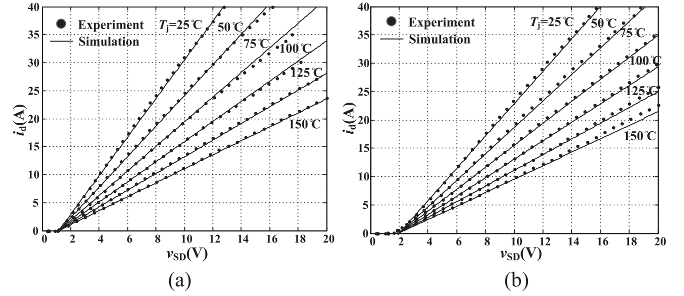

Fig. 5. Simulated antiparallel diode characteristics comparison with experimental results. (a) JBS diode. (b) Body diode.

C. Antiparallel Diode

The antiparallel diode of the MOSFET module consists of a 10-kV JBS diode and the MOSFET's body diode in parallel connection. Due to a high-energy gap E_g of SiC (>2 V), the body diode only turns on when $v_{SD} > 2$ V. For LV SiC JBS diodes, the forward voltage at its rated current is commonly lower than 2 V (e.g., $v_F = 1.6$ V at 50 A for Wolfspeed's 1.7-kV/50-A SiC JBS diode). Therefore, nearly all reverse current flows through the JBS diode in LV SiC MOSFET/JBS copack modules.

However, in 10-kV SiC MOSFETs, the resistance of the JBS diode becomes much larger due to a thicker base. The forward voltage can exceed E_g at its rated current. The reverse current which flows through the body diode cannot be ignored any more. As shown in Fig. 5, the currents of the body diode and the JBS diode are comparable. Because the body diode is a p-i-n diode, the excess carrier effect should be estimated in order to get an accurate assessment for the switching performance.

The JBS diode can be described by

$$v_{\mathrm{SD,JBS}} = v_f + i_d R_{B,\mathrm{JBS}} \quad (5)$$

where v_f is the ohmic contact voltage and $R_{Bd,\mathrm{JBS}}$ is the base resistance of the JBS diode. Similar with R_B, $R_{B,\mathrm{JBS}}$ can be represented as

$$R_{B,\mathrm{JBS}}(T_j) = R_{B,\mathrm{JBS},25}\left(\frac{T_j + 273}{298}\right)^{\alpha_{T,\mathrm{JBS}}} \quad (6)$$

where $R_{B,\mathrm{JBS},25}$ is the base resistance of the JBS diode at 25 °C and $\alpha_{T,\mathrm{JBS}}$ is the temperature coefficient of $R_{B,\mathrm{JBS}}$. v_f equals 1.16 V and is nearly constant at various T_j. $R_{B,\mathrm{JBS}}$ increases

from 290 mΩ at 25 °C to 800 mΩ at 150 °C. The extracted $\alpha_{T,\mathrm{JBS}}$ is 2.9 and slightly larger than the temperature coefficient of the MOSFET's base resistance. It means that with increasing T_j, the forward characteristics of the JBS diode become worse than the MOSFET's body diode. The simulation results have a good fit with experimental results, as shown in Fig. 5(a).

Different from the JBS diode, the MOSFET's body diode is a p-i-n diode. The excess carrier effect should be taken into consideration [39], [40]. In on-state, the injection of excess carriers brings a smaller base resistance, especially at a high conduction current. During the switching turn-off transient, the sweep out of these carriers causes the reverse recovery and increases the switching loss. The impact of the excess carriers can be estimated by the forward characteristics of the body diode. With the injection of excess carriers into the N− base, the base resistance decreases due to the increasing hole concentration. If the excess carriers effect plays a major role, the base resistance of the p-i-n diode will decrease dramatically with the increase of the conduction current and will be much smaller than R_B tested through output characteristics. However, the experimental results show that the resistance of the body diode is nearly constant for a conduction current less than 40 A and equals 0.35 Ω at 25 °C which is very close to R_B. The injection of excess carriers only brings less than 1.5% reduction in the resistance of the body diode. Therefore, only very few excess carriers are injected into the base, and the excess carrier effect is negligible here. The p-i-n diode can be described by

$$v_{\mathrm{SD,PiN}} = v_{\mathrm{PN}} + i_d R_B \tag{7}$$

where v_{PN} is the voltage drop in the p-n junction and equals 2 V. The simulated forward characteristics of the body diode are compared with experimental results in Fig. 5(b).

D. Parasitic Capacitances

The parasitic capacitances include C_{gs}, C_{gd}, C_{ds}, and C_s. C_{gs}, C_{gd}, and C_{ds} are internal parasitic capacitances of the MOSFET module and can be measured by the curve trace Keysight B1505A and its capacitance test fixture N1273A which can test *C–V* curves up to 3 kV. C_{gs}, which is the capacitance of the SiO_2 layer between the gate and the source, is constant and equals 4.7 nF. C_{gd} and C_{ds} are voltage-dependent capacitances. With the consideration of the kink in the *C–V* curves induced by the ion implantation [12], C_{gd} can be described as follows:

$$C_{gd} = \begin{cases} C_{gdi}/\sqrt{v_{dg}} & v_{dg} \le v_{\mathrm{lim}} \\ \frac{C_{gdi}/\sqrt{v_{\mathrm{lim}}}\cdot C_{gdb}/(v_{dg}-v_{\mathrm{lim}})^M}{C_{gdi}/\sqrt{v_{\mathrm{lim}}}+C_{gdb}/(v_{dg}-v_{\mathrm{lim}})^M} & v_{dg} > v_{\mathrm{lim}} \end{cases} \tag{8}$$

where C_{gdi} represents the capacitance of the ion implantation layer. v_{lim} is v_{dg} when the depletion region completely covers the ion implantation layer and equals 50 V. When v_{dg} is higher than v_{lim}, C_{gd} is the series connection of the capacitance of the ion implantation layer and the capacitance of the N− base region. C_{gdb} represents the capacitance of the N− base region. M is a voltage-dependent factor which is affected by the doping in the base, and can be extracted from the slope of $\log(v_{DS}) - \log(C)$ curves. The extracted values of C_{gdi} and C_{gdb} are 260 and 40 pF while M is 1/3. It should be noticed that M in LV SiC models is set as 0.5 by assuming the base is uniformly doped. This is not suitable for this 10-kV device. C_{ds} can be described with a similar equation. The extracted drain-to-source capacitance of the ion implantation layer C_{dsi} and drain-to-source capacitance of the base region C_{dsb} are 15 and 5.58 nF, while the voltage-dependent factor of C_{ds} is 0.5. The comparison between simulated parasitic capacitances and experimental results are shown in Fig. 6.

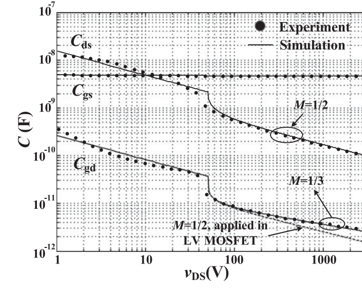

Fig. 6. Simulated parasitic capacitances comparison with experimental results.

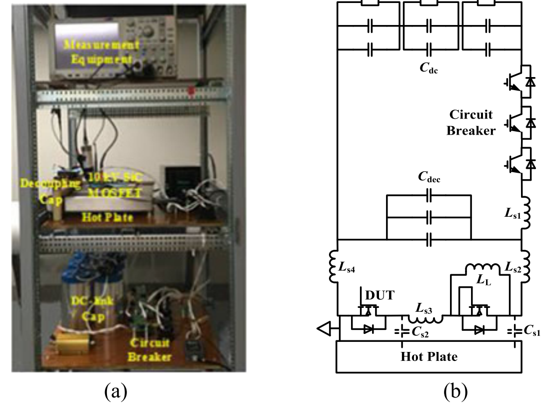

Fig. 7. DPT platform. (a) Picture of DPT platform. (b) Schematic of DPT platform.

C_s, which is the capacitance between the drain and the hotplate, can be calculated through

$$C_s = \frac{\varepsilon_t A_{\mathrm{drain}}}{d_t} \tag{9}$$

where A_{drain} is the copper area of the drain. ϵ_t and d_t are the permittivity and thickness of the insulated thermal pad between the drain and the hotplate. C_s is around 100 pF here.

III. Switching Characterization and Discussion

A. DPT Platform

The DPT platform is built to test the switching performance of HV SiC MOSFETs, as shown in Fig. 7. The key subcomponents with detailed descriptions are highlighted as follows.

The dc-link capacitor C_{dc} which consists of 4-kV capacitors in series connection is charged by a 15-kV dc power supply. C_{dc} is selected as 47 μF. The dc-link voltage is adjustable from 0 to 7 kV for the test of a 10-kV MOSFET. The parasitic inductances

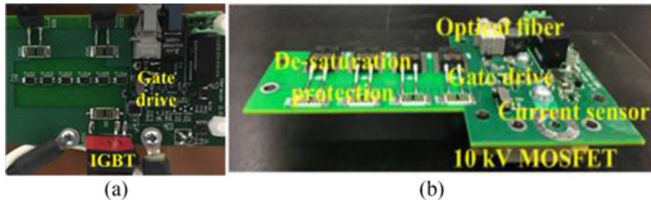

Fig. 8. Circuit breaker and gate driver of the 10-kV MOSFET. (a) Circuit breaker. (b) Gate driver of the 10-kV MOSFET.

and capacitances ($L_{s1} - L_{s4}$, C_{s1}, and C_{s2}) should be considered in the analysis of switching performance. The decoupling capacitor $C_{\rm dec}$ is applied to suppress the overvoltage caused by L_{s1} with the capacitance of 21 nF.

Two 10-kV/20-A MOSFETs are employed in the phase-leg configuration, where the lower switch is the device under test and the upper switch remains in off state during the pulse testing and its antiparallel diode is utilized as the freewheeling diode.

The junction temperature of the MOSFETs T_j in the phase leg can be adjusted from room temperature to 125 °C by a hotplate beneath them. A thermal pad is used to achieve the electrical isolation between the MOSFET and the hotplate. Due to the thermal pad, there is a temperature difference of several degrees Celsius between the MOSFET and the hotplate. The temperature difference can be obtained by an offline test. The source of the lower switch in the phase leg and the hotplate case is grounded.

The circuit breaker, as shown in Fig. 8(a), with three 4-kV Si IGBTs in series connection is used to limit the maximum current in the power stage when a short circuit happens [41]. The designed gate driver of 10-kV MOSFET is shown in Fig. 8(b). The power of the gate driver is supplied by a 10-kV insulated dc/dc power supply (ISO5125). The control signal and feedback signal are transmitted through optical fibers (AFBR-1624 and AFBR-2624) in order to achieve electrical isolation with less noise interference. AFBR-1624 and AFBR-2624, with a data rate of 50 MBd, have a propagation delay less than 30 ns. The positive and negative gate driver voltages are +15 and −5 V, respectively. The parasitic inductance in the gate driver loop is minimized by placing the gate driver board close to the MOSFET. A current sensor based on the Rogowski coil is designed to achieve overcurrent protection. The desaturation protection is also applied on the gate driver of the 10-kV MOSFET [42]. The details of the protection scheme will not be discussed in this paper.

The measurement setup is important and also a challenge for HV SiC MOSFET switching performance test. In probe selection, v_{DS} can be measured with HV passive probe (e.g., Tektronix P6015A) or differential probe (e.g., CIC research DP20-20K). The bandwidth of the commercial HV probe is lower than 100 MHz. Due to the high *dv/dt* during switching transients, the research of HV probe with a higher bandwidth (>100 MHz) is attractive. v_{gS} can be measured with LV probe (e.g., Tektronix TPP1000) in nonisolated conditions. Tektronix also has isolated voltage probe using fiber optics technique. With this probe, v_{gS} of upper device can be tested, but the price of the probe is extremely high. The bandwidth of the probes for v_{gS} is higher than 1 GHz which is already enough for DPT. The current can

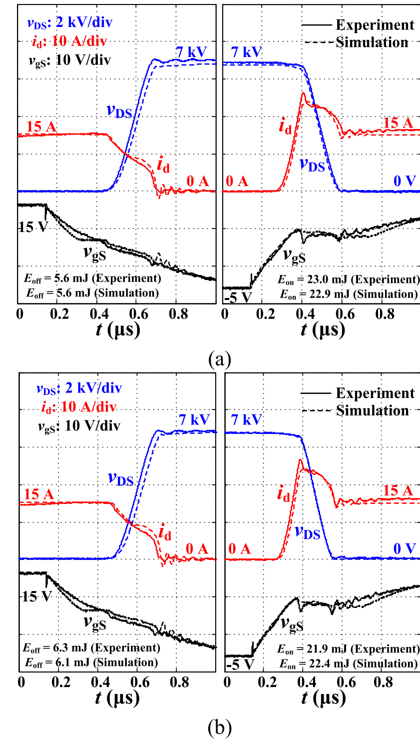

Fig. 9. Simulated switching waveforms comparison with experimental results ($R_{\rm goff} = R_{\rm gon} = 50\,\Omega$). (a) $T_j = 25\,°$C. (b) $T_j = 125\,°$C.

be tested by coaxial shunt (e.g., SSDN-10), current probe (e.g., Tektronix TCP0030A), or Rogowski coil (e.g., CWT ultramini). The coaxial shunt has the highest bandwidth but is connected into the power stage. The current probe and Rogowski coil have lower bandwidth but isolated with the power stage. Commonly, the bandwidth for the current test should be higher than 100 MHz. The probes should be placed properly to avoid the noise during switching transients. The common-mode current flows through the probe and oscilloscope. The current will generate a nonnegligible voltage drop on the stray inductance of the probe cable. Therefore, the stray inductance of the probe cable should be minimized by decreasing the area of the measurement loop. The high *dv/dt* easily causes noise in some kinds of probes such as Rogowski coil. Therefore, the Rogowski coil can only measure the current through wires with a low *dv/dt*.

B. Waveforms During Switching Transients

The switching transient waveforms are tested by the DPT platform at 7-kV dc-link voltage and from 5- to 20-A load current. The drain-to-source voltage is measured by the HV probe Tek P6015A and the current is measured by the current probe Tek TCP0030A. The turn-on external gate resistance changes from 15 to 50 Ω, while the turn-off external gate resistance changes from 3 to 50 Ω. The switching waveforms are tested from 25 to 125 °C with a 25 °C step. Fig. 9 shows the comparison between simulated and experimental waveforms during the switching transient at 25 and 125 °C with $R_{\rm goff} = R_{\rm gon} = 50\ \Omega$. Fig. 10 shows the comparison with $R_{\rm goff} = 3\,\Omega$ and $R_{\rm gon} = 15\,\Omega$. The simulations match well with the experimental waveforms. The

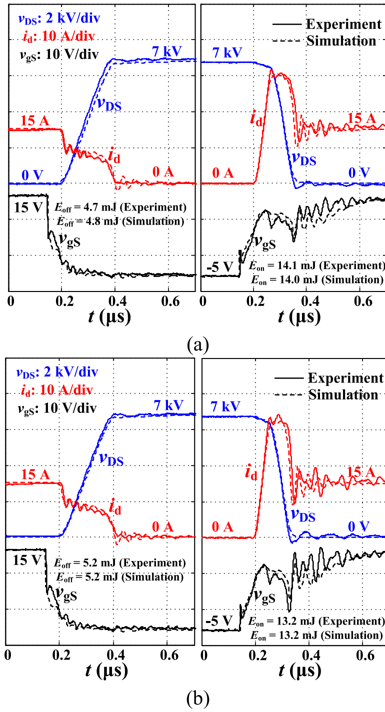

Fig. 10. Simulated switching waveforms comparison with experimental results ($R_{goff} = 3\,\Omega$ and $R_{gon} = 15\,\Omega$). (a) $T_j = 25\,°C$. (b) $T_j = 125\,°C$.

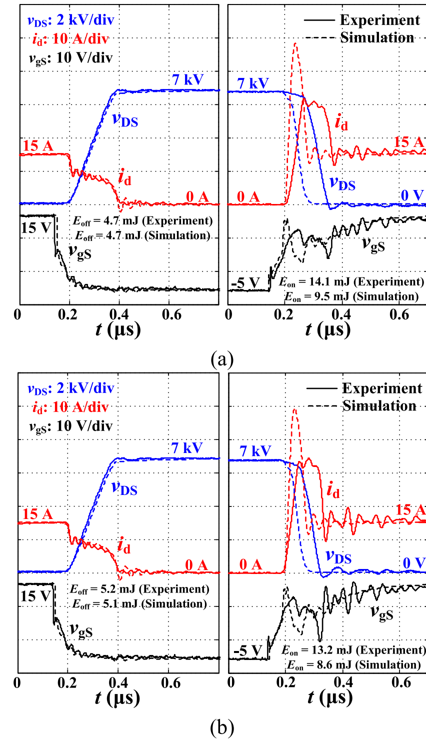

Fig. 11. Simulated switching waveforms using previous model comparison with experimental results ($R_{goff} = 3\,\Omega$ and $R_{gon} = 15\,\Omega$). (a) $T_j = 25\,°C$. (b) $T_j = 125\,°C$.

dv/dt and switching loss are two typical parameters to describe switching performance. The comparisons between the simulated and experimental results of these parameters are shown in Figs. 12 and 13. The simulated *dv/dt* and switching loss have a good agreement with experimental results.

The comparison between simulation results using previous model and experimental waveforms is shown in Fig. 11. In the previous model, the MOSFET channel current is considered to change with v_{ds} during switching transients when MOSFETs operate in the active region and the gate-to-drain capacitance is modeled with $M = 1/2$ which have been discussed in Section II. It can be seen that the simulation results using previous model is not accurate to describe the turn-on performance. There are obvious differences in *dv/dt* (117.2 V/ns in simulation and 81 V/ns in experiment at 25 °C) and turn-on loss (9.5 mJ in simulation and 14.1 mJ in experiment and at 25 °C).

C. Switching Loss

With a high turn-off gate resistance R_{goff} (e.g., $R_{goff} = 50\,\Omega$), the switching loss during the turn-off transient E_{off} slightly increases with elevating junction temperature T_j and increasing load current i_L. However, when R_{goff} decreases to a small value (lower than 20 Ω in this case), E_{off} is nearly constant and equals the energy stored in the parasitic capacitors of the MOSFET, indicating that most of the MOSFET's current during the turn-off transient flows through the parasitic capacitors rather than the MOSFET channel. The energy stored in the parasitic capacitors can be calculated by

$$E_{\text{off}} = \int_0^{v_{dc}} (C_s + C_{ds}(v))v\,dv. \tag{10}$$

The calculated result is 4.63 mJ at 7-kV dc-link voltage which is very similar with the simulation result 4.8 mJ. 4.8 mJ is also the minimum E_{off} of this platform.

The switching loss during the turn-on transient E_{on} is highly impacted by i_L and R_{gon}. When $i_L = 20\,\text{A}$, E_{on} decreases from 29.2 mJ with $R_{gon} = 50\,\Omega$ to 17 mJ with $R_{gon} = 15\,\Omega$. E_{on} can be further decreased by reducing R_{gon}. The impact of T_j on E_{on} can be neglected. The 10-kV MOSFET has very good temperature-independent performance in terms of the switching loss.

D. dv/dt

Because most of the MOSFET's current during the turn-off transient charges the parasitic capacitors, the impact of T_j on *dv/dt* during the turn-off transient can be neglected. The *dv/dt* slightly increases with decreasing R_{goff} (only from 36.3 V/ns with $R_{goff} = 50\,\Omega$ to 50 V/ns with $R_{goff} = 3\,\Omega$). When R_{goff} reduce to a small value (smaller than 20 Ω), the *dv/dt* is mainly decided by i_L and nearly independent from R_{goff}

$$(C_{\text{upper}} + C_{\text{lower}})\frac{dv}{dt} = i_L \tag{11}$$

where C_{upper} and C_{lower} are the parasitic capacitances of upper and lower devices

$$C_{\text{upper}} = C_s + \frac{C_{dsb}}{\sqrt{v_{\text{dc}} - v}},\ C_{\text{lower}} = C_s + \frac{C_{dsb}}{\sqrt{v}}. \tag{12}$$

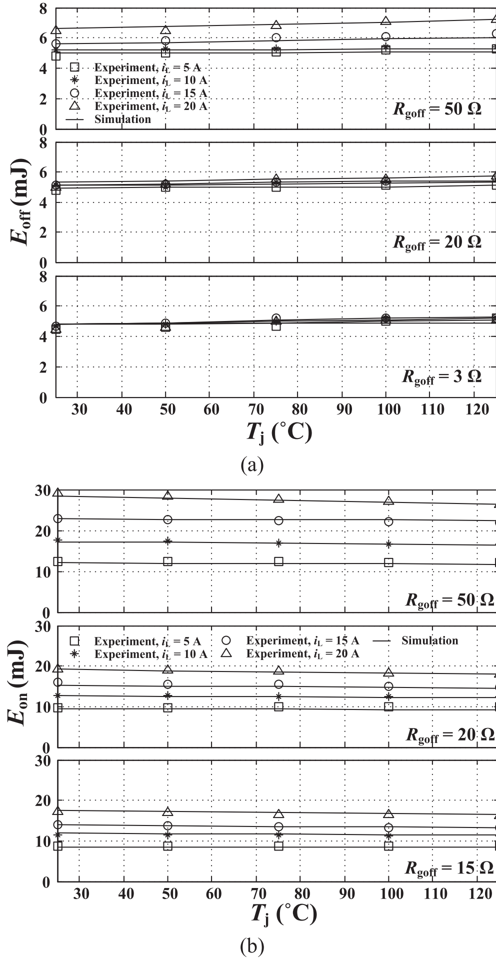

Fig. 12. Simulated switching loss comparison with experimental results. (a) During turn-off transient. (b) During turn-on transient.

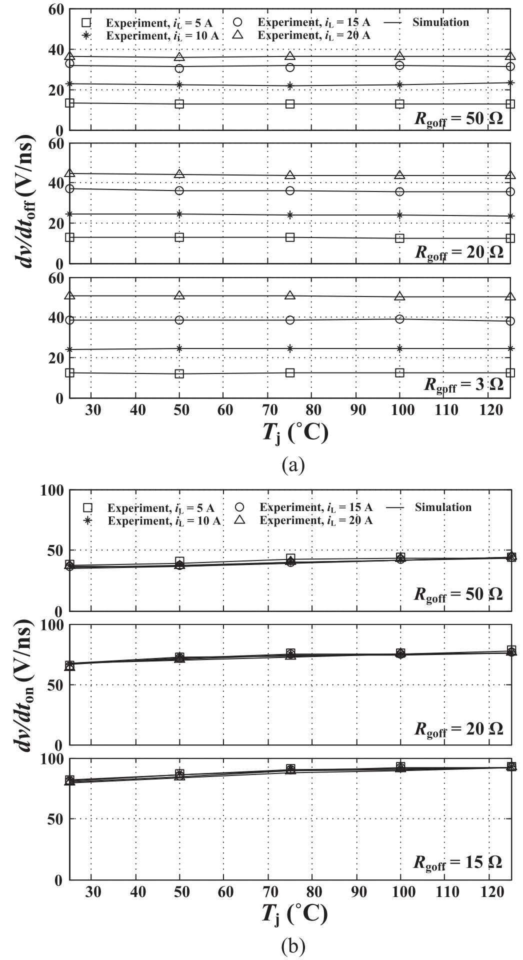

Fig. 13. Simulated *dv/dt* comparison with experimental results. (a) During turn-off transient. (b) During turn-on transient.

The rise time from 10% v_{dc} to 90% v_{dc} can be represented as

$$t_r = \frac{2.53C_{dsb}\sqrt{v_{\mathrm{dc}}} + 1.6C_s v_{\mathrm{dc}}}{i_{\mathrm{L}}}. \tag{13}$$

The calculation *dv/dt* is 49 V/ns at 20-A load current and 7-kV dc-link voltage which is close to the experimental result 50 V/ns. This is the maximum *dv/dt* of this platform during the turn-off transient.

The *dv/dt* during the turn-on transient is mainly decided by $R_{g\mathrm{on}}$ and nearly independent from the load current. It increases from 44 V/ns with $R_{g\mathrm{on}} = 50\,\Omega$ to 82 V/ns with $R_{g\mathrm{on}} = 15\,\Omega$. The *dv/dt* also slightly increases with higher T_j (e.g., increasing from 82 V/ns at 25 °C to 93 V/ns at 125 °C when $R_{g\mathrm{on}} = 15\,\Omega$). i_{ch} plays a major role during the turn-on transient. The current difference between the MOSFET and the load $i_d - i_L$ will charge the parasitic capacitance $C_{ds} + C_s$ of the upper bridge device. *dv/dt* can be described by

$$\frac{dv}{dt} = \frac{i_d - i_L}{C_s + C_{ds}} \tag{14}$$

dv/dt increases with elevating T_j due to the increase of i_d. The *dv/dt* during the turn-on transient can further increase through reducing $R_{g\mathrm{on}}$. Because *dv/dt* increases with increasing T_j, the simulation and experimental results at 125 °C will be used to analyze the switching speed limitation in the next section. It can be seen that the model is accurate enough to predict the switching performance from Figs. 12 and 13, and can be used in the analysis of switching speed.

E. Comparison With Previous 10-kV MOSFET

A comprehensive comparison with previous device is shown in Table I. 10-kV/5-A SiC MOSFET (M1) [12] and 10-kV/10-A SiC MOSFET (M2) [43] are used as two examples to compare with the device in this paper (M3). Four pieces of M1 and two pieces of M2 MOSFETs are assumed in parallel connection to achieve a 20-A MOSFET. The active area of the third-generation MOSFET is smaller than the previous device. So the MOSFET shows a higher $R_{ds\mathrm{on}}$ but a much lower parasitic capacitance, resulting in benefit in the switching loss but disadvantage in the conduction loss. The power loss using the three MOSFETs in a two-level converter is also estimated. The dc-link voltage of the converter is 6 kV and maximum current in ac output is 20 A. The modulation index and power factor are both 1. The device

TABLE I
COMPARISON OF SEVERAL GENERATIONS OF 10-KV/20-A MOSFETS

	Specific on resistance (mΩ·cm^2)	Active area (mm^2)	C_{ds} at 1 kV (pF/mm^2)	Power loss in 2L converter at 20 kHz (W)
M1	122	60.9	5.26	30 (CON) 77 (SW)
M2	111	66.0	5.45	24 (CON) 81 (SW)
M3	95	27.5	5.93	51 (CON) 40 (SW)

is assumed to operate at 75 °C. It can be seen that the switching loss with the latest MOSFET is much lower than that with the previous devices. The total loss is also saved 16 W (17.6%) and 14 W (15.4%). With the increase of the switching frequency, the latest MOSFET will show more attractive performance. Furthermore, the latest 10-kV/20-A MOSFET can be achieved in a single chip rather than several chips in parallel connection. It will improve the reliability to use 10-kV MOSFET in converters with higher power rating. Commonly, the specific on-resistance is a convincing parameter to show the device performance. The device with lower specific on-resistance shows a better comprehensive performance. The value of third-generation MOSFET is only 95 m$\Omega \cdot$ cm^2 which is 28.4% less than the previous device.

IV. SWITCHING SPEED DISCUSSION

The proper switching speed of the 10-kV SiC MOSFET will be studied in this section. The impact factors, which limit the switching performance, include: 1) the reverse recovery of SiC MOSFET's body diode, 2) the overvoltage caused by stray inductances, 3) interference of the lower and upper devices in a phase-leg configuration (i.e., crosstalk), 4) heat sink, and 5) EMI to the control. As discussed above, the reverse recovery of the body diode can be neglected. The overvoltage happens in two situations. The lower device withstands the overvoltage during its turn-off transient while the upper device withstands the overvoltage during the turn-on transient of the lower device. With the decoupling capacitor, both of them are smaller than 300 V even though $R_{\text{gon}} = 15\ \Omega$ and $R_{\text{goff}} = 3\ \Omega$. Due to a high breakdown voltage of the HV SiC MOSFET (e.g., at least 12 kV for the 10-kV SiC MOSFET), the overvoltage is not a strict limitation for the switching speed. Therefore, the crosstalk issue, the heat sink, and the EMI effect on the control are discussed in this section.

A. Crosstalk

With increasing *dv/dt* during lower device's turn-on transient, v_{gs} of upper device may be charged higher than the gate threshold voltage through its miller capacitance C_{gd}. This positive spurious gate voltage may generate a shoot-through current, flowing from the upper device to the lower one. The conducted current and turn-on loss of the lower device will increase due to the shoot-through current. Therefore, if crosstalk happens, the switching performance becomes worse with increasing *dv/dt*. In order to further increase *dv/dt* and reduce the turn-on loss, an anticrosstalk circuit will be critical in the gate driver. Similarly, during the turn-off transient, a negative spurious gate voltage would be induced, leading to degradation of the

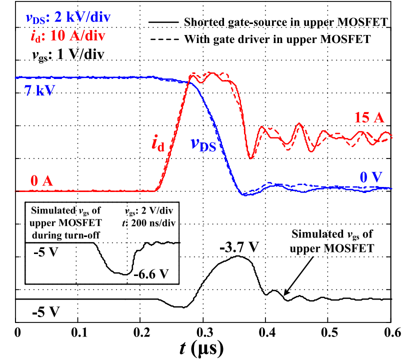

Fig. 14. Experimental and simulation results of crosstalk.

upper switch if its magnitude exceeds the maximum allowable negative-biased gate voltage acceptable to the semiconductor device itself. Therefore, the crosstalk issue may be a limitation for the switching speed both during the turn-on and turn-off transients, and its impact should be estimated.

The previous experimental results in last section are tested with a shorted gate source for the upper device. There is no crosstalk issue in this case. By using a gate driver for the upper device, the experimental results of i_d and v_{DS} when $R_{\text{gon}} = 15\ \Omega$ and $R_{\text{goff}} = 3\ \Omega$ are compared with that shorting gate terminal with source terminal in Fig. 14. The MOSFET currents during the turn-on transient in the two cases are very close and the turn-on losses are both 17 mJ. It is difficult to measure the v_{gS} of the upper device, because the HV differential probe is not accurate enough to measure LV signals. The v_{gs} of the upper device is obtained through simulation. Based on the model, the maximum v_{gs} of the upper device during the turn-on transient is only -3.7 V which is far lower than the gate threshold voltage 2.85 V. During the turn-off transient, the minimum v_{gs} of the upper device is -6.6 V which is much higher than the maximum allowable negative-biased gate voltage -10 V. Therefore, the crosstalk will not happen both during the turn-on and turn-off transients with a turn-on gate resistance of 15 Ω and a turn-off gate resistance of 3 Ω. By assuming that all the current flowing though the miller capacitor of the upper device charges its gate-to-source capacitor, the maximum gate voltage change in the upper device caused by interference of the lower device can be calculated by

$$\Delta v_{gs} = \frac{\int_0^{v_{dc}} C_{gd} dv}{C_{gs}}. \tag{15}$$

The calculated maximum Δv_{gs} is 5 V. Therefore, even though with smaller R_{gon} and R_{goff}, the crosstalk will also not happen. The crosstalk issue is not a limitation for the switching speed of

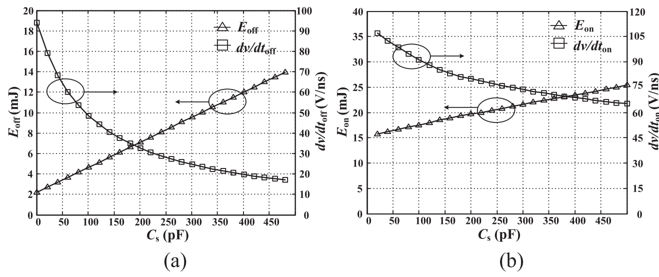

Fig. 15. Simulated *dv/dt* and switching loss with various C_s. (a) During turn-off transient. (b) During turn-on transient.

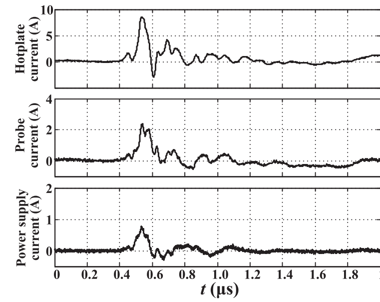

Fig. 16. Interference currents of hotplate, probe, and gate driver power supply.

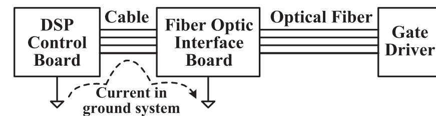

Fig. 17. Control system of the platform.

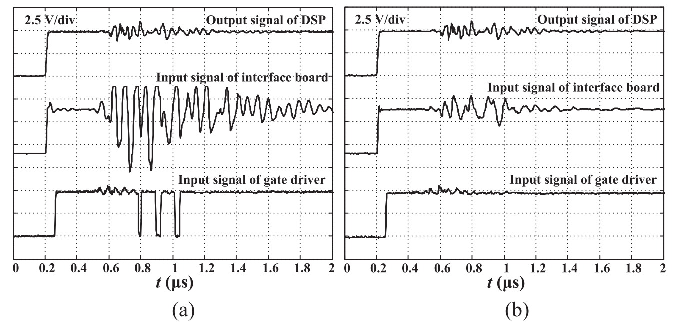

Fig. 18. Interference in control system. (a) 800-mm cable. (b) 100-mm cable.

the 10-kV SiC MOSFET due to its high ratio between gate-to-source capacitance and gate-to-drain capacitance.

B. Heat Sink

With the decrease of R_{goff}, the switching speed during the turn-off transient is mainly decided by the MOSFET's parasitic capacitance. A proper R_{goff} should be selected based on the maximum current of the gate driver buffer. Equations (10) and (13) show the capacitance between the MOSFET and heat sink C_s has a high impact on *dv/dt* and E_{off}. The simulated *dv/dt* and E_{off} at 7-kV dc-link voltage with various C_s are given in Fig. 15(a). E_{off} has an increase rate of 24.5 μJ/pF. The parasitic capacitance of the heat sink is a critical factor for the turn-off performance.

During the turn-on transient, the increasing C_s will also cause the decrease of *dv/dt*, leading to a higher switching loss. The simulated *dv/dt* and E_{on} are shown in Fig. 15(b). The increase rate of E_{on} is about 20 μJ/pF. A smaller C_s is also attractive during the turn-on transient. However, the impact of C_s on the turn-on performance is not as large as R_{gon}. The switching speed can be faster by reducing R_{gon}.

C_s is highly affected by device's package. As shown in Fig. 1, C_s of the 10-kV SiC MOSFET is mainly induced by a large area copper plate of the drain. The calculation of C_s in this case is given in (9).

C. EMI Effect on the Control

The high *dv/dt* during the switching transient induces a large common-mode interference current in the ground system of the platform, leading to disturbance in the control circuit. The common-mode interference current in this platform mainly has three paths, including MOSFET-hotplate capacitors, probes, and isolated power supplies of the gate driver. The currents through these three paths are measured by the current probe through power cords of the hotplate, oscilloscope, and gate driver power supply. The Tektronix current probe (TCP0030A) with 120-MHz bandwidth is applied. The currents through these paths during the turn-on transient with $R_{\mathrm{gon}} = 15\,\Omega$ at 7-kV dc-link voltage are tested and shown in Fig. 16. The interference current through the ground system can reach several amperes.

The control circuit of the platform is shown in Fig. 17. Control signals are generated by a DSP control board and changed into optical signals in a fiber optic interface board. The gate driver receives the optical signal from the interface board through optical fibers. The optical fibers achieve very good electrical isolation between the gate driver (HV side) and the interface board (LV side). The interface board and the DSP control board communicate through an electric cable. If the current, which flows through the ground loop of the DSP control board and the interface board, brings a significant voltage drop on the cable, the output signal of the DSP control board and the input signal of the interface board will have a large difference. Even though chokes are applied for the power supplies of the control board and interface board, the interference current in the ground system is not negligible. The control signals tested with an 800-mm electric cable are shown in Fig. 18(a). There is an obvious oscillation at the input signal of the interface board, leading to the incorrect operation at the input signal of the gate driver.

There are two ways to solve this problem. A capacitor can be placed at the input of the gate driver IC. However, in order to eliminate the interference in Fig. 18(a), the capacitance should be around several nanofarads which will cause severe gate delay. Another way is to minimize the cable length. By using a minimized cable with its length shorter than 100 mm, the incorrect operation at the input signal of the gate driver can be avoided, as shown in Fig. 18(b), but it can be seen that the oscillation at the input signal of the interface board still exists. With

increasing *dv/dt*, the incorrect operation signal will reappear at the input of the gate driver. Considering there are more paths of the common-mode current in a converter than in a DPT platform and more complex circuit in the control side which will include other sensors as well, the EMI to the control will be a challenge and a critical limitation for the switching speed.

V. Conclusion

The temperature-dependent characterization of the third-generation 10-kV SiC MOSFET both in steady state and during switching transients has been introduced in detail. A behavior model with its parameter extraction method is presented to describe the device's static and switching performance. The temperature-dependent factors are considered in each part. Based on the model, the switching speed limitations including the reverse recovery of SiC MOSFET's body diode, the overvoltage caused by stray inductances, crosstalk, heat sink, and EMI to the control are discussed. The turn-off performance is mainly limited by the parasitic capacitance of the heat sink. With a parasitic capacitance of 100 pF in this platform, the maximum *dv/dt* during the turn-off transient can reach 50 V/ns with a minimum turn-off loss of 4.8 mJ. For the turn-on performance, the EMI effect on the control is the critical limitation. In this platform, the maximum *dv/dt* during the turn-on transient is 93 V/ns, while the turn-on loss is 17 mJ with a turn-on gate resistance of 15 Ω.

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