Switched-Capacitor-Based Dual-Switch High-Boost DC–DC Converter

Minh-Khai Nguyen, *Member, IEEE*, Truong-Duy Duong, and Young-Cheol Lim, *Member, IEEE*

***Abstract*—A switched-capacitor-based dual-switch dc–dc converter with a high-boost voltage gain is proposed in this paper. The proposed converter can obtain a high-voltage gain with a small duty cycle, which decreases the voltage stress and the conduction loss on the power switches. This paper presents the key waveforms, the operating principles at the continuous conduction mode and the discontinuous conduction mode, and the parameter design. Moreover, a comparison between the proposed converter and other nonisolated converters has been completed. To verify the operating principle, a 200 W prototype is constructed with an input voltage of 25–50 V and an output voltage of 200 V. The simulation and experimental results are shown.**

***Index Terms*—Boost converter, continuous conduction mode (CCM), discontinuous conduction mode (DCM), dual-switch, high-voltage gain, nonisolated dc–dc converter, switched capacitor (SC).**

I. Introduction

BECAUSE of the depletion of the global fossil-energy sources, the development of renewable energy is the most-effective solution. However, the available renewable energies such as wind, solar, and fuel cells are reliant on the weather conditions, and their output voltages are low and variable. To connect them to the residential loads, the two-stage power-conversion system that is shown in Fig. 1 is widely used. In the first stage, a high-step-up dc–dc converter is used to convert a low voltage into a constant dc-bus voltage [1], [2]. Many high-step-up dc–dc converters have been proposed and investigated to obtain a high-voltage gain in both isolated and nonisolated topologies. For the isolated topologies [3], [4], a high-frequency transformer is used to insulate the input and the output with a two-stage dc–ac–dc power conversion. For the nonisolated topologies, various high-step-up dc–dc converters with and without a coupled inductor have been proposed in [5]–[25]. The coupled-inductor-based high-step-up converters are proposed in [5]–[9] to increase the voltage gain; however, the leakage inductance of the coupled inductor is a negative impact of the coupled-inductor-based converters. The non-coupled-inductor converters can achieve a high-voltage gain with a high efficiency and a high-power density because they lack magnetic components. The focus of the research studies of the noncoupled-inductor converters are the voltage-lift [10], cascaded [11]–[13], and interleaved [14], [15] techniques. Voltage-multiplier cells [16], a switched-inductor (SL), a switched-capacitor (SC) [17]–[21], and an active-switch network [22]–[25] have been used in other studies to provide a high boost to transformerless structures. Based on the SC converter and in combination with the switching mode, the converter in [19] can increase the voltage gain with two switches. An SC-based high-step-up voltage-gain active-network converter (ANC) with a low-voltage stress on the switches and diodes is proposed in [24].

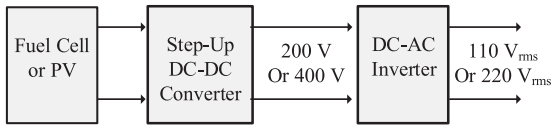

Fig. 1. Typical two-stage power-conversion system.

However, in the boost-based nonisolated dc–dc converters [5]–[25], the duty cycle is varied within a wider region of 0 to 1. When a high-step-up voltage gain is required, a larger duty cycle should be used. The use of a larger duty cycle results in a high conduction loss on the switches. To reduce the duty cycle of a switch in the range of [0, 0.5), a *Z*-source converter (ZSC) is proposed in [26] with a discontinuous-input current. A family of quasi-*Z*-source dc–dc converters is presented in [27] to improve the input-current profile. By changing the way the output is connected to the *Z*-source network, a common-grounded *Z*-source dc–dc converter (CG-ZSC) [28] can achieve a higher voltage gain in comparison with the traditional ZSC. In [29], three *Z* networks are used to achieve a high-step-up voltage. The use of a large number of passive components in the *Z*-network-based boost dc–dc converters [26]–[29], however, increases the size, weight, cost, and loss. A *Y*-source dc–dc converter is proposed in [30] to achieve a high-step-up voltage with a coupled inductor. Owing to the leakage inductance of the coupled inductor, a voltage spike appears on the switch.

This paper proposes an SC-based dual-switch high-boost dc–dc converter. The main features of the proposed converter are as follows: simple structure, high-step-up voltage- conversion ratio, using the small duty cycle for the reduction of the conduction loss on the power switches, and a low voltage stress on the MOSFETs and diodes. Section II proposes the converter topology with continuous conduction mode

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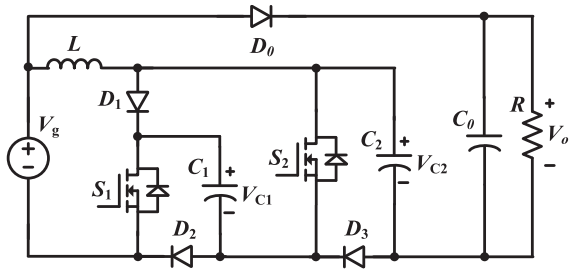


Fig. 2. Proposed SCDS converter.

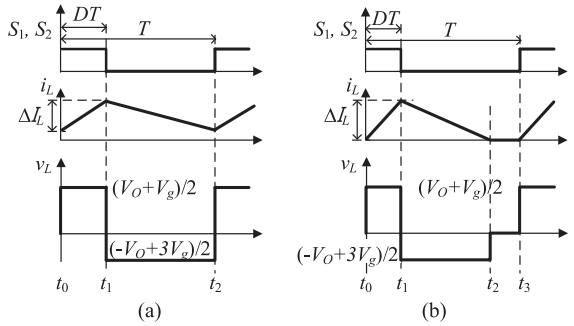


Fig. 3. Key waveforms of the proposed converter: (a) CCM and (b) DCM.

(CCM)- and discontinuous conduction mode (DCM)-circuit analyses. The parameter-design guideline is presented in Section III. Then, the proposed converter is compared with other nonisolated high-boost dc–dc converters in Section IV. Finally, the simulation and experimental results are shown in Section V.

II. Proposed Converter

Fig. 2 shows the proposed SC-based dual-switch (SCDS) converter with the high-voltage gain. It consists of one inductor (L), three capacitors ($C_0 - C_2$), four power diodes (D_0–D_3), two power switches (S_1 and S_2), and a resistive load (R). Fig. 3 shows the key waveforms of the proposed SCDS converter operating in the CCM and the DCM. Both switches, S_1 and S_2, are turned on and off simultaneously. To simplify the circuit analyses of the proposed converter in the CCM and the DCM, the following assumptions were made: 1) all devices are ideal and lossless; 2) the capacitance of the capacitors is large enough to maintain the constant capacitor voltage; and 3) the current flow to the inductor increases or decreases linearly.

A. Circuit Analysis in the CCM

Fig. 3(a) shows the key waveforms of the proposed converter in the CCM. Fig. 4(a) and (b) shows the operating modes of the proposed converter in the CCM.

Mode 1 [t_0–t_1, Fig. 4(a)]: S_1 and S_2 are turned "ON." The inductor is charged while the C_1 and C_2 capacitors are discharged. The D_0 diode is forward-biased, while the D_1, D_2, and D_3 diodes are reverse-biased. The time interval in this mode is $D{\cdot}T$, where D and T are the duty cycle and the switching period, respectively. By applying Kirchhoff's voltage law in Fig. 4(a), the following formula is derived:

$$\begin{cases} L\dfrac{di_L}{dt} = V_g + V_{C1} \\ V_o = V_g + V_{C1} + V_{C2}. \end{cases} \tag{1}$$

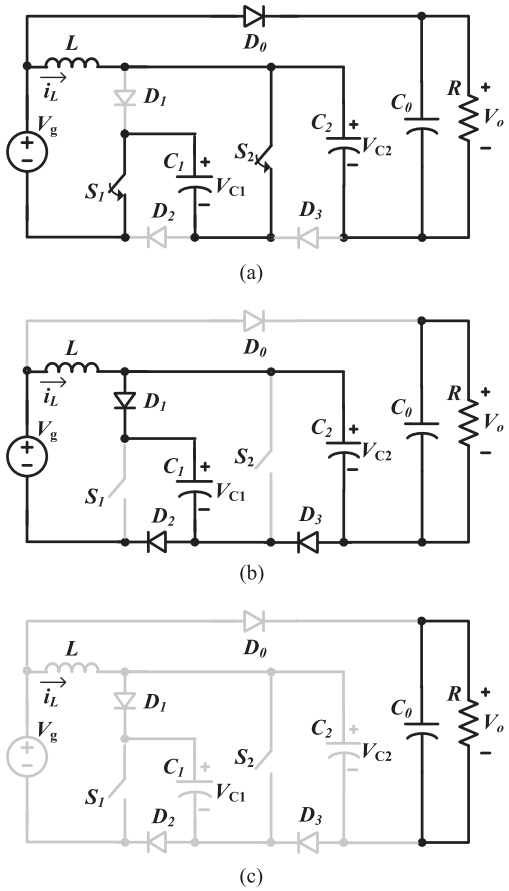


Fig. 4. Operating modes of the proposed converter: (a) mode 1, (b) mode 2, and (c) mode 3 in the DCM.

Mode 2 [t_1–t_2, Fig. 4(b)]: S_1 and S_2 are switched "OFF"; the D_1, D_2, and D_3 diodes are forward-biased while the D_0 diode is reverse-biased. The time interval in this mode is (1–D)·T. During this mode, the inductor L is discharged while the C_1 and C_2 capacitors are charged, and the following formula is derived:

$$\begin{cases} L\dfrac{di_L}{dt} = V_g - V_{C1} \\ V_{C1} = V_{C2}. \end{cases} \tag{2}$$

Through the application of the volt–second balance law to the inductor in a steady state, (1) to (2) yield the following equation:

$$V_{C1} = V_{C2} = \frac{1}{1 - 2D} V_g. \tag{3}$$

By substituting (3) into (1), the output-voltage gain of the proposed SCDS converter in the CCM is as follows:

$$G_{\mathrm{CCM}} = \frac{V_o}{V_g} = \frac{3 - 2D}{1 - 2D}. \tag{4}$$

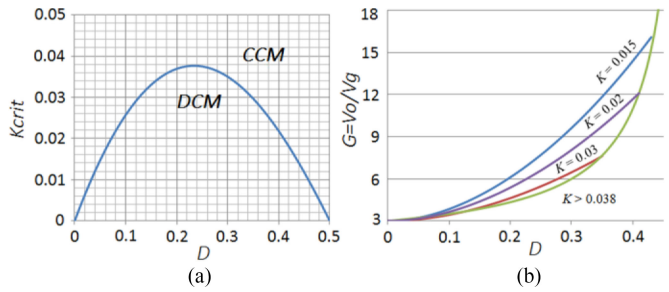


Fig. 5. (a) CCM/DCM boundary condition. (b) Relationship between the output voltage and the duty cycle.

B. Circuit Analysis in the DCM

The proposed converter works in the DCM when the light loads are used. This operating mode causes an overboost effect on the capacitor and the output voltages. Fig. 3(b) shows the key waveforms of the proposed converter in the DCM.

Mode 1 [t_0–t_1, Fig. 4(a)]*:* This mode is the same as mode 1 in the CCM. From (1), the peak-to-peak value of the inductor current in mode 1 is as follows:

$$\Delta I_L = \frac{V_g + V_{C1}}{L} DT. \tag{5}$$

Mode 2 [t_1–t_2]: The equivalent circuit in this mode in the DCM is shown in Fig. 4(b). The time interval in this mode is $D_x \cdot T$. The inductor voltage is calculated using (2). Mode 2 in the DCM ends when the inductor current is reduced to zero.

Mode 3 [$t_2 - t_3$, Fig. 4(d)]*:* S_1 and S_2 are still switched "OFF," and the inductor current is zero. The energy stored in the C_0 capacitor is released to the load. The inductor voltage in this mode is zero.

If the assumption of a no-loss power circuit is made, the average input current is as follows:

$$\overline{I}_{\text{in}} = \frac{P_o}{V_g} = \frac{V_o^2}{RV_g} \tag{6}$$

where P_o and R are the output power and the resistor load, respectively.

Because the average current of the capacitor C_0 is zero, the average current of the diode D_0 equals the output current. If KCL is applied at node A in Fig. 2, the average inductor current is as follows:

$$\bar{I}_L = \bar{I}_{\text{in}} - \bar{I}_o = \frac{V_o^2}{V_g R} - \frac{V_O}{R}. \tag{7}$$

The DCM occurs with the following condition:

$$\overline{I}_L < \Delta I_L/2. \tag{8}$$

The result of the substitution of (5) and (7) into (8) is as follows:

$$K < K_{\text{crit}}(D) \tag{9}$$

where $K = 2L/(RT)$ and $K_{\text{crit}}(D) = D \cdot (1 - D) \cdot (1 - 2D)/(3 - 2D)$.

Fig. 5(a) shows the plots of K_{crit} as a function of D at the CCM/DCM boundary. When $K > K_{\text{crit}}$, the converter operates in the CCM. When $K < K_{\text{crit}}$, the converter operates in the DCM.

From Fig. 3(b), the average inductor current is calculated as follows:

$$\overline{I}_L = \frac{1}{2T}\Delta I_L\,(D + D_x)\,T = \frac{V_g + V_{C1}}{2L} D\,(D + D_x)\,T. \tag{10}$$

The result of a steady-state application of the volt–second balance law to the inductor in the DCM is as follows:

$$D_x = \frac{D\,(V_{C1} + V_g)}{V_{C1} - V_g}. \tag{11}$$

From (7), (10), and (11), the output-voltage gain in the DCM is calculated as follows:

$$G_{\text{DCM}} = \frac{V_o}{V_g} = \frac{3}{2} + \frac{D^2}{2K} + \frac{1}{2}\sqrt{\left(3 + \frac{D^2}{K}\right)^2 + \frac{D^2}{K}}. \tag{12}$$

Fig. 5(b) shows the relationship between the output-voltage gain and the duty cycle. The output-voltage gain in the DCM is higher than that in the CCM. When the $K > 0.038$, the converter operates in the CCM.

III. Parameter-Design Guideline

A. Voltage and Current Stress on the Switches

The voltage stress on the switches is shown in Table I. The peak current value on both of the switches is calculated in the CCM as follows. As shown in Fig. 4(a) and (b), the input current is the switch current (I_{S_P}) in mode 1, while it equals the inductor current in mode 2; therefore, the average input current is as follows:

$$\overline{I}_{\text{in}} = \frac{P_o}{V_g} = DI_{S\_P} + (1 - D)I_L. \tag{13}$$

The substitution of (7) into (13) means that the peak current of the switches S_1 and S_2 is as follows:

$$I_{S\_P} = \frac{P_o}{D(3 - 2D)V_g}. \tag{14}$$

The root-mean-square (RMS) current of the switches S_1 and S_2 is as follows:

$$I_{S\_\text{RMS}} = \frac{P_o}{\sqrt{D}(3 - 2D)V_g}. \tag{15}$$

B. Voltage and Current Stresses on the Diodes

The voltage stress on the diodes is listed in Table I. Based on mode 2, as shown in Fig. 4(b), the peak current of the diodes D_1–D_3 is calculated as follows:

$$\begin{cases} I_{D1\_P} = I_{D3\_P} = 0.5I_L \\ I_{D2\_P} = I_L \end{cases} \tag{16}$$

where the I_L is calculated in (7). Based on mode 1, as shown in Fig. 4(a), the peak current of the diode D_0 is calculated as follows:

$$I_{D0\_P} = I_{S\_P} - I_L. \tag{17}$$

TABLE I
COMPARISON BETWEEN THE PROPOSED CONVERTER AND OTHER HIGH-BOOST DC–DC CONVERTERS

	IBC [14]	DIESC-SC [19]	SC-ANC [24]	ZSC [26]	CG-ZSC [28]	Proposed converter
Inductors	2	2	2	2	2	1
Capacitors	3	5	3	3	3	3
Diodes	4	4	3	2	2	4
Switches	2	1	2	1	1	2
Switched voltage, V_s	$V_o/2$	$V_o/(2+D)$	$(V_g+V_o)/4$	V_o	V_o-V_g	$(V_o-V_g)/2$
Diode voltage in SL or SC cell	V_o	$V_o/(2+D)$	$(V_o-V_g)/4$ & V_g	V_o	V_o-V_g	$(V_o-V_g)/2$
Output-diode voltage, V_{Do}	$V_o/2$	$V_o/(2+D)$	$(V_g+V_o)/2$	V_o	V_o-V_g	V_o-V_g
Capacitor voltage, V_C	$V_o/2$	$V_o/(2+D)$	$(V_g-V_o)/2$ & $(V_g+V_o)/2$	$(V_g+V_o)/2$	$V_o/2$	$(V_o-V_g)/2$
Voltage gain, G	$2/(1-D)$	$(2+D)/(1-D)$	$(3+D)/(1-D)$	$1/(1-2D)$	$2(1-D)/(1-2D)$	$(3-2D)/(1-2D)$
Input current	*Continuous*	*Continuous*	*Continuous*	*Discontinuous*	*Discontinuous*	*Continuous*
Input-current ripple	*Low*	*High*	*High*	*High*	*High*	*Low*

The RMS current of the diodes is as follows:

$$\begin{cases} I_{D0\_\mathrm{RMS}} = \sqrt{D}\,(I_{S\_P} - I_L) \\ I_{D1\_\mathrm{RMS}} = I_{D3\_\mathrm{RMS}} = 0.5\sqrt{1-D}I_L \\ I_{D2\_\mathrm{RMS}} = \sqrt{1-D}I_L. \end{cases} \tag{18}$$

C. Inductor Selection

The peak-to-peak inductor current ΔI_L is calculated using (5). Assuming from (4), (5), and (7) that $\Delta I_L = r_i\%I_L$, the required inductance should be as follows:

$$L = \frac{D(1-D)(3-2D)TV_g^2}{r_i\%(1-2D)P_o}. \tag{19}$$

D. Capacitor Selection

The capacitors are designed according to the capacitor–voltage ripple. As shown in Fig. 4(a), the current flow to the C_1 capacitor in mode 1 of the proposed converter equals the peak current of the switch S_1, while the current flow to the C_2 capacitor equals the peak current of the diode D_0, and it can be rewritten as follows:

$$\begin{cases} C_1\dfrac{\Delta V_{c1}}{DT} = \dfrac{P_o}{D\,(3-2D)\,V_g} \\ C_2\dfrac{\Delta V_{c2}}{DT} = \dfrac{P_o}{D\,(3-2D)\,V_g} - I_L. \end{cases} \tag{20}$$

If the passing-through peak-to-peak capacitor–voltage ripple is limited by the $r_v\%$, the capacitances for C_1 and C_2 of the proposed converter should be as follows:

$$\begin{cases} C_1 = \dfrac{(1-2D)TP_o}{r_v\%(3-2D)V_g^2} \\ C_2 = \dfrac{(1-2D)^2TP_o}{r_v\%(3-2D)V_g^2}. \end{cases} \tag{21}$$

As shown in Fig. 4(b), the current flow to the output C_0 capacitor in mode 2 equals the output current and can be rewritten as follows:

$$C_0\frac{\Delta V_o}{(1-D)T} = \frac{P_o}{V_o}. \tag{22}$$

To limit the ripple on the output voltage using the $r_v\%$, the C_0 capacitance should be as follows:

$$C_0 = \frac{(1-D)(1-2D)^2TP_o}{r_v\%(3-2D)V_g^2}. \tag{23}$$

IV. COMPARISON WITH OTHER NONISOLATED HIGH-BOOST CONVERTER

The comparison between the proposed converter and other nonisolated high-boost dc–dc converters is shown in Table I. In comparison to the interleaved boost dc–dc converter in [14], the proposed converter uses one less inductor with a lower voltage stress on the devices. Compared with the double-inductor-energy storage-cell-based SC (DIESC-SC) [19], the proposed converter uses one more active switch but fewer passive components. In comparison with the SC-ANC [24], the proposed converter uses one more diode and one less inductor. Compared with the *Z*-source dc–dc converter in [26] and the CG-ZSC in [28], the proposed converter uses one more switch, two more diodes, and fewer inductors to produce a high-voltage gain with the occurrence of a low-voltage stress on the components. In addition, the proposed converter has a lower input-current ripple than the conventional high-boost dc–dc converters.

Fig. 6 shows a comparison between the voltage gains of the nonisolated step-up dc–dc converters in the CCM. As shown in Fig. 6, the voltage gain of the proposed SCDS converter is the highest at the same duty cycle.

V. POWER LOSS CALCULATION

A. Power Loss in the Switches

The power losses of MOSFET consist of a conduction loss and a switching loss. The switches S_1 and S_2 are conducted at

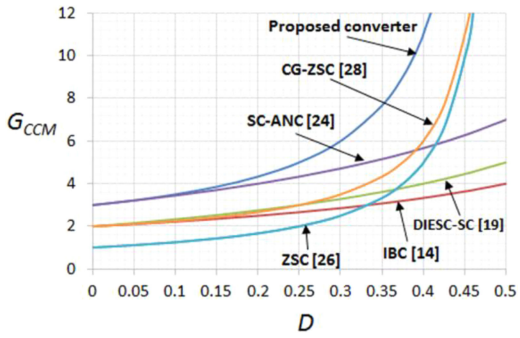


Fig. 6. Comparison of the voltage gains in the CCM.

the same time. Thus, the power loss of S_1 and S_2 are calculated

$$P_{cS} = R_{D\mathrm{Son}} \cdot D \cdot 2\left(\frac{P_o}{D\,(3\ -\ 2D)\,V_g}\right)^2 \tag{24}$$

where $R_{D\mathrm{Son}}$ is the drain-source ON-state resistance of the MOSFET.

The switching loss is

$$P_{swS} = 2V_{C1} \cdot \frac{P_o}{D\,(3\ -\ 2D)\,V_g} \cdot f_s \cdot \left(\frac{tru\ +\ tfi}{2} + \frac{tri\ +\ tfu}{2}\right) \tag{25}$$

where *tru*, *tfu*, *tri,* and *tfi* are the voltage rise time, voltage fall time, current rise time, and current fall time, respectively.

B. Power Loss in the Diodes

The power losses in the diodes include the conduction loss and reverse recovery loss. The conduction loss of free-wheeling and D_0–D_3 diodes are calculated by

$$\begin{aligned} P_{CD} = &\left[u_{D0} \cdot \left(\frac{P_o}{D\,(3\ -\ 2D)\,V_g} - I_L\right)\right. \\ &\left. +\ R_{D0} \cdot \left(\frac{P_o}{D\,(3\ -\ 2D)\,V_g} - I_L\right)^2\right] \cdot D \\ &+ \left(u_{D2} \cdot 0.5I_L + R_{D2} \cdot 0.25I_L^2\right) \cdot (1\ -\ D) \\ &+ \left(u_{D2} \cdot I_L + R_{D2} \cdot I_L^2\right) \cdot (1\ -\ D) \\ &+ \left(u_{D3} \cdot 0.5I_L + R_{D3} \cdot 0.25I_L^2\right) \cdot (1\ -\ D) \end{aligned} \tag{26}$$

where u_{Dx} and R_{Dx} are the ON-state zero-current voltage and the ON-state resistance of the D_x diodes $(x = 0 - 3)$, respectively.

The reverse recovery loss of the diodes is

$$\begin{aligned} P_{rrD} = &\ Q_{rr1} \cdot V_{C1} \cdot f_s + Q_{rr2} \cdot V_{C1} \cdot f_s \\ &+ Q_{rr3} \cdot V_{C1} \cdot f_s + Q_{rr0} \cdot (V_o - V_g) \cdot f_s, \end{aligned} \tag{27}$$

where Q_{rr0}, Q_{rr1}, Q_{rr2}, and Q_{rr3} are the reverse recovery charge of the free-wheeling, D_0, D_1, D_2, and D_3 diodes, respectively.

TABLE II
CONDUCTING CURRENT AND PERIOD OF COMPONENTS IN THE PROPOSED CONVERTER

Components	Conducting current	Conducting period
S_1 and S_2	$\frac{P_o}{D(3-2D)V_g}$	$D{*}T$
D_0	$\frac{P_o}{D(3-2D)V_g - I_L}$	$D{*}T$
D_1 and D_3	$0.5I_L$	$(1\ -\ D) * T$
D_2	I_L	$(1\ -\ D) * T$
L	I_L	T
C_1	$-\frac{P_o}{D(3-2D)V_g}$	$D{*}T$
	$0.5I_L$	$(1\ -\ D) * T$
C_2	$I_L - \frac{P_o}{D(3-2D)V_g}$	$D{*}T$
	$0.5I_L$	$(1\ -\ D) * T$
C_o	$\frac{P_o}{D(3-2D)V_g} - I_L - I_o$	$D{*}T$
	$-I_o$	$(1\ -\ D) * T$

C. Power Loss in the Capacitors

The capacitor power loss is calculated as

$$P_C = r_{C1} \cdot I_{C1}^2 + r_{C2} \cdot I_{C2}^2 + r_{Co} \cdot I_{Co}^2 \tag{28}$$

where r_{C1}, r_{C2}, and r_{Co} are the equivalent series resistances (ESRs) of C_1, C_2, and C_0 capacitors.

The RMS capacitor current of C_1, C_2, and C_0 capacitors are defined as follows:

$$\begin{cases} I_{C1} = \sqrt{\left(-\frac{P_o}{D(3-2D)V_g}\right)^2 \cdot D + 0.25I_L^2 \cdot (1\ -\ D)} \\ I_{C2} = \sqrt{\left(I_L - \frac{P_o}{D(3-2D)V_g}\right)^2 \cdot D + 0.25I_L^2 \cdot (1\ -\ D)} \\ I_{C0} = \sqrt{\left(\frac{P_o}{D(3-2D)V_g} - I_L - I_o\right)^2 \cdot D + I_o^2 \cdot (1\ -\ D)}. \end{cases} \tag{29}$$

D. Power Loss in the Inductor

The power loss in the inductor includes the core loss and the copper loss. For an MPP of 125 μ, the inductor core loss is obtained as follows:

$$P_{fe} = 0.33 \cdot B^{1.98} \cdot f^{1.64} \cdot A_c \cdot l_m \tag{30}$$

where B is the half of the ac flux swing, f is the frequency, A_c is the core cross-sectional area, and l_m is the core mean magnetic path length.

The inductor copper losses are given by

$$P_{cu} = R_L \cdot I_{L\_\mathrm{RMS}}^2 \tag{31}$$

where R_L is the resistance of the inductor.

The power loss calculation for the components is based on Table II. We assume that the converter operates in CCM. Fig. 7 shows the power-loss calculation of the proposed converter. The power loss of the proposed converter is calculated based on the parameters in Table III. When the minimum input voltage (V_g = 25 V) is applied, the large duty cycle that is used causes a low power-circuit efficiency. As shown in Fig. 7, the conduction loss

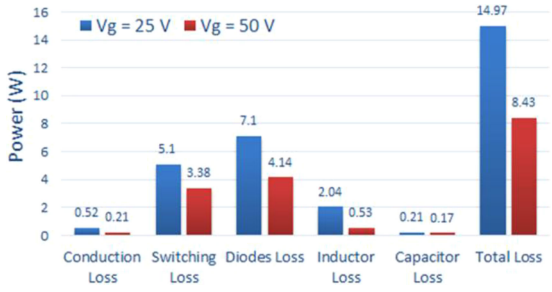


Fig. 7. Power-loss calculations at $V_o = 200$ V and $P_o = 200$ W when $V_g = 25$ V and 50 V.

TABLE III
PARAMETERS FOR THE POWER-LOSS CALCULATION

MOSFETs	IRFP4668PbF (200 V, 130 A, 8 mΩ)
Diodes	STPS60SM200C (200 V, 30 A)
ESR of C_1, C_2 (22 μF/ 100 VDC—Pilkor 223 MKT wk1133)	3.2 mΩ
ESR of C_0 capacitor (110 μF/450 VDC—Pilkor PCPW 245)	3.1 mΩ
Inductor core	CM777125 (142 nH/N^2
Copper-wire resistivity	$1.724 \cdot 10^{-6}\ \Omega \cdot$ cm

TABLE IV
SIMULATION AND EXPERIMENTAL PARAMETERS OF THE PROPOSED CONVERTER

Parameter		Values
Input voltage (V_g)		25–50 V
Output voltage (V_o)		200 V
Output power (P_o)		200 W
Inductor (L)		0.5 mH
Capacitors	C_1, C_2	22 μF/100 V
	C_0	110 μF/450 V
Switching frequency (f_{sw})		50 kHz
MOSFETs (S_1, S_2)		IRFP4668PbF
Diodes (D_0–D_3)		STPS60SM200C

of the switches is low, while the diode power loss is the highest; this is because the proposed converter uses four diodes while the conduction time of the three diodes D_1 to D_3 is $(1 - D) \cdot T$.

VI. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

To verify the properties of the proposed SCDS converter, as shown in Fig. 2, a PSIM simulation was performed with the following parameters: $L = 0.5$ mH, $C_1 = C_2 = 22\,\mu$F, $C_0 = 110\,\mu$F, $V_o = 200$ V, and $P_o = 200$ W. The switching frequency is 50 kHz and the input voltage is from 25 to 50 V. Table IV provides a list of the simulation parameters for the proposed converter.

Figs. 8 and 9 show the simulation results for the proposed inverter when $V_g = 50$ V and $V_g = 25$ V, respectively. As shown in Figs. 8(a) and 9(a), the voltage of the capacitor is boosted to 75 and 88 V, respectively. The output voltage of 200 V is the

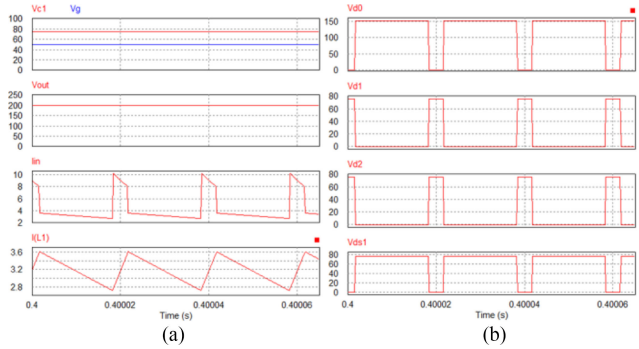


Fig. 8. Simulation results of the proposed converter when $V_g = 50$ V. From top to bottom: (a) capacitor-C_1 voltage, input voltage, output voltage, input current, and inductor current; and (b) diode-$D_0 - D_2$ voltages, and the drain-source voltage of S_1.

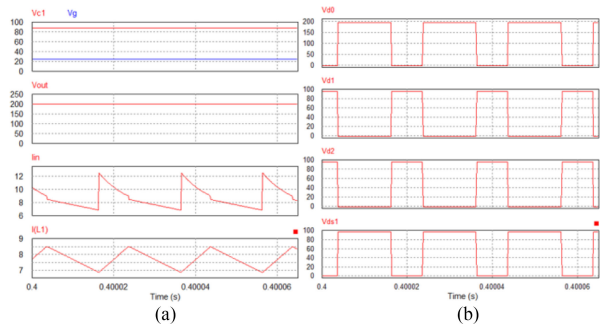


Fig. 9. Simulation results of the proposed converter when $V_g = 25$ V. From top to bottom: (a) capacitor-C_1 voltage, input voltage, output voltage, input current, and inductor current; and (b) diode-D_0–D_2 voltages, and the drain-source voltage of S_1.

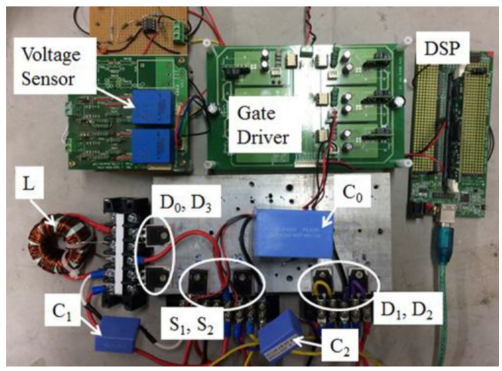


Fig. 10. Prototypal photograph of the proposed converter.

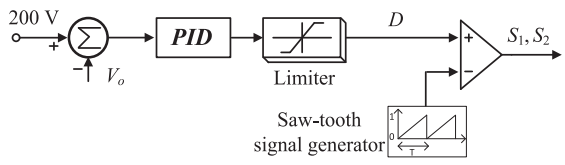
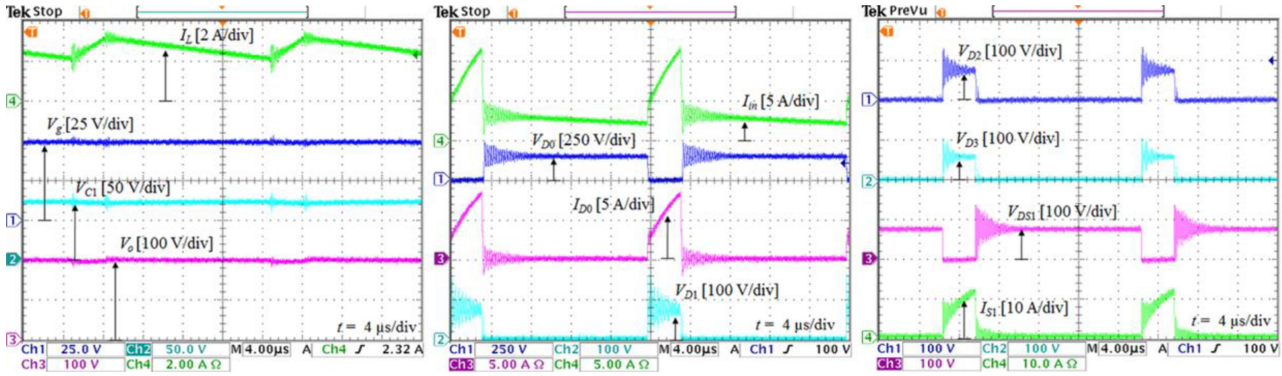


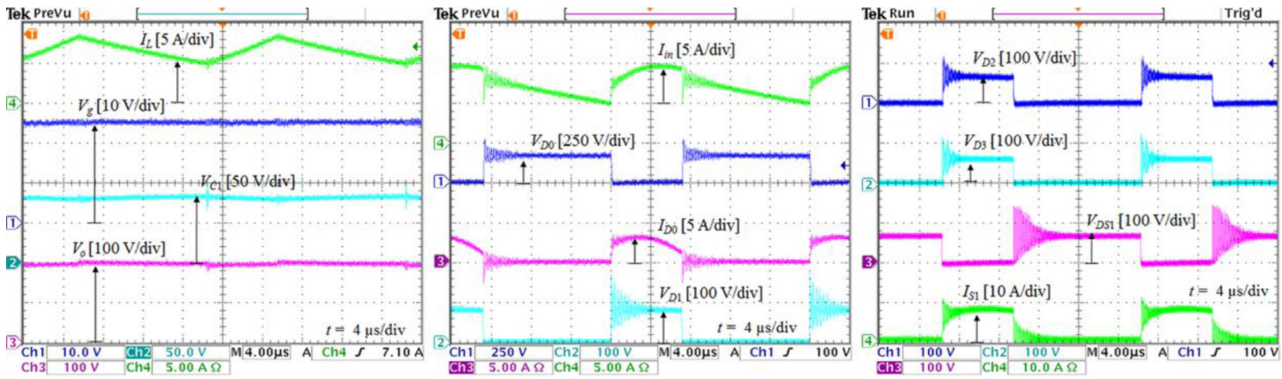
Fig. 11. PID-voltage control of the proposed converter.

total of the voltages of the capacitors C_1 and C_2 and the input voltage. The input current is continuous.



(a) (b) (c)

Fig. 12. Experimental results of the proposed inverter when $V_g = 50$ V.



(a) (b) (c)

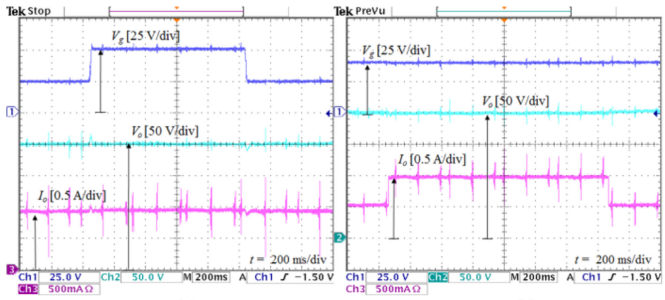
Fig. 13. Experimental results of the proposed inverter when $V_g = 25$ V.

B. Experimental Results

A 200 W laboratory prototype was constructed to verify the properties of the proposed converter. Fig. 10 shows a prototypal photograph. For the prototype, the parameters of the Table IV simulation were used. The input voltage is in the region of 25–50 V. The output voltage is 200 V. The switching frequency is 50 kHz. The two MOSFETs are IRFP4668PbF, and the four power diodes are STPS60SM200C. To maintain the output voltage at 200 V, a simple proportional-integral-derivative (PID)-feedback output-voltage control, as shown in Fig. 11, was used in the experiment.

The proposed converter was tested in the CCM at the output power of 200 W. Figs. 12 and 13 show the experimental results of the proposed converter when $V_g = 50$ V and $V_g = 25$ V, respectively. The input current is continuous. When the switches, S_1 and S_2, were turned on, the input current was increased; further, when S_1 and S_2 were turned off, the input current was decreased. As shown in Figs. 12(a) and 13(a), the voltage of the experimental capacitor C_1 is boosted to 75 and 87 V, respectively. The output voltage in both cases is 200 V.

In Figs. 12(a) and 13(a), the waveforms from the top to the bottom are the inductor current, input voltage, capacitor-C_1 voltage, and output voltage, respectively. In Figs. 12(b) and 13(b), the waveforms from the top to the bottom are the input current, diode-D_o voltage, diode-D_0 current, and diode-D_1 voltage, respectively. In Figs. 12(c) and 13(c), the waveforms from the top to the bottom are the D_2- and D_3-diode voltages, drain-source voltage, and S_1 current, respectively.



(a) (b)

Fig. 14. Experimental results with the dynamic response under the PID controller. (a) Input-voltage change and (b) load change.

Fig. 14 shows the experimental waveforms with the dynamic response of the proposed converter under the PID controller. In Fig. 14(a), the input voltage is changed from 25 to 50 V, while the output power is 198 W. In Fig. 14(b), the load is changed from 100 to 198 W, while the input voltage is 40 V. As shown from Fig. 14, the output voltage is always maintained at 200 V during the step change of the input voltage or the load.

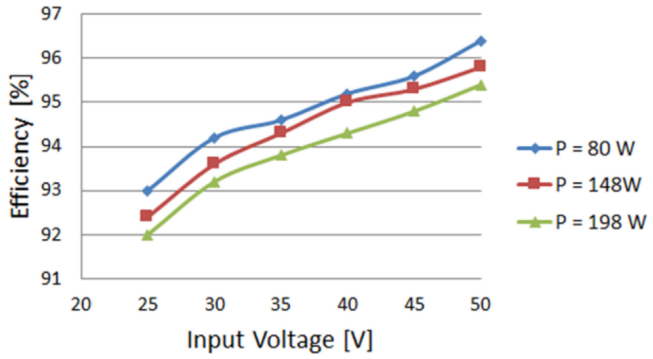


Fig. 15. Converter efficiency versus the variable input voltages at different output powers.

Fig. 15 shows the measured efficiency of the proposed converter with variable input voltages. Both the input and output powers were measured using the WT230 Digital Power Meter (Yokogawa, Japan). The maximum measured efficiency is 96.3%. The efficiency was decreased when the input voltage was reduced, and this is owing to the high conduction loss in the devices when a large duty cycle is used to obtain a high-voltage gain.

VII. Conclusion

An SCDS dc–dc converter is presented in this paper. The features of the proposed SCDS converter are as follows: a simple structure, thereby achieving a high-voltage gain with a small duty cycle for the reduction of the conduction loss of the power switches, and a low-voltage stress on the MOSFETs and diodes. The operating principle, CCM- and DCM-circuit analyses, and parameter design are presented. Also, an overall comparison between the proposed converter and other nonisolated dc–dc converters is addressed. The simulation and experimental results are shown to verify the theoretical analysis.

References

[1] F. L. Tofoli, D. C. Pereira, W. J. Paula, and D. S. O. Junior, "Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter," *IET Power Electron.*, vol. 8, no. 10, pp. 2044–2057, Oct. 2015.

[2] W. Li and X. He, "Review of nonisolated high-step-up dc/dc converters in photovoltaic grid-connected applications," *IEEE Trans. Ind. Electron.*, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.

[3] C. Yao, X. Ruan, and X. Wang, "Automatic mode-shifting control strategy with input voltage feed-forward for full-bridge-boost dc–dc converter suitable for wide input voltage range," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1668–1682, Mar. 2015.

[4] M. Nymand and M. A. E. Andersen, "High-efficiency isolated boost dc–dc converter for high-power low-voltage fuel-cell applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 505–514, Feb. 2010.

[5] Y. P. Hsieh, J. F. Chen, L. S. Yang, C. Y. Wu, and W. S. Liu, "High-conversion-ratio bidirectional DC/DC converter with couple inductor," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1311–1319, Mar. 2014.

[6] S. M. Chen, T. J. Liang, L. S. Yang, and J. F. Chen, "A boost converter with capacitor multiplier and coupled inductor for ac module applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1503–1511, Apr. 2013.

[7] B. Axelrod, Y. Beck, and Y. Berkovich, "High step-up dc–dc converter based on the switched-coupled-inductor boost converter and diode-capacitor multiplier: Steady state and dynamics," *IET Power Electron.*, vol. 8, no. 8, pp. 1420–1428, 2015.

[8] X. F. Hu and C. Y. Gong, "A high gain input-parallel output-series DC/DC converter with dual coupled inductors," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1306–1317, Mar. 2015.

[9] H. Liu, H. Hu, H. Wu, Y. Xing, and I. Batarseh, "Overview of high-step-up coupled-inductor boost converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 689–704, Jun. 2016.

[10] M. Zhu and F. L. Luo, "Enhanced self-lift Cuk converter for negative-to-positive voltage conversion," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2227–2233, Sep. 2010.

[11] L. huber and M. M. Jovanovic, "A design approach for server power supplies for networking applications," in *Proc. Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2000, pp. 1163–1169.

[12] X. G. Feng, J. J. Liu, and F. C. Lee, "Impedance specifications for stable dc distributed power systems," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 157–162, Mar. 2002.

[13] A. I. Bratcu, I. Munteanu, S. Bacha, D. Picault, and B. Raison, "Cascaded DC–DC converter photovoltaic systems: Power optimization issues," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 403–411, Feb. 2011.

[14] R. Gules, L. L. Pfitscher, and L. C. Franco, "An interleaved boost DC-DC converter with large conversion ratio," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2003, pp. 411–416.

[15] F. S. Garcia, J. A. Pomilio, and G. Spiazzi, "Modeling and control design of the interleaved double dual boost converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3283–3290, Aug. 2013.

[16] Y. J. A. Alcazar, D. S. Oliveira Jr., F. L. Tofoli, and R. P. Torrico-Bascopé, "DC–DC nonisolated boost converter based on the three-state switching cell and voltage multiplier cells," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4438–4449, Oct. 2013.

[17] Y. Jiao, F. L. Luo, and M. Zhu, "Voltage-lift-type switched-inductor cells for enhancing DC–DC boost ability: Principles and integrations in Luo converter," *IET Power Electron.*, vol. 4, no. 1, pp. 131–142, Jan. 2011.

[18] J. C. Rosas-Caro, J. M. Ramirez, F. Z. Peng, and A. Valderrabano, "A dc–dc multilevel boost converter," *IET Power Electron.*, vol. 3, no. 11, pp. 129–137, Jan. 2010.

[19] G. Wu, X. Ruan, and Z. Ye, "Nonisolated high step-up DC–DC converters adopting switched-capacitor cell," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 383–393, Jan. 2015.

[20] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid dc-dc PWM converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.

[21] Y. P. Hsieh, J. F. Chen, T. J. Liang, and L. S. Yang, "Novel high step-up DC-DC converter with coupled-inductor and switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 998–1007, Feb. 2012.

[22] L. S. Yang, T. J. Liang, and J. F. Chen, "Transformerless DC-DC converters with step-up voltage gain," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3144–3152, Aug. 2009.

[23] L. S. Yang and T. J. Liang, "Analysis and implementation of a novel bidirectional DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 1, pp. 422–434, Jan. 2012.

[24] Y. Tang, T. Wang, and Y. He, "A switched-capacitor-based active-network converter with high voltage gain," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2959–2968, Jun. 2014.

[25] Y. Tang and T. Wang, "Study of an improved dual-switch converter with passive lossless clamping," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 972–981, Feb. 2015.

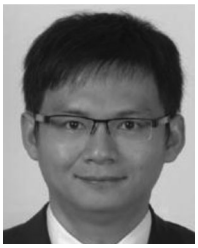
[26] P. Galigekere and M. K. Kazimierczuk, "Analysis of PWM Z-source dc-dc converter in CCM for steady state," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 4, pp. 854–863, 2012.

[27] D. Cao and F. Z. Peng, "A family of Z-source and quasi-Z-source dc-dc converter," in *Proc. IEEE App. Power Electron. Conf.*, 2009, pp. 1097–1101.

[28] H. Shen, B. Zhang, D. Qiu, and L. Zhou, "A common grounded Z-source dc–dc converter with high voltage gain," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2925–2935, May 2016.

[29] G. Zhang, B. Zhang, Z. Li, D. Qiu, L. Yang, and W. A. Halang, "A 3-Z-network boost converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 278–288, Jan. 2015.

[30] Y. P. Siwakoti, F. Blaabjerg, and P. C. Loh, "Quasi-Y-source boost dc-dc converter," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6514–6519, Dec. 2015.



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