Single-Phase to Three-Phase Unified Power Quality Conditioner Applied in Single-Wire Earth Return Electric Power Distribution Grids

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***Abstract*—This paper deals with the deployment of a local three-phase four-wire (3P4W) electrical power distribution system (EPDS), using a single- to three-phase unified power quality conditioner (UPQC) topology, called UPQC-1Ph-to-3Ph. The topology is indicated for applications in rural or remote areas in which, for economic reasons, only EPDS with single-wire earth return are accessible to the consumer. Since the use of three-phase loads is increasing in these areas, access to a three-phase distribution system becomes preponderant. By adopting a dual compensation strategy, the proposed UPQC-1Ph-to-3Ph is able of draining from the single-phase electrical grid a sinusoidal current and in phase with the voltage, resulting high-power factor. Furthermore, the system is also able to suppress grid voltage harmonics, as well as to compensate for other disturbances, such as voltage sags. Thus, a 3P4W system with regulated, balanced, and sinusoidal voltages with low-harmonic contents is provided for single- and three-phase loads. An analysis of the power flow through the series and parallel converters is performed in order to aid the designing of the power converters. Experimental results are presented for validating the proposal, as well as evaluating the static and dynamic performances of the proposed topology.**

***Index Terms*—Dual compensation strategy, rural and remote areas, single-wire earth return (SWER), unified power quality conditioner (UPQC).**

I. Introduction

In RURAL or remote regions in Brazil, as well as in some areas of countries such as Australia and New Zealand, for instance, electrical power distribution systems (EPDS) with single-wire earth return (SWER) have been commonly adopted as a solution for electrical power supplying. This is due to the fact that the reduction of costs in the distribution of energy to serve large territorial extensions with low-demographic densities is an important requirement [1]–[5], since lower installation and maintenance costs are achieved [4], [6].

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Other alternatives are the use of energy distribution by means of two conductors (phase-to-neutral) without earth return or even using two-phase systems (phase-to-phase). Considering these alternatives, capital investments for the realization of SWER distribution grid facilities installations are still lower [7].

The demand for electrical energy in single-phase rural distribution grids has considerably increased in the last decades, both in agriculture and in livestock, mainly due to the increasing evolution and modernization of the technologies used, as well as the increase in the mechanization of production processes. It is possible to mention, for example, the automation of irrigation, as well as the postharvest agricultural processing involving seed selection and milling, ventilation and refrigeration, washing and packaging lines, among others.

Within this context, there is an imminent trend of increasing energy demand in rural properties, as well as the need to improve power quality (PQ) enhancement due to the change in the characteristics of the loads.

The voltage regulation is characterized as one of the main problems of PQ found in the rural single-phase grids [4], [5], because when subjected to large loads, these grids have significant voltage drops, whereas at times of low consumption the voltage tends to rise [1]. Nevertheless, a solution not so efficient due to constant load variations can be adopted by adjusting the taps of the transformer of the SWER network. Another solution, more efficient in this case, is the use of single-phase voltage regulators [5].

Some ways to bypass large capital investments to meet the growing demand of rural properties have been adopted [3], [8]. In [3], the impacts caused between distributed generation systems implemented through photovoltaic systems and the SWER distribution systems are presented. On the other hand, in [8], the use of energy storage systems by means of batteries and their use at peak demand is discussed.

It is possible to notice an increasing need to use three-phase distribution grids to meet the demand for electrical energy in rural areas due to changes in the characteristics of the loads. Currently, most of them could be driven by three-phase induction motors instead of single-phase motors, for they have a higher starting torque [7]. Furthermore, the use of medium- and high-power three-phase voltage inverters involved in modern automated systems also justifies the need for three-phase grids in rural areas. Therefore, the presence of a local three-phase energy distribution system in areas that make

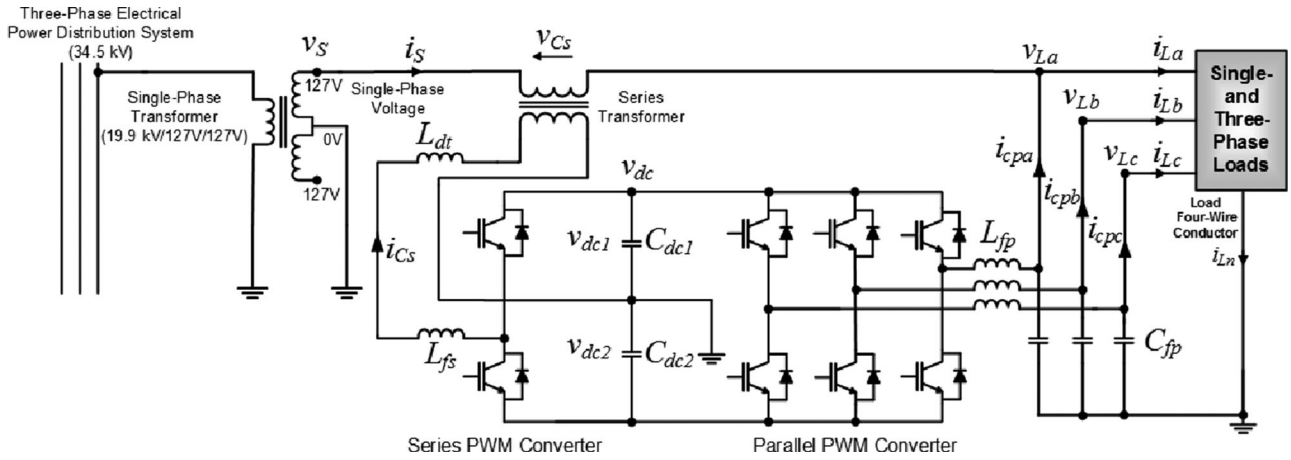

Fig. 1. Topology of the UPQC-1Ph-to-3Ph.

use of the SWER distribution system becomes more and more indispensable.

For this purpose, several solutions and/or configurations of single-phase-to-three-phase (1Ph-to-3Ph) converters have been addressed in the literature [6], [7], [9]–[11]. These include 1Ph-to-3Ph four-wire converters, which are able of supplying three-phase and single-phase loads [6], [7], [9], or 1Ph-to-3Ph three-wire converters intended to supply only three-phase loads [10], [11].

Dedicated to feed three-phase three-wire loads and integrating the functioning of the unified power quality conditioner (UPQC), the 1Ph-to-3Ph converter presented in [12] performs universal filtering, i.e., it operates as series–parallel active power filter, in which the series converter is composed of a single-phase full-bridge inverter (two inverter legs), while the parallel converter is composed of a three-phase three-leg inverter, totaling five inverter legs.

In [13], also integrating the functionality of a UPQC, a 1Ph-to-3Ph converter was dedicated for creating a local three-phase four-wire (3P4W) EPDS from a single-phase distribution system. The series converter is composed of a half-bridge inverter (one inverter leg), while the parallel converter is composed of a three-leg split-capacitor inverter, totaling four inverter legs. Thus, it was allowed feed single- and three-phase loads. On the other hand, limited results have only been presented by means of simulations. In addition, no detail regarding to the dimensioning and control of the converters were suitably treated.

In this paper, the 1Ph-to-3Ph converter presented in [13] is experimentally validated. It is called UPQC-1Ph-to-3Ph and its power circuit configuration is shown in Fig. 1. This system is indicated for applications in rural or remote areas where, for economic reasons, only single-phase EPDS, such as SWER system, is accessible to the consumer.

Once the proposed system deployed in this paper was conceived based on the UPQC functionalities, some discussions related to the UPQC should be performed.

Since they simultaneously perform the functions of series active power filter (SAPF) and parallel active power filter (PAPF), the UPQCs have been commonly employed to mitigate PQ problems, both in single-phase distribution systems [14] and in 3P4W distribution systems [15]–[19].

Usually, the UPQCs are controlled to perform series and parallel compensation, synthesizing nonsinusoidal quantities of voltage and current, i.e., the series converter synthesizes nonsinusoidal voltage quantities to compensate for grid voltage disturbances, while the parallel converter synthesizes nonsinusoidal current quantities with the purpose of suppressing harmonic currents and compensating the reactive power of the loads [15]. For this compensation strategy, some calculation method capable of generating the voltage and current compensation references should be used.

On the other hand, some studies presented in the literature have used the dual compensation strategy to control the series and parallel converters of the UPQC [16]–[19]. In this strategy, sinusoidal voltage and current references are employed to control both the converters. In this case, the series converter synthesizes sinusoidal current quantities and, consequently, operates as a sinusoidal current source, providing a high-impedance path for the current harmonics of the load. The parallel converter synthesizes sinusoidal voltage quantities and, in this case, operates as a sinusoidal voltage source, providing a low-impedance path for the current harmonics of the load.

It is also observed that the performances of the controllers are notably better when they operate with sinusoidal references, when compared to those that use nonsinusoidal references. In addition, since the control references are sinusoidal, the controllers implemented in the synchronous reference frame will have continuous reference of voltage and current, facilitating even more the control [19]. Another advantage of dual compensation is in the form of generation of control references, which is performed only with the use of a phase-locked loop (PLL) system [20].

The main contribution presented in this paper is to validate experimentally the UPQC-1Ph-to-3Ph destined to feed single- and three-phase loads from the SWER power distribution systems, commonly found in rural and/or remote areas and suffer with PQ problems. By adopting the dual compensation strategy, the proposed UPQC-1Ph-to-3Ph makes possible to drain

from the single-phase electrical grid a sinusoidal current in phase with the grid voltage. Furthermore, the system can also suppress harmonics from the grid voltage, as well as compensate for voltage disturbances, such as voltage sags/swell. In other words, the UPQC-1Ph-to-3Ph can conceive a local 3P4W system with regulated, balanced, and sinusoidal load voltages with low-harmonic contents improving the PQ indicators [23]. Therefore, the proposed system can achieve two important functions simultaneously, as described: 1) convert the single-phase grid into a three-phase grid, generating a 3P4W distribution system with earthed neutral wire to the final consumer, allowing to connect single- and there-phase loads; and 2) perform the series and parallel active power filtering improving PQ indicators, such as power factor and harmonic distortion [23]. Furthermore, in order to assist in the proper dimensioning of the UPQC-1Ph-to-3Ph power converters, an analysis involving the power flow through the serial and parallel converters is also presented.

II. Description of the UPQC-1Ph-to-3Ph Topology

The topology of the UPQC-1Ph-to-3Ph is shown in Fig. 1. This one is formed by two pulse width modulation (PWM) converters, being a half-bridge inverter and a split-capacitor three-leg inverter sharing the same dc-bus.

As can be noted, a half-bridge inverter is used to compose the series converter, while in [12], it was composed of a full-bridge inverter. Thus, besides using one leg less compared to the topology presented in [12], the dc-bus is formed by the split-capacitor configuration, allowing access to the earthed return conductor of the load, as well to be used in SWER distribution systems. As can be noted in Fig. 1, the four wires of the load are connected to the dc-bus central point.

The series converter, also called SAPF, is current controlled so that the input drained current is sinusoidal and in phase with the grid voltage, resulting in a power factor (PF) very close to 1. A filter inductor (L_{fs}) is placed in series with the primary winding of the single-phase series coupling transformer.

The parallel converter, called PAPF, is voltage controlled and it imposes three-phase sinusoidal, regulated, and balanced voltages to the loads. The load voltage of phase "*a*" (v_{La}) is controlled to be in phase with the grid voltage (v_s). Second-order *LC* filters are used to attenuate the high-frequency voltage components. Since the inverter leg connected to phase "*a*" is controlled to operate as a sinusoidal voltage source, the harmonic and fundamental components of the grid voltage are indirectly compensated by the system, and there is no need to use any specific algorithm to calculate/extract such components. The compensation voltage components, which are composed of harmonic and fundamental components, will appear across the terminals of the series coupling transformer.

The power flow through the UPQC-1Ph-to-3Ph will depend on both the load characteristics, such as fundamental power factor and total harmonic distortion (THD) of current, as well as the characteristics of the grid, such as the differences between the amplitudes of the grid and load voltage (phase "*a*"), as well as the grid voltage THD.

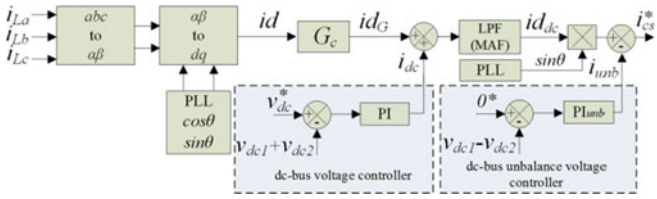

Fig. 2. Generation scheme of the series converter current reference the synchronous reference frame *dq*.

III. Generation of the Control References and Diagrams of the Converters

In this section, the strategies of generation of control references of the series and parallel converters as well as their modeling are presented.

A. Current Reference of the Series Converter

The single-phase current reference used to control the SAPF is obtained in the synchronous reference frame *dq*, as shown in Fig. 2. Thus, the load currents (i_{La}, i_{Lb}, i_{Lc}) are measured and transformed from the three-phase stationary reference frame (*abc*-axes) to the two-phase stationary reference frame ($\alpha\beta 0-$ axes) using the Clarke transformation. Then, by means of the Park transformation, the stationary current quantities of the reference frame $\alpha\beta 0$ are transformed to the synchronous reference frame (*dq*-axes). In the rotating frame, the coordinates of the unit vector $\sin(\theta)$ and $\cos(\theta)$ are obtained using the PLL system presented in [20], in which θ is the estimated phase angle of the grid voltage. The quantity i_d, shown in Fig. 2, represents the active components of the load currents, i.e., it is composed of an average component and oscillating components in the reference frame *d* (*d*-axis).

Once a 1Ph-to-3Ph system is being treated, the amplitude of the single-phase input/grid reference current (i^*_{cs}) must be properly adjusted to ensure that the average single-phase input power (P_s) is equivalent to the average three-phase output power (P_L).

In the synchronous reference frame, P_L and P_s are, respectively, given by

$$P_L = vd_{\rm dc} id_{\rm dc} \tag{1}$$

$$P_s = (V_{sp} I_{sp})/2 \tag{2}$$

where $vd_{\rm dc}$ and $id_{\rm dc}$ represent, respectively, the dc components of voltage and current in the *d*-axis, while V_{sp} and I_{sp} represent the respective peak voltage and peak current of the single-phase grid.

Assuming that the amplitudes of the three-phase output voltages (V_{Lp}) are equal in amplitude to the grid voltage V_{sp}, $vd_{\rm dc}$ can be written by

$$vd_{\rm dc} = \sqrt{(3/2)} V_{Lp} = \sqrt{(3/2)} V_{sp}. \tag{3}$$

Considering an ideal system, in a way that $P_s = P_L$ and through (1)–(3), the relationship between the current $id_{\rm dc}$ and

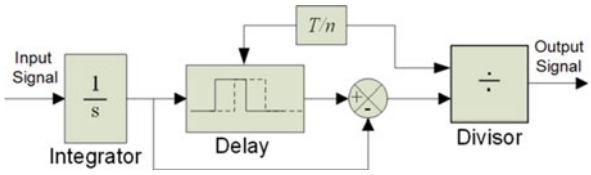

Fig. 3. Moving average filter (MAF).

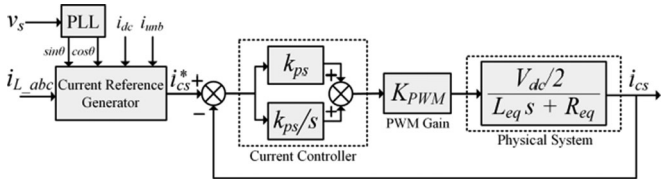

Fig. 4. Block diagram of the current controller and the average model of the series converter.

the current I_{sp} is given as follows:

$$I_{sp} = \sqrt{6} id_{\text{dc}} = G_c id_{\text{dc}}. \tag{4}$$

The presence of the gain $G_c = \sqrt{6}$ is observed in (4), which must necessarily be inserted in the algorithm of Fig. 2 to adapt the input and output powers of the UPQC-1Ph-to-3Ph.

The current i_{dc} shown in Fig. 2 represents the output signal of the dc-bus voltage proportional–integral (PI) controller. It is added to the direct synchronous axis current id_G and it is responsible for controlling the balance/power flow of the system. In other words, i_{dc} is used to perform the following functions: 1) regulate the voltage of the dc-bus to compensate for the losses involving the filtering passive elements and the switching devices; and 2) adjust the amplitude of the sinusoidal reference current i^*_{cs} (series converter), when there are variations of amplitude (sags/swells) between the input voltage and the output voltage (phase "*a*").

The current $id_G = \sqrt{6} id$ is added to i_{dc}, and then, filtered by means of a low-pass filter (LPF) generating id_{dc}.

Fig. 2 also shows the control loop used to cancel the voltage unbalances of the dc-bus capacitors, where the equivalent model adopted to represent the unbalance control is presented in [17]. The output signal of the mentioned controller (i_{unb}) acts adjusting the dc level of the grid current. Thus, the reference current of the series converter is given by

$$i^*_{cs} = id_{\text{dc}} \sin(\theta) - i_{\text{unb}}. \tag{5}$$

To improve the dynamic filtering response, a moving average filter (MAF) [21] was used acting as an LPF. The MAF is characterized by being an easy-to-implement filter capable of rejecting the multiple frequency components of the cutoff frequency, which is defined as the inverse of the integration period (*T*) or by the fundamental component period. Fig. 3 shows the structure of the MAF, which is composed of an integrator block, a transport delay block, a subtractor, and a divisor.

Since the single-phase system is connected to the grid, it should be considered the presence of voltage ripples at 120 Hz on the dc-bus of the UPQC-1Ph-to-3Ph. This ripple may result in the appearance of the 120-Hz harmonic in the series converter current reference (i^*_{cs}), since this current contains information of i_{dc}.

Therefore, one way of attenuating the signal amplitude at this unwanted frequency would be used an LPF in the dc-bus voltage control loop. Nevertheless, its use could interfere with the dynamics of the control making it slower. For this reason, it was opted to use only one LPF (MAF) after the sum of the dc-bus controller current (i_{dc}) with the direct axis current (id_G), as shown in Fig. 2.

Furthermore, if there are unbalanced load currents, a fundamental negative sequence component will also appear in the synchronous reference frame at the 120-Hz frequency, i.e., *T*/2 of the fundamental component period.

Consequently, it becomes necessary that the cutoff frequency of the MAF be 120 Hz, i.e., the integer *n* shown in Fig. 3 must be equal to 2.

B. Current Controller of the Series Converter

Fig. 4 shows, by means of a block diagram, the PI current controller as well as the average model of the series converter. Thus, the transfer function of the system can be written by

$$\frac{i_{cs}(s)}{i^*_{cs}(s)} = \frac{K_{\text{pwm}}(\frac{V_{\text{dc}}}{2})(K_{ps}s + K_{is})}{L_{eq}s^2 + (K_{ps}K_{\text{pwm}}\frac{V_{\text{dc}}}{2} + R_{eq})s + K_{is}K_{\text{pwm}}\frac{V_{\text{dc}}}{2}} \tag{6}$$

where K_{ps} and K_{is} are the PI current controller gains; K_{pwm} is the PWM gain; L_{eq} is the equivalent inductance ($L_{eq} = N^2 L_{dt} + L_{fs}$), such that L_{fs} is the series filter inductance, L_{dt} is the leakage inductance reflected to the primary of the transformer (grid side), *N* is the transformation ratio of the transformer, $R_{eq} = N^2 R_{dt} + R_{fs}$ is the equivalent resistance, such that R_{dt} is the resistance of the series transformer; and R_{fs} is the internal resistance of the series inductor and V_{dc} is the total dc-bus voltage, such that $V_{\text{dc}} = V_{\text{dc1}} + V_{\text{dc2}}$.

The transformation ratio of the transformer *N* was set equal to 1. The higher the transformation ratio ($N = 2$, for instance), the higher the current ripple in the filtering inductor (L_{fs}). Therefore, this ripple would be transferred to the primary side of the transformer, increasing the THD of the grid current. One solution to overcome this problem would be to increase the inductance L_{fs}. In this way, $N = 1$ has been adopted, as can be noticed in Table I.

C. Reference Voltage of the Parallel Converter

The output voltage of phase "*a*" is controlled to be in phase with the grid voltage. Thus, given the estimated phase angle θ of the grid voltage, as well as the desired voltage amplitude of the load V_{Lp}, the output voltage references are given by

$$v^*_{La} = V_{Lp} \sin(\theta) \tag{7}$$

$$v^*_{Lb} = V_{Lp} \sin(\theta - 120^\circ) \tag{8}$$

$$v^*_{Lc} = V_{Lp} \sin(\theta + 120^\circ). \tag{9}$$

TABLE I
PARAMETERS USED IN THE TESTS OF THE UPQC-1PH-TO-3PH

Apparent power of the 1Φ load 1	$S_{La} = 600$ VA, $S_{Lb} = 300$ VA, $S_{Lc} = 400$ VA
Apparent power of the 1Φ load 2	$S_{La} = S_{Lb} = S_{Lc} = 538$ VA
Apparent power of the 3Φ load 1	$S_L = 1860$ VA
Apparent power of the 3Φ load 2	$S_L = 1372$ VA
Nominal rms voltage of the 1Φ grid	$V_s = 127$ V
Nominal rms voltage of the 3Φ load (phase)	$V_{L\_a,b,c} = 127$ V
Nominal frequency of the grid	$f_s = 60$ Hz
Switching frequency of the inverters	$f_{ch} = 20$ kHz
Coupling inductances of the parallel converter	$L_{fp\_a,b,c} = 1.75$ mH
Internal resistances of the coupling inductors (parallel converter)	$R_{Lfp\_a,b,c} = 0.17\ \Omega$
Capacitances of the parallel filters	$C_{fp_a,b,c} = 50\ \mu$F
Coupling inductances of the series converter	$L_{fs\_a,b,c} = 1.75$ mH
Internal resistances of the coupling inductors (series converter)	$R_{Lfs} = 0.17\ \Omega$
Leakage inductance of the series transformer	$L_{dt} = 0.18$ mH
Resistance of the series transformer	$R_{dt} = 0.162\ \Omega$
Transformation ratio of the series transformer	$N = 1$
DC-bus voltage	$V_{\text{dc}} = 500$ V
DC-bus capacitance	$C_{\text{dc}} = 9400\ \mu$F
Sampling frequency of the DSC	$f_a = 60$ kHz
Gain of the PWM modulator	$K_{PWM} = 2.66 \cdot 10^{-4}$

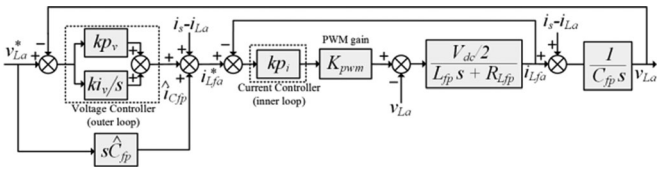

Fig. 5. Block diagram of the voltage control loops and of the average model of the parallel converter.

D. Voltage Controller of the Parallel Converter

Fig. 5 presents, by means of a block diagram, the voltage control loops as well as the average model of the parallel converter considering only phase "*a*." The multiloop control is implemented by an internal current control loop, where only a proportional controller is used, and an external voltage control loop, in which a PI controller is used. Thus, from the diagram of Fig. 4, the transfer function of the system can be written by

$$\frac{v_{La}(s)}{v^*_{La}(s)} = \frac{A(X_1 s^2 = X_2 s + X_3)}{Y_1 s^3 + Y_2 s^2 + Y_3 s + Y_4} \tag{10}$$

where

$$A = K_{\text{pwm}}(V_{\text{dc}}/2);$$
$$X_1 = \hat{C}_{fp} K p_i;$$
$$X_2 = K p_v K p_i; \quad X_3 = K i_v K p_i;$$
$$Y_1 = L_{fp} C_{fp}; \quad Y_2 = C_{fp}[K p_i K_{\text{pwm}}(V_{\text{dc}}/2) + R_{Lfp}];$$
$$Y_3 = [K_{pv} K_{pi} K_{\text{pwm}}(V_{\text{dc}}/2) + 1]; \text{ and}$$
$$Y_4 = K i_v K p_i K_{\text{pwm}}(V_{\text{dc}}/2).$$

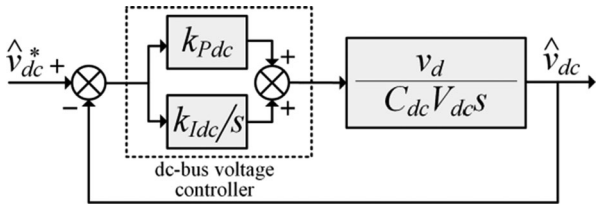

Fig. 6. Block diagram of the dc-bus control system.

Based on (10), Kp_v and Ki_v represent the respective proportional and integral controller gains of the external voltage loop, Kp_i is the proportional gain of the internal current loop, K_{pwm} is the PWM gain, C_{fp} is the filter capacitor, $\hat{C}_{fp}$ is the estimated filter capacitor, L_{fp} is the filtering inductance, R_{Lfp} is the internal resistance of the filter inductor L_{fp} and V_{dc} is the total dc-bus voltage.

As shown in Fig. 5, a feed-forward control loop is used in the output voltage control. The current $\hat{i}_{C_{fp}}$ of the filter capacitor $\hat{C}_{fp}$ is estimated, since it is not measured.

E. DC-Bus Voltage Controller

By adopting a procedure similar to that presented in [22], it is possible to obtain the voltage control of the dc-bus diagram as shown in Fig. 6. Thus, the small signal closed-loop transfer function of the dc-bus control system is given by

$$\frac{\hat{v}_{\text{dc}}(s)}{\hat{v}^*_{\text{dc}}(s)} = \frac{v_d K_{P\text{dc}} s + v_d K_{I\text{dc}}}{C_{\text{dc}} V_{\text{dc}} s^2 + v_d K_{P\text{dc}} s + v_d K_{I\text{dc}}} \tag{11}$$

where $K_{P\text{dc}}$ and $K_{I\text{dc}}$ are the respective proportional and integral gains of the dc-bus PI controller; C_{dc} is the equivalent dc-bus capacitance; V_{dc} is the total dc-bus voltage; and $v_d = \sqrt{3/2} V_{sp}$ is the direct voltage in the synchronous reference frame.

Equation (11) was obtained considering that a sinusoidal and balanced three-phase system is provided to the load. In addition, it was assumed that the current drained from the grid is sinusoidal and in phase with the voltage, i.e., the UPQC-1Ph-to-3Ph operates with unity PF.

IV. POWER FLOW THROUGH THE SERIES AND PARALLEL CONVERTERS

This section has the purpose of measuring quantitatively in steady state, the apparent powers that flow through the series (S_{cs}) and parallel (S_{pc_a}) converters connected to phase "*a*" of the load. Both the apparent power (S_{cs}) and (S_{pc_a}) are normalized as a function of the total apparent power of the load (S_L). The parallel converter connected to phase "*a*" of the UPQC-1Ph-to-3Ph will necessarily process more power if compared to the converters connected to phases "*b*" and "*c*." In this case, more attention should be paid to this converter regarding its designing.

For the analysis of the power flow, the relationship between the rms value of the fundamental output voltages (v_{L_abc}), represented by V_L, and the rms value of the fundamental

grid voltage (v_s), represented by V_{s1}, i.e., (V_{s1}/V_L), is taken into account. In addition, the THDs of current of each one of the load terminals (THDi_{La}, THDi_{Lb}, THDi_{Lc}) and the fundamental power factors ($\cos\,\phi_{1a}$, $\cos\,\phi_{1b}$, $\cos\,\phi_{1b}$) are also considered.

A. Apparent Power Flow Through the Series Converter

For steady-state analysis, to determine the power flow through the series converter, the following conditions are considered:

1) the input current is sinusoidal (without harmonics) and is in phase with the fundamental component of the grid voltage;
2) the phase "*a*" load voltage (v_{La}) is sinusoidal (without harmonics) and is in phase with the grid voltage fundamental component (v_{s1});
3) the grid voltage (v_s), whose its rms value is defined by V_s, is composed of voltage fundamental (v_{s1}) and harmonic components (v_{sh});
4) the load voltages (v_{L_abc}) are sinusoidal and balanced and they have the same rms values, i.e., $V_{L\_abc} = V_L$; and
5) the rms values of the fundamental voltages between the input and output of the UPQC are within a limit of $\pm$ 25%, i.e., $0.75 < V_{s1}/V_{La} < 1.25$.

The series converter complex apparent power is given by:

$$\dot{S}_{sc} = \dot{V}_{Cs}\dot{I}_s^* \tag{12}$$

where $V_{Cs} = V_s - V_L$ is the rms voltage across the series transformer and I_s is the rms current (grid current) that flows through the series transformer (primary side).

Assuming the conditions 1)–4), the module of the series converter apparent power $|S_{sc}|$ is given by

$$|S_{sc}| = P_L\sqrt{\left(1-\frac{V_L}{V_{s1}}\right)^2 + \text{THD}_{Vs}^2}. \tag{13}$$

Now, supposing balanced loads, such that the fundamental apparent power of the phases *abc* ($S_{1a} = S_{1b} = S_{1c}$) are equal to each other, the module of the normalized apparent power $|S_{sc}|$ can be found as

$$\left|\frac{S_{sc}}{S_L}\right| = \left(\frac{\cos\,\phi_{1a} + \cos\,\phi_{1b} + \cos\,\phi_{1c}}{\sqrt{1+\text{THD}_{i_{La}}^2} + \sqrt{1+\text{THD}_{i_{Lb}}^2} + \sqrt{1+\text{THD}_{i_{Lc}}^2}}\right) \sqrt{\left(1-\frac{V_L}{V_{s1}}\right)^2 + \text{THD}_{Vs}^2} \tag{14}$$

where $P_L = P_a + P_b + P_c$ is the total active power of the load; and THD$_{Vs}$ is the THD of the grid voltage.

Fig. 7(a) shows the normalized curve $|S_{sc}/S_L|$, taking into account that the fundamental power factors $\cos\,\phi_{1a} = \cos\,\phi_{1b} = \cos\,\phi_{1c} = \cos\,\phi_1$ and THDi_{La} = THDi_{Lb} = THDi_{Lc} = THDi_L. It can be clearly seen that two factors influence more significantly the increase of the power processed by the series converter, and they are the relation V_{s1}/V_L and the THD$_{Vs}$. To obtain the curves "a1," it was considered THD$_{Vs}$ = 0%, $\cos\,\phi_{1abc} = 1.0$, and THDi_{Labc} ranging from 0 to 90%, while for curves "b1," it was considered THD$_{Vs}$ = 0%, $\cos\,\phi_{1abc} = 0.7$, and THDi_{Labc} ranging from 0 to 90%.

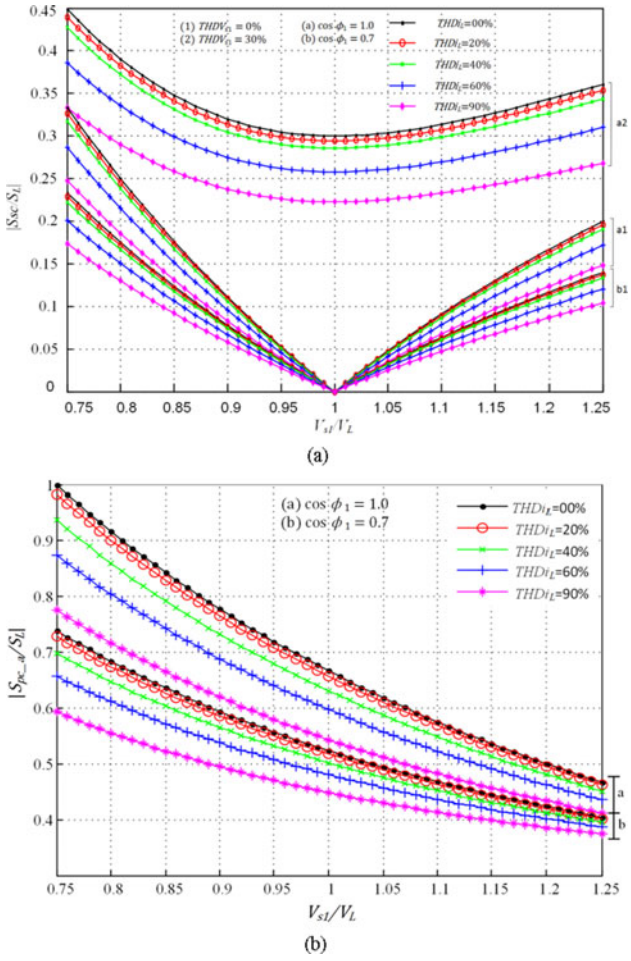

Fig. 7. Normalized apparent powers: (a) Series converter $|S_{sc}/S_L|$; (b) Parallel converter of phase "*a*" $|S_{pc\_a}/S_L|$.

Finally, for the curves "a2," it was considered THD$_{Vs}$ = 30%, $\cos\,\phi_{1abc} = 1.0$, and THDi_{Labc} ranging from 0 to 90%.

It is possible to observe that the series converter always operates with apparent power lower than the nominal apparent power of the load ($|S_{sc}/S_L| < 1$). Thus, to meet the most critical operating condition of those presented in Fig. 7(a), i.e. $V_{s1} = 0.75\ V_L$ (curve a2), the series converter must be designed at around only 45% of the nominal power of the system. This clearly represents an advantage when compared to the conventional topologies of single-to-three-phase converters.

B. Apparent Power Flow Through the Parallel Converter

For the calculation of the apparent power processed in phase "*a*" of the parallel converter, it was considered that the load voltage v_{La}, the grid voltage v_s, and the grid current i_s are sinusoidal and harmonic free. In addition, it was considered that the three quantities cited above (v_{La}, v_s, and i_s) are in phase with each other.

The complex apparent power of the parallel converter (phase "*a*") is given by

$$\dot{S}_{pc\_a} = \dot{S}_{Cs} - \dot{S}_{La} = \dot{V}_s\dot{I}_s^* - \dot{S}_{La} = (V_L/V_{s1})P_L - \dot{S}_{La}. \tag{15}$$

Thus, based on (12) and the other considerations described previously, the module of the parallel converter apparent power normalized as a function of the apparent power of the load $|S_{pc\_a}/S_L|$ is given by

$$\left|\frac{S_{pc\_a}}{S_L}\right| = \frac{\sqrt{A\cos^2\phi_{1a}+2B\cos\phi_{1a}+C+D}}{\sqrt{1+\text{THD}^2_{i_{La}}}+\sqrt{1+\text{THD}^2_{i_{Lb}}}+\sqrt{1+\text{THD}^2_{i_{Lc}}}} \tag{16}$$

where

$$A = \left[\frac{V_L}{V_{s1}}\left(\frac{V_L}{V_{s1}}-2\right)\right];$$

$$B = \left[\frac{V_L}{V_{s1}}\left(\frac{V_L}{V_{s1}}-1\right)(\cos\phi_{1b}+\cos\phi_{1c})\right];$$

$$C = (V_L/V_{s1})^2(\cos\phi_{1b}+\cos\phi_{1c})^2;\ D = \left(1+\text{THD}^2_{i_{La}}\right).$$

Fig. 7(b) shows the normalized curve $|S_{pc\_a}/S_L|$ in which it is possible to notice that even under optimum conditions in which $V_{s1}/V_L = 1$, $\cos\phi_{1abc} = 1.0$, and $\text{THD}i_{Labc} = 0\%$, there is still a power flow flowing through the parallel converter connected to phase "*a*." This occurs due to the active power consumed by the loads connected to phases "*b*" and "*c*." To obtain the curves represented by "a," $\cos\phi_{1abc} = 1.0$, and $\text{THD}i_{Labc}$ ranging from 0 to 90% were considered, while for the curves "b," $\cos\phi_{1abc} = 0.7$, and $\text{THD}i_{Labc}$ ranging from 0 to 90% were considered.

As previously stated, the parallel converter connected to phase "*a*" of the load always operates at higher powers when compared to phases "*b*" and "*c*." In critical operating condition, the parallel converter must be designed with power equivalent to 100% of the nominal power of the load. However, only the converter connected to phase "*a*" must meet this specification.

C. Active Power Flow Through the Series and Parallel Converters

The directions of the instantaneous active power flow "$p = 1$ p.u." can be seen in Fig. 8, in which three different operating situations were considered in steady state, i.e., $V_{s1} = 0.75\ V_L$, $V_{s1} = V_L$, and $V_{s1} = 1.25\ V_L$. In this analysis, the passive elements and the semiconductor losses are not considered.

Fig. 8(a) shows a sag disturbance equivalent to 25%, i.e., $V_{s1} = 0.75\ V_L$. In this case, it is possible to observe that the power *p* flows from the grid to the parallel converter (1 p.u.) and from the dc-bus to the series converter (0.33 p.u.). One notices that in this operating condition (25% voltage sag), the parallel converter connected to phase "*a*" processes power equal to the total active power of the load. As can be noted from Figs. 7(b) and 8(a), the oversizing of the parallel converter connected to the phase "*a,*" equivalent to three times the nominal power of phases "*b*" and "*c,*" occurs only when $V_{s1} = 0.75\ V_L$ (25% of voltage sag). This operation condition rarely will occur during long time. Thereby, a safe margin for the dimensioning of the converter connected to phase "*a*" can be adopted as around twice the nominal power of phases "*b*" and "*c*".

The operating condition in which $V_{s1} = V_L$ is shown in Fig. 8(b). In this condition, the active power processed by the series converter is null. Nevertheless, 2/3 (66%) of the active power of the load flows through the parallel converter connected to phase "*a.*" This represents the amount of active power required to supply the loads connected to phases "*b*" and "*c*".

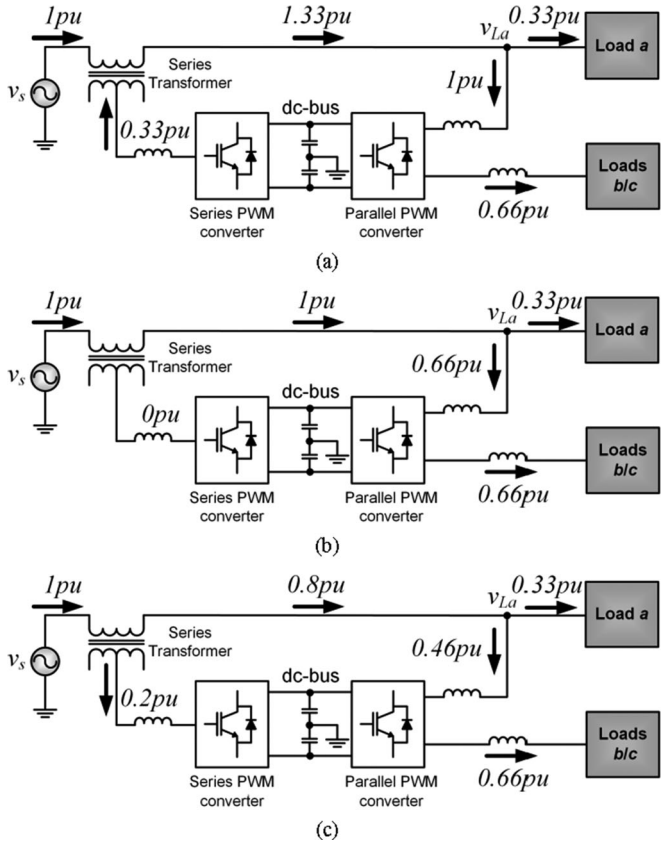

Fig. 8. Active power flow: (a) $V_{s1} = 0.75\ V_L$; (b) $V_{s1} = V_L$; (c) $V_{s1} = 1.25\ V_L$.

In Fig. 8(c), there is an overvoltage (swell) operating condition equivalent to 25%, i.e., $V_{s1} = 1.25\ V_L$. In this case, the power *p* flows from the grid to the parallel converter (0.46 p.u.) and from the grid to the dc-bus through the series converter (0.20 p.u.), totaling 2/3 (66%) of the active power required to supply the loads connected to phases "*b*" and "*c.*" It is possible to notice that in this operating condition (25% of swell), the parallel converter connected to phase "*a*" processes less power when compared to the condition of voltage sag.

V. Experimental Results

The static and dynamic performances of the UPQC-1Ph-to-3Ph under study were experimentally evaluated. The electrical power scheme is shown in Fig. 9(a), while the photo of the prototype is shown in Fig. 9(b).

The power set consists of an inverter module (SKS 50F B6U, Semikron), which has four SKM100GB 124D (100 A/1200 V) IGBT legs. An inverter leg is used for construction the series inverter, while the other three legs make up the parallel inverter. This module still has four isolated drivers (SKHI22B) and electrolytic capacitors placed in the dc-bus.

As observed in Fig. 9(a), the algorithms for generating control references, current and voltage controllers and the

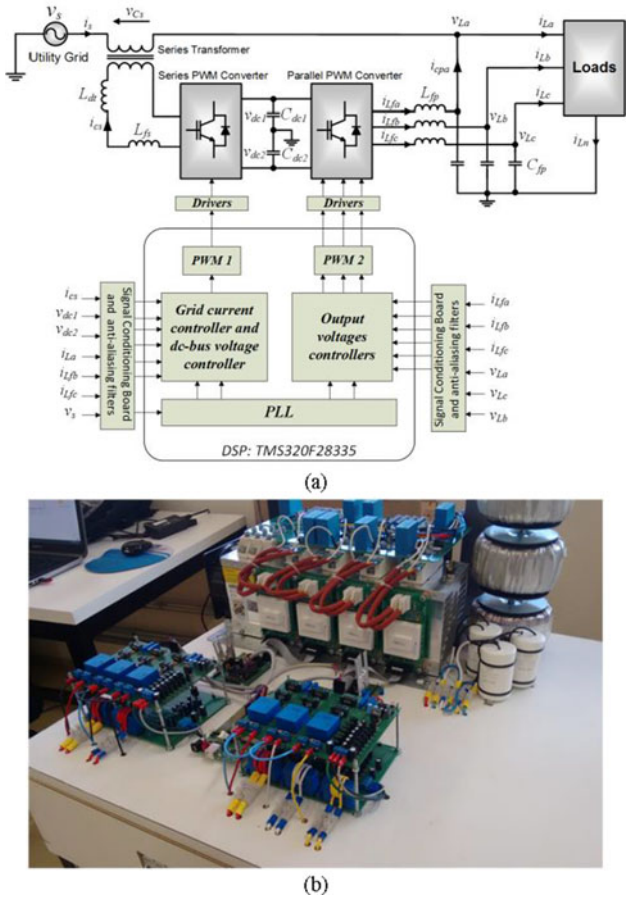

Fig. 9. Prototype of the UPQC-1Ph-to-3Ph.

PLL system were embedded in the digital signal controller (DSC) (TMS320F28335, Texas Instruments). Current transductors (LEM LA 100-P) were used to measure the load currents, as well as the inductor currents of the series and parallel inverters used in the control. The input and output ac voltages and the dc-bus voltage were measured using the LEM LV 25-P voltage transductors.

Table I presents the parameters of the UPQC-1Ph-to-3Ph. The passive elements of the system were designed based on the method presented in [24]. Once the nominal peak amplitude of grid voltage is equal to 180 V (it is supposed that the worst case occurs when $V_{s\text{-peak}} = 180\,\text{V} \pm 25\% = 225\,\text{V}$), as well as the three-leg split-capacitor inverter is employed, the amplitude of the dc-bus voltage was set at 500 V. In this paper, the sinusoidal pulse width modulation was adopted, such that the PWM static gain, defined by $K_{PWM} = 1/P_{PWM}$ can be obtained [25], in which P_{PWM} is the peak amplitude of the PWM triangular carrier in the DSC.

In Table II, the linear and nonlinear loads used in the experimental tests are shown, while the controller gains, conjunctly with their respective design specifications, are presented in Table III. In this paper, the method based on frequency response in open loop was adopted for tuning the PI controllers, in which was considered the phase margin and the gain crossover frequency in 0 dB as design specifications [22]. For simplification

TABLE II
PARAMETERS OF THE LOADS USED IN THE EXPERIMENTS

Single-phase load (1Φ)		Phase A	Phase B	Phase C
1Φ full-bridge rectifier	1	R = 20 Ω L = 200 mH	R = 40 Ω L = 346 mH	R = 30 Ω L = 400 mH
	2	R = 30 Ω	R = 30 Ω	R = 30 Ω
Three-phase loads (3Φ)		Phases ABC		
3Φ full-bridge rectifier	1	R = 50 Ω		
Three-phase induction motor	2	220V/1CV (60Hz, 1730 rpm, 4 poles, $\cos\varphi = 0.76$, $\eta = 70.6\%$)		

TABLE III
CONTROLLER GAINS AND DESIGN SPECIFICATIONS

	Parallel Converter			Series Converter	
Axes	Outer Loop		Inner Loop	Kp_{s_a}	Ki_{s_a}
	$Kp_{v\ abc}$	$Ki_{v\ abc}$	$Kp_{i\ abc}$		
abc	0.1337	391.6086	137.45	248.043	1.0455×10^{6}
dc-bus voltage controller gains				K_{Pdc}	K_{Idc}
				0.618	2.487
dc-bus unbalance voltage controller gains				K_{Punb}	K_{Iunb}
				0.2853	1.8965
Crossover frequency of the inner current loop of the parallel converter				$\omega_{cp\_i} = 10.47\times10^{3}$ rad/s	
Crossover frequency of the outer voltage loop of the parallel converter				$\omega_{cp\_i} = 3.49\times10^{3}$ rad/s	
Phase margin				$PM_{p} = 50^{o}$	
Crossover frequency of the current loop of the series converter				$\omega_{csi} = 19.33\ \ 10^{3}$ rad/s	
Phase margin				$PM_{s} = 78^{o}$	
Crossover frequency of the voltage loop of the dc-bus				$\omega_{c\_dc} = 25.13\times10^{3}$ rad/s	
Phase margin				$PM_{v_{dc}} = 75^{o}$	
Crossover frequency of the unbalance voltage loop of the dc-bus				$\omega_{c\_unb} = 37.67\times10^{3}$ rad/s	
Phase margin				$PM_{v_{unb}} = 80^{o}$	

purposes, the delays related to the digital implementation were disregarded in the design.

The first test involving the UPQC-1Ph-to-3Ph took into account the system feeding the set of single-phase loads 1 (see Table II), as seen in Fig. 10. The unbalanced phase currents (i_{La}, i_{Lb}, and i_{Lc}) and current (i_{Ln}) are shown in Fig. 10(a). Fig. 10(b) shows the load supply voltages (v_{La}, v_{Lb}, and v_{Lc}) conjunctly with the current drained from the single-phase grid i_s, where it is observed that i_s is in phase with v_{La}. Fig. 10(c) shows the voltage v_s and the current i_s of the grid. As can be observed,i_s is sinusoidal and in phase with v_s, resulting in a high PF. Fig. 10(d) shows the load current of the phase "*a*" i_{La}, the current of the grid i_s, as well as the compensation current that flows through the parallel converter connected to the phase "*a*" (i_{cpa}). It can be observed that the waveform of the current i_{cpa} is close to a sinusoid, indicating that, besides theharmonic load components of phase "*a,*" the parallel converter connected to the respective phase also processes active energy (fundamental component) to feed the loads connected to the phases "*b*" and "*c.*"

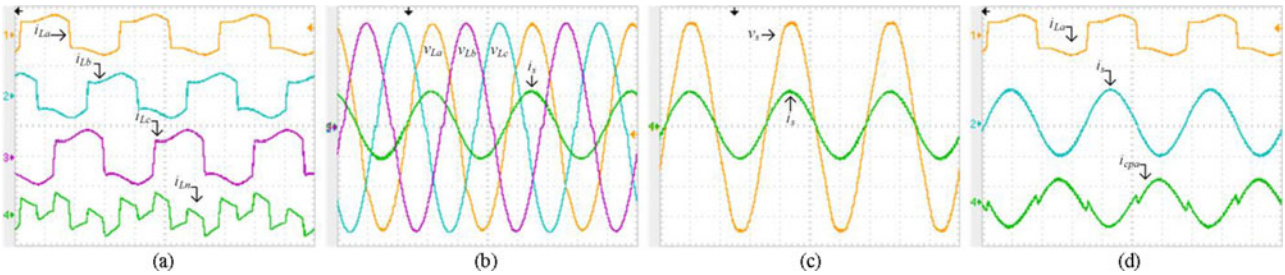

Fig. 10. UPQC-1Ph-to-3Ph (Load 1Φ 1) (5 ms/div): (a) Load currents i_{La} (10 A/div), i_{Lb}, i_{Lc}, and i_{Ln} (5 A/div); (b) Load voltages v_{L_abc} (50 V/div), and grid current i_s (20 A/div); (c) Voltage (50 V/div) and current (20 A/div) of the grid; (d) Currents: load i_{La} (10 A/div), grid i_s (20 A/div), and parallel converter i_{cpa} (20 A/div).

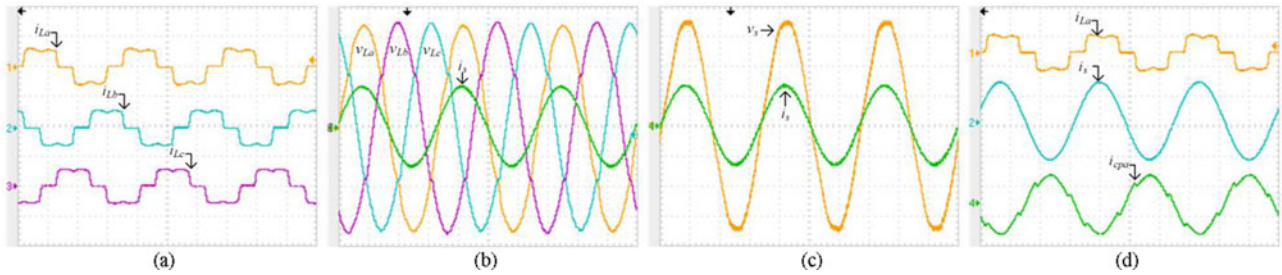

Fig. 11. Currents and voltages of the UPQC-1Ph-to-3Ph feeding the three-phase load 1 (5 ms/div): (a) Load currents i_{La}, i_{Lb}, and i_{Lc} (10 A/div); (b) Load voltages v_{La}, v_{Lb}, and v_{Lc} (50 V/div), and grid current i_s (20 A/div); (c) Grid voltage (50 V div) and grid current (20 A/div); (d) Currents: load i_{La} (10 A/div) (phase "*a*"), grid i_s (20 A/div) and parallel converter i_{cpa} (20 A/div) (phase "*a*").

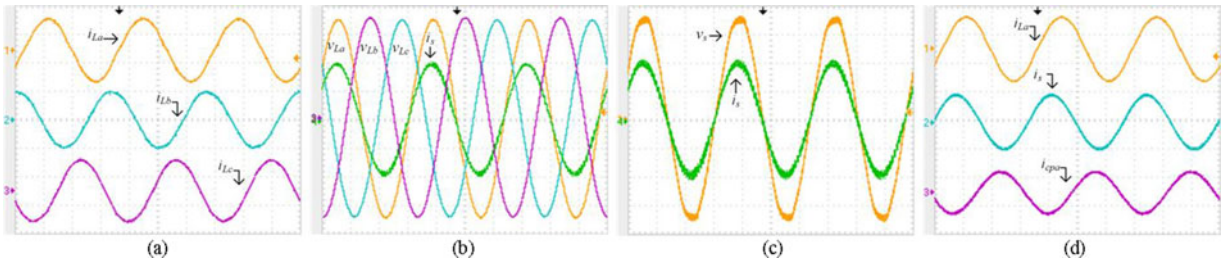

Fig. 12. Currents and voltages of the UPQC-1Ph-to-3Ph feeding the three-phase load 2 (5 ms/div): (a) Load currents i_{La}, i_{Lb}, and i_{Lc} (5 A/div); (b) Load voltages v_{La}, v_{Lb}, and v_{Lc} (50 V/div) and grid current i_s (10 A/div); (c) Grid voltage (50 V/div) and grid current (10 A/div); (d) Currents: load i_{La} (5 A/div) (phase "*a*"), grid i_s (20 A/div), and parallel converter i_{cpa} (20 A/div) (phase "*a*").

TABLE IV
THD OF THE CURRENT AND VOLTAGE QUANTITIES

LOADS	Total harmonic distortion (THD%)							
	i_{La}	i_{Lb}	i_{Lc}	i_s	v_{La}	v_{Lb}	i_{Lc}	v_s
Load 1 (1Φ)	34.4	32.8	30.8	4.0	3.4	3.8	3.2	2.3
Load 2 (1Φ)	27.1	26.3	23.6	4.0	3.7	4.5	4.5	2.3
Load 3Φ	2.6	2.6	2.6	4.3	1.5	1.5	1.4	2.0

TABLE V
POWERS (S, P, AND N) AND POWER FACTORS (PF AND PF_1)

Powers and PFs		Load 1 (1Φ)			Load 1 (3Φ)			Load 2 (3Φ)
		a	*b*	*c*	*a*	*b*	*c*	*abc*
S (kVA)	*L*	0.61	0.31	0.39	0.50	0.48	0.51	1.40
	G	1.7	–	–	2.04	–	–	1.51
P (kW)	*L*	0.56	0.29	0.36	0.48	0.46	0.48	1.15
	G	1.71	–	–	2.02	–	–	1.51
N (kVAr)	*L*	0.23	0.13	0.15	0.15	0.15	0.15	0.79
	G	0.24	–	–	0.30	–	–	0.26
PF	*L*	0.93	0.92	0.92	0.96	0.96	0.96	0.83
	G	0.99	–	–	0.99	–	–	0.98
PF_1	*L*	1.00	0.99	0.99	1.00	1.00	1.00	0.83
	G	1.00	–	–	1.00	–	–	1.0

In the second test, the three-phase load 1 (see Table II) was fed by the UPQC, as shown in Fig. 11, while in Fig. 12, the results of the third test considering the three-phase load 2 (see Table II) are presented. It is possible to notice from the tests presented in Figs. 10–12 that, regardless of the type of load fed, the static behaviors of the grid current (i_s) and output voltages (v_{La}, v_{Lb}, and v_{Lc}) are similar to each other.

For tests 1 and 2, thecompensation current i_{cpa} is composed of nonactive components (harmonic and reactive) involved in the load current compensation (phase "*a*"), as well as of active

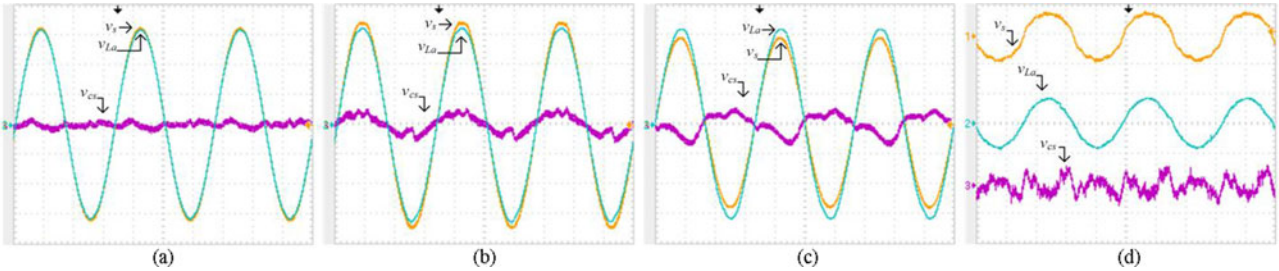

Fig. 13. UPQC-1Ph-to-3Ph operating with the set of single-phase loads 2: Voltages of the grid v_s and load v_{La} (50 V/div, 5 ms/div) and voltage of the series coupling transformer v_{Cs} (20 V/div, 5 ms/div): (a) $V_s \cong V_{La}$, (b), $V_s > V_{La}$, (c) $V_s < V_{La}$; (d) $V_s \cong V_{La}$: v_s and v_{La} (200 V/div, 5 ms/div) and v_{Cs} (50 V/div, 5 ms/div).

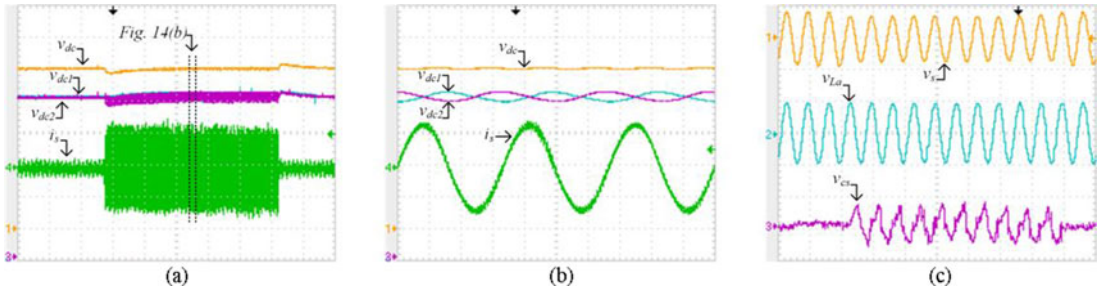

Fig. 14. Dynamic tests of the UPQC-1Ph-to-3Ph: (a) Load transients (Load 1Φ 2) (2.5 s/div): total dc-bus voltage (100 V/div 2.5 s/div), dc-bus capacitors' voltages (50 V/div), and grid current (20 A/div); (b) Detail of (a) (5 ms/div); (c) Voltage sag (25 ms/div): grid voltage v_s (200 V/div), load voltage v_{La} (176 V/div), and series transformer voltage v_{Cs} (50 V/div).

components of current destined to the feeding of phases "*b*" and "*c*." For test 3, since it is a three-phase induction motor, the current i_{cpa} is predominantly composed of active and reactive fundamental components of current.

Table IV presents the THDs of the current and voltage quantities for all the performed experiments. The THDs were measured using a power quality analyzer (PQA) (Fluke 43B). It is observed that in all cases the THDs of the grid current and of the load voltages are below than 5%.

Table V shows the powers and the power factors measured in the loads (*L*) and in the grid (*G*), also using the same PQA (Fluke 43B).

It was considered the powers in the grid, as well as in each of the phases (*abc*) connected to the load, in which the apparent powers (*S*), the active powers (*P*), and the nonactive powers (*N*) were measured. The power *N* (VAr) defined in [23] includes all the powers that are not active, i.e., the reactive and/or harmonic powers.

The PF and the fundamental PF (PF1) [23], also known as the displacement factor, are also shown in Table V. It can be noticed that the PF in the grid is very close to one considering all the performed experiments.

The static behavior of the UPQC voltages can be observed in Fig. 13, in which the phase "*a,*" load voltage v_{La}, the grid/input voltage v_s, and the voltage across the terminals of the series transformer v_{Cs} are shown. In Fig. 13(a)–(c), the rms voltage values are distinct between the grid and the voltage of phase "*a,*" i.e.,$V_s \cong V_{La}$, $V_s > V_{La}$, and $V_s < V_{La}$. In Fig. 13(d), the grid voltage was emulated by an ac voltage source (FCATH 450-22-50, Supplier), in which 12% of THD was introduced. In this case, the calculated THD (%) of the load voltage was 4% (phase "*a*"). It is possible to notice that the difference between the grid voltage and the voltage of phase "*a*" of the load appears on the terminals of the series coupling transformer (v_{Cs}). This voltage is composed of harmonics and fundamental components.

Fig. 14 presents some experimental results that allow to evaluate the dynamic behavior of UPQC-1Ph-to-3Ph, by using the set of single-phase loads 2 (Load 1Φ 2) described in Table II. The grid current (i_s) and the dc-bus voltages ($v_{\rm dc}$, v_{dc1}, and v_{dc2}) are shown in Fig. 14(a), in which the dynamic responses of the dc-bus voltages considering load transients can be observed. It can be noted that the action of the dc-bus voltage controller on the grid current is to keep the dc-bus voltage constant at 500 V. The balance of the dc-bus voltages across the capacitors can be observed in detail in Fig. 14(b). As can be noted, the experimental results shown in Fig. 14(b) were obtained from Fig. 14(a). Fig. 14(c) shows the existence of a voltage sag equivalent to 15% of the nominal grid voltage during ten cycles (0.166 ms). It is observed that during the voltage sag, the output voltage at phase "*a*" remains unchanged, which indicates that it is not affected by the disturbance. The series transformer voltage (v_{Cs}) shows the behavior of the system related to the disturbance.

VI. Conclusion

This paper presented the study and the experimental validation of a local 3P4W power distribution system. The system, indicated for applications in rural or remote areas where three-phase distribution grids are not accessible, was conceived based on UPQC functionalities.

With serial and parallel filtering capability, two inverter topologies were used to compose the UPQC-1Ph-to-3Ph. Thereby, the single-phase series converter was deployed using

a half-bridge inverter, while the three-phase parallel converter was implemented using a three-leg split capacitor inverter.

Using the dual compensation strategy, the proposed system was able of feeding linear and nonlinear three-phase loads acting with universal active filtering capability, i.e., acting as SAPF and PAPF.

In addition, a procedure was presented that allows the dimensioning the power structures of the series and parallel converters under various operating conditions of the utility grid and the load. The good static and dynamic behavior of the UPQC-1Ph-to-3Ph has been proven through extensive experimental results.

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