Modular Multilevel Converter Control Strategy Based on Arm Current Control Under Unbalanced Grid Condition

Zhujian Ou, Guangzhu Wang, *Member, IEEE*, and Lanhua Zhang, *Member, IEEE*

***Abstract*—The existing control strategies of modular multilevel converter (MMC) balance the capacitor voltage on the premise that the active power of ac side is balanced with that of dc bus. Thus, the symmetrical ac-side current references and the unevenly distributed dc current references in three legs are obtained by coordinate transformation, precise calculation, and numerous filters under unbalanced grid condition. However, by controlling capacitor voltages, the active powers between ac side and dc bus can self-regulate to balance, and this could simplify the obtainment of ac-side current references and dc-bus current references. Based on this idea, this paper proposed a control strategy, which combines the multi-hierarchy control with the arm current control for MMC under unbalanced grid condition. Within the multi-hierarchy control, the symmetrical ac-side current references and the unevenly distributed dc current references in three legs could be obtained easily by three voltage controllers in the abc coordinate, avoiding coordinate transformation, precise calculation, and numerous filters in the existing methods. Besides, the employment of the arm current control removes the need of the three-sequence ac-side current controllers and the three-sequence circulating current suppressing controllers. The proportional regulator with a feedforward steady-state duty cycle is designed for arm current regulator, which can perfectly track its reference and is easy to design, avoiding the complicated design of proportional resonant (PR) controllers. Both system-level simulation results and low-level experiment results verify the feasibility and effectiveness of proposed strategy.**

***Index Terms*—Arm current control, circulating current, modular multilevel converter (MMC), multi-hierarchy control, unbalanced grid condition.**

I. Introduction

THE modular multilevel converter (MMC) was introduced by Lesnicar and Marquardt in 2003 [1]. This converter possesses merits as upgraded capacity, lower switching frequency, lower output harmonics, modular design, and so on. Thus, it is suitable for medium-/high-voltage applications, such as high-power motor drives [2], [3], unified power flow controller (UPFC) [4], grid-connected inverter [5], and high-voltage direct current transmission (HVDC) [6]–[23]. However, it has demerits as capacitor voltage balancing and circulating current.

Multiple modulation strategies are applied as the bottom-level modulation strategies to balance the capacitor voltage, such as phase disposition pulsewidth modulation (PD-PWM) [6], [7], nearest-level modulation (NLM) [8]–[10], and phase-shifted carriers pulse width modulation (PSC-PWM) [17]–[20]. Based on these modulation strategies, conventional ac-side current feedback control method applied in two-level converter is adopted in MMC [3]–[17]. However, since the ac-side current is only the summation of the upper and the lower arm currents, simply controlling ac-side current will leave the current component with opposite polarity in the upper and the lower arms uncontrolled, e.g., circulating current. Thus, the circulating current suppressing controllers are designed.

Under unbalanced grid condition, the control of MMC is more complex. Symmetrical ac-side currents and zero power ripples in dc bus can be achieved simultaneously because the capacitors in MMC could absorb all the active power ripples in ac side. To control MMC properly, the following controllers are indispensable. First, the dual vector current control (DVCC) scheme is needed to eliminate the negative-sequence current in ac side [6], [11], [12]. Second, the zero-sequence current canceller is needed for ac side in event of asymmetrical faults on the converter side of the transformer or in a transformerless scheme [12], [13]. Third, circulating current suppressing controllers should be designed to eliminate the three-sequence circulating currents [13]–[16]. Under unbalanced grid condition, the dc current is no longer averagely distributed among three legs, and this increases the difficulty to extract the circulating current from the arm current [16], [21]–[23]. What's more, dc-bus voltage ripple suppressing controller is needed [11], [13]. However, since ac-side power ripples are manifested as the zero-sequence circulating currents, the dc-bus voltage ripple suppressing controller can be removed if circulating currents are well suppressed [16], [21]–[23]. The comprehensive control is rather complicated when conventional ac-side current feedback control is applied under unbalanced grid condition [21], [22].

However, the arm current contains all the current messages in MMC, including the three-sequence ac-side currents, dc-bus

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current, and the three-sequence circulating currents. Controlling the arm current will realize the control of the above currents [19]. The comprehensive control strategy based on arm current control was first given in [20]. However, the strategy in [20] is not suitable for unbalanced grid condition because none of the control targets in [22] is satisfied. Moon *et al*. [21] proposed the MMC control strategy based on arm current control under unbalanced grid condition. This paper focused on eliminating the active power ripples of ac grid and adopted the proportional resonant (PR) controllers as the arm current controller. However, the ac-side currents in this paper are seriously asymmetrical, which will cause the protective devices malfunction [13]. Liang *et al*. [22] proposed a PI plus vector proportional integral (VPI) controller, which has a better performance and stability margin than the PR controller. Ou *et al*. [23] presented two control strategies based on arm current control for MMC under unbalanced grid condition. This paper is inadequate in analysis and short of experiment results. To the authors' best knowledge, all the control strategies proposed for unbalanced grid condition until now were verified only by simulations, and short of experiment verification.

The capacitor is a key component in MMC. The existing control strategies, including ac-side current feedback control and arm current control both balance the capacitor voltages on the premise that the active power of ac side is balanced with that of dc bus. In this situation, the ac-side current references are precisely calculated by the active power and the reactive power references in *dq* SRF with coordinate transformation [12], [13], [16], [21], [22], and the dc current references in three legs of MMC are calculated by the measured ac-side voltages and currents with three low-pass filters [21], [22]. However, by controlling the capacitor voltages, the active powers between ac grid and dc bus can self-regulate to balance, and this could simplify the obtainment of the symmetrical ac-side currents and the unevenly distributed dc currents in three legs. Based on this idea, this paper analyzed the active power in MMC and proposed a comprehensive control strategy combined the arm current control with the multi-hierarchy control for MMC under unbalanced grid condition. In this strategy, the ac-side currents are controlled to be symmetrical by adjusting active power distribution among three legs. The symmetrical ac-side current references and the unevenly distributed dc current references in three legs are obtained by average voltage controllers of three legs in the abc frame, avoiding the coordinate transformation, precise calculation, and numerous filters in the existing methods. Besides, the employment of the arm current control removes the need of the three-sequence ac-side current controllers and the three-sequence circulating current suppressing controllers. The proportional regulator with a feedforward steady-state duty cycle is applied for arm current regulator, which perfectly tracks its reference. Both simulation and experiment results verify the feasibility and effectiveness of the proposed strategy.

The rest of this paper is organized as follows. In Section II, power analysis of MMC is done to elicit the control strategy and to choose appropriate control variables for dc-bus voltage and capacitor voltage. Detailed control strategies are shown in Section III, including arm current control, multi-hierarchy control, and the comprehensive control strategy. Simulations and experiments are, respectively, presented in Sections IV and V. Section VI concludes this paper.

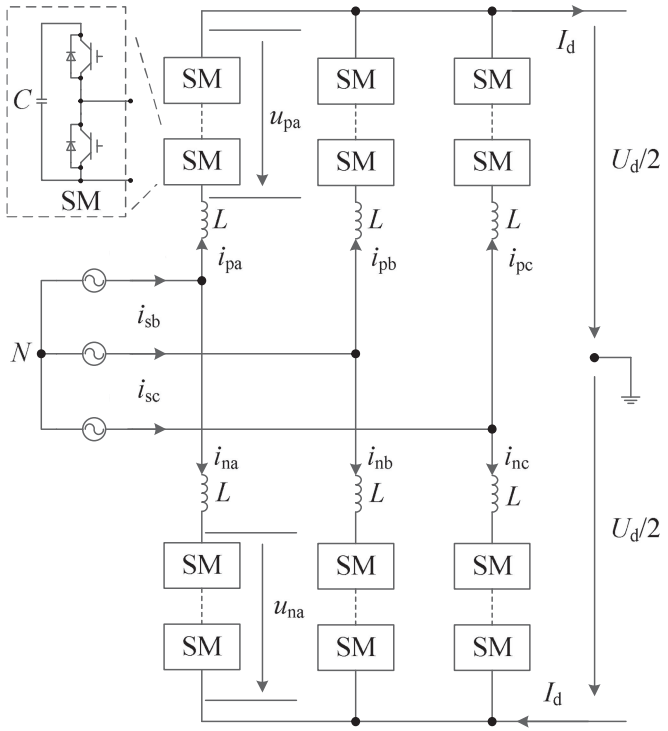

Fig. 1. Basic structure of MMC.

II. Power Analysis of MMC

The basic structure of MMC is shown in Fig. 1. Each phase contains an upper arm and a lower arm. The upper arm and the lower arm of a phase form a leg. Each arm is constituted by *N* submodules (SMs) connected with an inductor *L*. $u_{\mathrm{p}x}$ and $u_{\mathrm{n}x}$ ($x = \mathrm{a}, \mathrm{b}, \mathrm{c}$) are the output voltages of the upper and the lower arms, respectively. $i_{\mathrm{p}x}$ and $i_{\mathrm{n}x}$ are, respectively, the upper and the lower arm currents. $u_{\mathrm{s}x}$ and $i_{\mathrm{s}x}$ are, respectively, the ac-side voltage and current. U_{d} and I_{d} are, respectively, the dc-bus voltage and current.

The capacitor of SM is the only energy-storage element except the arm inductor in MMC. When an arm absorbs active power, the voltages of arm capacitors will rise. When an arm outputs active power, the voltages of arm capacitors will fall. Thus, the voltages of arm capacitors can be controlled if active power absorbed by an arm is controlled. In order to elicit the control strategy and choose appropriate control variables for dc bus and capacitor voltages, power analysis is done first.

In steady state, ignoring the influences of arm inductances, the relationship of voltages can be obtained as follows:

$$\begin{cases} u_{\mathrm{p}x} \approx U_d/2 - u_{\mathrm{s}x} \\ u_{\mathrm{n}x} \approx U_d/2 + u_{\mathrm{s}x} \end{cases}. \tag{1}$$

The upper and the lower arm currents $i_{\mathrm{p}x}$ and $i_{\mathrm{n}x}$ satisfy

$$\begin{cases} i_{\mathrm{p}x} = i_{\mathrm{sp}x} + i_{\mathrm{diff}x} = i_{\mathrm{sp}x} + I_{\mathrm{d}x} + i_{\mathrm{cir}\_x} \\ i_{\mathrm{n}x} = i_{\mathrm{sn}x} - i_{\mathrm{diff}x} = i_{\mathrm{sn}x} - I_{\mathrm{d}x} - i_{\mathrm{cir}\_x} \end{cases} \tag{2}$$

where $i_{\mathrm{sp}x}$ and $i_{\mathrm{sn}x}$ are the parts of ac-side current; $i_{\mathrm{diff}x}$ is the inner unbalanced current, containing the dc current component $I_{\mathrm{d}x}$ and the circulating current i_{cir_x}. Relationship between ac-side current and arm currents satisfies

$$i_{\mathrm{s}x} = i_{\mathrm{p}x} + i_{\mathrm{n}x} = i_{\mathrm{sp}x} + i_{\mathrm{sn}x}. \tag{3}$$

DC-bus current I_{d} satisfies the following equation:

$$I_d = \frac{1}{2}\left[(i_{\mathrm{pa}} - i_{\mathrm{na}}) + (i_{\mathrm{pb}} - i_{\mathrm{nb}}) + (i_{\mathrm{pc}} - i_{\mathrm{nc}})\right] = I_{\mathrm{da}} + I_{\mathrm{db}} + I_{\mathrm{dc}}. \tag{4}$$

Currents $i_{\mathrm{sp}x}$, $i_{\mathrm{sn}x}$, $I_{\mathrm{d}x}$, and i_{cir_x} satisfy

$$\begin{cases} \int_0^T U_d i_{\mathrm{sp}x} dt = 0 \\ \int_0^T U_d i_{\mathrm{sn}x} dt = 0 \\ \int_0^T U_d i_{\mathrm{cir}\_x} dt = 0 \\ \int_0^T u_{\mathrm{s}x} i_{\mathrm{cir}\_x} dt = 0 \\ \int_0^T u_{\mathrm{s}x} I_{\mathrm{d}x} dt = 0 \end{cases} \tag{5}$$

where T is the period of ac-gird. Thus, (6) can be derived from the law of energy conservation according to (5)

$$P_{\mathrm{s}x} = P_{\mathrm{d}x} + P_{\mathrm{p}x} + P_{\mathrm{n}x} \tag{6}$$

where $P_{\mathrm{s}x}$ is the active power absorbed from ac grid; $P_{\mathrm{d}x}$ is the active power flowing into dc bus; $P_{\mathrm{p}x}$ and $P_{\mathrm{n}x}$ are, respectively, the active power absorbed by the upper and the lower arms of MMC. Each power can be expressed as

$$\begin{cases} P_{\mathrm{s}x} = \frac{1}{T}\int_0^T u_{\mathrm{s}x} i_{\mathrm{s}x} dt \\ P_{\mathrm{d}x} = \frac{1}{T}\int_0^T U_d I_{\mathrm{d}x} dt \end{cases} \tag{7}$$

$$\begin{cases} P_{\mathrm{p}x} = -\frac{1}{T}\int_0^T u_{\mathrm{p}x} i_{\mathrm{p}x} dt = -\frac{1}{T}\int_0^T \frac{U_d}{2} I_{\mathrm{d}x} dt + \frac{1}{T}\int_0^T u_{\mathrm{s}x} i_{\mathrm{sp}x} dt \\ P_{\mathrm{n}x} = \frac{1}{T}\int_0^T u_{\mathrm{n}x} i_{\mathrm{n}x} dt = -\frac{1}{T}\int_0^T \frac{U_d}{2} I_{\mathrm{d}x} dt + \frac{1}{T}\int_0^T u_{\mathrm{s}x} i_{\mathrm{sn}x} dt \end{cases}. \tag{8}$$

A. Two Control Strategies

If device loss of MMC is ignored, i.e.,

$$P_{\mathrm{p}x} = P_{\mathrm{n}x} \approx 0 \tag{9}$$

then the active power absorbed from ac-grid and output to dc bus by MMC should be equivalent. For convenience, (10) is shown in the form of phases a, b, and c

$$\begin{cases} P_{\mathrm{sa}} = P_{\mathrm{da}} \Rightarrow \frac{1}{T}\int_0^T u_{\mathrm{sa}} i_{\mathrm{sa}} dt = \frac{1}{T}\int_0^T U_d I_{\mathrm{da}} dt \\ P_{\mathrm{sb}} = P_{\mathrm{db}} \Rightarrow \frac{1}{T}\int_0^T u_{\mathrm{sb}} i_{\mathrm{sb}} dt = \frac{1}{T}\int_0^T U_d I_{\mathrm{db}} dt \\ P_{\mathrm{sc}} = P_{\mathrm{dc}} \Rightarrow \frac{1}{T}\int_0^T u_{\mathrm{sc}} i_{\mathrm{sc}} dt = \frac{1}{T}\int_0^T U_d I_{\mathrm{dc}} dt \end{cases}. \tag{10}$$

Under unbalanced grid condition, ac-grid voltage will be asymmetrical. On this basis, two control strategies of MMC could be deduced from (10).

1) Strategy One: Ensure that $I_{\mathrm{da}} = I_{\mathrm{db}} = I_{\mathrm{dc}} = I_{\mathrm{d}}/3$, whereas i_{sa}, i_{sb}, and i_{sc} are asymmetrical.

Since $I_{\mathrm{da}} = I_{\mathrm{db}} = I_{\mathrm{dc}}$, according to (10), relationships among active powers should satisfy

$$P_{\mathrm{da}} = P_{\mathrm{db}} = P_{\mathrm{dc}} \Rightarrow P_{\mathrm{sa}} = P_{\mathrm{sb}} = P_{\mathrm{sc}} \Rightarrow \frac{1}{T}\int_0^T u_{\mathrm{sa}} i_{\mathrm{sa}} dt = \frac{1}{T}\int_0^T u_{\mathrm{sb}} i_{\mathrm{sb}} dt = \frac{1}{T}\int_0^T u_{\mathrm{sc}} i_{\mathrm{sc}} dt. \tag{11}$$

According to (11), since u_{sa}, u_{sb}, u_{sc} are asymmetrical, ac-side currents i_{sa}, i_{sb}, i_{sc} will be asymmetrical too. Protective devices may malfunction if relatively serious negative-, or zero-sequence currents are detected [13]. Thus, this strategy is not suitable for unbalanced grid condition. However, it works well under balanced grid condition.

2) Strategy Two: Ensure that i_{sa}, i_{sb}, i_{sc} are symmetrical, whereas $I_{\mathrm{da}} \neq I_{\mathrm{db}} \neq I_{\mathrm{dc}}$.

If i_{sa}, i_{sb}, i_{sc} are controlled to be symmetrical, then active power absorbed by three legs of MMC from ac-grid will be unequal since u_{sa}, u_{sb}, u_{sc} are asymmetrical, then exists

$$P_{\mathrm{sa}} \neq P_{\mathrm{sb}} \neq P_{\mathrm{sc}} \Rightarrow P_{\mathrm{da}} \neq P_{\mathrm{db}} \neq P_{\mathrm{dc}} \Rightarrow \frac{1}{T}\int_0^T U_d I_{\mathrm{da}} dt \neq \frac{1}{T}\int_0^T U_d I_{\mathrm{db}} dt \neq \frac{1}{T}\int_0^T U_d I_{\mathrm{dc}} dt \Rightarrow I_{\mathrm{da}} \neq I_{\mathrm{db}} \neq I_{\mathrm{dc}}. \tag{12}$$

On the basis of not affecting I_{d}, adjusting dc current distribution among three legs of MMC can realize the adjustment of active power distribution among three legs; thus, the ac-side currents can be controlled to be symmetrical. Thus, power relationship in (12) is realized. This strategy is suitable for both balanced and unbalanced grid conditions.

B. Control Variables for DC-Bus Voltage and Capacitor Voltage

From (7), active power issued from ac-grid can be regulated by adjusting ac-side active currents; if dc-bus voltage remains constant, the active power transmitted to dc bus can be regulated by adjusting dc current.

From (8), average active powers of the upper and the lower arms are constituted by two parts. The first part is relevant to $I_{\mathrm{d}x}$; the second part is relevant to $i_{\mathrm{sp}x}$ and $i_{\mathrm{sn}x}$. By controlling either $I_{\mathrm{d}x}$ or $i_{\mathrm{sp}x}$ (and $i_{\mathrm{sn}x}$) can realize the control of $P_{\mathrm{p}x}$ and $P_{\mathrm{n}x}$, thereby controlling the capacitor voltages.

In general case, $i_{\mathrm{sp}x}$ and $i_{\mathrm{sn}x}$ are set equal, that is

$$i_{\mathrm{sp}x} = i_{\mathrm{sn}x} = i_{\mathrm{s}x}/2. \tag{13}$$

However, when taking asymmetrical device loss of the upper and the lower arms into consideration, there should be a fine-tuning of ac-side current distribution in the upper and the lower arms, thus $\Delta i_{\mathrm{s}x\mathrm{P}}$ in (14) is introduced. The frequency and phase angle of $\Delta i_{\mathrm{s}x\mathrm{P}}$ are the same as $u_{\mathrm{s}x}$ and satisfy

$$P_{\mathrm{p}x} - P_{\mathrm{n}x} = \frac{1}{T}\int_0^T u_{\mathrm{s}x}\left(i_{\mathrm{sp}x} - i_{\mathrm{sn}x}\right) dt = \frac{1}{T}\int_0^T u_{\mathrm{s}x} \Delta i_{\mathrm{s}x\mathrm{P}} dt. \tag{14}$$

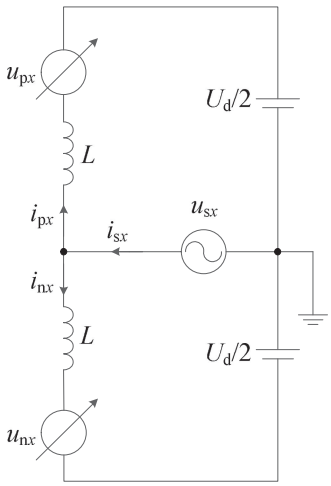

Fig. 2. Single-phase equivalent circuit of MMC.

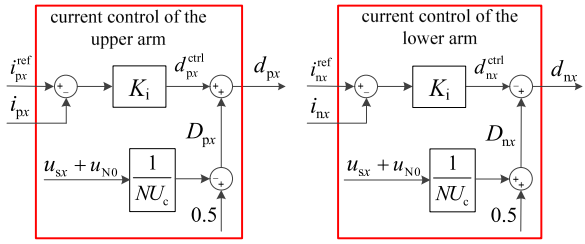

Fig. 3. Arm current control scheme.

In fact, device loss differences exist among all submodules of an arm, so fine-tuning of active power of each submodule should be designed or the NLM should be adopted to realize the balance of capacitor voltages within an arm.

III. Control Method

A. Arm Current Control Method

Fig. 2 shows the single phase equivalent circuit of MMC. In Fig. 2, the upper and the lower arms are similar and are almost independent of each other; thus, the upper and the lower arm currents i_{px} and i_{nx} can be controlled directly by corresponding PWM duty cycles. From (3) and (4), ac-side currents and dc-bus current can be controlled only if arm currents are controlled. At the same time, it does not require a circulating current suppressing controller.

Arm current control scheme of MMC is shown in Fig. 3. In Fig. 3, U_c is the rated voltage of capacitor; i_{px}^{ref} and i_{nx}^{ref} are, respectively, the upper and the lower arm current references of phase x; u_{N0} is the zero-sequence voltage, and it could be

$$u_{N0} = -0.5\left[\max\left(u_{sa}, u_{sb}, u_{sc}\right) + \min\left(u_{sa}, u_{sb}, u_{sc}\right)\right]. \tag{15}$$

D_{px} and D_{nx} in Fig. 3 are steady-state PWM duty cycles of the upper and the lower arms used as feedforward variables; d_{px}^{ctrl} and d_{nx}^{ctrl} are the duty cycles output by the upper and the lower arm current controllers; d_{px} and d_{nx} are PWM duty cycles

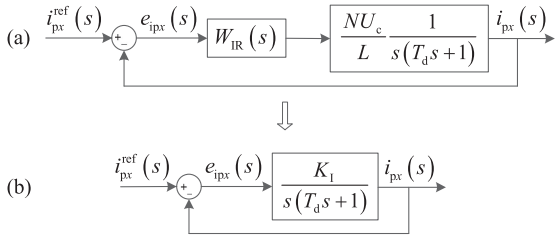

Fig. 4. Arm current controller design method.

of the upper and the lower arms. Duty cycles satisfy

$$\begin{cases} d_{px} = D_{px} + d_{px}^{ctrl} \\ d_{nx} = D_{nx} - d_{nx}^{ctrl} \end{cases} \tag{16}$$

where

$$\begin{cases} D_{px} = \dfrac{0.5U_d - (u_{sx} + u_{N0})}{NU_c} = 0.5 - \dfrac{u_{sx} + u_{N0}}{NU_c} \\ D_{nx} = \dfrac{0.5U_d + (u_{sx} + u_{N0})}{NU_c} = 0.5 + \dfrac{u_{sx} + u_{N0}}{NU_c} \end{cases}. \tag{17}$$

Arm voltages are controlled by applying the modulation method (e.g., PSC-PWM, NLM, etc.) with the duty cycles in (16).

The detailed design procedure of arm current regulator refers to [19]. Different from [19], calibrating the closed-loop control diagram in Fig. 4(a) as the one in Fig. 4(b), the current controller could be a proportional controller as

$$W_{IR}(s) = K_i = \frac{L}{3T_d NU_c} \tag{18}$$

where T_d is the time delay of control system. From Fig. 4(b), the steady-state error is expressed as

$$\left|e_{ipx}(j\omega)\right| = \left|i_{px}^{ref}(j\omega)\right| \frac{1}{\left|1+\frac{K_I}{j\omega(j\omega T_d+1)}\right|}. \tag{19}$$

In experiments of this paper, $T_d = 25\,\mu s$, $K_I = 1/(3T_d)$. For sine wave with frequency of 50 Hz, $\omega_1 = 100\pi$. Putting it into (19), then the steady-state error is obtained as

$$\left|e_{ipx}(j\omega_1)\right| \approx \left|i_{px}^{ref}(j\omega_1)\right|/43. \tag{20}$$

As for sine wave with frequency of 100 Hz, $\omega_2 = 200\pi$ (e.g., circulating current)

$$\left|e_{ipx}(j\omega_2)\right| \approx \left|i_{px}^{ref}(j\omega_2)\right|/22. \tag{21}$$

The steady-state errors are small enough in practice.

B. Control of DC-Bus Voltage and Capacitor Voltage

Strategy two in Section II-A2 is adopted here to control the MMC under unbalanced grid condition.

1) DC-Bus Voltage Control: From (10), active power flowing into dc bus and absorbed from the ac grid of each phase are equivalent. Thus, controlling ac-side current i_{sx} could indirectly control the dc-bus voltage. If so, the magnitudes of ac-side currents references can be set identical directly. Combined with the control in the following Section III-B2, the ac-side currents

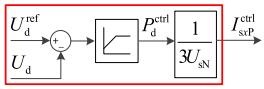

Fig. 5. DC-bus voltage control.

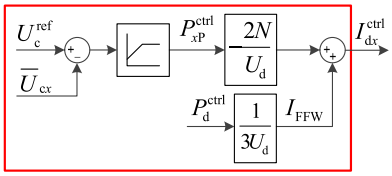

Fig. 6. Average voltage control of a leg.

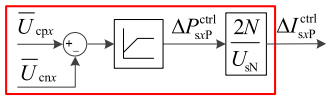

Fig. 7. Voltage control between the upper and the lower arms.

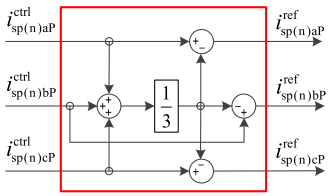

Fig. 8. Zero-sequence current canceller.

could be controlled to be symmetrical automatically under unbalanced grid condition. So the ac-side current i_{sx} is chosen to control dc bus, as shown in Fig. 5. In Fig. 5, $P_d^{\rm ctrl}$ is the output active power of controller, $U_{\rm sN}$ is the root-mean-square (RMS) value of the ac-side phase voltage, and $I_{\rm sxP}^{\rm ctrl}$ is the RMS value of ac-side active current reference.

Taking active power balance between ac side and dc bus into consideration, $P_d^{\rm ctrl}$ could be used as a feedforward signal of dc component of arm current to improve the dynamic property, i.e.,

$$I_{\rm FFW} = P_d^{\rm ctrl} / (3U_d). \tag{22}$$

2) Capacitor Voltage Control: Multi-hierarchy control is adopted to balance the capacitor voltage.

The first hierarchy is average voltage control of a leg, which keeps capacitors' average voltage of a leg balanced with its rated value. Since i_{sx} is chosen to control dc bus voltage, $I_{{\rm d}x}$ is chosen to control capacitor voltage here. In this situation, dc current (namely power) distribution among three legs of MMC will be automatically adjusted according to the active power absorbed from the ac grid by each leg. Taking the feedforward signal in (22) into consideration, average voltage control of a leg is shown in Fig. 6. In Fig. 6, $\overline{U}_{{\rm c}x}$ is the average voltage of leg x, $U_c^{\rm ref}$ is the corresponding reference value, $P_{x{\rm P}}^{\rm ctrl}$ is the output of controller, and $I_{{\rm d}x}^{\rm ctrl}$ is the dc current reference of phase x. By adjusting the distribution of dc currents among three legs, the symmetrical ac-side current references and the unevenly distributed dc current references of three legs are obtained.

The second hierarchy is voltage control between the upper and the lower arms, which keeps the average voltage of the upper arm balanced with that of the lower arm. This hierarchy can perfectly resolve the asymmetry problem of the upper arm and the lower arm, especially in experiment with a small amount of SMs or when taken asymmetry inductance of each arm into consideration. However, when the MMC operates in high-voltage situation with hundreds of SMs and ignores the asymmetry inductance of each arm, this hierarchy can be removed. This hierarchy is realized by controlling $\Delta i_{sx{\rm P}}$, as shown in Fig. 7. In Fig. 7, $\overline{U}_{{\rm cp}x}$ and $\overline{U}_{{\rm cn}x}$ are, respectively, the average voltages of the upper and the lower arm of phase x and $\Delta P_{\rm sxP}^{\rm ctrl}$ is the output of the controller.

The third hierarchy is the balance control of the capacitor voltages within an arm. It could be achieved by NLM, or the fine-tuning control combined with PSC [19], [20], [23].

3) Active Current References of the Upper and the Lower Arms: From the aforementioned analysis, the active current references of the upper and the lower arms can be obtained as

$$\begin{cases} I_{{\rm sp}x{\rm P}}^{\rm ctrl} = 0.5\left(I_{\rm sxP}^{\rm ctrl} + \Delta I_{\rm sxP}^{\rm ctrl}\right) \\ I_{{\rm sn}x{\rm P}}^{\rm ctrl} = 0.5\left(I_{\rm sxP}^{\rm ctrl} - \Delta I_{\rm sxP}^{\rm ctrl}\right) \end{cases} \tag{23}$$

where $I_{{\rm sp}x{\rm P}}^{\rm ctrl}$ and $I_{{\rm sn}x{\rm P}}^{\rm ctrl}$ are the RMS values of ac active current components of the upper and the lower arm current references. The RMS values can be transformed to be instantaneous values as

$$\begin{cases} i_{{\rm sp}x{\rm P}}^{\rm ctrl} = I_{{\rm sp}x{\rm P}}^{\rm ctrl} \cdot \sin_x \\ i_{{\rm sn}x{\rm P}}^{\rm ctrl} = I_{{\rm sn}x{\rm P}}^{\rm ctrl} \cdot \sin_x \end{cases} \tag{24}$$

where $\sin_x$ is the phase message of u_{sx}, which can be obtained by a phase-locked loop (PLL).

4) Zero-Sequence Current Canceller: As shown in (23), asymmetrical device loss of each arm will cause

$$\Delta I_{\rm saP} \neq \Delta I_{\rm sbP} \neq \Delta I_{\rm scP}. \tag{25}$$

According to (23), (24), and (25), asymmetrical device loss will generate zero-sequence fundamental-frequency current which will flow into dc bus. To prevent the zero-sequence fundamental-frequency current flowing into the dc bus, a zero-sequence current canceller is designed, as in Fig. 8. Since this current canceller exists accompanied with the voltage control between the upper and the lower arms, if the voltage control between the upper and the lower arms is omitted, as discussed in Section III-B2, then this current canceller can be removed too.

C. Comprehensive Control Strategy

Based on the aforementioned dc-bus voltage control and capacitor voltage control, the upper and the lower arm reference currents of phase x can be obtained according to (2)

$$\begin{cases} i_{{\rm p}x}^{\rm ref} = i_{{\rm sp}x{\rm P}}^{\rm ref} + 0.5 i_{{\rm s}x{\rm Q}}^{\rm ref} + I_{{\rm d}x}^{\rm ref} + i_{{\rm cir}\_x}^{\rm ref} \\ i_{{\rm n}x}^{\rm ref} = i_{{\rm sn}x{\rm P}}^{\rm ref} + 0.5 i_{{\rm s}x{\rm Q}}^{\rm ref} - I_{{\rm d}x}^{\rm ref} - i_{{\rm cir}\_x}^{\rm ref} \end{cases} \tag{26}$$

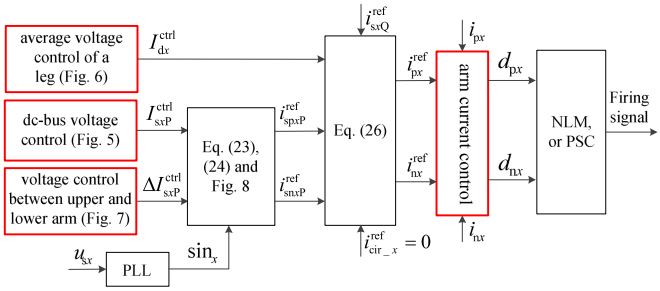

Fig. 9. Proposed control strategy for MMC.

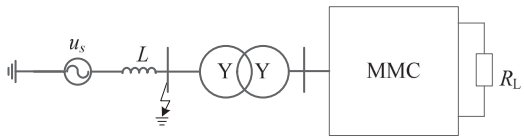

Fig. 10. Grid fault scheme in the simulation.

TABLE I
CIRCUIT PARAMETERS IN SIMULATIONS

Items	Values
Rated power P_{N}	600 MW
Rated RMS line-to-line voltage of ac side U_{s}	230 kV
Rated voltage of dc bus U_{d}	600 kV
SM capacitor voltage U_{c}	2.4 kV
Arm inductance L	60 mH
SM capacitance C	15 mF
Resistance of dc bus R_{L}	600 Ω
Number of SMs per arm N	250
Carrier frequency f	80 Hz
Arm current controller K_{i}	1.333
DC-bus controller K_{bus}	1.667
DC-bus controller T_{bus}	0.00025 s
Capacitor voltage controller K_{c}	1.543
Capacitor voltage controller T_{c}	0.07 s

where $i_{sx\mathrm{Q}}^{\mathrm{ref}}$ is the reactive reference current of ac side and $i_{\mathrm{cir}\_x}^{\mathrm{ref}}$ is the reference circulating current. In a general case, reference circulating current should be set to zero, i.e., $i_{\mathrm{cir}\_x}^{\mathrm{ref}} = 0$, which also means omissible. However, when MMC works under no-load condition, circulating current could be set to an appropriate value to provide arm current for realizing the voltage balance of submodules. The complete control strategy is shown in Fig. 9.

IV. SIMULATION RESULTS

In order to verify the proposed control strategy in system-level performance, simulations are carried out by PSCAD/EMTDC. The grid fault scheme is designed as shown in Fig. 10. The single-phase to ground fault happens in phase a at $t = 1.0\,\mathrm{s}$. In these simulations, NLM is adopted as the third hierarchy to balance the capacitor voltages within an arm. Parameters in the simulations are shown in Table I.

Fig. 11 shows the arm current tracking results of phase a respectively before and after the fault happens. It is clear from Fig. 11 that the arm current perfectly tracks its reference with almost zero tracking error whether before or after the faults. This shows the effectiveness of the arm current regulator, which

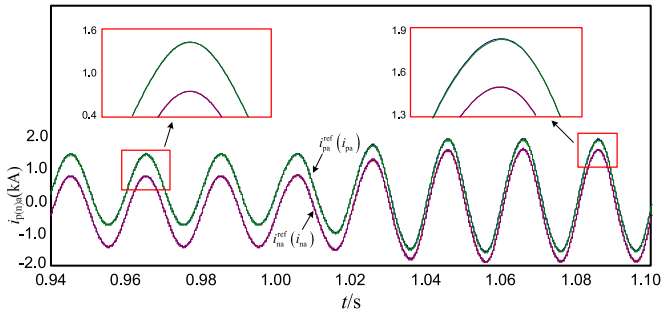

Fig. 11. Arm current tracking result.

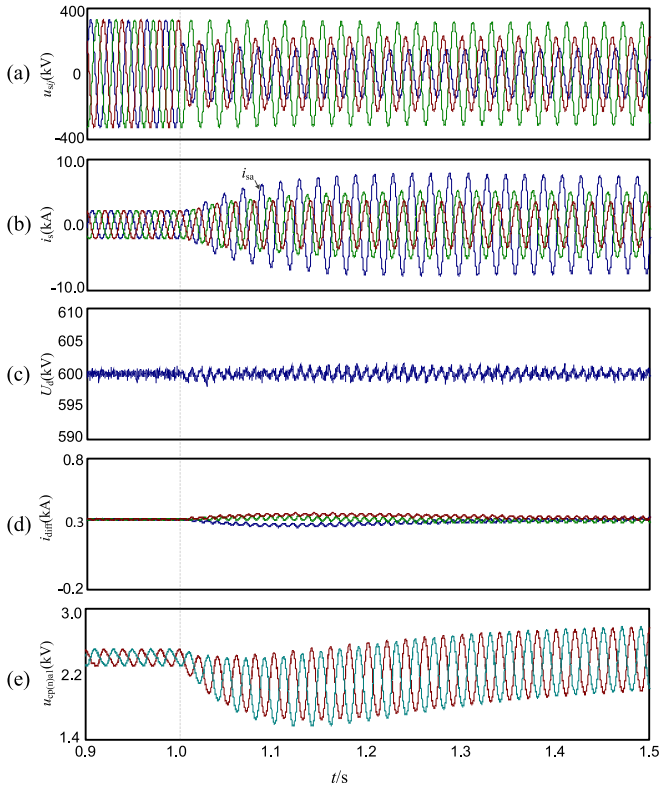

Fig. 12. Simulation results when control strategy in [20] is adopted. (a) Line-to-line voltages of ac grid; (b) ac-side currents; (c) dc-bus voltage; (d) inner unbalanced currents of three phases; (e) the voltages of the first capacitor of, respectively, the upper and the lower arms in phase a.

is composed by the proportional regulator with a feedforward steady-state duty cycle.

Fig. 12 shows the simulation results when control strategy in [20] is adopted. The idea of this control strategy is the same with the one in Section II-A1, which ensures that the dc current is evenly distributed among three legs. As a result, the ac-side current will be asymmetrical under unbalanced grid condition. Fig. 12(a) shows the line-to-line voltage of ac side before and after the single-line-to-ground fault happens. In Fig. 12(b), the ac-side currents become asymmetrical when fault happens and the current of phase a increases apparently larger than those of phases b and c. The ac-side current relationship is in accordance with the analysis in Section II-A1. The dc-bus voltage is shown in Fig. 12(c). There is a small fluctuation with double frequency

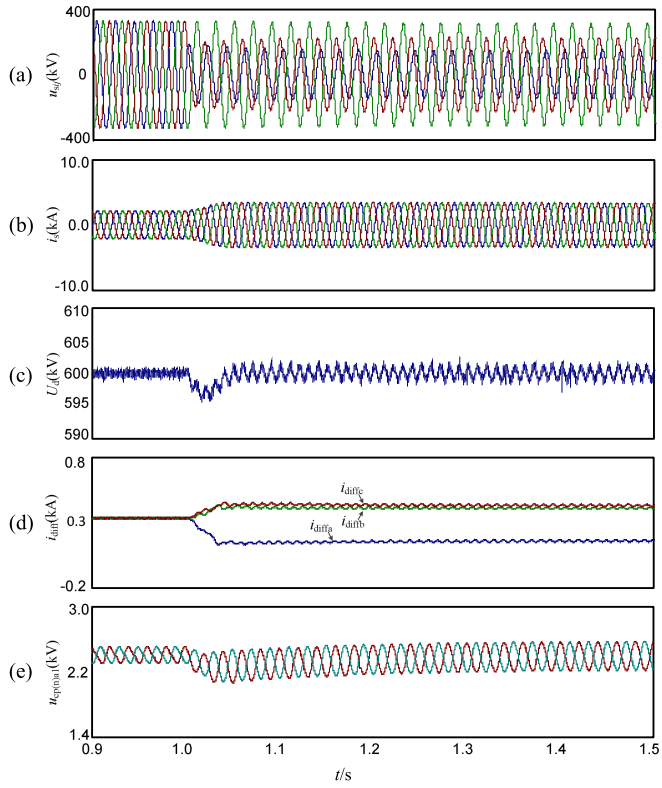

Fig. 13. Simulation results when the proposed control strategy is adopted. (a) Line-to-line voltages of ac grid; (b) ac-side currents; (c) dc-bus voltage; (d) inner unbalanced current of three phases; (e) the voltages of the first capacitor of, respectively, the upper and the lower arms in phase a.

in dc-bus voltage after the fault happen, which is caused by the small tracking error of the arm current regulator at the double frequency. However, the fluctuation is less than 0.33% of the dc-bus voltage, which can be ignored approximately. Fig. 12(c) shows a good control effect of the dc-bus voltage control and the arm current regulator. The inner unbalanced currents of three phases, which contain the dc current and the circulating current, are shown in Fig. 12(d). It is clear from Fig. 12(d) that the dc current distributes evenly in three legs before fault happens. When the fault happens, a small divarication happens in dc current distribution. However, the divarication disappears soon and the dc currents recover to evenly distributed state. It is also clear that there is small circulating current after the fault happens, which is caused by the tracking error of the arm current regulator. However, the circulating current is so small that it can be ignored. The voltages of the first capacitor of respectively the upper and the lower arms in phase a are shown in Fig. 12(e). From Fig. 12(e), the capacitor voltage recovers to its reference value after a divarication. It is also clearly that the voltage fluctuations of the capacitors become larger after the fault happen, and this is caused by the larger arm current after the fault happens.

Fig. 13 shows the simulation results when the proposed control strategy is adopted. This control strategy ensures that the ac-side currents are symmetrical, whereas the dc current does not distribute averagely among three legs. Fig. 13(a) shows the line-to-line voltage of ac side before and after the fault happens.

Fig. 14. Three-phase back-to-back MMC prototype.

In Fig. 13(b), the ac-side currents keep symmetrical when fault happens and all of the currents increase in a relatively small amplitude when compared to the currents in Fig. 12(b). The dc-bus voltage is shown in Fig. 13(c). There is also a small fluctuation with double-frequency in dc-bus voltage after the fault happen, and the fluctuation is less than 0.33% of the dc-bus voltage too, which can be ignored approximately. The inner unbalanced currents of three legs which contain dc current and the circulating current are shown in Fig. 13(d). It is clear from Fig. 13(d) that the dc current does not distribute evenly in three legs when fault happens. From Fig. 12(b), the ac-side current of phase a is larger than those of phases b and c. According to (12), in order to realize the symmetry of ac-side currents, the dc current (active power) distribution among three legs should be adjusted. The dc currents of phases b and c should be increased whereas that of phase a should be decreased, and this agrees with Fig. 13(d) and the analysis in Section II-A2. It is also clear from Fig. 13(d), the circulating current is so small that it can be ignored. The voltages of the first capacitor of respectively the upper and the lower arms in phase a are shown in Fig. 13(e). The capacitor voltage fluctuations in Fig. 13(e) are smaller and recover to their reference value in a shorter time when compared to the capacitor voltages in Fig. 12(e). It is because the arm current in the proposed strategy is much smaller than that in the control strategy in [20].

V. Experimental Results

Fig. 14 shows the experimental prototype of a back-to-back MMC. Both rectifier side and inverter side are isolated from the ac-grid by three-phase transformers: one is in Y/Y structure, the other is in Y/Δ structure. In order to verify the feasibility and effectiveness of the proposed control strategy in rectifier side, the rectifier side with the Y/Y transformer is employed in our experiments. Parameters in the experiment are shown in Table II. The grid fault scheme in the experiment is designed as shown in Fig. 15. Under balanced grid condition, ac grid of phase a is not grounded at the point G_s, and the transformer is connected to ac-

TABLE II
CIRCUIT PARAMETERS IN EXPERIMENTS

Items	Values
Rated power P_{N}	10 kW
Rated RMS voltage of ac side U_{sx}	220 V
Rated voltage of dc bus U_{d}	800 V
Rated current of dc bus I_{d}	12.5 A
SM capacitor voltage U_{c}	200 V
Arm inductance L	10 mH
SM capacitance C	2400 μF
Resistance of dc bus R_{L}	64 Ω
Number of SMs per arm N	4
Carrier frequency f	5 kHz
Arm current controller K_{i}	0.167
DC-bus controller K_{bus}	20.833
DC-bus controller T_{bus}	0.00025 s
Capacitor voltage controller K_{c}	20.57
Capacitor voltage controller T_{c}	0.07 s

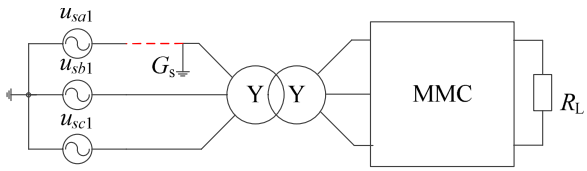

Fig. 15. Grid fault scheme in the experiment.

grid through the dotted line. Under unbalanced grid condition, the dotted line is broken, and the primary side of transformer of phase a is directly grounded at the point G_s. It should be noted here that under unbalanced grid condition, resistance of dc bus R_{L} is twice of the rated value for avoiding overcurrent of arm switch devices. In experiments, the fine-tuning control combined with PSC is adopted as the third hierarchy to balance the capacitor voltages within an arm.

A. Case One: Under Balanced Grid Condition

Under balanced grid condition, MMC operates at rated power. Experimental results are shown in Fig. 16. DC-bus voltage and the symmetrical ac-side currents are shown in Fig. 16(a). In Fig. 16(b), the voltages of the first capacitor, respectively, of the upper arm and the lower arm in phase a are well balanced. The currents of, respectively, the upper arm and the lower arm in phase a present as sine wave without double-frequency circulating component, and this shows a good performance of arm current control to suppress the circulating current. Fig. 16(c) shows the upper arm output voltage of phase c and the upper arm currents of three phases. The arm output voltage appears as a five-level wave, and the upper arm currents of three phases are symmetrical. Fig. 16 shows the good static characteristics of the proposed control strategy under balanced grid condition.

B. Case Two: A Switchover from Inductive Reactive Current to Capacitive Reactive Current

At the beginning, MMC operates at rated inductive reactive current. Then change this current into rated capacitive reactive current. In Fig. 17(a), at the switching moment, a small fluctuation happens in the dc-bus voltage, and it disappears quickly. A phase reversal happens in the ac-side current since the current changes from inductive into capacitive. In Fig. 17(b), the capacitor voltage waveform changes when the arm current changes from inductive into capacitive. Both the capacitor voltages and arm currents recover to balance quickly after the switching. In Fig. 17(c), the arm output voltage changes accompanied with the variation of the capacitor voltage. Arm currents of three phases recover to symmetrical quickly after the switching moment. Fig. 17 shows a rapid response speed to the switchover of reactive current and a good control performance of dc-bus voltage and capacitor voltages.

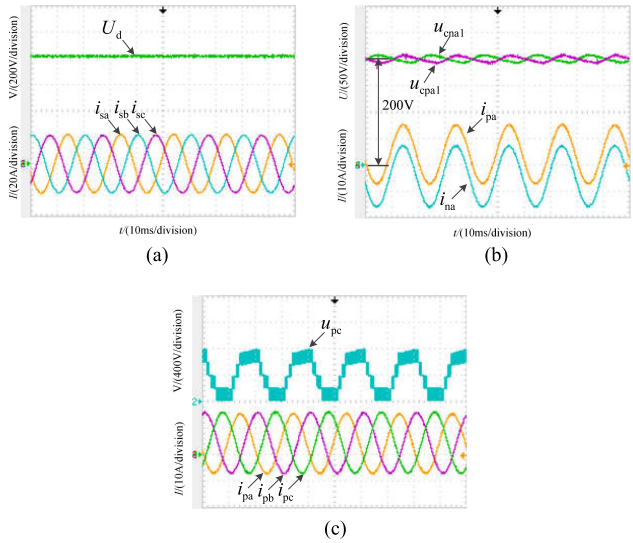

Fig. 16. Waveforms in case one. (a) DC-bus voltage U_{d} and ac-side currents i_{sa}, i_{sb}, i_{sc}; (b) capacitor voltages u_{cpa1}, u_{cna1} and arm currents i_{pa}, i_{na} of phase a; (c) upper arm currents i_{pa}, i_{pb}, i_{pc} of three phases and upper arm output voltage u_{pc} of phase c.

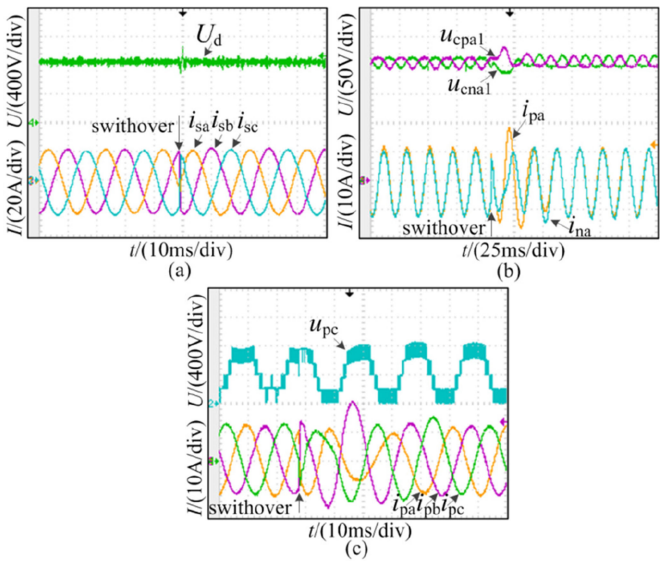

Fig. 17. Waveforms in case two. (a) DC-bus voltage U_{d} and ac-side currents i_{sa}, i_{sb}, i_{sc}; (b) capacitor voltages u_{cpa1}, u_{cna1} and arm currents i_{pa}, i_{na} of phase a; (c) upper arm currents i_{pa}, i_{pb}, i_{pc} of three phases and upper arm output voltage u_{pc} of phase c.

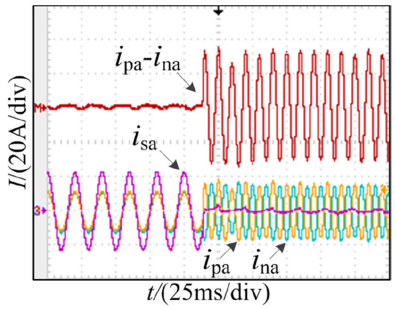

Fig. 18. Waveforms in case three.

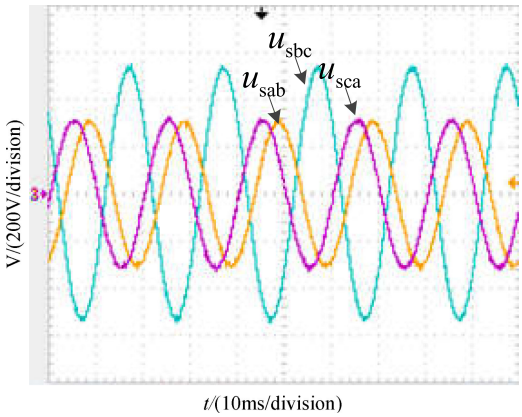

Fig. 19. Unbalanced line-to-line voltages in the secondary side of transformer.

C. Case Three: A Switchover from Capacitive Reactive Current Reference to Circulating Current Reference

At the beginning, there is only capacitive reactive reference current in ac side. Then change this current reference into circulating current reference. Experiment results are shown in Fig. 18. In Fig. 18, $i_{\rm pa}-i_{\rm na}$ is the difference value of the upper and the lower arm currents of leg a, and it is twice the value of $i_{\rm diffa}$. When there is only reactive reference current, $i_{\rm pa}-i_{\rm na}$ is almost zero since there is no dc current and the circulating current is suppressed. However, a small ripple of fundamental-frequency exists in $i_{\rm pa}-i_{\rm na}$. This small ripple is caused by the device loss difference of the upper arm and the lower arm as mentioned in (14). When change the reactive current reference into circulating current reference, $i_{\rm pa}-i_{\rm na}$ changes into double- frequency circulating current instantaneously. The ac-side current $i_{\rm sa}$ changes into almost zero, and the arm current $i_{\rm pa}$ and $i_{\rm na}$ change from fundamental frequency into double frequency with opposite phase instantaneously. Fig. 18 shows a good control performance of the proposed strategy on circulating current and ac-side current.

D. Case Four: Under Unbalanced Grid Condition

Grid fault scheme is shown as in Fig. 15. The unbalanced line-to-line voltages in secondary side of Y/Y transformer are shown in Fig. 19. Control strategy in [20] and the one proposed in this paper are adopted for comparison. The experiment results

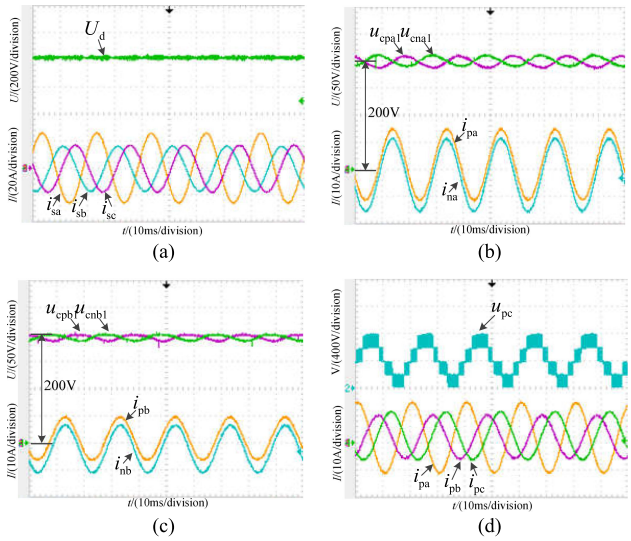

Fig. 20. Waveforms when control strategy in [20] is adopted. (a) DC-bus voltage $U_{\rm d}$ and ac-side currents $i_{\rm sa}$, $i_{\rm sb}$, $i_{\rm sc}$; (b) Capacitor voltages $u_{\rm cpa1}$, $u_{\rm cna1}$ and arm currents $i_{\rm pa}$, $i_{\rm na}$ of phase a; (c) capacitor voltages $u_{\rm cpb1}$, $u_{\rm cnb1}$ and arm currents $i_{\rm pb}$, $i_{\rm nb}$ of phase b; (d) upper arm currents $i_{\rm pa}$, $i_{\rm pb}$, $i_{\rm pc}$ of three phases and upper arm output voltage $u_{\rm pc}$ of phase c.

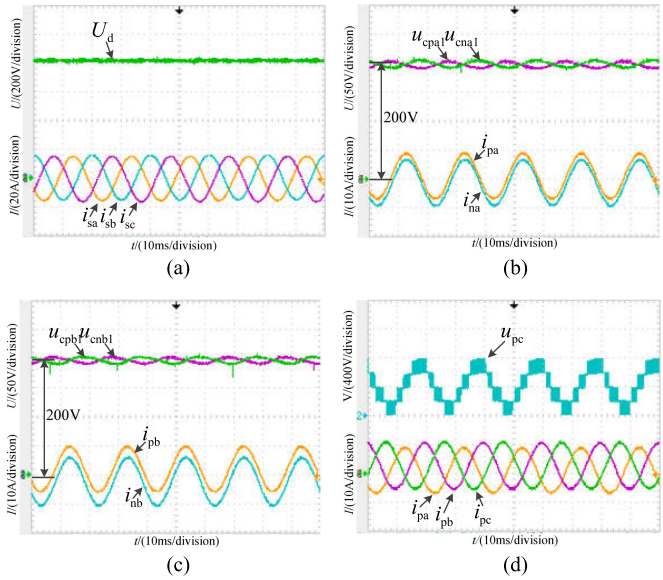

Fig. 21. Waveforms when proposed strategy is adopted. (a) DC-bus voltage $U_{\rm d}$ and ac-side currents $i_{\rm sa}$, $i_{\rm sb}$, $i_{\rm sc}$; (b) capacitor voltages $u_{\rm cpa1}$, $u_{\rm cna1}$ and arm currents $i_{\rm pa}$, $i_{\rm na}$ of phase a; (c) capacitor voltages $u_{\rm cpb1}$, $u_{\rm cnb1}$ and arm currents $i_{\rm pb}$, $i_{\rm nb}$ of phase b; (d) upper arm currents $i_{\rm pa}$, $i_{\rm pb}$, $i_{\rm pc}$ of three phases and upper arm output voltage $u_{\rm pc}$ of phase c.

of the control in [20] are shown in Fig. 20, and the results of the proposed control are shown in Fig. 21.

In Fig. 20(a), it is clearly that the ac-side currents are asymmetrical and dc-bus voltage does not contain ac fluctuation. The arm current control method suppresses the circulating current well since the dc-bus voltage does not contain ac fluctuation. The ac-side current of phase a increases to much larger than those of phases b and c because of the single-phase to ground fault in phase a. Fig. 20(b) and (c) shows the capacitor voltages and arm currents, respectively, of phases a and b. The capaci-

tor voltages are well balanced under unbalanced grid condition. However, the fluctuations of the capacitor voltages in phase a is larger than those in phase b. This larger fluctuation is caused by the larger arm current. Fig. 20(d) shows the upper arm currents of three phases and upper arm output voltage of phase c. From the arm currents, the dc current components of three phases are almost the same, which means three legs contribute almost the same active power to the dc bus, and this is in accordance with the analysis in Section II-A1.

Fig. 21(a) shows the dc-bus voltage and ac-side currents by applying the proposed control strategy under unbalanced grid condition. The ac-side currents are controlled to be symmetrical, and the dc-bus voltage does not contain ac fluctuation. Fig. 21(b) and (c) shows the capacitor voltages and the upper and the lower arm currents of phases a and b. The arm currents in phase a have the same amplitude with those in phase b. However, the dc current components, respectively, in phases a and b are different, which can be shown by the distance between the upper arm current and the lower arm current. The capacitor voltages are well balanced under the unbalanced grid condition. The fluctuations of the capacitor voltages in phase a are almost the same with those in phase b, which is because of the same amplitude of arm current. Fig. 21(d) shows upper arm currents of three phases and upper arm output voltage of phase c. The peak-to-peak values of three arm currents are almost the same, whereas the dc components of them are different: the dc current components of phases b and c are almost the same, while that of phase a is apparently smaller. From Fig. 20(a), the ac-side current of phase a is larger than those of phases b and c. According to (12), in order to realize the symmetry of ac-side currents, the dc current (active power) distribution among three legs should be adjusted. The dc currents of phases b and c should be increased whereas that of phase a should be decreased, and these agree with Fig. 21(d) and the analysis in Section II-A2.

VI. Conclusion

This paper analyzed the active power in MMC and proposed a control strategy which combines the arm current control with the multi-hierarchy control for MMC under unbalanced grid condition. Within the multi-hierarchy control, by adjusting active power distribution among three legs, the symmetrical ac-side current references and the unevenly distributed dc current references in three legs are obtained easily by three voltage controllers in the abc coordinate, avoiding the coordinate transformation, precise calculation, and numerous filters in the existing methods. Besides, the employment of the arm current control removes the need of the three-sequence ac-side current controllers and the three-sequence circulating current suppressing controllers. A proportional regulator with a feedforward steady-state duty cycle is designed for arm current regulator, which can perfectly track its reference. Both the system-level simulations and the low-level experiments are performed to verify the good effect of the arm current regulator, and the feasibility and effectiveness of the proposed strategy.

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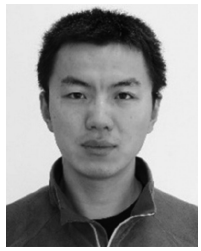

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