An MMC Topology Based on Unidirectional Current H-Bridge Submodule With Active Circulating Current Injection

Wenbo Yang, Qiang Song, *Member, IEEE*, Shukai Xu, Hong Rao, *Senior Member, IEEE*, and Wenhua Liu

***Abstract*—This study proposed a novel modular multilevel converter (MMC) based on unidirectional current H-bridge submodule (UCH-SM) with active circulating current injection (ACCI). Under the premise of keeping the arm current unidirectional, the UCH-SM was developed by optimizing the full-bridge submodule (FBSM). Although the number of required switching devices of the UCH-SM-based MMC (UCH-MMC) is nearly half of that of FBSM-based MMC (FB-MMC), the advantages of the FB-MMC, such as the dc fault blocking and bidirectional dc-link voltage capabilities, were preserved. The proposed ACCI technique can help keep the arm current unidirectional and reduce the overall semiconductor usage. The parameter design method for keeping the arm current unidirectional and the characteristics of the UCH-MMC with ACCI were also analyzed. The control schemes of the UCH-MMC for the dc-link voltage control and dc-link current control modes were presented. Simulation and experimental results were presented to verify the feasibility and characteristics of the proposed UCH-MMC.**

***Index Terms*—Active circulating current injection (ACCI), dc fault blocking, high-voltage direct current (HVDC), modular multilevel converter (MMC), submodule (SM).**

I. Introduction

THE high-voltage direct current (HVDC) transmission system based on modular multilevel converter (MMC) has been increasingly applied because of its advantages, such as simple scaling, low harmonics, and low switching losses [1]–[3]. As transmission distance increases to hundreds or thousands of kilometers, the cost of cables becomes extremely high compared with that of overhead lines. However, dc-side short-circuit fault is a major problem in an overhead line-based HVDC.

Half-bridge submodule (HBSM)-based MMCs (HB-MMCs) are currently the most mature and economical MMC topology; however, they cannot clear the dc-side short-circuit current themselves and are thus unsuitable for overhead line applications. Full-bridge submodule (FBSM)-based MMCs (FB-MMCs) are inherently advantageous owing to their dc fault blocking capability [4]. However, the number of required insulated gate bipolar transistors (IGBTs) of FB-MMCs is two times as that of HB-MMCs. To reduce the cost and power loss, a clamp-double submodule (CDSM) was proposed by inserting a clamped circuit between two HBSMs [5]. The clamped circuit comprises two additional diodes and one extra IGBT. The number of required IGBTs and diodes of the CDSM-MMC is around 1.25 times as that of the HB-MMC. The CDSM-MMC has semiconductor losses that are higher than those of the HB-MMC but lower than those of the FB-MMC [5], [6]. Various new submodule (SM) topologies based on clamped circuits, such as cross-connected SM [7], diode clamp SM [8], and unipolar-voltage FBSM [9], have been proposed. Using hybrid MMCs composed of FBSMs and HBSMs can also block the dc fault [10], [11]. To avoid influencing the dc fault blocking capability, at least half of the SMs in hybrid MMCs should be FBSMs. Hence, the number of required IGBTs is 1.5 times that of HB-MMCs, and the cost is still high.

Although the cost and power loss of FB-MMCs are higher than those of the HB-MMCs and CDSM-MMCs, only the FB-MMC can operate under a wide range of dc-link voltage, from rated positive to rated negative. For an MMC-HVDC system, the power reversal has conventionally been achieved by reversing the dc current direction without changing the dc-line voltage polarity. However, the FB-MMC can operate under positive and negative dc-line voltage, thereby allowing its power flow to be reversed by changing the dc-line voltage polarity instead of reversing the dc-line current direction. In this case, the dc-line voltage of the MMC-HVDC system is bidirectional, and the dc-line current is unidirectional.

The hybrid HVDC system composed of an MMC and a line-commutated converter (LCC) is another typical application with a unidirectional dc-line current. When a hybrid HVDC link is used for long-distance bulk power transmission applications, an LCC can be employed at the sending end, and an MMC can be employed at the receiving end that supplies weak networks [12], [13]. For these applications, the power flow is mostly transmitted from the generation center to the load center. If the power flow needs to be reversed, then the hybrid HVDC system with an FB-MMC can change the dc-line voltage polarity, as the dc-line current should always flow in the same direction.

Manuscript received November 26, 2016; revised February 13, 2017 and May 5, 2017; accepted June 20, 2017. Date of publication July 3, 2017; date of current version February 1, 2018. This work was supported by the National Key Research and Development Program under Grant 2016YFB0901002. Recommended for publication by Associate Editor ZiXin Li. *(Corresponding author: Qiang Song.)*

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Digital Object Identifier 10.1109/TPEL.2017.2722011

Based on the characteristic of the unidirectional dc-line current, the unidirectional SM topologies can be employed to reduce the active switches and lower the costs [2], [14]–[17]. A unidirectional cascade H-bridge converter was presented by Iman-Eini *et al.* [16]. In this topology, the upper two switches of the H-bridge cell are replaced with fast diodes, and the cascade H-bridge converter transfers unidirectional active power and functions as unidirectional rectifier. The unidirectional half-bridge cell for MMC was published by de Sousa and Heldwein [14], [15], and unidirectional H-bridge cell was also mentioned in [14]. However, the arm current should also be kept unidirectional to enable the proper operation of the unidirectional SM; thus, the operation principle of the unidirectional MMC is more complicated than that of convention bidirectional MMC. In [14] and [15], special predefined arm current reference waveforms were used to guarantee the proper operation of unidirectional MMC. This arm current pattern is far different from that of conventional MMC and may lead to the loss of flexibility. In [17], a lower rated dc-link voltage was selected to increase the dc component of the arm current in a unidirectional MMC. However, lowering the rated dc-link voltage results in the decrease in transmission capacity and is usually inapplicable to large power transmission system. Exploring an efficient operation strategy for unidirectional MMC is challenging. In addition, studies focusing on the costs, losses, and other characteristics of the unidirectional MMC are few.

This study proposed a novel MMC based on a unidirectional current H-bridge SM (UCH-SM) with an active circulating current injection (ACCI) technique. The proposed UCH-SM requires only two SM current rated IGBTs, two SM current rated diodes, and two precharge current rated diodes. The UCH-SM-based MMC (UCH-MMC) can be operated in a way similar to the conventional MMC. The current flow through UCH-SM is kept always in the same direction through parameter selection and ACCI technique. The proposed ACCI technique helps shape the arm current, significantly lowers the demand for ac-side voltage, and reduces the overall semiconductor usage. The cost of the proposed UCH-MMC with ACCI is similar to that of the HB-MMC. The UCH-MMC also possesses the advantages of FB-MMCs, such as bidirectional dc-link voltage. The power flow can also be reversed by reversing the dc-link voltage polarity. The advantage of dc-side fault blocking capability is also reserved.

The remainder of the paper is organized as follows. Sections II and III describe the structure and characteristics of the proposed UCH-MMC with ACCI. Section IV discusses the control method of the UCH-MMC. Sections V and VI present the simulation and experimental results, respectively, to verify the feasibility and characteristics of the UCH-MMC. Finally, Section VII elaborates the conclusions of the study.

II. UCH-MMC With ACCI

A. Structure of the UCH-MMC

Fig. 1 illustrates the structure of an MMC and defines the positive direction of each voltage and current. The circulating current $i_{\rm cir}$ herein only contains the internal components that flow among the three phases but does not contain dc-link current component. In the following analysis, the dc-line current $i_{\rm dc}$ is supposed to be unidirectional and flows always from the dc-line into the converter. The currents of the three-phase upper and lower arms are expressed as

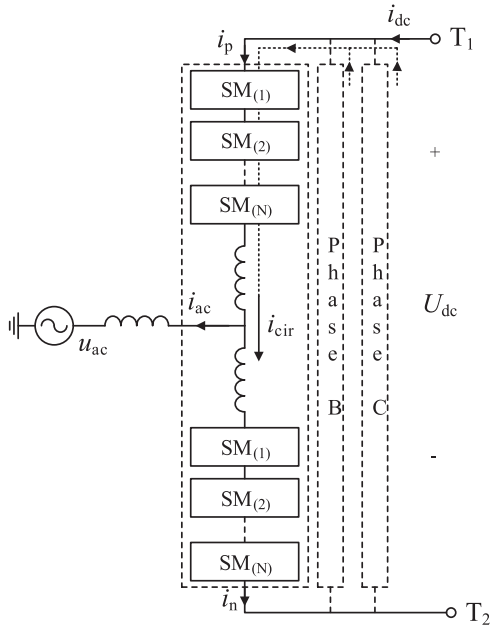

Fig. 1. Structure of MMC.

$$\begin{cases} i_{a(p,n)} = \pm\dfrac{\sqrt{2}}{2} I_{\rm ac}\sin(\omega t - \varphi) + \dfrac{1}{3} I_{\rm dc} \\ i_{b(p,n)} = \pm\dfrac{\sqrt{2}}{2} I_{\rm ac}\sin\left(\omega t - \dfrac{2}{3}\pi - \varphi\right) + \dfrac{1}{3} I_{\rm dc} \\ i_{c(p,n)} = \pm\dfrac{\sqrt{2}}{2} I_{\rm ac}\sin\left(\omega t + \dfrac{2}{3}\pi - \varphi\right) + \dfrac{1}{3} I_{\rm dc} \end{cases} \quad (1)$$

where $I_{\rm ac}$ denotes the root mean square (rms) value of the fundamental component of the ac-side output current, and φ denotes the corresponding phase angle. Subscript *p* denotes the upper arm, and subscript *n* denotes the lower arm. The second-harmonic circulating current is an inherent characteristic of MMC. However, various methods can suppress the second-harmonic circulating currents [18]–[21]. Therefore, in (1), the internal second-harmonic circulating currents were ignored under the assumption that they have been suppressed to zero.

Compared with HBSM that can generate only two voltage states, each FBSM can generate an additional negative state [4]. As a result, the ac-side voltage of the FB-MMC is not constrained by the dc-line voltage [22], [23]. Without changing the dc-line voltage, the rated ac-side voltage can be increased as long as a sufficient number of FBSMs are employed in each arm [22], [23]. For example, for an MMC with *N* SMs in each arm, if *M* additional FBSMs are added in each arm and are allowed to generate negative voltage output, the peak ac-side voltage can be extended to $1 + 2M/N$ times, while the rated dc-link voltage is still *N* times of the SM capacitor voltages [23]. With the increase in the rated ac-side voltage, the rated ac-side

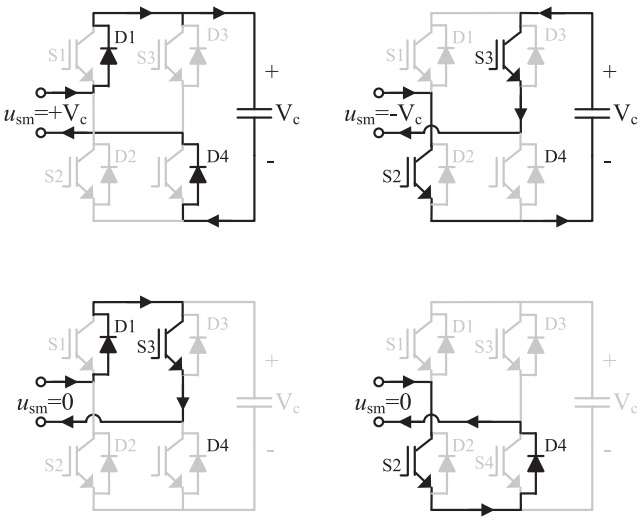

Fig. 2. Current path of the FBSM.

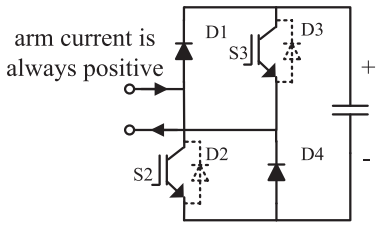

Fig. 3. Unidirectional current H-bridge SM.

current decreases correspondingly. According to (1), the arm current can become always positive if the ac-side current and dc-line current fulfill the following condition:

$$I_{\rm ac} \le \frac{\sqrt{2}}{3} I_{\rm dc}. \tag{2}$$

The active power balance relationship between the ac-side and dc-side is expressed as

$$P = 3U_{\rm ac} I_{\rm ac} \cos\varphi = U_{\rm dc} I_{\rm dc} \tag{3}$$

where $U_{\rm ac}$ is the rms phase voltage of the ac grid, and $U_{\rm dc}$ is the dc-line voltage. Substituting (3) into (2), it can be obtained that the ac-side voltage should fulfill the following condition in order to fulfill the condition shown in (2):

$$U_{\rm ac} \ge \frac{U_{\rm dc}}{\sqrt{2}\cos\varphi}. \tag{4}$$

Therefore, under a certain dc-line voltage and power factor range, if the rated ac-side voltage of FB-MMC is increased to a sufficiently high value, then the arm currents shown in (1) can be always positive and flow always in the same direction.

Fig. 2 illustrates the current path of FBSM when the arm current is positive. If the arm current is always positive, then switching devices S_1, S_4, and D_2, D_3 are never used during normal operation. Based on the above-mentioned analysis, a UCH-SM is proposed as shown in Fig. 3. If the arm current can be kept always positive during normal operation through parameter design and control means, then the SM can contain only two IGBTs S_2 and S_3, and two diodes D_1 and D_4 (see Fig. 3). Two additional diodes D_2 and D_3 can be noted in the UCH-SM. Although D_2 and D_3 are not necessary for normal operation, they provide a current path when precharging the SM capacitors. The current rating of D_2 and D_3 can be selected according to the precharge state current, which is limited by the precharge resistors and usually much lower than the normal operating current; thus, the current rating of D_2 and D_3 can be much lower than that of other devices. For an HVDC system with unidirectional dc-line current, the MMC can employ UCH-MMCs. Compared with FB-MMCs, UCH-MMCs are more cost effective without affecting the inherent advantage of dc-side fault blocking capability.

B. Active Circulating Current Injection

The premise of the operation of UCH-MMC is that the arm currents are always positive. Increasing the rated ac-side voltage to a certain value is the most direct way to ensure that the arm currents flow always in the same direction. According to (4), the rated ac-side voltage should be increased to more than two times that of conventional HB-MMCs. An excessively high ac-side voltage may induce difficulties for ac-field equipment selection and design in real voltage source converter-based HVDC systems. Similar to the third-harmonic injection technique for pulse width modulation, an ACCI technique is proposed to help ensure that the arm currents are always positive. The ACCI technique lessens the demand on the increase in rated ac-side voltage.

The injected circulating currents can be calculated as follows:

$$\begin{cases} i_{{\rm inj}\_a} = \left|\dfrac{i_a}{3}\right| - \left|\dfrac{i_b}{6}\right| - \left|\dfrac{i_c}{6}\right| \\ i_{{\rm inj}\_b} = \left|\dfrac{i_b}{3}\right| - \left|\dfrac{i_a}{6}\right| - \left|\dfrac{i_c}{6}\right| \\ i_{{\rm inj}\_c} = \left|\dfrac{i_c}{3}\right| - \left|\dfrac{i_a}{6}\right| - \left|\dfrac{i_b}{6}\right| \end{cases}. \tag{5}$$

The derivation of (5) is presented in Appendix A.

The arm currents with injected circulating current can be expressed as

$$\begin{cases} i_{{\rm a1}(p,n)} = i_{a(p,n)} + \alpha i_{{\rm inj}\_a} = \pm\dfrac{\sqrt{2}}{2} I_{\rm ac} \sin(\omega t - \varphi) \\ \qquad\qquad + \dfrac{1}{3} I_{\rm dc} + \alpha i_{{\rm inj}\_a} \\ i_{{\rm b1}(p,n)} = i_{b(p,n)} + \alpha i_{{\rm inj}\_b} = \pm\dfrac{\sqrt{2}}{2} I_{\rm ac} \sin\left(\omega t - \dfrac{2}{3}\pi - \varphi\right) \\ \qquad\qquad + \dfrac{1}{3} I_{\rm dc} + \alpha i_{{\rm inj}\_b} \\ i_{{\rm c1}(p,n)} = i_{c(p,n)} + \alpha i_{{\rm inj}\_c} = \pm\dfrac{\sqrt{2}}{2} I_{\rm ac} \sin\left(\omega t + \dfrac{2}{3}\pi - \varphi\right) \\ \qquad\qquad + \dfrac{1}{3} I_{\rm dc} + \alpha i_{{\rm inj}\_c} \end{cases} \tag{6}$$

where α is the injection index, which should be between 0 (no injection) and 1 (full injection). Equation (6) shows that the injected circulating currents do not affect the ac-side output current. Given that the sum of the three-phase injected circulating

currents is zero, they do not affect the dc-line current. Equation (6) also shows that the injected circulating currents trim the distribution of the dc current among the three phases to ensure that all arm currents are positive. For example, at a certain instant, if the arm current in phase A is negative, then it can "borrow" some dc current components from the other phases through the injected circulating current. This condition is under the premise of not affecting the direction of the other arm currents.

Considering that the three-phase currents in (6) are symmetrical, only the currents in phase A are analyzed in following parts. To ensure that the arm currents are always positive, the following equation should be satisfied at any instant:

$$\min(i_{a1p}, i_{a1n}) \geq 0. \tag{7}$$

Considering the harmonic components that may exist in the arm current, a margin should be reserved to ensure that the direction of the arm currents is not affected by the harmonics in real operation. Therefore, the condition shown in (7) can be revised as follows:

$$\min(i_{a1p}, i_{a1n}) \geq hI_{\text{dc}} \tag{8}$$

where h is an index that denotes the reserved margin. The harmonic current of MMCs is usually small; thus, a value of 1% is usually sufficiently high for h. By substituting (5) and (6) into (8), (8) can be rewritten as

$$\min_{\omega t\in[0,2\pi]} \left\{ \frac{1}{3}I_{\text{dc}} - \frac{\sqrt{2}}{6}I_{\text{ac}} \left((3-2\alpha)\left|\sin(\omega t-\varphi)\right| + \alpha\left|\sin\left(\omega t-\frac{2}{3}\pi-\varphi\right)\right| + \alpha\left|\sin\left(\omega t+\frac{2}{3}\pi-\varphi\right)\right| \right) \right\} \geq hI_{\text{dc}}. \tag{9}$$

Given that I_{dc} and I_{ac} are all non-negative, (9) can be rewritten as

$$\frac{\sqrt{2}}{2}I_{\text{ac}}f(\alpha) \leq (1-3h)I_{\text{dc}} \tag{10}$$

where

$$f(\alpha) = \max_{\omega t\in[0,2\pi]} \left\{ (3-2\alpha)\left|\sin(\omega t-\varphi)\right| + \alpha\left|\sin\left(\omega t-\frac{2}{3}\pi-\varphi\right)\right| + \alpha\left|\sin\left(\omega t+\frac{2}{3}\pi-\varphi\right)\right| \right\} \tag{11}$$

Solving (11) analytically is difficult because of the existence of absolute value functions. $f(\alpha) = 3 - \alpha$ can be obtained on the basis of the numerical solutions of $f(\alpha)$. Thus, (10) can be simplified as

$$\frac{\sqrt{2}}{2}I_{\text{ac}}(3-\alpha) \leq (1-3h)I_{\text{dc}}. \tag{12}$$

By substituting (3) into (12), the following equation is obtained:

$$U_{\text{ac}} \geq \frac{\sqrt{2}(3-\alpha)}{6(1-3h)\cos\varphi}U_{\text{dc}}. \tag{13}$$

It can be seen that the power factor also affects the parameter design for the rated ac-side voltage. The reason is that sufficient dc components should exist in the arm current to ensure that the arm current is always positive. The condition mentioned above also means that the output reactive power is limited by the output active power. A minimum power factor $\text{PF}_{\min}$ can be preset when designing system parameters, and the rated ac-side voltage should fulfill the following condition:

$$U_{\text{ac}} \geq \frac{\sqrt{2}\times(3-\alpha)}{6\times(1-3h)\times\text{PF}_{\min}}U_{\text{dc}}. \tag{14}$$

In other words, if the rated ac-side voltage is designed according to (14), then all the arm currents can be kept always positive by actively injecting the circulating currents calculated using (5) with the injection index α. Compared with (4), the required rated ac-side voltage can decrease by 1/3 at most when $\alpha = 1$.

The rated summed SM capacitor voltages in one arm is defined as

$$U_{\text{cap}} = NU_c \tag{15}$$

where N is the number of SMs in one arm, and U_c is the rated voltage of each SM capacitor. The rated summed SM capacitor voltage indicates the maximum available output voltage of the arm. The relationship between the ac-side output voltage and the rated summed SM capacitor voltages can be described as

$$\sqrt{2}U_{\text{ac}} = m\times\left(U_{\text{cap}} - \frac{1}{2}U_{\text{dc}}\right) \tag{16}$$

where m is a generalized modulation index that ranges from 0 to 1.0. Therefore, the required rated summed SM capacitor voltage can be expressed as

$$U_{\text{cap}} = \frac{\sqrt{2}U_{\text{ac}}}{m} + \frac{1}{2}U_{\text{dc}}. \tag{17}$$

In an example case, $\text{PF}_{\min}$ is set as 0.894 [i.e., the UCH-MMC can output no less than 0.5 per unit (p.u.) reactive power when outputting 1.0 p.u. active power]. Considering the fluctuation of the ac-grid voltage in a real application, m is set as 0.85 at the rated operating point. Using (14) and (17), the curves of the required U_{ac} and U_{cap} varying with the injection index α can be obtained. The rms value of the arm current I_{arm} can be calculated by the definition of rms with the time domain expressions of arm currents in (6). As shown in Fig. 4(a), the required U_{ac} and U_{cap} can be decreased effectively by increasing the injection index. The arm current I_{arm} increases with the decrease in U_{ac} and U_{cap}. With the increase in injection index α, the injected circulating current also contributes to the increase in arm current. U_{cap} decreases to 75.6% as α increases from 0 to 1. I_{arm} indicates the current load per semiconductor, and U_{cap} indicates the amount of semiconductors. Accordingly, the product of U_{cap} and I_{arm} can be used to evaluate the semiconductor cost and conduction loss. As shown in Fig. 4(b), the product of U_{cap} and I_{arm} decreases with the increase in α and reaches its minimum at $\alpha = 0.84$. Then, the product increases by 0.3% as α increases from 0.84 to 1.0. Therefore, the injected circulating current increases the current load of each semiconductor but decreases the amount

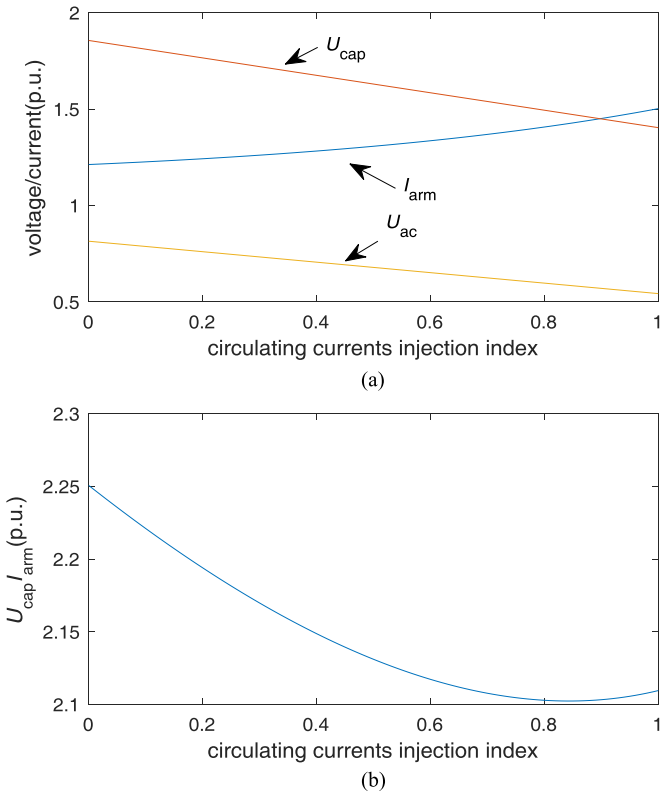

Fig. 4. Effects of circulating currents on converter parameters (the base voltage is the dc-link voltage U_{dc}, and the base current is the dc-link current component in each phase $I_{dc}/3$).

of the required semiconductors. Therefore, the overall semiconductor cost and conduction loss will become small when ACCI is applied. The ACCI with $\alpha = 1$ will be adopted when using the UCH-MMC in the following analysis.

C. Reactive Power Output Capability

Given that sufficient dc components should exist in the arm current to ensure that the arm current is always positive, the output reactive power of the UCH-MMC is limited by the output active power. The relationship between ac/dc voltage ratio and maximum reactive/active power ratio (maximum reactive power output capability when output 1 unit of active power) can be drawn according to (13) as shown in Fig. 5. It can be obtained that lower power factor (higher reactive/active power ratio) results in higher ac voltage requirement. In the case of $\mathrm{PF}_{\min} = 0.894$ and when U_{ac} and U_{dc} are at their rated value, the *P*–*Q* diagram of UCH-MMC is shown in Fig. 6(a).

The short-term reactive power capability of UCH-MMC can be improved. The UCH-MMC can adjust the dc-link voltage in a wide range and can thus be operated as a dc current source converter. To maximally improve the reactive power capability, the dc-link current can be maintained at its rated value and the dc-link voltage can be changed with the output active power. In this case, the dc component in the arm current can be kept as large as possible to ensure that the arm current is always positive, and the *P*–*Q* diagram can be extended as shown in Fig. 6(b).

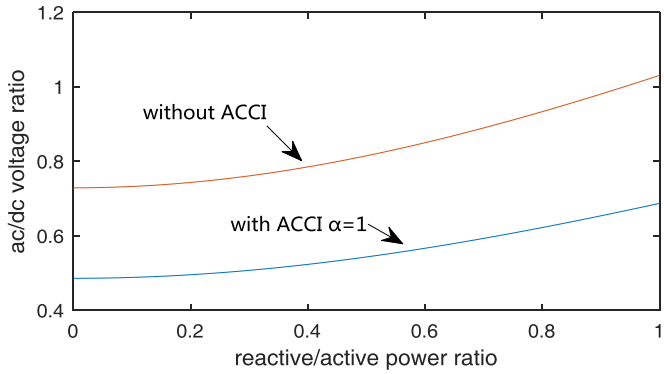

Fig. 5. Relationship between ac/dc voltage ratio and maximum reactive/active power ratio.

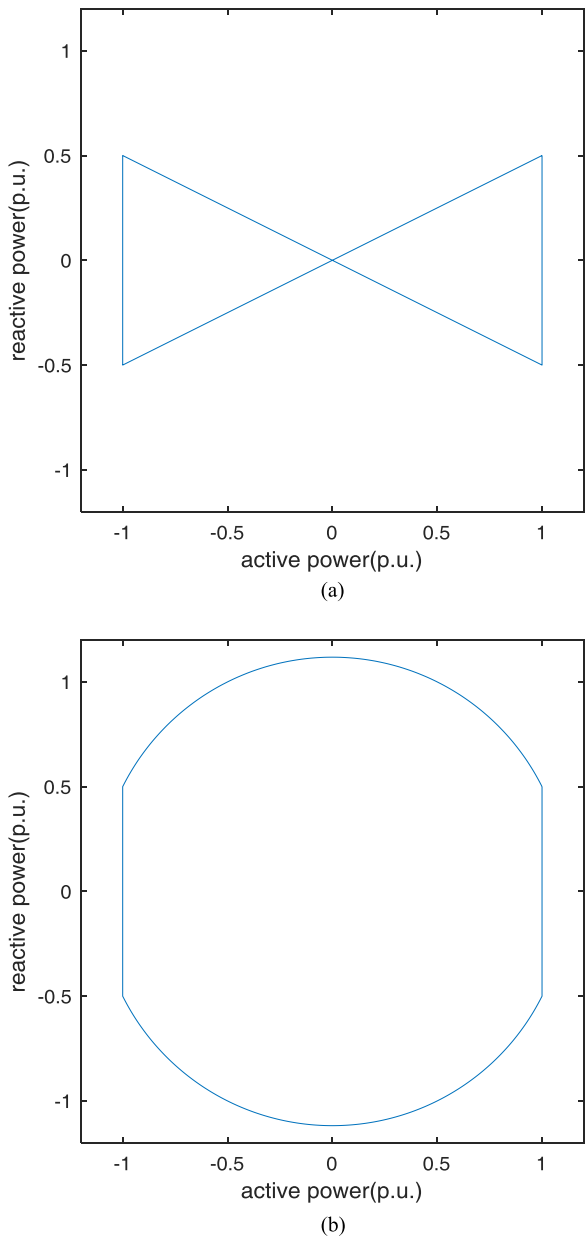

Fig. 6. *P*–*Q* diagram of UCH-MMC. (a) Rated dc-link voltage mode; and (b) rated dc-link current mode.

TABLE I
PARAMETERS OF THE DESIGN EXAMPLE

	HB-/FB-/Hybrid-MMC	UCH-MMC without ACCI	UCH-MMC with ACCI
Active Power Range	±500 MW	±500 MW	±500 MW
Reactive Power Range	±250 MVAr	±250 MVAr*	±250 MVAr*
Rated DC Voltage	320 kV	320 kV	320 kV
Rated DC Current	1562.5 A	1562.5 A	1562.5 A
Rated AC Voltage	166.56 kV	451.84 kV	301.12 kV
Rated AC Current	1937.7 A	714.30 A	1071.8 A
Summed SM Capacitor Voltages in an Arm	320 kV	594 kV	450 kV
SM Capacitor Voltage	1.80 kV	1.80 kV	1.80 kV
Number of SM per Arm	178	330	250
Rated Arm Current	1099.8 A	631.5 A	782.5 A
Arm Inductance	31.594 mH (0.2 p.u.)	232.50 mH (0.2 p.u.)	103.26 mH (0.2 p.u.)
SM Capacitance	8.0 mF	2.6 mF	2.4 mF

*This reactive power range has some limitations, details are given in Sections II-B and II-C.

Compared with rated dc-link voltage mode, the rated dc-link current mode will result in high losses under the condition of light load. Therefore, the rated dc-link current mode is mainly suitable for output short-term large reactive power. The system can temporally switch into rated dc-link current mode and output a short-term reactive power, if the required output reactive power is out of the range shown in Fig. 6(a). The reactive power of MMC is mostly used to dynamically support the grid voltage during system transients, such that the short-term large reactive power capability is usually acceptable in real applications.

In Fig. 6, only the current direction and power balance limitations of UCH-MMC are considered. Other factors, such as arm inductance and SM capacitance, may also influence the *P–Q* diagram.

III. DESIGN EXAMPLE AND CHARACTERISTIC COMPARISON

A. Parameters of the Design Example

A 320 kV/500 MW monopolar system is used as a design example. The main parameters of conventional HB-MMCs, FB-MMCs, hybrid MMC composed of half-FB and half-HB SMs, and the proposed UCH-MMCs are shown in Table I for comparison. The ac voltages and summed capacitor voltages can be calculated using (14) and (17). The arm inductance is designed as 0.2 p.u. For UCH-MMCs, the rated ac-side voltage should be increased to a certain value to ensure that all the arm currents are always positive. The required arm voltage of UCH-MMCs is thus higher than that of conventional FB-MMCs, thereby leading to a large number of SMs. However, the rated arm current of UCH-MMCs decreases. As analyzed in Section II-B, the adoption of ACCI can significantly lower the demand for ac-side voltage and reduce the overall semiconductor usage. Thus, ACCI will be always adopted when using the UCH-MMC in the following analysis.

The SM capacitance is designed on the basis of avoiding overvoltage and over-modulation [24]. The upper limit of summed SM capacitor voltages is designed as 1.1 p.u. (1980 V per SM on average). Table I shows that the SM capacitance of the UCH-MMC can be significantly lower than that of the HB-MMC or FB-MMC. Although the UCH-MMC requires a large number of SMs, the overall capacitance usage is still significantly low. Given that capacitance usage is a complex problem, it will be analyzed in detail in future studies. However, the simulations in Section V confirm that the UCH-MMC can operate normally with a low capacitance.

TABLE II
COMPARISON OF THE IGBT COST

	HB-MMC	Hybrid MMC	FB-MMC	UCH-MMC with ACCI
SM Capacitor Voltage (Vc)	1.80 kV	1.80 kV	1.80 kV	1.80 kV
Rated Arm Current (I_{arm})	1099.8 A	1099.8 A	1099.8 A	782.5 A
IGBTs/per SM	2	2/4	4	2
IGBTs/per Arm	356	534	712	500
IGBTs/per Converter (K)	2136	3204	4272	3000
S_{IGBT}	4229 MVA	6343 MVA	8457 MVA	4226 MVA

B. Cost Comparison for Required IGBTs

The cost of MMCs mainly comprises the costs of switching devices and capacitors. The major proportion of the switching device cost is the cost of IGBTs. Considering the number, rated voltage, and rated current of required IGBTs, an index is defined below to evaluate the cost of IGBTs in an MMC:

$$S_{\text{IGBT}} = K \times V_C \times I_{\text{arm}} \tag{18}$$

where K is the numbers of the IGBTs in the converter, V_C is the rated SM capacitor voltage, and I_{arm} is the rated arm current.

The IGBT cost of the HB-MMC, FB-MMC, hybrid MMC composed of half-FB and half-HB SMs, and UCH-MMC with ACCI in the design example is shown in Table II for comparison. The UCH-MMC needs a large number of IGBTs because of its large number of SMs; however, its S_{IGBT} is nearly the same as that of the HB-MMC and is significantly lower than that of hybrid MMC and FB-MMC because of its lower rated arm current.

C. Semiconductor Loss Evaluation

For a given operating condition, the ideal waveforms of the arm currents, arm output voltages, and sum of arm capacitor voltages can be calculated using a steady-state model; these parameters can be used in semiconductor loss evaluation [25]. The conduction states and switching events of the switching devices were computed with carrier phase-shifted pulse-width modulation method. The carrier frequency is 150 Hz. The capacitor voltages were assumed to be balanced. The conduction and switching characteristics (e.g., V_{ce}, E_{on}, and E_{off}) of IGBTs were obtained from the xml format datasheet provided by the manufacturer [26] with linear interpolation. Switching devices

TABLE III
SEMICONDUCTOR LOSS EVALUATION RESULTS (MW)

Converter type	Conduction loss	Switching loss	Overall loss	Loss ratio
HB-MMC	2.694	0.665	3.359	0.601%
Hybrid MMC	3.783	0.665	4.449	0.796%
FB-MMC	4.873	0.665	5.538	0.991%
UCH-MMC with ACCI	4.508	0.510	5.019	0.898%

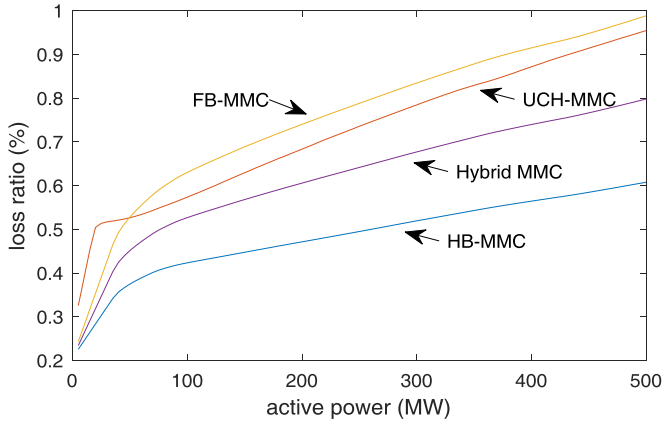

Fig. 7. Semiconductor loss under different power outputs.

of 3300 V/1000 A (5SNA-1000N330300/5SLD-1000N330300) were used in the SMs of the UCH-MMC, and switching devices of 3300 V/1500 A (5SNA-1500E330305) were used in the SMs of the HB-MMC, FB-MMC, and hybrid MMC. The losses of MMCs in the design example when the output was an active power of 500 MW and a reactive power of 250 MVAr are presented in Table III. The loss ratio curves when converters output different amounts of active power are presented in Fig. 7.

The evaluation results show that the full-load loss of the UCH-MMC is higher than that of the HB-MMC and hybrid MMC but is slightly lower than that of the FB-MMC.

Semiconductor losses under different circulating current injection indexes were also evaluated, and the results are shown in Fig. 8. The output active power is 500 MW, and the output reactive power is 250 MVAr. Jags are observed on the curves because the amount of SMs is discrete. This result shows that loss will become small when ACCI is applied because injected circulating currents can reduce the amount of semiconductors.

IV. CONTROL METHOD

Usually at least one of the converters of a two-terminal or multiterminal HVDC system should operate in constant dc-link voltage mode. The other MMCs or LCCs can operate in constant active power or constant dc-link current control mode. The UCH-MMC can directly control the dc-link voltage similar to a conventional MMC. Furthermore, the UCH-MMC can adjust the dc-link voltage in a wide range and can thus operate in dc-link current control mode similar to an LCC.

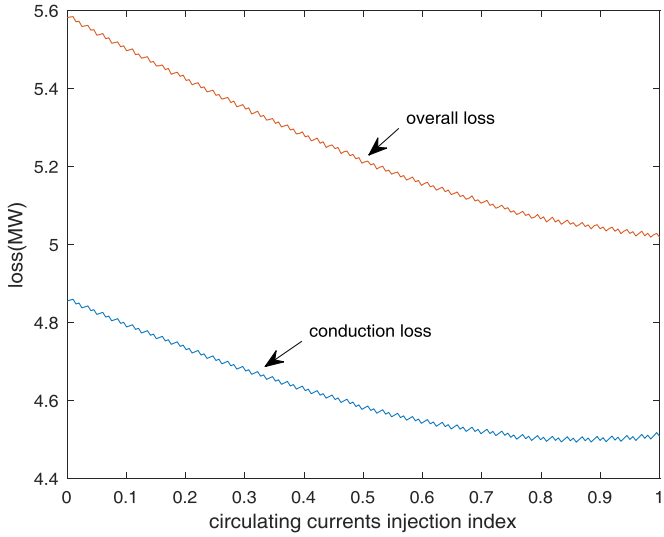

Fig. 8. Relationship between semiconductor loss and circulating current injection index.

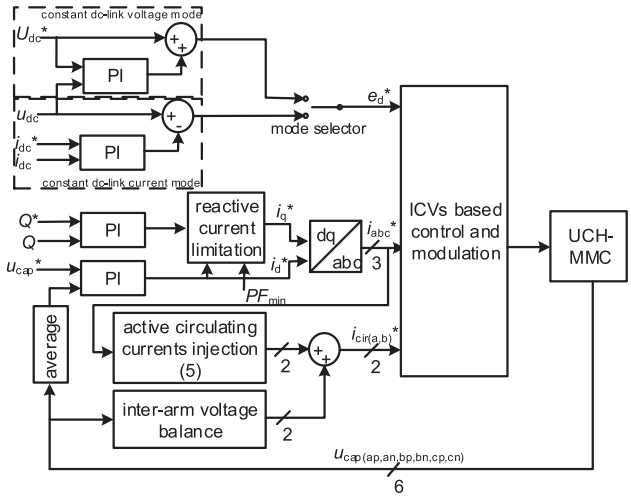

Fig. 9. UCH-MMC controller structure.

The controller structure of the UCH-MMC is shown in Fig. 9. The decoupled controller based on intermediate controllable voltages (ICVs) [21] is used as the core part of the controller.

For a UCH-MMC that operates in constant dc-link voltage control mode, a closed control loop for the dc-link voltage is used to generate the reference value of the dc-link ICV e_d^*. The d-axis current reference i_d^* is generated by a closed control loop to maintain the SM capacitor voltages. The q-axis current reference i_q^* is generated according to the required ac-side reactive power. As analyzed in Section II-B, the output range of the reactive power should be limited by the output active power. To ensure that all the arm currents are always positive, the required injected circulating currents are calculated using (5). The circulating currents are also used to balance the voltages between the arms [21]. Then, the reference values of the injected circulating currents $i_{\mathrm{cir}a}^*$ and $i_{\mathrm{cir}b}^*$ are determined by the two control targets mentioned above. These control references are used as the inputs of the ICV-based controller, and the output voltage references for the six arms can be calculated [21].

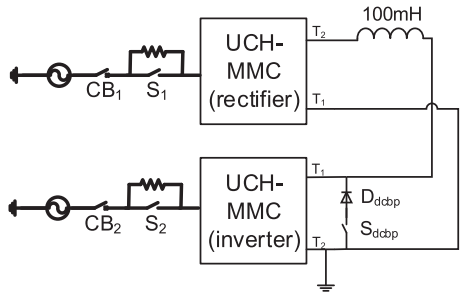

Fig. 10. Monopolar UCH-MMC-based HVDC simulation model.

TABLE IV
UCH-MMC-BASED HVDC PARAMETERS

	Value
Rated power	500 MW
Rated dc voltage	320 kV
Number of submodules per arm	250
Rated ac-side voltage	301.12 kV
Rated summed SM capacitor voltages in an arm	450 kV
Arm inductance	103.26 mH
Submodule capacitance	2.40 mF
Switching frequency of IGBT*	75 Hz

*Equivalent switching frequency of SM is 150 Hz, given that one SM contains two independently controlled IGBT. The switching events are generated with carrier phase-shifted pulse-width modulation method, and are distributed to SMs by SM voltages sorting method.

For a UCH-MMC that operates in constant dc-link current control mode, the dc-link current reference $i_{\rm dc}^*$ can be set according to the operating requirements of the HVDC link. Then, the dc-link current is controlled to track its reference by adjusting the dc-link ICV reference e_d^* [21]. The ac-side active and reactive power control and circulating currents control are similar to those in constant dc-link voltage mode.

V. SIMULATION RESULTS

A. Simulation of the UCH-MMC-Based HVDC

A monopolar HVDC system, composed of two UCH-MMCs, was simulated in Simulink. The structure of the simulation model is shown in Fig. 10, and its parameters are listed in Table IV. An equivalent model of converter arms was built to simulate large amounts of SMs. This equivalent model was built using a technique similar to that in [27], in which equivalent voltage sources for positive and negative current directions are built and then connected to the main circuit by ideal diodes of corresponding directions.

The dc-link current of the UCH-MMC should be above a certain level at any time to ensure that the arm currents are always positive. Therefore, a start-up bypass circuit comprising a diode $D_{\rm dcbp}$ and a switch $S_{\rm dcbp}$ was designed. For the system shown in Fig. 10, the start-up bypass circuit can provide a dc current path when only the inverter-side UCH-MMC is in a deblocked state during the start-up process. The UCH-MMC at the rectifier side can take the dc current after it finishes its start-up process, and the current flow through $D_{\rm dcbp}$ will be zero.

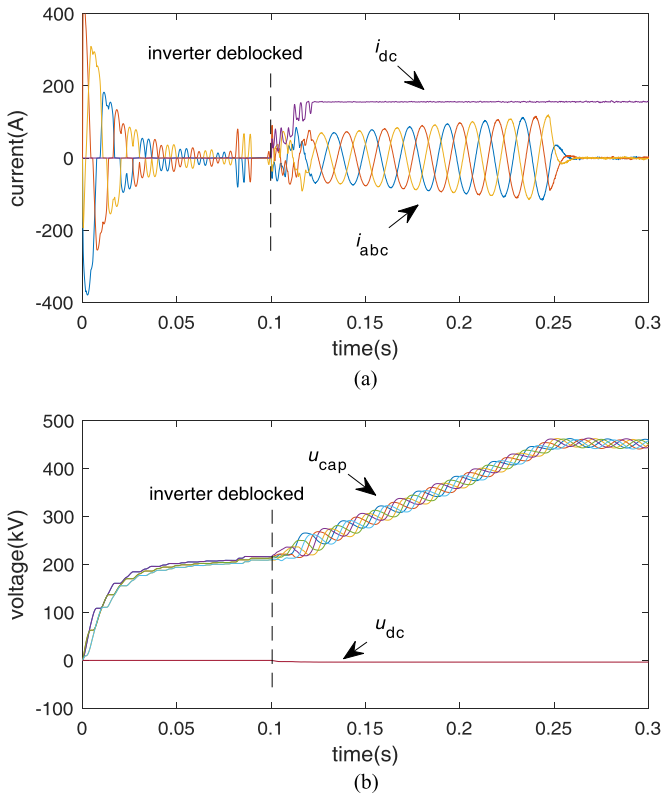

Fig. 11. Start-up process of the UCH-MMC at the inverter side. (a) DC-link and ac-side currents; and (b) summed SM capacitor voltages in each arm and dc-link voltage.

The diode $D_{\rm dcbp}$ can also be cut off by the switch $S_{\rm dcbp}$ after the startup; thus, the dc voltage polarity can be reverted when needed.

1) Start-Up Process: In the start-up process of a UCH-MMC-based HVDC, the inverter side MMC should start first and charge its SM capacitors to rated voltage. The dc-link voltage remains zero and the dc-link current flows through the start-up bypass circuit during the start-up of the inverter. Then, the rectifier side MMC can be started, and the current of the start-up bypass circuit can be transferred to the rectifier side MMC thereafter.

Fig. 11 shows the start-up process of the UCH-MMC at the inverter side. The switch $S_{\rm dcbp}$ was closed first. Then, the circuit breakers $\rm CB_1$ and $\rm CB_2$ were closed, and the ac grid started to charge the SM capacitors through the precharge resistors and the free-wheeling diodes, including D_2 and D_3. Thereafter, the precharge resisters were bypassed by closing switches S_1 and S_2 at 0.08 s. The precharge resistance in the simulation was low to accelerate the precharge process. The precharge currents in real applications are usually much lower than here in the simulation.

At 0.1 s, the UCH-MMC at the inverter side was deblocked and operated in constant dc-link current control mode. The dc-link current reference was set to 156 A (0.1 p.u.). This reference should be higher than the peak value of ac currents during the start-up process to ensure that the arm currents are positive. Fig. 11(a) shows the waveforms of the dc-link current and the

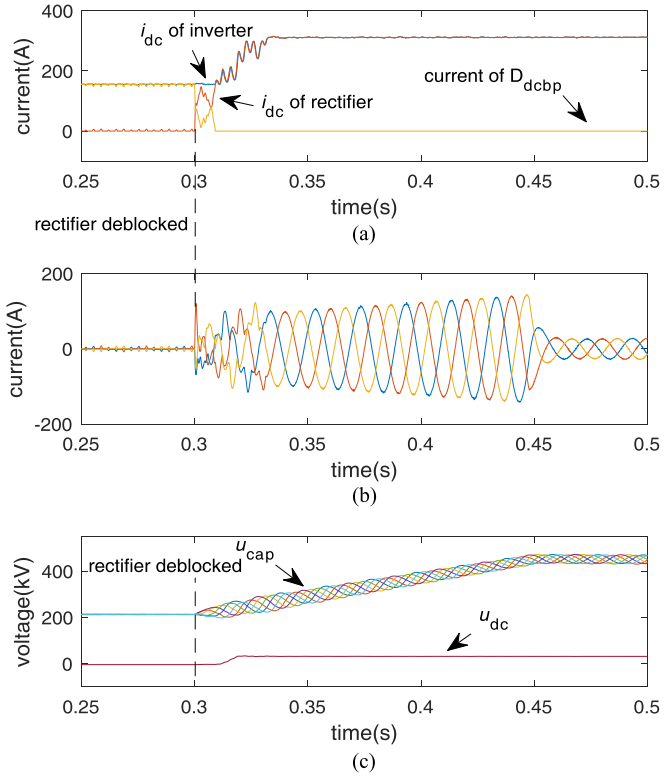

Fig. 12. Start-up procedure of rectifier. (a) DC-link currents; (b) ac-side currents; and (c) summed SM capacitor voltages in each arm and dc-link voltage.

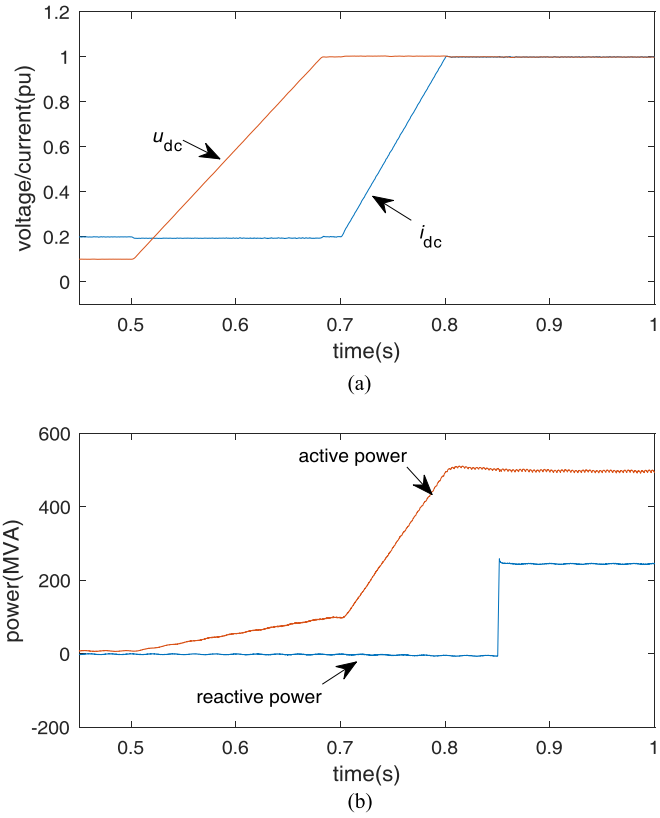

Fig. 13. Voltage and power adjustment. (a) DC-link voltage and current; and (b) ac power of inverter.

three-phase ac-side currents at the inverter side. Fig. 11(b) shows the waveforms of the summed SM capacitor voltages of each arm. After the UCH-MMC was deblocked, the reference of the SM capacitor voltages was raised gradually, and the SM capacitor voltages were charged to their rated value accordingly by the active power control loop. Prior to the startup of the UCH-MMC at the rectifier side, the dc current flowed through the start-up bypass diode, and the dc-link voltage was zero.

Fig. 12 illustrates the start-up process of the UCH-MMC at the rectifier side. After the startup of the inverter-side UCH-MMC was finished, the UCH-MMC at the rectifier side could be started. Fig. 12(a) shows the waveforms of the dc-link current and the three-phase ac-side currents at the rectifier side. At 0.3 s, the rectifier-side UCH-MMC was deblocked and operated in constant dc-link current control mode. The dc-link current reference was set as 312 A (0.2 p.u.), which is higher than that of the inverter, such that the dc-line current could be forced to be transferred from D_{dcbp} to the rectifier. Fig. 12(b) shows the waveforms of the summed SM capacitor voltages of each arm and the dc-link voltage. As soon as the rectifier-side UCH-MMC was deblocked, the inverter-side UCH-MMC was switched to constant dc-link voltage control mode. The dc-link voltage reference was set as 32 kV (0.1 p.u.). In a similar way to that of inverter-side UCH-MMC, the SM capacitor voltages of the rectifier-side UCH-MMC were gradually charged to their rated value.

2) Normal Operation: After the start-up processes of the UCH-MMCs had finished, the HVDC system could enter normal operation. Fig. 13(a) shows that the dc-link voltage was first raised to the rated value by the inverter-side UCH-MMC. Then, the dc-link current was raised to the rated value by the rectifier-side UCH-MMC. Fig. 13(b) shows that, after the dc-line voltage and dc-line current had reached their rated value, the transmitted active power of the HVDC system reached its rated value (500 MW). The output reactive power of the two UCH-MMCs could be independently controlled. In this simulation, the inverter-side output reactive power was set to 250 MVAr.

Fig. 14 shows the steady-state waveforms of the inverter-side UCH-MMC when it outputs the rated active and reactive power. Fig. 14(a) shows the waveforms of the SM capacitor voltage and the output voltage of the upper arm of phase A. Fig. 14(b) shows the waveforms of dc-line current, arm current, ac-side output current, and circulating current. The actively injected circulating current helped ensure that the arm current is always positive by cutting the negative peak of the arm current.

3) Short-Term Reactive Power Support: As analyzed in Section II-C, low power factor can be obtained by lowering dc voltage in short-term reactive power support process. Fig. 15 shows the short-term reactive power support process of the inverter-side UCH-MMC. At the beginning, the inverter-side UCH-MMC output active power of 0.5 p.u. and reactive power of 0.2 p.u., and the dc-link voltage was 1.0 p.u. Thus, the reactive power output could not be greater than 0.25 p.u. under this condition. At 0.18 s, the reactive power demand started to increase, such that the inverter-side UCH-MMC decreased the dc-link voltage to obtain great reactive power output capability.

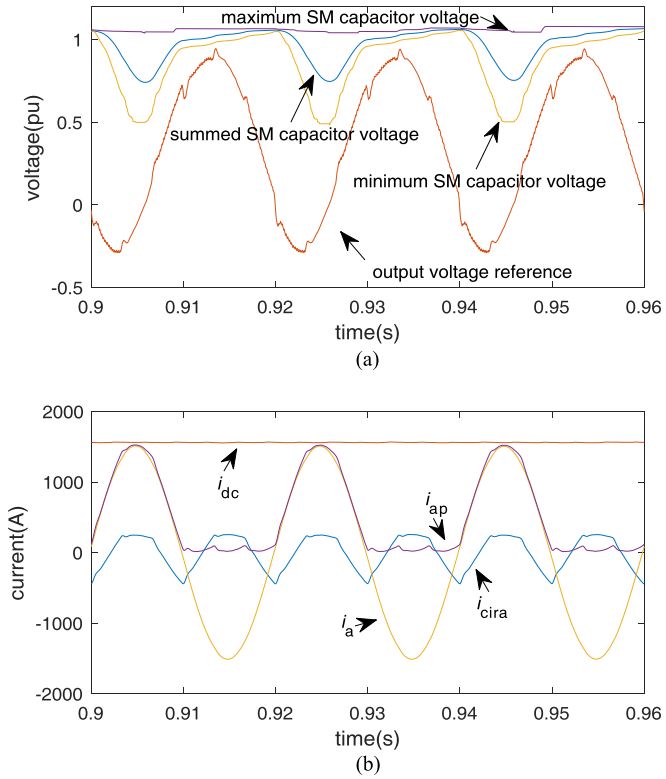

Fig. 14. Steady-state waveforms of inverter-side UCH-MMC. (a) Voltages of the upper arm of phase A; and (b) currents of phase A.

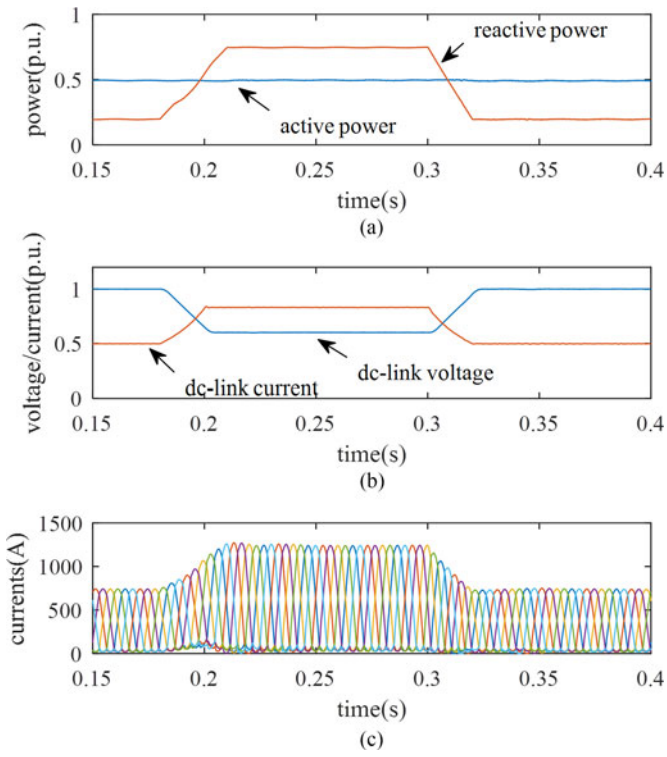

Fig. 15. Short-term reactive power support waveforms of the inverter-side UCH-MMC. (a) AC-side power; (b) dc-link voltage and current; and (c) arm currents.

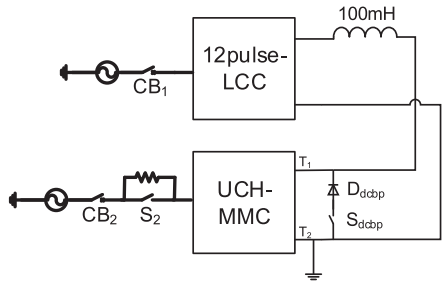

Fig. 16. Monopolar hybrid HVDC simulation model.

TABLE V
LCC PARAMETERS OF HYBRID HVDC MODEL

	Value
Rated power	500 MW
Rated dc voltage	320 kV
Rated valve-side voltage	136.42 kV
Transformer leakage reactance	0.08 p.u.

The dc-link voltage was decreased to 0.6 p.u. and the reactive power output was increased to 0.75 p.u. Meanwhile, the dc-link current was increased to 0.833 p.u. by the rectifier-side UCH-MMC to maintain the active power transmission. At 0.3 s, the reactive power demand decreased, and the system switched back to rated dc-link voltage mode. The arm currents were all kept positive during this process.

B. Simulation of Hybrid HVDC

A monopolar hybrid HVDC system comprising an LCC and a UCH-MMC was simulated in Simulink. The structure of the simulation model is illustrated in Fig. 16. The parameters of LCC are listed in Table V, and the parameters of MMC are the same as in Table IV.

The start-up process of this hybrid HVDC system is similar to that of a two-terminal UCH-MMC-based HVDC system, and the simulation results of the start-up process are not presented herein. A power-reversing process was simulated to verify the feasibility of this hybrid HVDC system and the power-reversing capability of UCH-MMC.

Prior to reversing the power, the HVDC system transmitted active power of 500 MW from LCC to UCH-MMC. At 0.2 s, the LCC decreased the dc-link current to 0.1 p.u. At 0.35 s, the UCH-MMC started to reverse the dc-link voltage polarity gradually. After the dc-link voltage polarity was reversed, the LCC operated as an inverter and the UCH-MMC operated as a rectifier. Then, the LCC raised the dc-link current to 1.0 p.u., and the HVDC system transmitted active power of 500 MW from UCH-MMC to LCC. Fig. 17 shows the waveforms during the power-reversing process. The dc-link voltage and current were both well controlled, and the arm currents were kept positive during the power-reversing process.

VI. EXPERIMENTAL RESULTS

The proposed UCH-MMC topology was verified using a 190 V/5 kVA prototype, as shown in Fig. 18. Fig. 19 shows

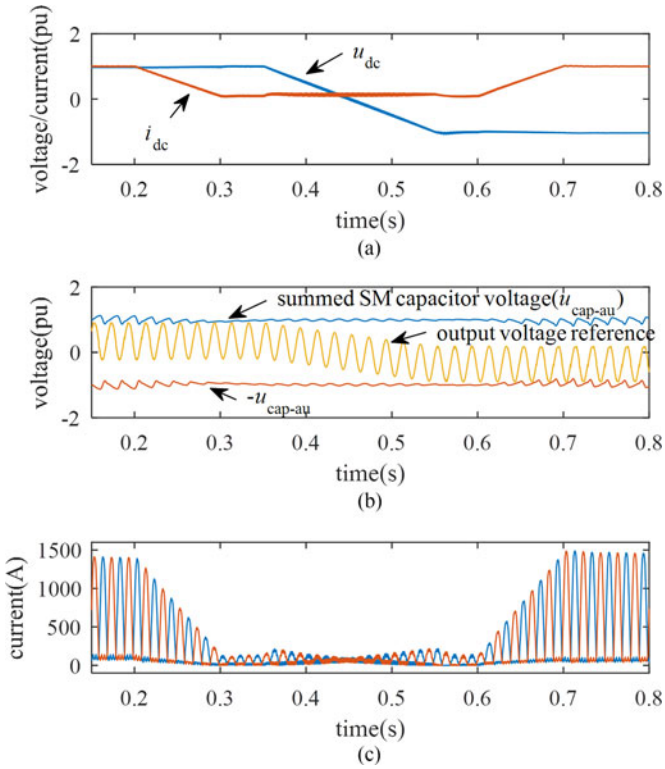

Fig. 17. Power-reversing process. (a) DC-link voltage and current of UCH-MMC; (b) voltages of the upper arm of phase A; and (c) arm currents of phase A.

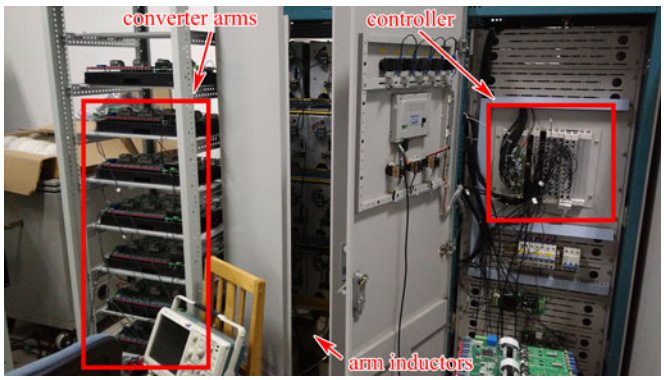

Fig. 18. Photograph of the UCH-MMC prototype.

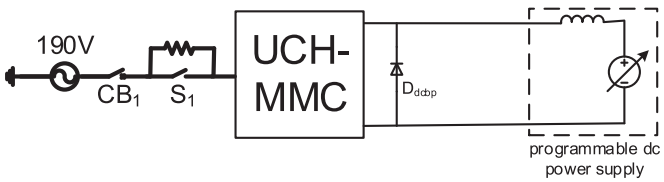

Fig. 19. Experiment circuit of the UCH-MMC prototype.

the experimental circuit. In the experiments, the UCH-MMC operated as an inverter. A programmable dc power supply was used to simulate the rectifier-side converter. The ac side of the UCH-MMC was connected to a regenerative grid simulator. The main parameters of the UCH-MMC prototype are listed in Table VI. The rated active power of the converter itself is 5 kW,

TABLE VI
UCH-MMC PROTOTYPE PARAMETERS

Parameter	Value
Rated active power (W)	3000
Rated line-line ac voltage (V)	190
Rated dc voltage (V)	200
Summed SM capacitor voltages in an arm (V)	300
Arm inductance (mH)	5
Submodule capacitance (μF)	2000
Number of submodules per arm	4

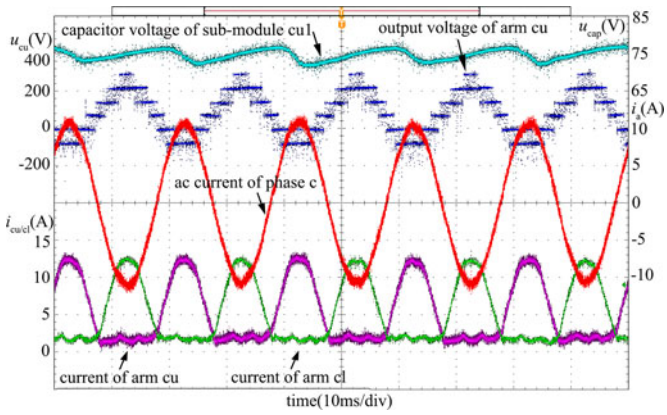

Fig. 20. Steady-state waveforms of UCH-MMC prototype.

but the rated active power of the prototype system is only 3 kW due to the current limit of the dc power supply (15 A).

A. Normal Operation

The start-up process is similar to that in the simulation. Here, only the steady-state waveforms are presented. Fig. 20 shows the steady-state waveforms of the upper arm of phase C when the prototype output rated active power. The experimental waveforms of the arm currents are consistent with the simulated waveforms shown in Fig. 14. The actively injected circulating current effectively cut the negative peak without affecting the ac-side output current, and the arm currents were kept always positive.

B. AC-Side Disturbance

An ac-grid fault was simulated using the regenerative grid simulator. Prior to the occurrence of the ac-grid fault, the UCH-MMC prototype operated as an inverter and in constant dc-link current mode. Moreover, the steady-state dc-line voltage and current were 200 V and 5 A, respectively. The fault lasted for 200 ms, and the ac-grid line-line voltage decreased to 130 V during the fault. This ac voltage overstepped the lower limit given by (13), and active power balance was not maintained even when the power factor was 1.0. However, Fig. 21 shows that the arm currents were still well controlled during the fault. The arm currents were kept always positive even during the transient. No overcurrent appeared in the arm currents or in the ac-side output currents. Given the active power imbalance

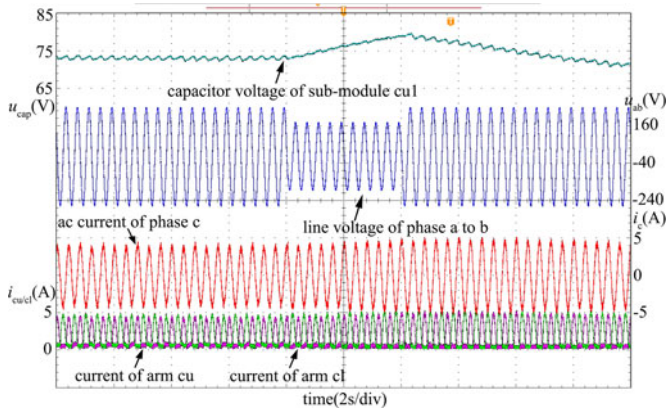

Fig. 21. Experiment results of ac voltage sag.

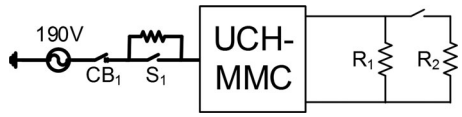

Fig. 22. Experiment circuit of dc-side short fault clearance.

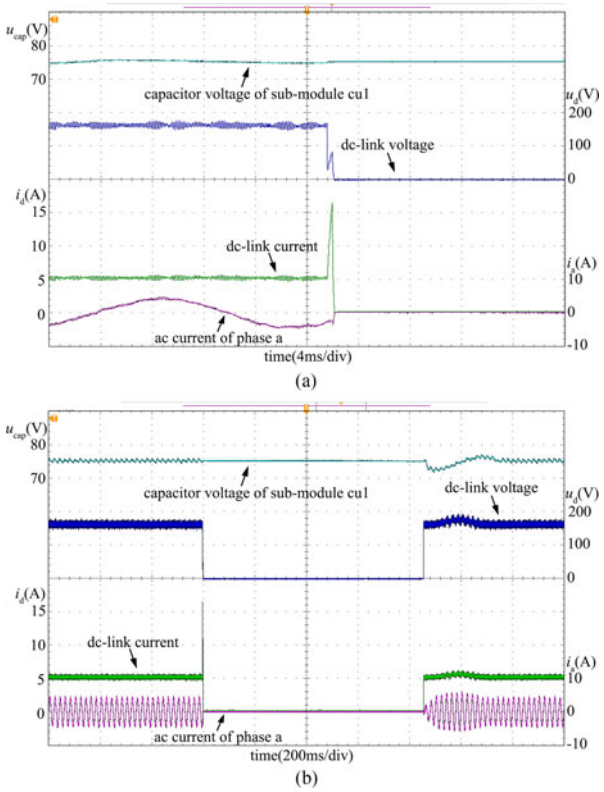

Fig. 23. Experiment results of dc-side short fault clearance. (a) Fault protection; and (b) fault clearance and system restart.

between the ac side and dc side, the SM capacitor voltages rose slightly during the fault.

C. DC-Side Short Fault

Fig. 22 shows the experiment circuit to verify the capability of dc-side short-circuit fault clearance. Prior to the occurrence of the dc fault, the UCH-MMC prototype operated as a rectifier and in constant dc-link voltage control mode. The dc-link output voltage was 180 V, and a 32 Ω resister R_1 was used to simulate the normal dc load. The nonpermanent dc short-circuit fault was simulated by switching in and out a 6 Ω resister R_2. The threshold of dc-link overcurrent protection was set to 15 A. Fig. 23(a) shows that the UCH-MMC was blocked as soon as the dc short-circuit fault protection was triggered and that the dc-link fault current was successfully cleared. Fig. 23(b) shows that, after the short-circuit resistor was switched OFF, the UCH-MMC resumed normal power transmission.

VII. Conclusion

This study proposed a novel UCH-MMC with ACCI. The UCH-MMC was developed from an FB-MMC and possesses the advantages of FB-MMC, such as dc fault blocking and bidirectional dc-link voltage capabilities. By keeping the arm current always positive, the proposed UCH-SM requires fewer switching devices than the FB-MMC. The power flow of the UCH-MMC-based HVDC system can also be reversed by reversing the dc-link voltage polarity. The analysis shows that the rated ac-side voltage should be at a certain value to ensure that the arm currents flow always in the same direction. The power factor of UCH-MMC is limited, and the limitation is associated with ac/dc voltage ratio. The proposed ACCI technique can make it less demanding on the increase in rated ac-side voltage. A detailed comparison for the given example showed that the cost of the required IGBTs of a UCH-MMC is nearly the same as that of an HB-MMC and is significantly lower than that of a hybrid MMC or FB-MMC. The full-load loss of a UCH-MMC is higher than that of a hybrid MMC but slightly lower than that of an FB-MMC.

The UCH-MMC can operate on either constant dc-link voltage control mode or constant dc-link current control mode. The control schemes for the two control modes were presented. The feasibility and the characteristics of the UCH-MMC with ACCI were verified by various simulation results. The characteristics of the start-up process, normal operation, and short-term reactive power support capability were illustrated using the simulation results for a two-terminal UCH-MMC based HVDC. The feasibility of the unidirectional hybrid HVDC system composed of a UCH-MMC and an LCC was also verified using simulation results. Because the characteristics of the UCH-MMC in a hybrid HVDC system are same with those in a two-terminal UCH-MMC-based HVDC system, only the simulation results for a power-reversing process of the hybrid HVDC system are presented in this paper. To further illustrate the feasibility and the characteristics of the UCH-MMC with ACCI, a 190 V/5 kVA prototype of the UCH-MMC was developed and various experiments were also done. The steady-state experimental waveforms show that the actively injected circulating current effectively cut the negative peak and keep the arm currents always positive. The responses of the UCH-MMC under ac-grid faults and dc-line faults were also illustrated using the experimental results.

APPENDIX

A. Injected Circulating Current Calculation

The arm currents can be expressed as

$$i_{x(p,n)} = \pm\frac{1}{2}i_x + \frac{1}{3}i_{\mathrm{dc}} + i_{\mathrm{cir}x} \tag{A-1}$$

where x is *a, b*, or *c* and i_x are the ac-side current of the phase x, and $i_{\mathrm{cir}x}$ is the circulating current of phase x. The following equation can then be obtained easily:

$$\min(i_{xp}, i_{xn}) = \frac{1}{3}i_{\mathrm{dc}} + i_{\mathrm{cir}x} - \frac{1}{2}|i_x|. \tag{A-2}$$

The sum of each phase's minimum arm current is the positive offset current that can be redistributed among three phases to ensure that all the arm currents are positive. This offset current can be distributed into three phases equally to provide a large margin. That is, the minimum arm current of each phase can be the same and can be expressed as

$$i_{\min} = \frac{1}{3}(\min(i_{ap}, i_{an}) + \min(i_{bp}, i_{bn}) + \min(i_{cp}, i_{cn})). \tag{A-3}$$

The sum of circulating currents is always zero. Thus, the following equation can be obtained easily by substituting (A-2) into (A-3):

$$i_{\min} = \frac{1}{3}i_{\mathrm{dc}} - \frac{1}{6}|i_a| - \frac{1}{6}|i_b| - \frac{1}{6}|i_c| \tag{A-4}$$

where $i_{\min}$ should be equal to the minimum arm current of each phase. Therefore, substituting (A-4) into (A-2) can yield the following equation:

$$i_{\mathrm{cir}x} = \frac{1}{2}|i_x| - \frac{1}{6}|i_a| - \frac{1}{6}|i_b| - \frac{1}{6}|i_c|. \tag{A-5}$$

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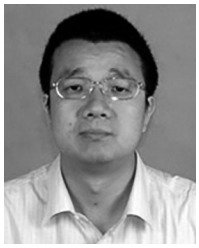

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