An Improved Modulation Scheme of Current-Fed Bidirectional DC–DC Converters For Loss Reduction

Zhiqiang Guo, *Member, IEEE*, Kai Sun, *Senior Member, IEEE*, Tsai-Fu Wu, *Senior Member, IEEE*, and Canbing Li, *Senior Member, IEEE*

***Abstract*—Current-fed bidirectional dc–dc converters have attracted much attention in battery energy storage system applications due to their zero-voltage-switching performances and greater degree of control freedom. However, high efficiency cannot be achieved for both light and heavy load ranges with the present modulation schemes for a current-fed bidirectional dc–dc converter, especially with low battery voltages. A new modulation scheme is proposed to improve the conversion efficiency over a wide load range and with variations in the battery voltage. The relationship between the duty cycle of the secondary full bridge and the phase-shift angle was investigated to lower the power losses with the wide load variations. Based on the operation mode analysis, the control loop with the proposed pulse wide modulation plus phase-shift modulation scheme was developed. Comparisons of the switch conduction loss and the core loss in the series inductor for the previous modulation schemes and the proposed modulation scheme were carried out. The results show that lower power losses occur with the proposed scheme. The experimental results verify the theoretical analysis and effectiveness of the proposed modulation scheme on loss reduction.**

***Index Terms*—Current-fed, dual active bridge (DAB), low conduction loss, pulse wide modulation (PWM) plus phase-shift (PPS).**

I. Introduction

BIDIRECTIONAL dc–dc converters are widely used in energy storage systems, solid state transformers, and electrical vehicle chargers. A dual active bridge (DAB) is the typical solution to bidirectional dc–dc converters [1]–[3]. The simple phase-shift modulation for a DAB can achieve the bidirectional power flow and soft switching. However, when the effective conversion ratio of the converter deviates from 1, a large circulation current may decrease the efficiency.

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Z. Guo is with the School of Automation, Beijing Institute of Technology, Beijing 100081, China (e-mail: guozq@mail.bit.edu.cn).

K. Sun is with the State Key Laboratory of Power Systems, Tsinghua University, Beijing 100084, China (e-mail: sun-kai@mail.tsinghua.edu.cn).

T.-F. Wu is with the Department of Electrical Engineering, National Tsing Hua University, Hsinchu 30013, Taiwan (e-mail: tfwu@ee.nthu.edu.tw).

C. Li is with the College of Electrical and Information Engineering, Hunan University, Changsha 410082, China (e-mail: licanbing@qq.com).

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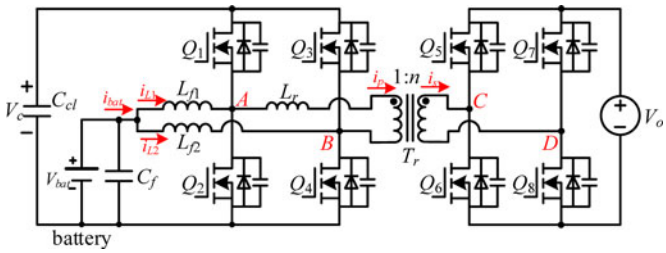


Fig. 1. Current-fed bidirectional dc–dc converter.

Xu *et al.* [4] proposed the PWM plus phase-shift (PPS) control for bidirectional dc–dc converters. Many modulation strategies derived from the PPS have been proposed, including the extended phase-shift modulation [5] and triple phase-shift modulation [6], [7]. In [8], the modulation algorithm was deduced from the particular calculations and analysis of the converter loss. The essence of these modulations is to extend the degree of freedom of the modulation for a wide range of the soft switching and low conduction loss. Researchers have investigated the triangular current mode modulation (TCM) [9] and trapezoidal modulation (TZM) [10] to reduce the peak current in the transformer. TCM and TZM are improved triple phase-shift modulations. In [11], a modified DAB was derived by inserting a small inductor between the transformer center tap and the midpoint of two split output capacitors; this can achieve a wide soft switching for wide voltage conversions. In [12], a fundamental–optimal strategy for a DAB was analyzed using harmonic analysis to optimize the conduction loss. However, the zero voltage switching (ZVS) of the switches was not considered. Recently, frequency domain analyses were conducted to achieve a compromise between the conduction loss and ZVS of the switches [13], [14]. However, it is difficult to implement in a closed-loop control.

A buck/boost converter cascaded with a DAB converter is an excellent solution for a bidirectional dc–dc converter in an energy-storage system, since it meets the requirements of a wide input or output range. The buck/boost converter can work in the PWM to control the output voltage, and the effective conversion ratio of the DAB converter can be set to 1. The DAB converter works with low conduction loss. However, the buck/boost converter works in hard switching. A current-fed bidirectional dc–dc converter was proposed in the literature [15], combining a buck/boost converter and DAB converter by sharing some switches. This type of converter is shown in Fig. 1.

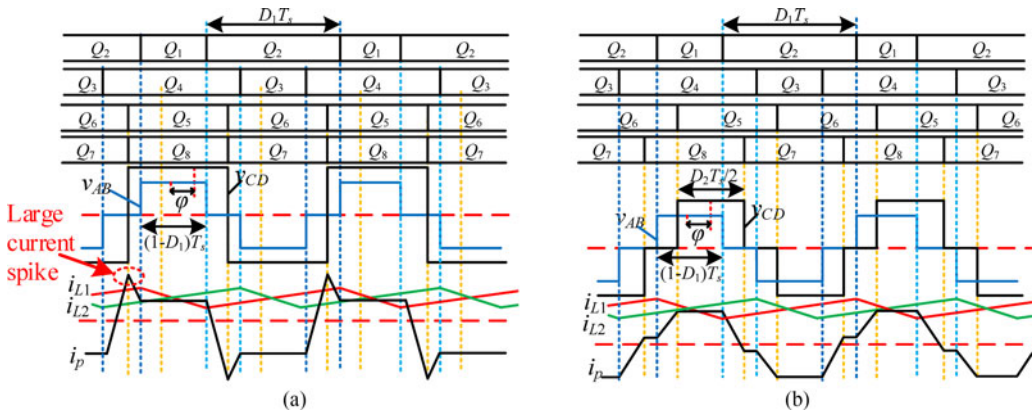


Fig. 2. Conventional modulation strategies for a current-fed bidirectional dc–dc converter. (a) PPS. (b) PPDPS.

A winding-coupled bidirectional ZVS converter was proposed by integrating the winding of the filter inductor into the transformer [16]. By using PPS control, all of the switches worked in soft switching. The clamping voltage was controlled by the PWM of the primary switches, and the bidirectional power flow was controlled by the phase-shift modulation. However, the converters could not achieve high efficiency for light loads because of the large conduction loss. In [17], an optimized PWM plus dual phase-shift (PPDPS) was employed to reduce the conduction loss. However, the converter could not achieve ZVS with heavy loads. A current-fed semi-DAB [18] was developed by replacing two switches with diodes. The converter achieved a highly efficient unidirectional power flow. All of the switches achieved ZVS, and the diodes achieved zero-current switching (ZCS). In [19], [20], the researchers developed a three-phase full-bridge current-fed dc–dc converter without a clamp capacitor. However, it still had difficulty in soft starting. In [21], a modified current-fed dc–dc converter can achieve wide soft switching. However, it increases the conduction loss.

In recent researches, current-fed dc–dc converters have been extended to renewable power systems and hybrid energy storage systems [22]–[29]. Naturally clamped current-fed push-pull dc–dc converters are proposed and studied in [22]–[24]. Without active clamp or snubber circuits, the power density of the converter can be improved. The current-fed converter can achieve soft-switching and low voltage stress in the switches. Impulse commutated current-fed converters are proposed in [25], [26]. The converter maintains ZCS for all the switches, reducing the current stress of the switches. In [27], photovoltaic systems and energy storage systems are integrated in a current-fed dc–dc converter to supply power for the load. Because of a greater degree of freedom, the photovoltaic system, and energy storage system are decoupled in the control loop. A dual input current-fed DAB converter powering a fuel-cell-battery system achieves a near-ripple-free dc bus voltage [28]. Ding *et al.* [29] develop a current-fed bidirectional dc–dc converter as a symmetric structure for a battery and super-capacitor system. The above research shows that current-fed bidirectional dc–dc converters are more flexible and applicable because they offer a greater degree of freedom for control.

The main purpose of this paper is to improve its efficiency of the current-fed bidirectional dc–dc converter. Based on the premise that all the switches can achieve ZVS, there are two main objectives in this paper. First is to reduce root-mean-square (RMS) current in the switches to reduce the conduction loss, and second is to reduce the peak current in the transformer to reduce the core loss in the series inductor. This paper is organized as follows. In Section II, different operation modes for current-fed bidirectional dc–dc converters are analyzed. Then, the modified operation modes are proposed. The ZVS conditions of the proposed modified operation modes were analyzed for modulation and converter design. In Section III, an improved modulation scheme is developed by synthesizing the modified operation modes with the advantages of a reduced conduction loss and core loss during the entire loads. The modulation trajectories are investigated, and the switch conduction loss and core loss in the series inductor for the proposed modulation are compared with the other modulation strategies. In Section IV, the experimental results verified the highly efficient performance in the system. Section V provides the conclusions.

II. Operation Modes of the Current-Fed Bidirectional DC–DC Converter

A. Review of the Modulations for the Current-Fed Bidirectional DC–DC Converter

Fig. 1 shows the circuit of the current-fed bidirectional dc–dc converter. L_{f1} and L_{f2} are the dc inductors on the battery side, and $L_{f1} = L_{f2} = L_f$. The average current in i_{L1} and i_{L2} is defined as I_L. L_r is the series inductor for the phase-shift modulation. V_{bat} is the battery voltage. V_o is the output voltage, and V_c is the voltage of the clamping capacitor. The reference V_c was set to be V_o/n, where n is the turns ratio of the transformer. $nV_c/V_o = 1$ is not the optimized condition for minimum RMS current in the transformer at high power [17]. However, if nV_c/V_o is not equal to 1, the converter may not maintain ZVS of all the switches [17]. Therefore, $nV_c/V_o = 1$ is a good precondition for all the switches to work in ZVS. Moreover, when $nV_c/V_o = 1$, the peak current in the transformer during heavy load is reduced, and the core loss in the series inductor can be reduced. To synthesize conduction loss and soft-switching

analyses, the premise of $nV_c/V_o = 1$ is set. Fig. 2 shows the modulation strategies for the current-fed bidirectional dc–dc converter. Fig. 2(a) is the PPS modulation [14]. On the battery side, $Q_1 - Q_4$ are modulated by the PWM to control the voltage of the clamping capacitor, where D_1 is the duty cycle of Q_2 and Q_4. T_s is the switching period. The bidirectional power flow is modulated by the phase shift between $v_{\rm AB}$ and $v_{\rm CD}$, where φ is the phase-shift angle. The voltage amplitude of $v_{\rm AB}$ is V_o/n, and the voltage amplitude of $v_{\rm CD}$ is V_o. In Fig. 2(a), Q_5 and Q_8 are the same gate signal, and Q_6 and Q_7 are the same gate signal. Therefore, $v_{\rm CD}$ has a square waveform. The peak current in the transformer is expressed as $\frac{V_o D_1 T_s}{2nL_r} - \frac{V_o T_s}{4nL_r}$, and this will be analyzed in the following section. The peak current is not associated with the phase shift angle φ. Especially under light loads, the transformer and switches have to handle a large current amplitude. The efficiency under light loads becomes very low. Fig. 2(b) is the PPDPS modulation [17]. In this modulation scheme, the primary switches work in PWM control, and the secondary full bridge works in a phase shift manner. D_2 is the effective duty cycle in the secondary full bridge. The power flow is controlled by the phase shift between $v_{\rm AB}$ and $v_{\rm CD}$. Compared with PPS modulation, the peak current in the transformer is reduced. The time interval for power transmission is the positive or negative voltage overlap of $v_{\rm AB}$ and $v_{\rm CD}$, which decreases with the increase of the phase shift angle φ. Based on voltage-second balance, the decrease of the time interval causes a large peak current in the transformer for the constant power transmission. This occurs under heavy loads. To overcome the drawback of these modulation schemes, this paper will investigate the different operation modes for the converter shown in Fig. 1.

The ZVS conditions for the switches are shown in Table I, where ΔI_p is the minimum current amplitude to charge and discharge the junction capacitors of the switches on the battery side for ZVS, and ΔI_s is the minimum current to charge and discharge the junction capacitors of the switches on the output side for ZVS. The ZVS conditions for $Q_1 - Q_4$ are associated with the current ripple of the dc inductor current. If the dc inductor currents i_{L1} and i_{L2} have a large current ripple, $Q_1 - Q_4$ can easily achieve ZVS. The research focus in this paper is how to optimize the modulation scheme to reduce losses on the premise of the ZVS.

TABLE I
ZVS CONDITIONS

Switches	Current during the switch-on	ZVS conditions during commutation
Q_1	$i_p(t)$-max (i_{L1})	max (i_{L1})-$i_p(t)$ >ΔI_p
Q_2	min (i_{L1})-$i_p(t)$	$i_p(t)$ - min (i_{L1})>ΔI_p
Q_3	- max (i_{L2})-$i_p(t)$	max (i_{L2})+$i_p(t)$>ΔI_p
Q_4	min (i_{L2})+$i_p(t)$	- min (i_{L2})-$i_p(t)$> ΔI_p
Q_5	-$i_p(t)$ /n	$i_p(t)$ /n >ΔI_s
Q_6	$i_p(t)$/n	-$i_p(t)$/n>ΔI_s
Q_7	$i_p(t)$ /n	-$i_p(t)$ /n >ΔI_s
Q_8	-$i_p(t)$ /n	$i_p(t)$ /n >ΔI_s

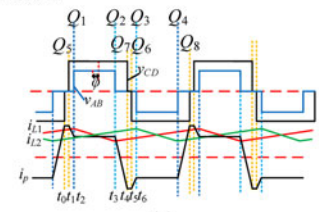
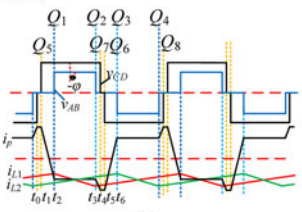
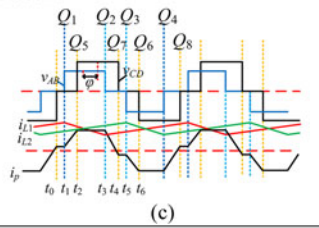
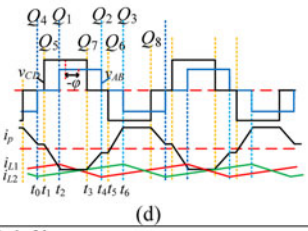
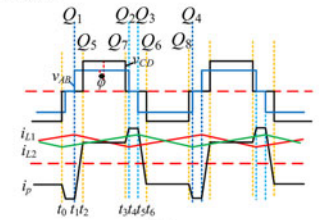
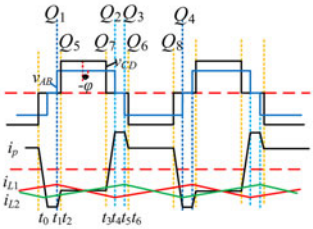
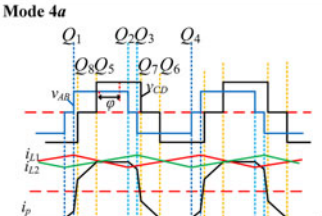
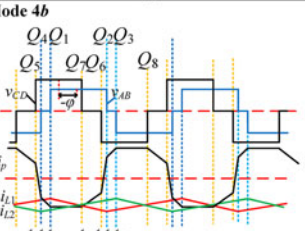
B. Analyses of the Key Operation Modes

Considering the practical operation modes, the converter should have a sufficient time interval to transmit power. As seen in Fig. 2, the positive or negative voltage overlap of $v_{\rm AB}$ and $v_{\rm CD}$ needs to be as much as possible. Table II shows the different practical operation modes of the current-fed bidirectional dc–dc converter for the case when $-\pi/2 \le \varphi \le \pi/2$; these modes take into consideration of the variables D_1, D_2, and φ. The power transmitted from the battery to the output is defined as the forward power flow, where φ is greater than zero. The power transmitted from the output to the battery is defined as the reverse power flow, where φ is less than zero. Because the forward and reverse power flows are symmetric, only the forward power flow was analyzed. Furthermore, the reverse power flow can be analyzed in the same manner, and the same conclusion can be drawn.

For the forward power flow in Table II, the ZVS for Q_1 and Q_2 is determined by the error between the current in the filter inductor L_{f1} and the current in the transformer; ZVS for Q_3 and Q_4 is determined by the sum of the currents in the filter inductor L_{f2} and the transformer. Because $nV_c/V_o = 1$, the slew rate of the current in the transformer is zero during the time interval of a positive or negative voltage overlap in $v_{\rm AB}$ and $v_{\rm CD}$. As long as the current ripple in L_{f1} and L_{f2} is large enough, ZVS for $Q_1 - Q_4$ can be achieved. As show in Mode 1*a* in Table II(a), $i_p(t_1)$ is greater than zero, and $i_p(t_4)$ are less than zero. According to Table I, Q_5 and Q_7 have the potential to achieve ZVS. For Mode 2*a* in Table II(c), $i_p(t_2)$ is greater than zero, and $i_p(t_4)$ are less than zero, hence Q_5 and Q_7 have the potential to achieve ZVS. For Mode 3*a* in Table II(g), $i_p(t_2)$ and $i_p(t_3)$ are both greater than zero, in which Q_5 has the potential to achieve ZVS. However, Q_7 cannot achieve ZVS in this case. For Mode 4*a* in Table II(e), $i_p(t_2)$ is greater than zero and $i_p(t_5)$

$$i_p(t) = \begin{cases} I_{p0} & (t_0 < t < t_1) \\ I_{p1} - \dfrac{V_o}{nL_r}(t - t_1) & (t_1 < t < t_2) \\ I_{p2} & (t_2 < t < t_3) \\ I_{p3} - \dfrac{V_o}{nL_r}(t - t_3) & (t_3 < t < t_4) \end{cases} \quad \begin{aligned} t_0 &= 0 \\ t_1 &= \left(\frac{1}{2} - \frac{D_2}{2}\right) T_s \\ t_2 &= \left(\frac{D_1}{2} - \frac{D_2}{4} - \frac{\varphi}{2\pi}\right) T_s \\ t_3 &= \left(1 - \frac{D_1}{2} - \frac{D_2}{4} - \frac{\varphi}{2\pi}\right) T_s \\ t_4 &= \tfrac{1}{2} T_s \end{aligned} \tag{1}$$

TABLE II
DIFFERENT OPERATION MODES OF THE CURRENT-FED BIDIRECTIONAL DC–DC CONVERTER

	Forward power flow (φ>0)	Reverse power flow (φ<0)
D_1>0.5, 0<D_2<1 **Mode 1*a*:** 0<φ<$\pi(D_1$-1 +D_1/2); **Mode 1*b*:** $\pi(1$-D_1-D_2/2)<φ<0;	**Mode 1*a***  (a)	**Mode 1*b***  (b)
D_1>0.5, 0<D_2<1 **Mode 2*a*:** 0<max{$\pi(1$-D_1-D_2/2), $\pi(D_2$/2+D_1-1)} <φ<min{$\pi(D_1$-D_2/2), $\pi(1$-D_1+D_2/2)}; **Mode 2*b*:** max{$\pi(D_1$-1-D_2/2), $\pi(D_2$/2-D_1)} <φ<min{$\pi(D_1$-1+D_2/2), $\pi(1$-D_1-D_2/2)}<0;	**Mode 2*a***  (c)	**Mode 2*b***  (d)
D_1>0.5, 0<D_2<1 **Mode 3*a*:** 0<φ<$\pi(1$-D_1-D_2/2); **Mode 3*b*:** $\pi(D_1$-1+D_2/2)<φ<0;	**Mode 3*a***  (e)	**Mode 3*b***  (f)
D_1>0.5, 0<D_2<1 **Mode 4*a*:** 0<$\pi(D_1$-D_2/2)<φ<min{$\pi(1$-D_1+D_2/2), π/2}; **Mode 4*b*:** max{$\pi(D_1$-1-D_2/2), -π/2}<φ<$\pi(D_2$/2–D_1)<0;	**Mode 4*a***  (g)	**Mode 4*b***  (h)

is less than zero, so Q_5 and Q_7 have the potential to achieve ZVS. For Q_6, the same conclusion with Q_5 can be derived. For Q_8, the same conclusion with Q_7 can be derived. Not all the switches in Mode 3*a* can achieve ZVS, but all the switches in Modes 1*a*, 2*a*, and 4*a* have the potential to achieve ZVS. Modes 1*a*, 2*a*, and 4*a* will be the key operation modes analyzed in this paper. To simplify the analyses in this section, the commutation during the dead time interval is ignored.

1) Mode 1a: The key waveforms of Mode 1*a* are shown in Table II(a). The current in the transformer during half of the switching period is expressed in (1) at the bottom of the previous page, where

$$\begin{aligned} I_{p0} &= I_{p1} = \frac{V_o D_2 T_s}{4nL_r} - \frac{V_o(1-D_1)T_s}{2nL_r} \\ I_{p2} &= I_{p3} = \frac{V_o T_s}{nL_r}\left(\frac{\varphi}{2\pi}\right) \\ I_{p4} &= \frac{V_o(1-D_1)T_s}{2nL_r} - \frac{V_o D_2 T_s}{4nL_r}. \end{aligned} \tag{2}$$

When D_2 is equal to 1, Mode 1*a* becomes the PPS modulation. Substituting $D_2 = 1$ into (2), the peak current in PPS is expressed as $\frac{V_o D_1 T_s}{2nL_r} - \frac{V_o T_s}{4nL_r}$.

The transmitted power in Mode 1*a* is expressed as

$$P_o = \frac{2}{T_s}\int_{t_0}^{t_4} (v_{\mathrm{AB}} i_p)\, dt = \frac{V_o^2 T_s}{n^2 L_r}(1-D_1)\frac{\varphi}{\pi}. \tag{3}$$

The power is associated with D_1 and φ, but independent of D_2. In this mode, the phase angle is in the range of $0 < \frac{\varphi}{2\pi} < \frac{D_2}{4} - \frac{1-D_1}{2}$. Equation (2) shows that, in order to reduce the peak current, D_2 should be reduced. The minimum value of D_2 in this mode is $\frac{2\varphi}{\pi} + 2(1-D_1)$. In this case, the key waveforms of the modified Mode 1*a* are shown in Fig. 3. During the switching period, Q_1 and Q_5 are commutated at the same time, and Q_3 and Q_6 are commutated at the same time. The peak current amplitude is reduced.

2) Mode 2a: The key waveforms of Mode 2*a* are shown in Table II(c). The current in the transformer during half of the

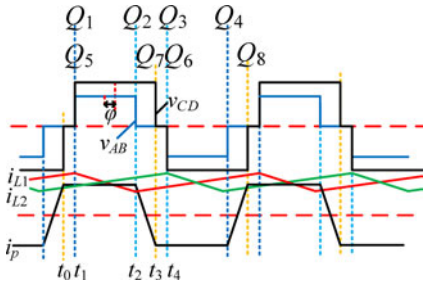


Fig. 3. Modified Mode 1*a*.

switching period is expressed in (4) at the bottom of this page, where

$$\begin{aligned} I_{p0} &= I_{p1} = \frac{V_o D_2 T_s}{4nL_r} - \frac{V_o(1-D_1)T_s}{2nL_r} \\ I_{p2} &= I_{p3} = \frac{V_o T_s}{nL_r}\left(\frac{\varphi}{2\pi}\right) \\ I_{p4} &= \frac{V_o(1-D_1)T_s}{2nL_r} - \frac{V_o D_2 T_s}{4nL_r}. \end{aligned} \tag{5}$$

The transmitted power is expressed as

$$\begin{aligned} P_o &= \frac{2}{T_s}\int_{t_0}^{t_4} (v_{\mathrm{AB}} i_p)\, dt \\ &= \frac{V_o^2 T_s}{2n^2 L_r}\left(\frac{D_2}{2} - \frac{{D_2}^2}{8} - \frac{\varphi^2}{2\pi^2} - \frac{D_1 D_2}{2}\right. \\ &\quad \left. + \frac{\varphi}{\pi} - \frac{{D_1}^2}{2} + D_1 + \frac{D_2\varphi}{2\pi} - \frac{D_1\varphi}{\pi} - \frac{1}{2}\right). \end{aligned} \tag{6}$$

In this mode, the phase angle is in the range expressed by (7), in which (8) is satisfied.

$$\begin{aligned} 0 &< \max\left\{\pi\left(1-D_1-\frac{D_2}{2}\right), \pi\left(\frac{D_2}{2}+D_1-1\right)\right\} \\ &\le \varphi \le \min\left\{\pi\left(D_1-\frac{D_2}{2}\right), \pi\left(1-D_1+\frac{D_2}{2}\right)\right\} \end{aligned} \tag{7}$$

$$\begin{cases} \frac{dP_o}{d\varphi} = \left(\frac{V_o}{n}\right)^2 \frac{T_s}{2\pi L_r}\left(1 - \frac{\varphi}{\pi} + \frac{D_2}{2} - D_1\right) > 0 \\ \frac{dP_o}{dD_2} = \left(\frac{V_o}{n}\right)^2 \frac{T_s}{4L_r}\left(1 - D_1 - \frac{D_2}{2} + \frac{\varphi}{\pi}\right) > 0 \\ \frac{d^2 P_o}{dD_2\, d\varphi} = \left(\frac{V_o}{n}\right)^2 \frac{T_s}{4\pi L_r} > 0. \end{cases} \tag{8}$$

Therefore, the output power is increased with the increase of D_2 or φ. The RMS current in the transformer is expressed as $i_{p\_\mathrm{rms}}(D_2,\varphi) = \sqrt{\frac{2}{T_s}\int_0^{T_s/2} i_p(t)dt}$. With the help of Mathcad 15, the relationship of the D_2 and φ for different output powers in Mode 2*a* is shown in Fig. 4, where $V_c = V_o/n = 134$ V, $L_r = 14\,\mu$H, $V_{\mathrm{bat}} = 48$ V, and $T_s = 12.5\,\mu s$. Fig. 4(a) shows D_2 versus φ for different output powers. In order to keep the output power constant, D_2 is decreased with the increase of the phase-shift angle φ. Fig. 4(b) shows the RMS current in the transformer versus φ for different output powers. For a constant output power, the RMS current in the transformer increases with the increase of the phase-shift angle φ. Simultaneously, D_2 is decreased. Therefore, in order to reduce the RMS current in the transformer, the phase-shift angle φ should be as low as possible. Hence, the reactive power during the switching period can be reduced. Equation (7) shows that the minimum value of φ in Mode 2*a* is expressed as $\max\{\pi(1-D_1-\frac{D_2}{2}), \pi(\frac{D_2}{2}+D_1-1)\}$. As long as $D_2 > 2(1-D_1)$, the minimum value of φ is equal to $\pi[\frac{D_2}{2} - (1-D_1)]$. The key waveforms of Mode 2*a* are shown in Fig. 5 for this case. Modified Mode 2*a* coincides with modified Mode 1*a*. Actually, it is the boundary mode of Mode 1*a* and Mode 2*a*, which is defined as Mode 2*a_m*. The current in the transformer during half of the switching period for Mode 2*a_m* is expressed in (9).

$$i_p(t) = \begin{cases} I_{p1} = I_{p0} & (t_0 < t < t_1) \\ I_{p2} = I_{p1} & (t_1 < t < t_2) \\ I_{p2} - \frac{V_o}{nL_r}(t-t_2) & (t_2 < t < t_2) \end{cases} \begin{aligned} &t_0 = 0 \\ &t_1 = \left(\tfrac{1}{2} - \tfrac{D_2}{2}\right) T_s \\ &t_2 = \left(\tfrac{3}{2} - D_1 - \tfrac{D_2}{2}\right) T_s \\ &t_3 = \tfrac{1}{2} T_s \end{aligned} \tag{9}$$

where

$$\begin{aligned} I_{p0} = I_{p1} = I_{p2} &= \frac{V_o D_2 T_s}{4nL_r} - \frac{V_o(1-D_1)T_s}{2nL_r} \\ I_{p3} &= \frac{V_o(1-D_1)T_s}{2nL_r} - \frac{V_o D_2 T_s}{4nL_r}. \end{aligned} \tag{10}$$

$$i_p(t) = \begin{cases} I_{p0} & (t_0 < t < t_1) \\ I_{p1} + \frac{V_o}{nL_r}(t-t_1) & (t_1 < t < t_2) \\ I_{p2} & (t_2 < t < t_3) \\ I_{p3} - \frac{V_o}{nL_r}(t-t_3) & (t_3 < t < t_4) \end{cases} \begin{aligned} &t_0 = 0 \\ &t_1 = \left(\tfrac{D_1}{2} - \tfrac{D_2}{4} - \tfrac{\varphi}{2\pi}\right) T_s \\ &t_2 = \left(\tfrac{1}{2} - \tfrac{D_2}{2}\right) T_s \\ &t_3 = \left(1 - \tfrac{D_1}{2} - \tfrac{D_2}{4} - \tfrac{\varphi}{2\pi}\right) T_s \\ &t_4 = \tfrac{1}{2} T_s \end{aligned} \tag{4}$$

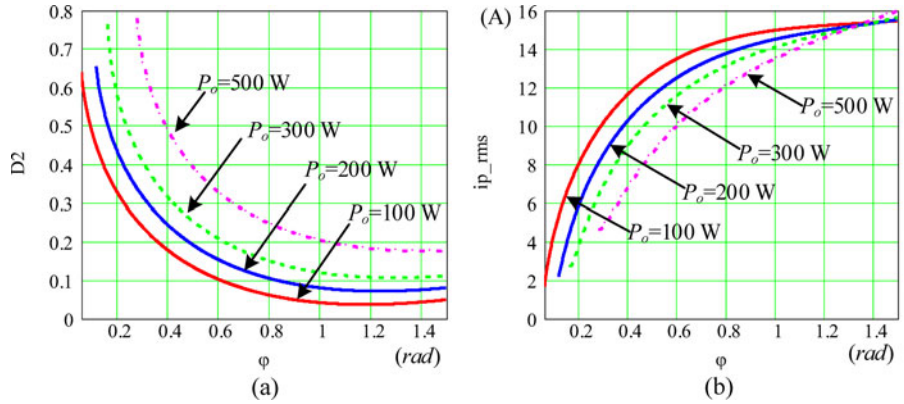


Fig. 4. Relationship between D_2 and φ for different output powers in Mode 2*a*. (a) D_2 versus φ for different output powers. (b) RMS current in the transformer versus φ for different output powers.

The transmitted power in Mode 2*a_m* is expressed as

$$P_o = \frac{2}{T_s}\int_{t_0}^{t_4} (v_{\mathrm{AB}} i_p)\, dt = \frac{V_o^2 T_s}{n^2 L_r}(1-D_1)\frac{\varphi}{\pi}. \tag{11}$$

3) Mode 4a: The key waveforms of Mode 4*a* are shown in Table II(g). The current in the transformer during half of the switching period is expressed in (12) at the bottom of this page, where

$$\begin{aligned}
I_{p0} &= \frac{V_o T_s}{nL_r}\left(\frac{D_1}{2}-\frac{\varphi}{2\pi}\right) - \frac{V_o(1-D_1)T_s}{2nL_r}\\
I_{p1} &= \frac{V_o D_2 T_s}{4nL_r} - \frac{V_o T_s}{nL_r}\left(\frac{1}{2}-\frac{D_2}{4}-\frac{\varphi}{2\pi}\right)\\
I_{p2} &= I_{p3} = \frac{V_o T_s}{nL_r}\left(\frac{\varphi}{2\pi}\right)\\
I_{p4} &= \frac{V_o(1-D_1)T_s}{2nL_r} - \frac{V_o T_s}{nL_r}\left(\frac{D_1}{2}-\frac{\varphi}{2\pi}\right).
\end{aligned} \tag{13}$$

The transmitted power is expressed as

$$\begin{aligned}
P_o &= \frac{2}{T_s}\int_{t_0}^{t_4} (v_{\mathrm{AB}} i_p)\, dt\\
&= \frac{V_o^2 T_s}{2n^2 L_r}\left(\frac{D_2}{2}+D_1+\frac{\varphi}{\pi}-\frac{{D_2}^2}{4}-{D_1}^2-\frac{\varphi^2}{\pi^2}-\frac{1}{2}\right).
\end{aligned} \tag{14}$$

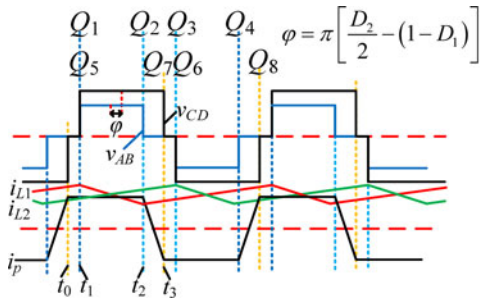


Fig. 5. Key waveforms in Mode 2*a_m*.

In this mode, the phase angle is in the range expressed in (15), in which (16) is satisfied,

$$0 < \pi\left(D_1-\frac{D_2}{2}\right) < \varphi < \min\left\{\pi\left(1-D_1+\frac{D_2}{2}\right), \frac{\pi}{2}\right\} \tag{15}$$

$$\begin{cases}
\dfrac{dP_o}{d\varphi} = \left(\dfrac{V_o}{n}\right)^2 \dfrac{T_s}{2\pi L_r}\left(1-\dfrac{2\varphi}{\pi}\right) > 0\\
\dfrac{dP_o}{dD_2} = \left(\dfrac{V_o}{n}\right)^2 \dfrac{T_s}{4L_r}(1-D_2) > 0\\
\dfrac{d^2 P_o}{dD_2 d\varphi} = 0.
\end{cases} \tag{16}$$

$$i_p(t) = \begin{cases}
I_{p0} + \dfrac{2V_o}{nL_r}(t-t_0) & (t_0 < t < t_1)\\
I_{p1} + \dfrac{V_o}{nL_r}(t-t_1) & (t_1 < t < t_2)\\
I_{p2} & (t_2 < t < t_3)\\
I_{p3} - \dfrac{V_o}{nL_r}(t-t_3) & (t_3 < t < t_4)
\end{cases} \qquad \begin{aligned}
t_0 &= 0\\
t_1 &= \left(\frac{D_2}{4}-\frac{D_1}{2}+\frac{\varphi}{2\pi}\right)T_s\\
t_2 &= \left(\frac{1-D_1}{2}-\frac{D_2}{4}+\frac{\varphi}{2\pi}\right)T_s\\
t_3 &= (1-D_1)\,T_s\\
t_4 &= \frac{1}{2}T_s
\end{aligned} \tag{12}$$

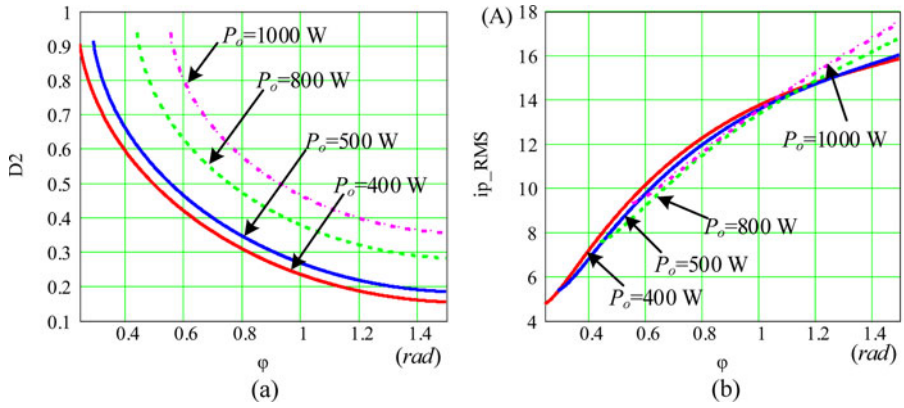


Fig. 6. Relationship between D_2 and φ for different output powers in Mode 4*a*. (a) D_2 versus φ for different output powers. (b) RMS current in the transformer versus φ for different output powers.

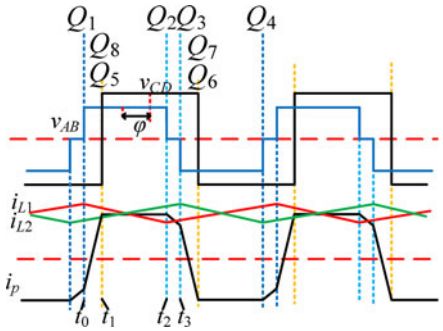


Fig. 7. Modified Mode 4*a*.

Therefore, the output power increases with the increase of D_2 and φ. The RMS current in the transformer in this case is expressed as $i_{p\_\mathrm{rms}}(D_2,\varphi)=\sqrt{\frac{2}{T_s}\int_0^{T_s/2} i_p(t)dt}$. With the help of Mathcad 15, the relationship of the D_2 and φ for different output powers in Mode 4*a* is shown in Fig. 6, where $V_c = V_o/n = 134$ V, $L_r = 14\,\mu$H, $V_{\mathrm{bat}} = 48$ V, and $T_s = 12.5\,\mu s$. Fig. 6(a) shows D_2 versus φ for different output powers. Fig. 6(b) shows the RMS current in the transformer versus φ for different output powers. Based on Fig. 6, conclusions similar to those for Mode 2*a* can be drawn. To reduce the RMS current in the transformer, D_2 should be as large as possible, so φ becomes lower. The maximum value of D_2 is equal to 1 in Mode 4*a*. In this case, the key waveforms of Mode 4*a* are shown in Fig. 7, which is defined as Mode 4*a_m*. Actually, Mode 4*a_m* is the PPS when the phase-shift angle becomes larger. The current in the transformer during half of the switching period for Mode 4*a_m* is expressed as follows:

$$i_p(t)=\begin{cases} I_{p0}+\frac{2V_o}{nL_r}(t-t_0) & (t_0<t<t_1) \\ I_{p1}=I_{p2} & (t_1<t<t_2) \\ I_{p2}-\frac{V_o}{nL_r}(t-t_3) & (t_2<t<t_3) \end{cases} \quad \begin{aligned} t_0&=0 \\ t_1&=\left(\tfrac{D_2}{4}-\tfrac{D_1}{2}+\tfrac{\varphi}{2\pi}\right)T_s \\ t_2&=(1-D_1)\,T_s \\ t_3&=\tfrac{1}{2}T_s \end{aligned} \tag{17}$$

where

$$\begin{aligned} I_{p0}&=\frac{V_oT_s}{nL_r}\left(\frac{D_1}{2}-\frac{\varphi}{2\pi}\right)-\frac{V_o\,(1-D_1)\,T_s}{2nL_k} \\ I_{p1}&=I_{p2}=\frac{V_oT_s}{nL_r}\left(\frac{\varphi}{2\pi}\right) \\ I_{p3}&=\frac{V_o(1-D_1)T_s}{2nL_r}-\frac{V_oT_s}{nL_r}\left(\frac{D_1}{2}-\frac{\varphi}{2\pi}\right). \end{aligned} \tag{18}$$

The transmitted power is expressed as

$$\begin{aligned} P_o&=\frac{2}{T_s}\int_{t_0}^{t_4}(v_{\mathrm{AB}}i_p)\,dt \\ &=\frac{V_o^2T_s}{2n^2L_r}\left(D_1+\frac{\varphi}{\pi}-{D_1}^2-\frac{\varphi^2}{\pi^2}-\frac{1}{4}\right). \end{aligned} \tag{19}$$

The modified operation modes for the reverse power flow were derived by analyzing the reverse power flow (Mode 1*b*, Mode 2*b*, and Mode 4*b*) in the same manner, as shown in Fig. 8.

C. ZVS Conditions for the Modified Operation Mode

In Section II-B, the modified operation modes were proposed for optimizing the peak current and RMS current without considering the ZVS condition of the switches. In this section, the ZVS conditions for the modified operation modes will be analyzed.

1) Mode 2a_m: According to (9) and (10), i_p should be no less than $n\Delta I_s$ to achieve the ZVS for Q_5 and Q_7. The following conditions should be satisfied:

$$\begin{aligned} I_{p0}=I_{p1}&=\frac{V_oD_2T_s}{4nL_r}-\frac{V_o(1-D_1)T_s}{2nL_r}\geq n\Delta I_s \\ D_2&\geq 2(1-D_1)+\frac{4L_rn^2\Delta I_s}{V_oT_s}=D_{2m}+D_m, \\ D_{2m}&=2(1-D_1), D_m=\frac{4L_rn^2\Delta I_s}{V_oT_s}. \end{aligned} \tag{20}$$

Therefore, the minimum duty cycle of D_2 is equal to $D_{2m}+D_m$.

$$L_f \le \frac{D_1\left(1-D_1\right)T_sV_o}{2n\Delta I_p - \frac{V_oT_s}{2n^2L_r}\left(\frac{1}{2}+\frac{1}{\pi}+\frac{2nL_rI_L}{V_oT_s}-\sqrt{D_1\left(1-D_1\right)-\frac{2P_on^2L_r}{{V_o}^2T_s}}\right)}. \tag{29}$$

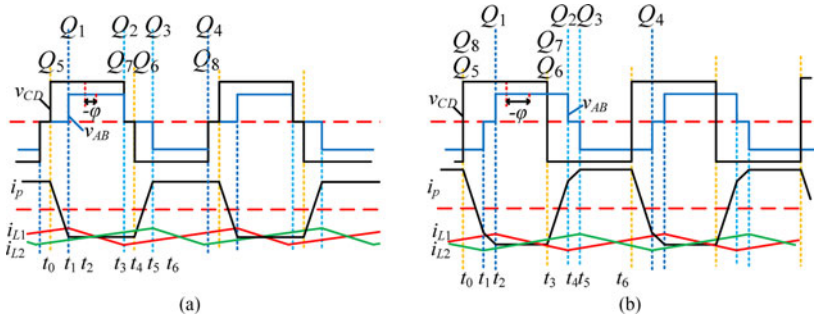


Fig. 8. Modified mode operation in the reverse power flow. (a) Mode 2*b_m*. (b) Mode 4*b_m*.

The current ripple of the dc filter inductor is expressed as $\Delta I_L = \frac{D_1(1-D_1)T_sV_o}{nL_f}$. The maximum and minimum current in i_{L1} and i_{L2} are expressed as

$$I_{L1\_\max} = I_{L2\_\max} = I_L + \frac{\Delta I_L}{2} = I_L + \frac{D_1\left(1-D_1\right)T_sV_o}{2nL_f}$$
$$I_{L1\_\min} = I_{L2\_\min} = I_L - \frac{\Delta I_L}{2} = I_L - \frac{D_1\left(1-D_1\right)T_sV_o}{2nL_f} \tag{21}$$

where I_L is the average current in i_{L1} and i_{L2}, and $I_L = \frac{P_o}{2V_{\text{bat}}}$. To achieve the ZVS for Q_2, the following condition is derived:

$$I_{p2} - I_{L2\_\min} = \frac{V_oT_s}{nL_r}\left(\frac{\varphi}{2\pi}\right) - \left(I_L - \frac{D_1\left(1-D_1\right)T_sV_c}{2L_f}\right) \ge \Delta I_p$$
$$\varphi \ge \frac{2\pi nL_r}{V_oT_s}\Delta I_p + \frac{2\pi nL_r}{V_oT_s}\left(I_L - \frac{D_1\left(1-D_1\right)T_sV_c}{2L_f}\right). \tag{22}$$

By substituting (11) into (22), the ZVS condition for Q_2 is expressed as

$$L_f \le \frac{D_1\left(1-D_1\right)T_sV_o}{2n\Delta I_p}. \tag{23}$$

The ZVS condition for Q_1 is expressed as

$$I_{L1\_\max} - I_{p0} = \left(I_L + \frac{D_1\left(1-D_1\right)T_sV_o}{2nL_f}\right) - \frac{V_oT_s}{nL_r}\left(\frac{\varphi}{2\pi}\right) \ge \Delta I_p. \tag{24}$$

The ZVS condition for Q_1 is expressed in (25) by substituting (11) into (24), and it is the same as the ZVS condition for Q_1,

$$L_f \le \frac{D_1\left(1-D_1\right)T_sV_o}{2n\Delta I_p}. \tag{25}$$

2) Mode 4a_m: According to (17) and (18), the ZVS condition for Q_5 and Q_7 is expressed in (26). ΔI_s is very low, and φ is greater than $\pi\left(D_1-0.5\right)$ in this case. Therefore, the ZVS of Q_5 and Q_7 is easy to achieve,

$$I_{p1} = \frac{V_oT_s}{nL_r}\left(\frac{\varphi}{2\pi}\right) \ge n\Delta I_s. \tag{26}$$

The ZVS condition for Q_1 in Mode 4*a_m* is expressed as

$$I_{L1\_\max} - I_{p0} = \left(I_L + \frac{D_1\left(1-D_1\right)T_sV_o}{2nL_f}\right) - \left[\frac{V_oT_s}{nL_r}\left(\frac{D_1}{2} - \frac{\varphi}{2\pi}\right) - \frac{V_o\left(1-D_1\right)T_s}{2nL_r}\right] > \Delta I_p. \tag{27}$$

According to (19), the phase angle φ is expressed as

$$\varphi = \frac{\pi}{2} - \pi\sqrt{D_1 - {D_1}^2 - \frac{2P_on^2L_r}{{V_o}^2T_s}}. \tag{28}$$

Equation (29) as shown at the top of this page is derived by substituting (28) into (27),

Because

$$\frac{V_oT_s}{2n^2L_r}\left(\frac{1}{2}+\frac{1}{\pi}+\frac{2nL_rI_L}{V_oT_s}-\sqrt{D_1(1-D_1)-\frac{2P_on^2L_r}{{V_o}^2T_s}}\right)$$

is greater than zero, the ZVS condition for Q_1 in this case is expressed as

$$L_f \le \frac{D_1\left(1-D_1\right)T_sV_o}{2n\Delta I_p}. \tag{30}$$

The ZVS condition for Q_2 is expressed as

$$I_{p2} - I_{L1\_\min} = \frac{V_oT_s}{nL_r}\left(\frac{\varphi}{2\pi}\right) - \left(I_L - \frac{D_1\left(1-D_1\right)T_sV_c}{2L_f}\right) \ge \Delta I_p$$
$$\varphi \ge \frac{2\pi nL_r}{V_oT_s}\Delta I_p + \frac{2\pi nL_r}{V_oT_s}\left(I_L - \frac{D_1\left(1-D_1\right)T_sV_c}{2L_f}\right). \tag{31}$$

$$L_f \le \frac{D_1\left(1-D_1\right)V_oT_s}{2n\Delta I_p+\left[\frac{V_oT_s}{nL_r}\sqrt{D_1\left(1-D_1\right)-\frac{2P_on^2L_r}{{V_o}^2T_s}}+\frac{nP_o}{V_o\left(1-D_1\right)}-\frac{V_oT_s}{2nL_r}\right]}. \tag{32}$$

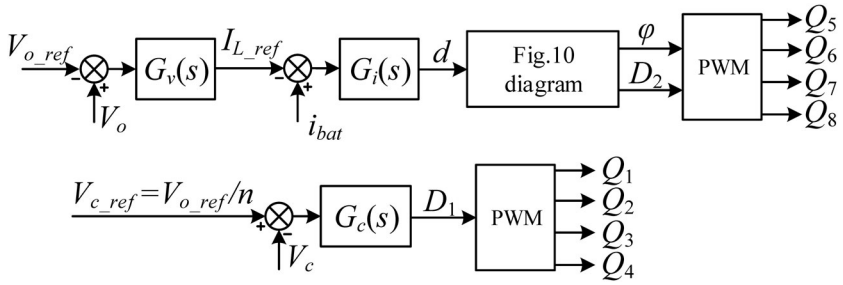


Fig. 9. Control diagram of the current-fed bidirectional dc–dc converter.

Equation (32) as shown at the top of this page was derived by substituting (28) into (31),

Because $\frac{V_oT_s}{nL_r}\sqrt{D_1(1-D_1)-\frac{2P_on^2L_r}{{V_o}^2T_s}}+\frac{nP_o}{V_o(1-D_1)}-\frac{V_oT_s}{2nL_r}$ is no more than zero, the ZVS condition for Q_2 is expressed as

$$L_f \le \frac{D_1\left(1-D_1\right)T_sV_o}{2n\Delta I_p}. \tag{33}$$

3) Mode 1a: Because Mode 2*a_m* and Mode 4*a_m* do not meet very light load requirements in forward power flow, Mode 1*a* will be used in this occasion. The ZVS condition for Mode 1*a* will be analyzed in this section.

According to (1) and (2), the ZVS condition for Q_5 and Q_7 is expressed as

$$I_{p0}=I_{p1}=\frac{V_oD_2T_s}{4nL_r}-\frac{V_o(1-D_1)T_s}{2nL_r}\ge n\Delta I_s$$

$$D_2\ge 2(1-D_1)+\frac{4L_rn^2\Delta I_s}{V_oT_s}=D_{2m}+D_m$$

$$D_{2m}=2(1-D_1), D_m=\frac{4L_rn^2\Delta I_s}{V_oT_s}. \tag{34}$$

Compared with (20), the ZVS conditions for Q_5-Q_7 in Mode 1*a* are the same as for Mode 2*a_m*.

The ZVS condition for Q_1 in Mode 1*a* is expressed as

$$I_{L1\_\max}-I_{p2}=\left(I_L+\frac{D_1\left(1-D_1\right)T_sV_o}{2nL_f}\right)-\frac{V_oT_s}{nL_r}\left(\frac{\varphi}{2\pi}\right)>\Delta I_p. \tag{35}$$

According to (3), the phase angle φ is expressed as

$$\varphi=\frac{\pi P_on^2L_r}{V_oT_s(1-D_1)}. \tag{36}$$

Substituting (36) into (35), (37) is derived as

$$L_f \le \frac{D_1\left(1-D_1\right)T_sV_o}{2n\Delta I_p}. \tag{37}$$

The ZVS for Q_2 is expressed as

$$I_{p3}-I_{L2\_\min}=\frac{V_oT_s}{nL_r}\left(\frac{\varphi}{2\pi}\right)-\left(I_L-\frac{D_1\left(1-D_1\right)T_sV_o}{2nL_f}\right)\ge\Delta I_p. \tag{38}$$

Substituting (36) into (38), (39) is derived as

$$L_f \le \frac{D_1\left(1-D_1\right)T_sV_o}{2n\Delta I_p}. \tag{39}$$

The ZVS condition for Mode 2*a_m* and Mode 1*a* are actually the same. The ZVS conditions for Mode 2*a_m*, Mode 4*a_m*, and Mode 1*a* are synthesized as

$$\begin{cases} L_f \le \dfrac{D_1\left(1-D_1\right)T_sV_o}{2n\Delta I_p} \\ D_2 \ge D_{2m}+D_m \end{cases}. \tag{40}$$

According to (40), the minimum current ripple is calculated based on the ZVS for Q_1-Q_4. Furthermore, low current ripple causes the reduction of the core loss in L_{f1} and L_{f2}. The maximum inductance of L_{f1} and L_{f2} for the modified operation modes is $\frac{D_{1\_\max}(1-D_{1\_\max})T_sV_o}{2n\Delta I_p}$.

III. Modulation and Control Scheme for the Modified Operation Mode

A. Modified PWM Plus Phase-Shift (MPPS) Modulation Scheme and Control Diagram

The proposed MPPS modulation scheme and control based on the modified operation modes are shown in Figs. 9 and 10, respectively. Fig. 9 shows the control diagram of the current-fed bidirectional dc–dc converter. As seen in Fig. 9, control variable *d* is the output of the inner-current loop controller, where $-1 \le d \le 1$. There are two closed-loop controls: the output-voltage control loop and clamping-capacitor-voltage control loop. The clamping-capacitor-voltage control loop adjusts the clamping capacitor to be a required voltage. The reference of

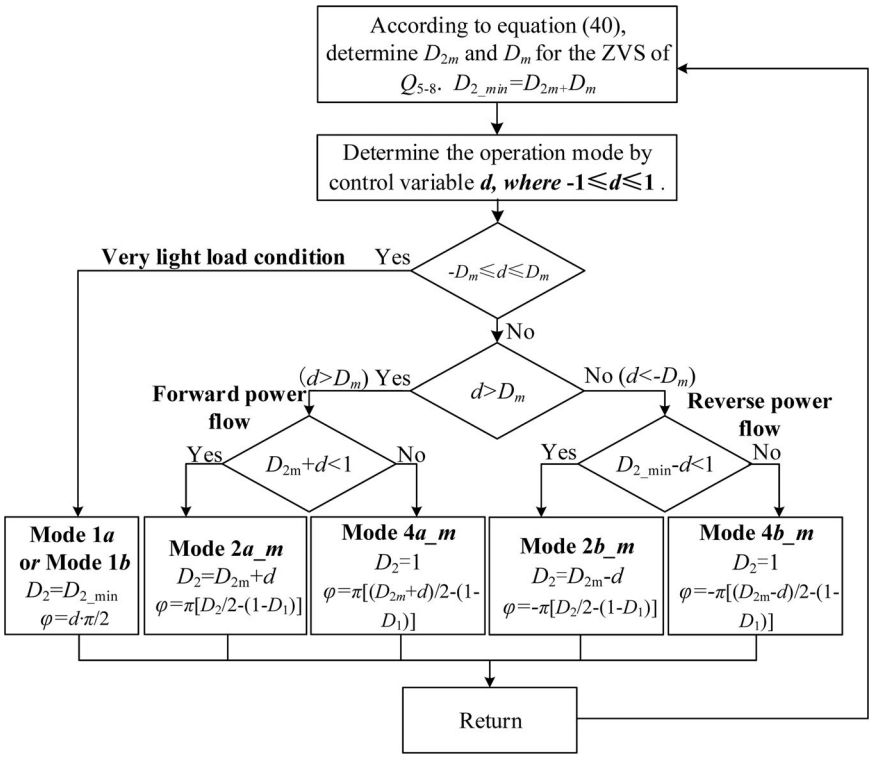


Fig. 10. Modulation scheme for the current-fed bidirectional dc–dc converter.

the clamping capacitor voltage is equal to V_{o_ref}/n, where V_{o_ref} is the reference of the output voltage. The output of the controller $G_c(s)$ is used to generate D_1 for the PWM signals of Q_1, Q_2, Q_3, and Q_4. The output-voltage control loop has a dual-loop structure. The inner control loop adjusts the required current, and the superimposed voltage control loop regulates the output voltage. The output of the output-voltage controller $G_v(s)$ is the reference of the inner-control loop. The feedback of the inner control loop is the battery current. D_2 and φ are calculated to generate the PWM signals of Q_5, Q_6, Q_7, and Q_8.

Fig. 10 shows the MPPS modulation scheme of the current-fed bidirectional dc–dc converter. As seen in Fig. 10, the values of D_2 and φ are calculated through d in different operation modes. The minimum duty cycle of D_2 is calculated according to (40). When $-D_m \leq d \leq D_m$, the converter works under no load or a very light load cases. However, Mode 2*a_m*, Mode 2*b*_m, Mode 4*a_m*, and Mode 4*b_m* do not address this situation. Therefore, the converter must work in Mode 1*a* or Mode1*b*. When $d \geq D_m$, the converter works in the forward power flow. If $D_{2\_\min}+d<1$, the converter works in Mode 2*a_m*. Otherwise, the converter works in Mode 4*a_m*. When $d \leq -D_m$, the converter works in the reverse power flow. If $D_{2\_\min}-d<1$, the converter works in Mode 2*b_m*. Otherwise, the converter works in Mode 4*b_m*.

Defining the base output power P_{base} as $\frac{V_o^2 T_s}{2n^2 L_k}$, Fig. 11 shows the output power in per unit (p.u.) versus the control variable *d*, where $V_o/n=V_c=133$ V, $T_s=12.5\,\mu$s, $L_r=14\,\mu$H, and $n=1.5$. It illustrates the modulation scheme shown in Fig. 10 facilitates a seamless transition in all the modified operation

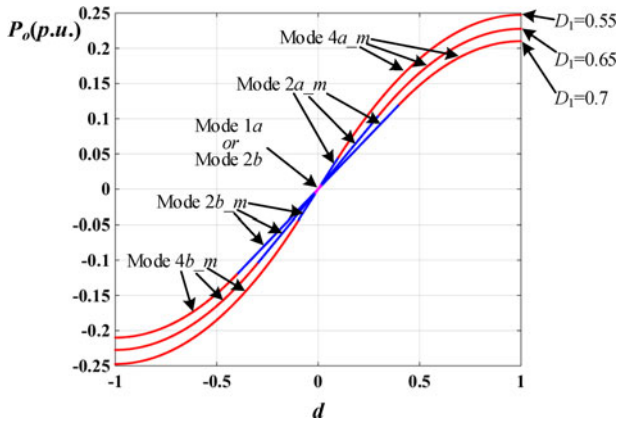


Fig. 11. Output power per unit (p.u.) versus the control variable *d*.

modes. The output power is determined by the control variable *d*. When *d* is positive, the energy is transmitted from the battery to the output. When *d* is negative, the energy is transmitted from the output to the battery.

The trajectories of the modulation scheme versus D_2 and φ for different values of D_1 in three-dimensional coordinates are shown in Fig. 12(a). D_2 and φ move on a trajectory for a specific D_1, as shown in Fig. 12(a). Fig. 12(b) and (c) is the lateral view of Fig. 23(a). Fig. 12(b) shows the output power versus φ, and Fig. 12(c) shows the output power versus D_2. Fig. 12(d) shows the top view of Fig. 12(a), which demonstrates the relationship of D_2 and φ.

The output power versus phase shift φ for PPDPS, PPS, and MPPS modulations is shown in Fig. 13. As seen, PPS and MPPS

$$i_{cc\_Q1\&Q2} = \sqrt{\frac{1}{T_s}\left[\int_{t_{c0}}^{t_{c1}} \left(i_{L1}(t) - i_p(t)\right)^2 dt + \int_{t_{c2}}^{t_{c3}} \left(i_{L1}(t) - i_p(t)\right)^2 dt\right]} \tag{41}$$

$$i_{cc\_Q3\&Q4} = \sqrt{\frac{1}{T_s}\left[\int_{t_{c0}}^{t_{c1}} \left(i_{L2}(t) + i_p(t)\right)^2 dt + \int_{t_{c2}}^{t_{c3}} \left(i_{L2}(t) + i_p(t)\right)^2 dt\right]}. \tag{42}$$

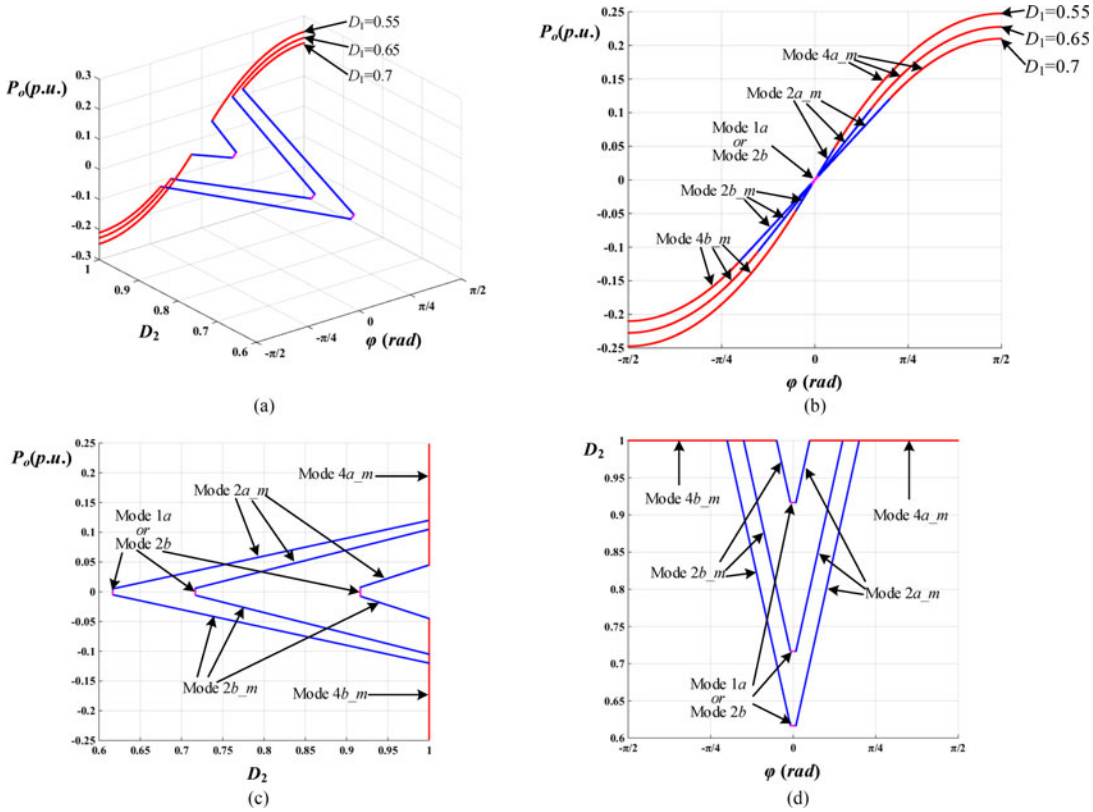


Fig. 12. Trajectories of the modulation scheme. (a) Output powers in p.u. versus D_2 and φ. (b) Right lateral view of Fig. 12(a). (c) Left lateral view of Fig. 12(a). (d) Top view of Fig. 12(a).

have the same curve. For the same phase shift angle, MPPS modulation can transmit more power than PPDPS.

B. Switch Conduction Loss Comparison

Fig. 14 shows the time interval for circulating current in different operation modes. During the shadowed time intervals, the circulating current freewheels in the switches. For the different operation modes shown in Fig. 14, the RMS of the circulating current in switches Q_1 and Q_2 can be synthetically expressed as Eq. (41) as shown at the top of this page.

The RMS of the circulating current in switches Q_3 and Q_4 is expressed as Eq. (42) as shown at the top of this page.

The RMS of the circulating current on the battery side of the switches is equal to $\sqrt{i_{cc\_Q1\&Q2}^2 + i_{cc\_Q3\&Q4}^2}$. The RMS of the circulating current on the battery side of the switches versus output power for PPS, PPDPS, and MPPS modulations is shown in Fig. 15, where $V_o/n = V_c = 133$ V, $T_s = 12.5\,\mu$s, $L_r = 14\,\mu$H, $L_f = 110\,\mu$H, and $n = 1.5$.

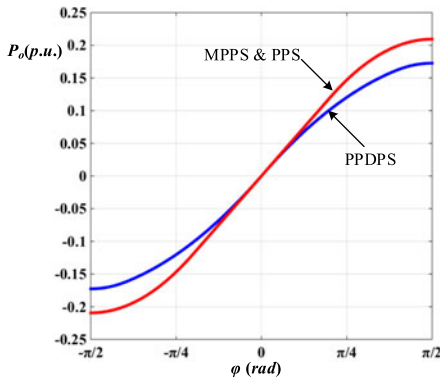


Fig. 13. Output powers in p.u. versus φ for the PPDPS, PPS, and MPPS when $D_1 = 0.7$.

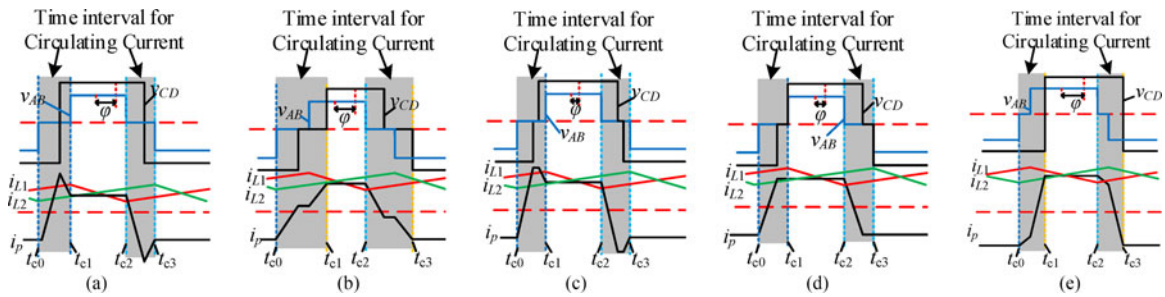


Fig. 14. Time interval for circulating current in different operation modes. (a) PPS. (b) PPDPS. (c) Mode 1*a*. (d) Mode 2*a_m*. (e) Mode 4*a_m*.

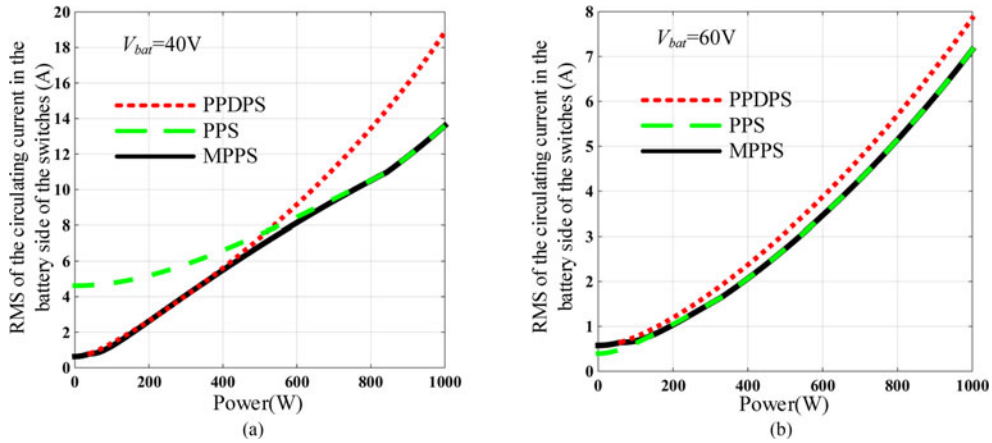


Fig. 15. RMS of the circulating current in the battery side of the switches versus output power. (a) $V_{\rm bat} = 40$ V. (b) $V_{\rm bat} = 60$ V.

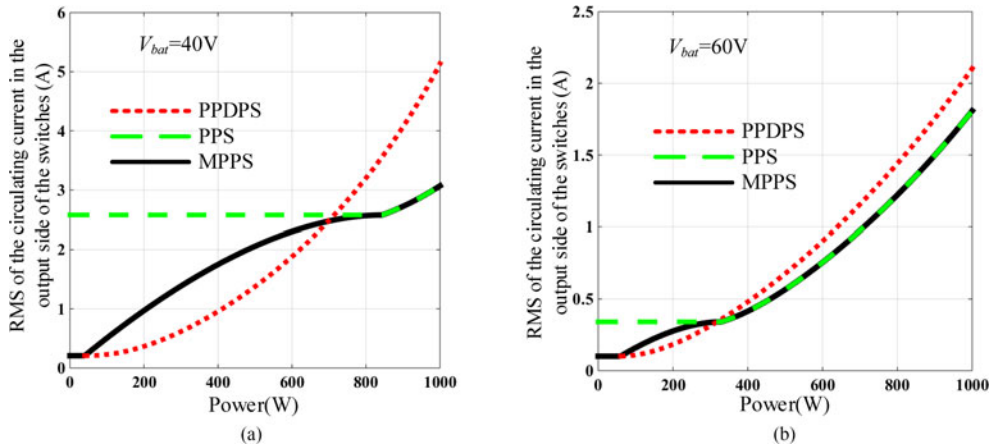


Fig. 16. RMS of the circulating current in the battery side of the switches versus output power. (a) $V_{\rm bat} = 40$ V. (b) $V_{\rm bat} = 60$ V.

When the battery voltage is 40 V, D_1 is equal to 0.7. In this case, there is a large time-interval of zero voltage in $v_{\rm AB}$ during the switching period, which can be seen in Fig. 2(a). As seen in Fig. 2(a), there is a large current spike in the transformer in the PPS. Therefore, there is a large circulating current on the primary side of the switches in light loads. With the increase of the output power, the circulating current in primary side of the switches for PPDPS becomes larger. In the whole load range, MPPS modulation has the least circulating current. When the battery voltage is 60 V, D_1 is equal to 0.55, closer to 0.5. The time-interval of zero voltage in $v_{\rm AB}$ becomes shorter. $v_{\rm AB}$ is close to a square waveform, so the large current spike of the transformer in the PPS disappears. As seen in Fig. 15(b), the circulating current curves for the three modulations become closer.

The circulating current in the output side of the switches for the operation modes shown in Fig. 14 can be synthetically expressed as

$$i_{cc\_Q5-Q8} = \sqrt{\frac{1}{T_s}\left[\int_{t_{c0}}^{t_{c1}} \left(\frac{i_p(t)}{n}\right)^2 dt + \int_{t_{c2}}^{t_{c3}} \left(\frac{i_p(t)}{n}\right)^2 dt\right]}. \tag{43}$$

The circulating current in the output side of the switches versus output power for PPS, PPDPS, and MPPS modulations is shown in Fig. 16. The MPPS modulation has less circulating

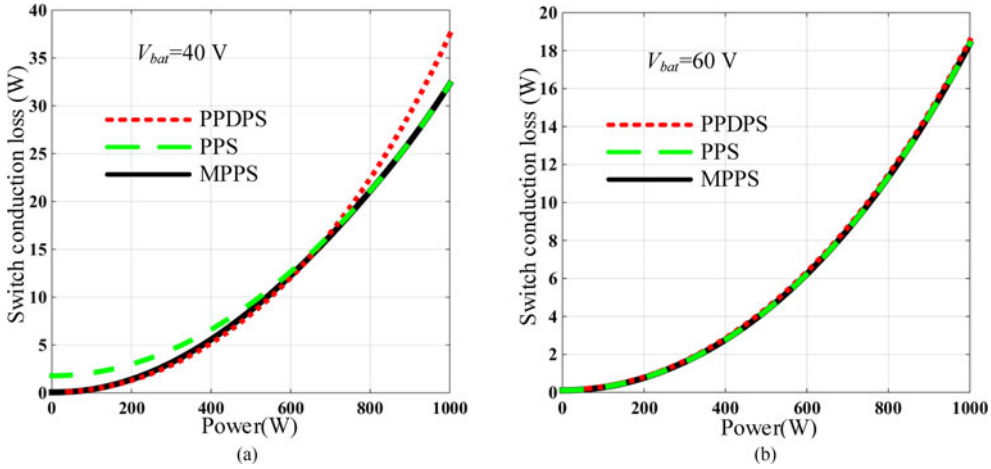


Fig. 17. Switch conduction losses for the PPDPS, PPS, and MPPS. (a) $V_{\text{bat}} = 40$ V. (b) $V_{\text{bat}} = 60$ V.

current on the output side of the switches than PPS modulation with light loads, and it also has less circulating current than PPDPS modulation with heavy loads.

The switch turn-ON resistance for $Q_1 - Q_8$ is $50\,m\Omega$. Fig. 17 shows the conduction loss in the switches for different values of the output power. Fig. 17(a) shows the conduction loss in switches, when the battery voltage is 40 V. As seen in Fig. 17(a), the conduction loss in the PPS is greater than that in the PPDPS and MPPS for light loads. For heavy loads, the phase angle in the PPDPS becomes larger than that in the PPS and MPPS as the load power increases. It results in more conduction loss. Fig. 17(b) shows that the conduction losses of the three modulation schemes are almost the same, when the battery voltage is 60 V. The MPPS has a low conduction loss performance during the entire load range and experiences wide battery voltage variations.

As seen in Fig. 16, MPPS modulation on the output side of the switches does not have the least circulating current within the entire load range, but it still has better performance for conduction loss in the switches than PPS and PPDPS modulations.

C. Comparison of the Core Loss in the Series Inductor

The core loss in the series inductor L_r is associated with the peak current. In the experimental prototype, Kool Mμ (77191), produced by *Magnetics*, is used as the material of the inductor core. The parameters of the core are illustrated in [30]. The core loss in the series inductor versus the output power is shown in Fig. 18, where $V_o/n = V_c = 133$ V, $T_s = 12.5\,\mu$s, $L_r = 14\,\mu$H, and $n = 1.5$. Fig. 18(a) shows the core loss when the battery voltage is 40 V. The MPPS has a low core loss over the whole load range because of the lower peak current. Fig. 18(b) shows that the core losses under the three strategies become more similar when the battery voltage is 60 V. In summary, the MPPS modulation scheme performs well in the reduction of the core loss in the series inductor.

IV. Experimental Verifications

An 800W experimental prototype with a 40–60V battery and 200 V output voltage was built to verify the modulation scheme. The detailed specifications are shown in Table III. In terms of (40), the filter inductance L_f was calculated as $L_f \le \frac{D_{1_\max}(1-D_{1_\max})T_s V_o}{2n\Delta I_p} = 116.7\ \mu$H. Therefore, the value for L_f was $110\,\mu$H.

TABLE III
Detailed Specifications

Items	Symbol	Parameter
Battery voltage	V_{bat}	40 V~60 V
Output voltage	V_o	200 V
Clamping capacitor voltage	V_c	133 V
Turns ratio of the transformers	n	1.5
Range of D_1		[0.55, 0.7]
Switching frequency	$f_s\,(T_s)$	80 kHz (12.5 μs)
Primary switches	$Q_{1\text{-}4}$	IPP110N20N3 G
Secondary switches	$Q_{5\text{-}8}$	IRFB4137PbF
Series inductor	L_r	14 μH
Output filter capacitance	C_o	220 μF

Figs. 19 and 20 show the key waveforms for different battery voltages and output powers in the forward power flow. Fig. 19 shows that D_2 increases with the increase of the load power. The converter works in Mode 2*a_m* when the load power is 200 or 500 W. As seen in Fig. 19(c), D_2 is equal to 1 at 800 W. In this case, the converter works in Mode 4*a_m*. Fig. 20 shows the key waveforms when the battery voltage is 60 V. In Fig. 20,

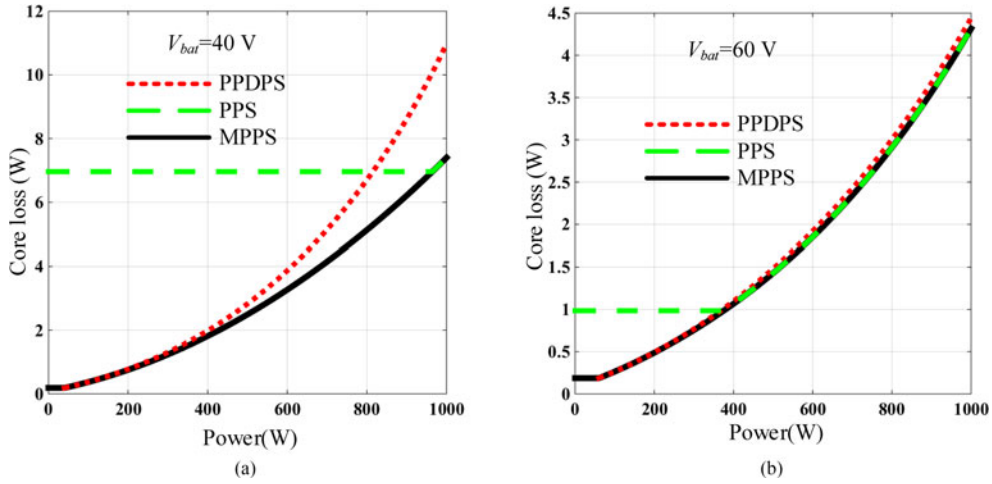


Fig. 18. Core losses in the series inductor L_r for the PPDPS, PPS, and MPPS. (a) $V_{\text{bat}} = 40$ V. (b) $V_{\text{bat}} = 60$ V.

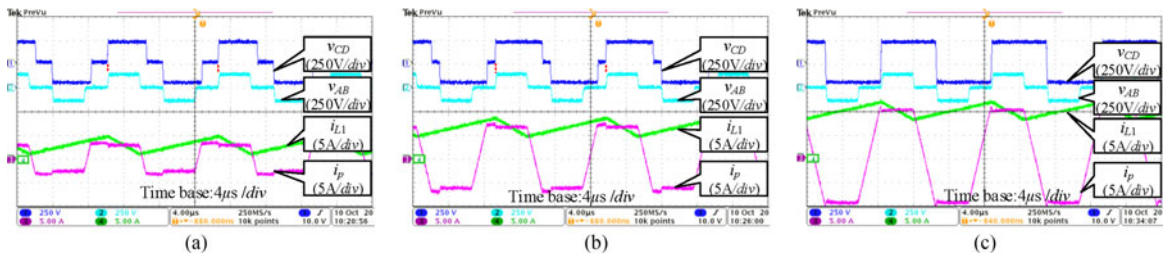


Fig. 19. Measured key waveforms for the 40 V battery voltage. (a) $P_o = 200$ W. (b) $P_o = 500$ W. (c) $P_o = 800$ W.

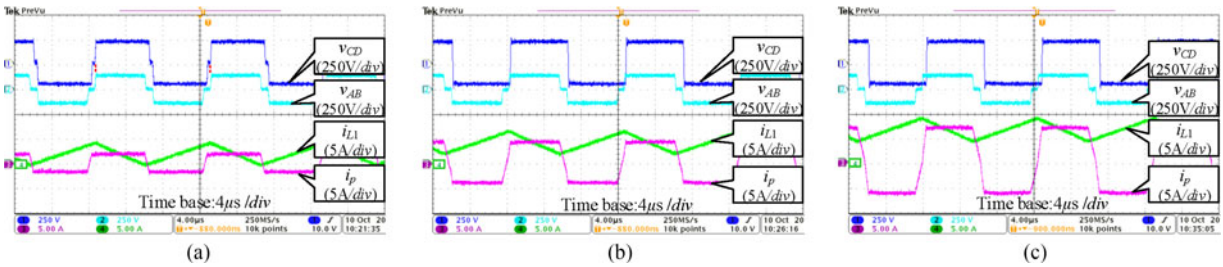


Fig. 20. Measured key waveforms for the 60 V battery voltage. (a) $P_o = 200$ W. (b) $P_o = 500$ W. (c) $P_o = 800$ W.

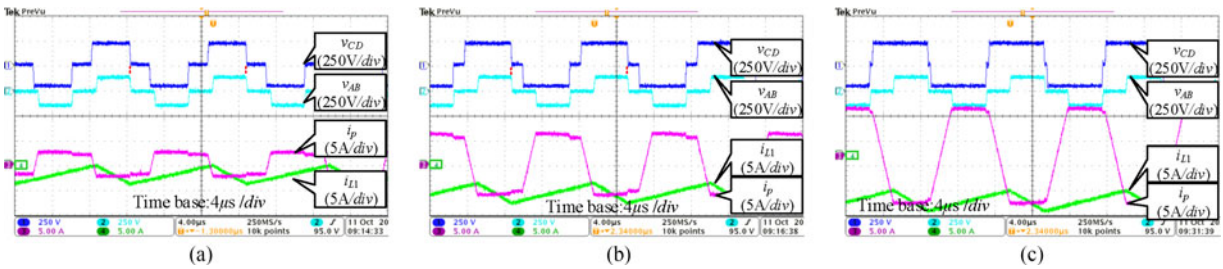


Fig. 21. Measured key waveforms for the 40 V battery voltage. (a) $P_o = -200$ W. (b) $P_o = -500$ W. (c) $P_o = -800$ W.

the value of D_1 is less than that at the 40 V battery voltage. The converter works in Mode 4*a_m* when the output power is greater than 500 W. The converter is more inclined to work in Mode 4*a_m* with the increase of the battery voltage.

Figs. 21 and 22 show the key waveforms for different battery voltages and output powers in the reverse power flow. The filter inductor current i_{L1} becomes negative, which illustrates that the power is transmitted from the output to the battery. Fig. 21 is nearly symmetric to Fig. 19. Fig. 22 is nearly symmetric to Fig. 20.

Fig. 23 shows the gate signal and drain–source voltage of Q_1 in the forward and reverse power flows. The ZVS performance was achieved. Since Q_3 operates in the same mode with Q_1 in the other half of the switching period, the ZVS

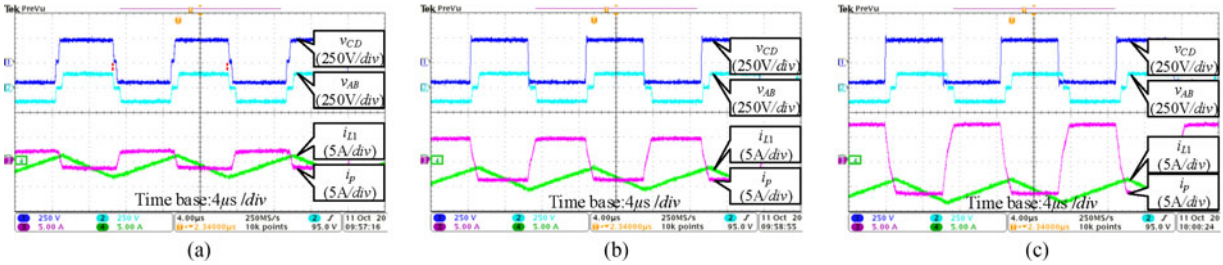


Fig. 22. Measured key waveforms for the 60 V battery voltage. (a) $P_o = -200$ W. (b) $P_o = -500$ W. (c) $P_o = -800$ W.

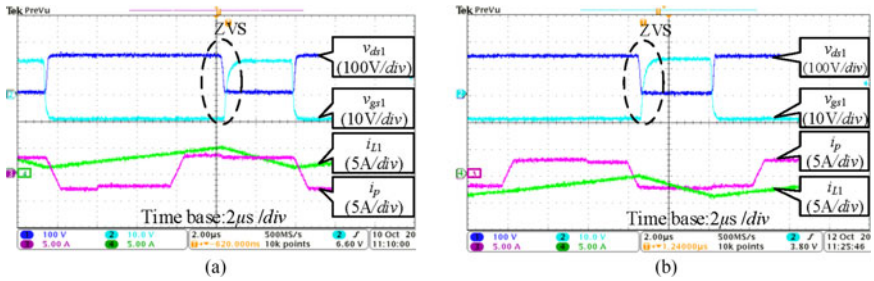


Fig. 23. Gate signal and drain–source voltage of switch Q_1 at $V_{\text{bat}} = 40$ V. (a) $P_o = 200$ W. (b) $P_o = -200$ W.

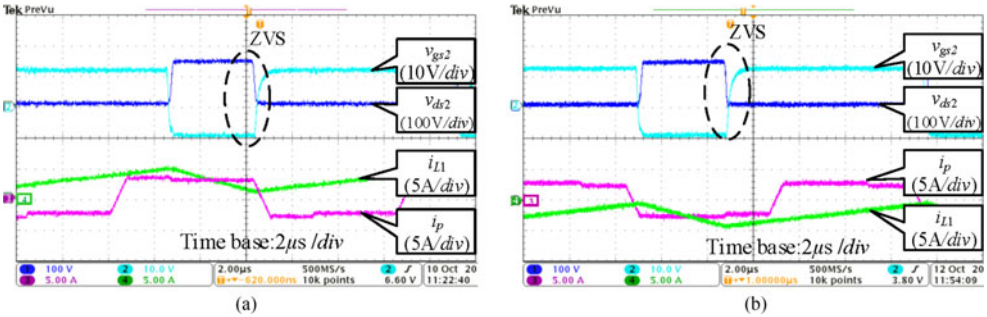


Fig. 24. Gate signal and drain–source voltage of switch Q_2 at $V_{\text{bat}} = 40$ V. (a) $P_o = 200$ W. (b) $P_o = -200$ W.

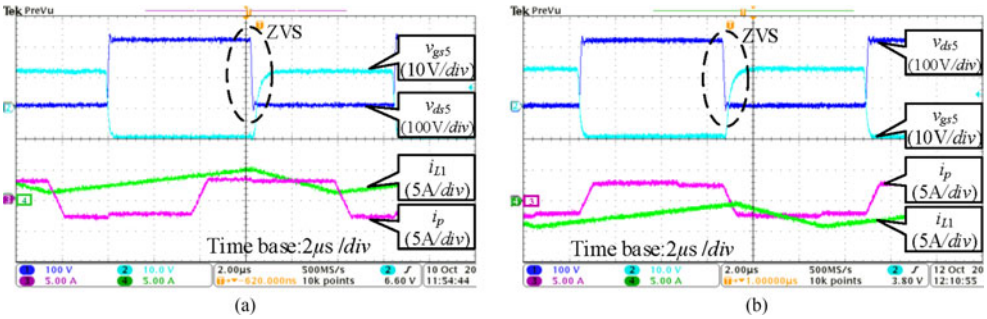


Fig. 25. Gate signal and drain–source voltage of switch Q_5 at $V_{\text{bat}} = 40$ V. (a) $P_o = 200$ W. (b) $P_o = -200$ W.

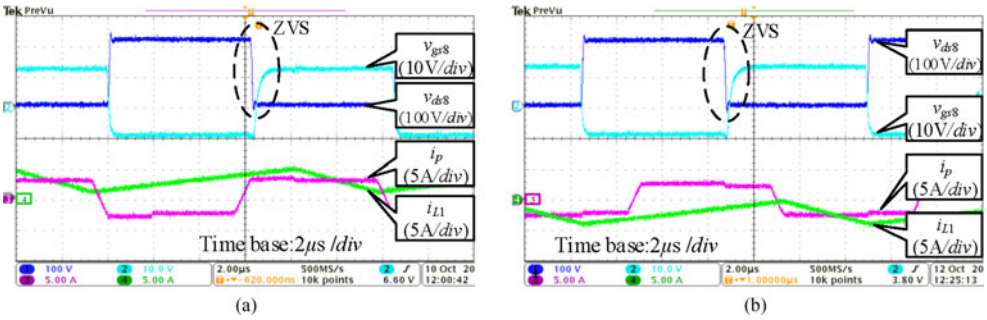


Fig. 26. Gate signal and drain–source voltage of switch Q_8 at $V_{\text{bat}} = 40$ V. (a) $P_o = 200$ W. (b) $P_o = -200$ W.

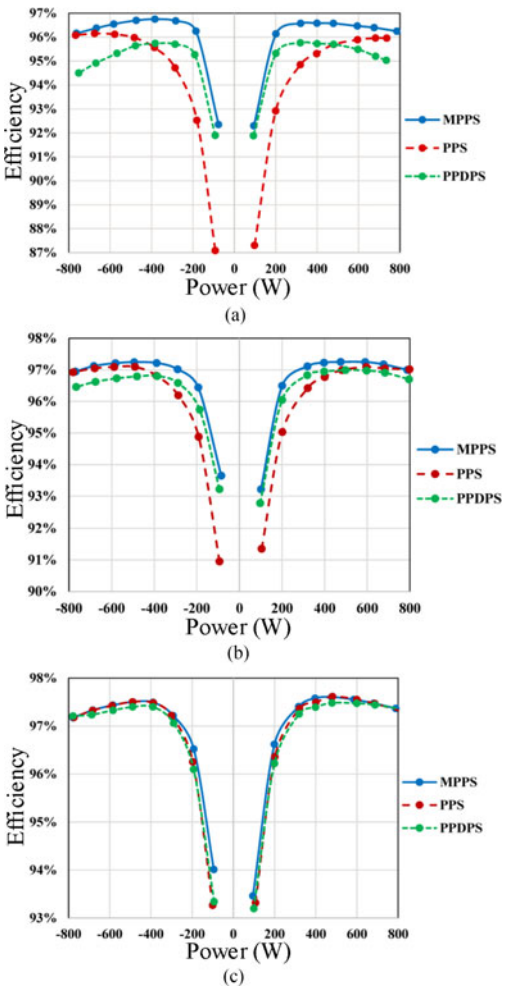


Fig. 27. Efficiency curves for the proposed MPPS, conventional PPS, and PPDPS at (a) Vbat = 40 V, (b) Vbat = 50 V, and (c) Vbat = 60 V.

for Q_3 is also accomplished in both the forward and reverse power flows. Fig. 24 shows the gate signal and drain–source voltage of Q_2, which also highlights the ZVS performance of Q_2. Since Q_4 operates in the same mode with Q_2 in the other half of the switching period, the ZVS for Q_4 also can be achieved in both the forward and reverse power flows.

Figs. 25 and 26 show the gate signal and drain–source voltage of Q_5 and Q_8 in the forward and reverse power flows, respectively. The experimental results demonstrate the ZVS performance of Q_5 and Q_8 in both the forward and reverse power flow. In a switching period, Q_6 operates in the same mode with Q_5 in the other half of the switching period, and Q_7 operates in the same mode with Q_8 in the other half of the switching period. Therefore, the ZVS of Q_6 and Q_7 can be achieved simultaneously.

The measured efficiency curves for the proposed MPPS, PPS, and PPDPS are shown in Fig. 27. Fig. 27(a) shows the efficiency curve for the 40 V battery voltage. In this case, D_1 is 0.7. With light loads, the PPS has a large conduction loss, so the PPS has the lowest efficiency. As the power increases, the PPDPS needs a greater phase-shift angle to meet the load requirements, which causes a large RMS current and peak current in the transformer. Therefore, the efficiency curve drops dramatically with a heavy load. The operation mode for the PPS is closer to the proposed MPPS with the increase in the load power. The two efficiency curves converge in heavy loads. D_1 decreases with the increase of the battery voltage. Meanwhile, the time interval of zero voltage in v_{AB} during a switching period decreases. The waveforms of the three modulation schemes become closer. Fig. 27(b) and (c) shows that the efficiency curves become more closer with the increase of the battery voltage. In all of the experimental results, the proposed MPPS has the lowest losses, so the proposed MPPS has a better efficiency performance than the conventional PPS and PPDPS for wide battery voltage.

V. Conclusion

In this paper, an improved modulation scheme was proposed for the current-fed bidirectional dc–dc converter. The previous modulation strategies were reviewed, and different operation modes were analyzed. Then, the modified operation modes were derived to minimize the conduction loss. Based on the modified operation mode, a closed-loop control with the MPPS modulation was proposed. In the MPPS, the converter can achieve a high efficiency over the entire load range and with wide input voltage variations. The MPPS synthesizes the advantages of the different modulation strategies. The trajectories of the modulations were analyzed. The conduction loss and core loss comparisons with other modulation strategies have demonstrated the low losses in MPPS. The experimental results verified the operation modes and high efficiency performance in the proposed MPPS.

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Zhiqiang Guo (S'11–M'15) received the B.S. degree in automation from the Hebei University of Technology, Tianjin, China, in 2008, and the M.S. and Ph.D. degrees in electrical engineering from the Beijing Institute of Technology, Beijing, China, in 2010 and 2015.

He was a Postdoctoral Research Fellow with the Department of Electrical Engineering, Tsinghua University, Beijing, from 2015 to 2017. In 2017, He joined the faculty of the School of Automation, Beijing Institute of Technology, Beijing, where he is an Assistant Professor. His current research interests include dc–dc converters, distributed generation, and microgrid applications.

Kai Sun (M'12–SM'16) received the B.E., M.E., and Ph.D. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2000, 2002, and 2006, respectively.

He joined the Faculty of Electrical Engineering, Tsinghua University, in 2006, where he is currently an Associate Professor. From September 2009 to August 2010, he was a Visiting Scholar at the Department of Energy Technology, Aalborg University, Aalborg, Denmark. From January to August 2017, he is a Visiting Professor at the Department of Electrical and Computer Engineering, University of Alberta, Edmonton, AB, Canada. His current research interests include power electronics for renewable generation systems, microgrids, and active distribution networks.

Dr. Sun is a member of IEEE Power Electronics Society Sustainable Energy Systems Technical Committee, a member of IEEE Power Electronics Society Power and Control Core Technologies Committee, a member of IEEE Industrial Electronics Society Renewable Energy Systems Technical Committee, and a member of IEEE IAS Industrial Drive Committee Awards Subcommittee. He is an Associate Editor for the IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS, and the *Journal of Power Electronics*. He served as the TPC Vice Chair of IEEE ECCE2017 and IEEE ECCE-Asia2017. He received the Delta Young Scholar Award in 2013.

Tsai-Fu Wu (S'88–M'91–SM'98) received the B.S. degree in electronic engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1983, the M.S. degree in electrical and computer engineering from Ohio University, Athens, OH, USA, in 1988, and the Ph.D. degree in electrical engineering and computer science from the University of Illinois, Chicago, IL, USA, in 1992.

From 1985 to 1986, he was a System Engineer at SAMPO, Inc., Taiwan, where he was involved in developing and designing graphic terminals. From 1988 to 1992, he was a Teaching and Research Assistant in the Department of Electrical Engineering and Computer Science, University of Illinois, Chicago. From 1993 to 2012, he was with the Department of Electrical Engineering, National Chung Cheng University, Chia-Yi, Taiwan. He is currently a Distinguished Professor in the Department of Electrical Engineering, National Tsing Hua University, Hsinchu. His current research interests include development and modeling of power converters, design of solar-array supplied inverters for grid connection, design and development of D-Σ digital controlled single-phase and three-phase inverters with grid connection, rectification, APF, STATCOM, and UPS functions.

Dr. Wu has been an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS since 2000. He was the Guest Editor-in-Chief for the IEEE TRANSACTIONS ON POWER ELECTRONICS in dc distribution systems from 2012 to 2013.

Canbing Li (M'06–SM'13) received the B.Sc. and Ph.D. degree in electrical engineering from Tsinghua University, Beijing, China, in 2001 and 2006, respectively.

He is currently a Professor in the College of Electrical and Information Engineering, Hunan University, Changsha, China. His research interests include smart grid, energy efficiency, and energy policy.